



LV2460/2461

Preliminary

LINEAR INTEGRATED CIRCUIT

FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

DESCRIPTION

The UTC **LV2460/2461** is a low-power rail-to-rail input/output op amplifier with low supply current (500uA) and low voltage (2.7-6V), that can be designed into a wide range of applications. The UTC **LV2460** offers a shutdown terminal, which places the amplifier in an ultralow supply current mode ($I_{CC} = 0.3\mu A$).

The UTC **LV2460/2461** have a guaranteed 1.6 V/ μs slew rate and low supply current. rail-to-rail output and high output current make the IC's ideal for buffering analog-to-digital converters. And the input common-mode voltage range includes ground and V_{CC} . Besides, they are also able to drive large capacitive loads.

Good AC performance can be provided because of 6.4MHz of bandwidth and 1.6 V/ μs of slew rate. Furthermore, low input noise voltage ($11nV/\sqrt{Hz}$) and low input offset voltage (100 μV) make good DC performance.

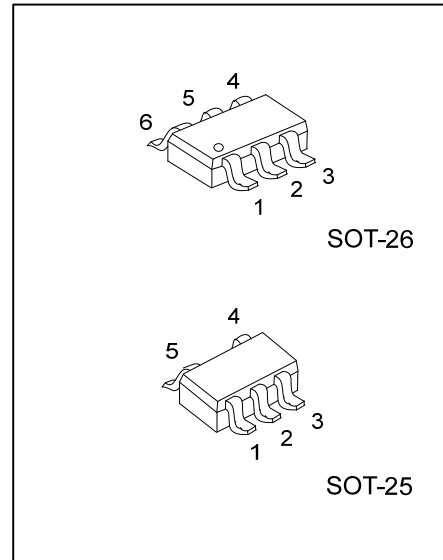
FEATURES

- * Rail-to-Rail Output Swing
- * Gain Bandwidth Product: 6.4 MHz
- * $\pm 48mA$ Output Drive Capability
- * Supply Current: 500 μA
- * Input Offset Voltage: 100 μV
- * Input Noise Voltage: $11nV/\sqrt{Hz}$
- * Slew Rate: 1.6V/ μs
- * Universal Operational Amplifier
- * Micropower shutdown mode (LV2460) 0.3 μA

ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
LV2460L-AG6-R	LV2460G-AG6-R	SOT-26	Tape Reel
LV2461L-AF5-R	LV2461G-AF5-R	SOT-25	Tape Reel

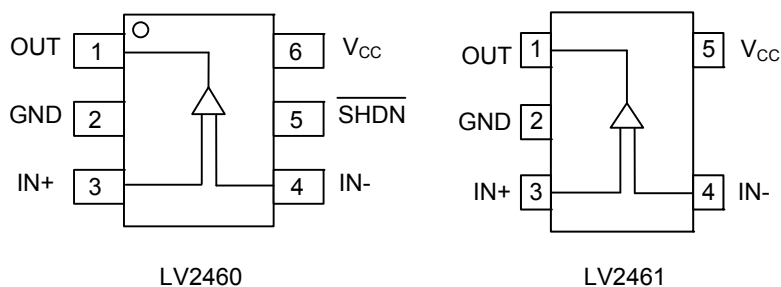
<p>LV2460G-AG6-R</p> <ul style="list-style-type: none"> (1)Packing Type (2)Package Type (3)Green Package 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) AG6: SOT-26, AF5: SOT-25 (3) G: Halogen Free and Lead Free, , L: Lead Free
---	---



MARKING

LV2460	LV2461

PIN CONFIGURATION

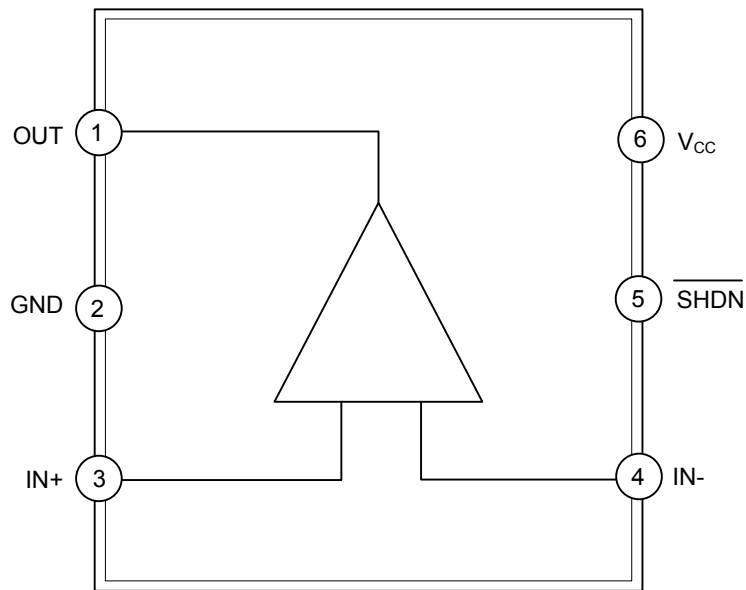


PIN DESCRIPTION

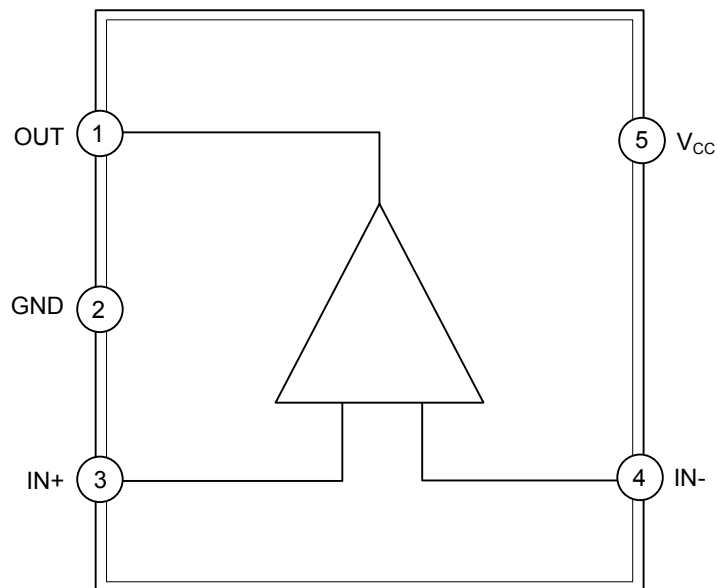
PIN NO.		PIN NAME	DESCRIPTION
LV2460	LV2461		
1	1	OUT	Output
2	2	GND	Ground
3	3	IN+	Positive input
4	4	IN-	Negative input
5	-	$\overline{\text{SHDN}}$	Shutdown
6	5	V _{CC}	Supply power

■ BLOCK DIAGRAM

For LV2460

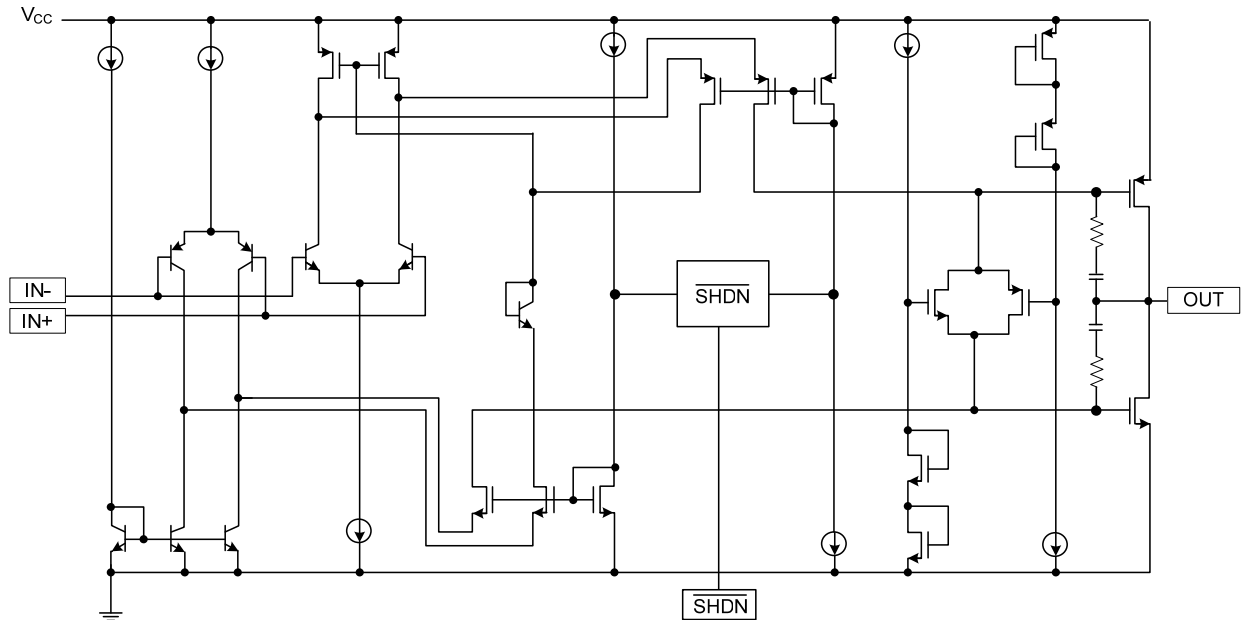


For LV2461

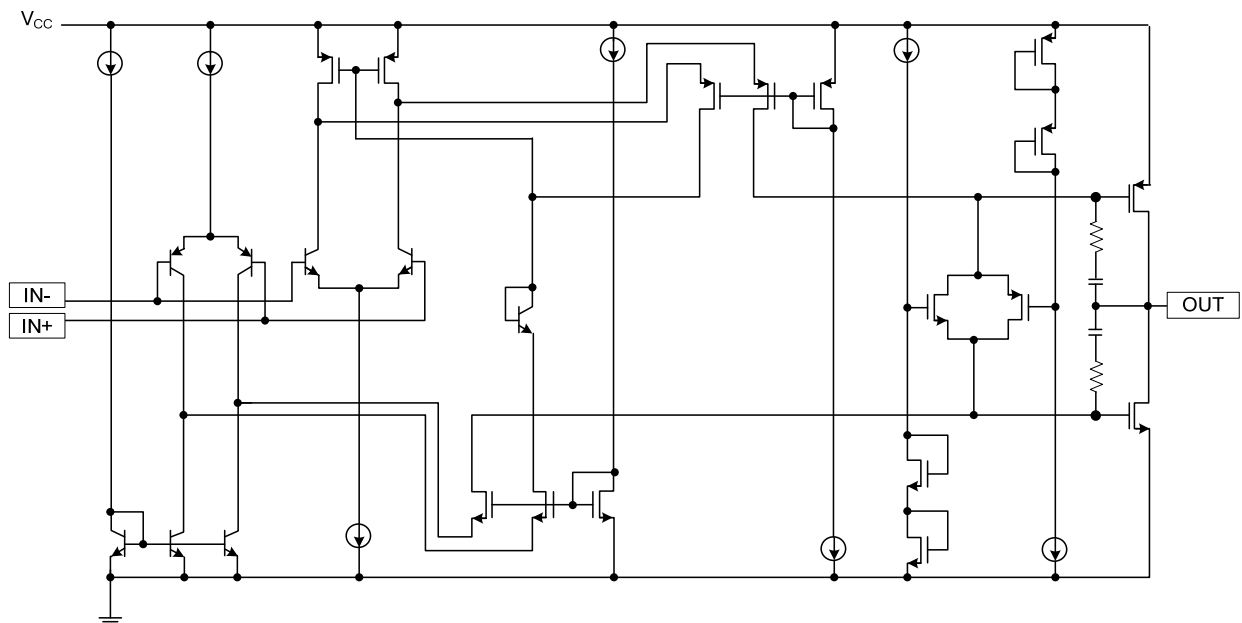


■ INTERNAL SIMPLE CIRCUIT

For LV2460



For LV2461



■ ABSOLUTE MAXIMUM RATING ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage (Note 1)		V_{CC}	6	V
Differential Input Voltage		V_{ID}	$-0.2 \sim V_{CC}+0.2$	V
Output Current		I_O	± 175	mA
Power Dissipation	$T_A \leq 25^\circ\text{C}$ SOT-25	P_D	385	mW
	$T_A \leq 25^\circ\text{C}$ SOT-26		425	
Operating Free-Air Temperature		T_A	$-40 \sim +125$	$^\circ\text{C}$
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature		T_{STG}	$-60 \sim +150$	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. All voltage values, except differential voltages, are with respect to GND.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOT-25	θ_{JA}	324	$^\circ\text{C}/\text{W}$
	SOT-26		294	$^\circ\text{C}/\text{W}$
Junction to Case	SOT-25	θ_{JC}	55	$^\circ\text{C}/\text{W}$
	SOT-26		55	$^\circ\text{C}/\text{W}$

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	RATINGS	UNIT
Supply Voltage	Single supply	V_{CC}	$2.7 \sim 6$	V
	Split supply		$\pm 1.35 \sim \pm 3$	V
Common-Mode Input Voltage		V_{ICR}	$0 \sim V_{CC}$	V
Operating Free-Air Temperature		T_A	$-40 \sim +125$	$^\circ\text{C}$
Shutdown on/off voltage level (Note 1)		$V_{IH \text{ MIN}}$	2	V
		$V_{IL \text{ MAX}}$	0.7	V

Note: Relative to voltage on the GND terminal of the device.

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

$V_{CC}=3\text{V}$

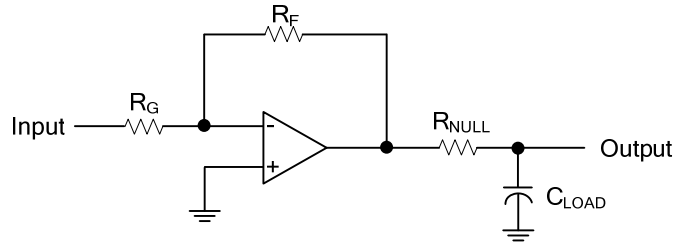
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	V_{IO}	$V_{CC}=3\text{V}$, $V_{IC}=1.5\text{V}$, $V_O=1.5\text{V}$, $R_S=50\Omega$		500	2000	μV
Input Offset Current	I_{IO}	$V_{CC}=3\text{V}$, $V_{IC}=1.5\text{V}$,		2.8	7	nA
Input Bias Current	I_{IB}	$V_O=1.5\text{V}$, $R_S=50\Omega$		4.4	14	nA
High-Level Output Voltage	V_{OH}	$I_{OH}=-2.5\text{mA}$		2.9		V
		$I_{OH}=-10\text{mA}$		2.7		V
Low-Level Output Voltage	V_{OL}	$V_{IC}=1.5\text{V}$, $I_{OL}=2.5\text{mA}$		0.1		V
		$V_{IC}=1.5\text{V}$, $I_{OL}=10\text{mA}$		0.3		V
Short-Circuit Output Current	I_{OS}	Sourcing		50		mA
		Sinking		40		mA
Output Current	I_O	Measured 1V form rail		± 40		mA
Large-Signal Differential Voltage Amplification	A_{VD}	$R_L=10\text{k}\Omega$, $V_{O(PP)}=1\text{V}$	90	105		dB
Differential Input Resistance	$r_{i(D)}$	$T_A=25^\circ\text{C}$		10^9		Ω
Common-Mode Input Capacitance	$C_{i(C)}$	$f=10\text{kHz}$, $T_A=25^\circ\text{C}$		7		pF
Closed-Loop Output Impedance	Z_O	$f=100\text{kHz}$, $A_V=10$, $T_A=25^\circ\text{C}$		33		Ω
Common-Mode Rejection Ratio	CMRR	$V_{ICR}=0\sim 3\text{V}$, $R_S=50\Omega$	66	80		dB
Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$)	k_{SVR}	$V_{CC}=2.7\sim 6\text{V}$, $V_{IC}=V_{CC}/2$, No load	80	85		dB
		$V_{CC}=3\sim 5\text{V}$, $V_{IC}=V_{CC}/2$, No load	85	95		dB
Supply Current	I_{CC}	$V_O=1.5\text{V}$, No load		0.5	0.575	mA
Supply current in shutdown(LV2460)	$I_{CC(SHDN)}$	$SHDN < 0.7\text{V}$		0.3		μA
Slew Rate at Unity Gain	SR	$V_{O(PP)}=0.8\text{V}$, $R_L=10\text{k}\Omega$, $C_L=160\text{pF}$	0.9	1.6		$\text{V}/\mu\text{s}$
Equivalent Input Noise Voltage	V_N	$f=100\text{Hz}$		16		$\text{nV}/\sqrt{\text{Hz}}$
		$f=1\text{kHz}$		11		$\sqrt{\text{Hz}}$
Equivalent Input Noise Current	I_N	$f=1\text{kHz}$		0.13		$\text{pA}/\sqrt{\text{Hz}}$
Total Harmonic Distortion Plus Noise	THD+N	$V_{O(PP)}=2\text{V}$, $R_L=10\text{k}\Omega$, $f=1\text{kHz}$	$A_V=1$	0.006		%
			$A_V=10$	0.02		%
			$A_V=100$	0.08		%
Gain-Bandwidth Product		$f=10\text{kHz}$, $C_L=160\text{pF}$, $R_L=10\text{k}\Omega$		5.2		MHz
Setting Time	t_S	$V_{(STEP)PP}=2\text{V}$, $R_L=10\text{k}\Omega$, $A_V=-1$, $C_L=10\text{pF}$	0.1%	1.47		μs
			0.01%	1.78		μs
		$V_{(STEP)PP}=2\text{V}$, $R_L=10\text{k}\Omega$, $A_V=-1$, $C_L=56\text{pF}$,	0.1%	1.77		μs
			0.01%	1.98		μs
Phase Margin at Unity Gain	Φ_M	$R_L=10\text{k}\Omega$, $C_L=160\text{pF}$		44		$^\circ$
Gain Margin				7		dB

■ ELECTRICAL CHARACTERISTICS (Cont.)

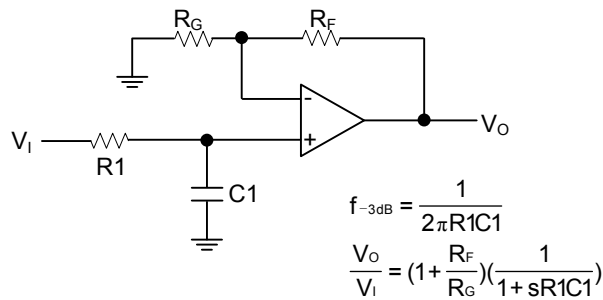
$V_{CC}=5V$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	V_{IO}	$V_{CC}=5V, V_{IC}=2.5V,$ $V_O=2.5V, R_S=50\Omega$		500	2000	μV
Input Offset Current	I_{IO}	$V_{CC}=5V, V_{IC}=2.5V,$ $V_O=2.5V, R_S=50\Omega$		0.3	7	nA
Input Bias Current	I_{IB}			1.3	14	nA
High-Level Output Voltage	V_{OH}	$I_{OH}=-2.5mA$		4.9		V
		$I_{OH}=-10mA$		4.8		V
Low-Level Output Voltage	V_{OL}	$V_{IC}=2.5V, I_{OL}=2.5mA$		0.1		V
		$V_{IC}=2.5V, I_{OL}=10mA$		0.2		V
Short-Circuit Output Current	I_{OS}	Sourcing		145		mA
		Sinking		100		mA
Output Current	I_O	Measured 1V form rail		± 48		mA
Large-Signal Differential Voltage Amplification	A_{VD}	$V_{IC}=2.5V, R_L=10k\Omega, V_O=1\sim 4V$	92	109		dB
Differential Input Resistance	$r_{i(D)}$	$T_A=25^\circ C$		10^9		Ω
Common-Mode Input Capacitance	$C_{i(C)}$	$f=10kHz, T_A=25^\circ C$		7		pF
Closed-Loop Output Impedance	Z_O	$f=100kHz, A_V=10, T_A=25^\circ C$		29		Ω
Common-Mode Rejection Ratio	CMRR	$V_{ICR}=0\sim 5V, R_S=50\Omega$	71	85		dB
Supply Voltage Rejection Ratio ($\Delta V_{CC}/\Delta V_{IO}$)	k_{SVR}	$V_{CC}=2.7\sim 6V, V_{IC}=V_{CC}/2, \text{No load}$	80	85		dB
		$V_{CC}=3\sim 5V, V_{IC}=V_{CC}/2, \text{No load}$	85	95		dB
Supply Current	I_{CC}	$V_O=2.5V, \text{No load}$		0.55	0.65	mA
Supply current in shutdown(LV2460)	$I_{CC(SHDN)}$	$SHDN < 0.7V$		1		μA
Slew Rate at Unity Gain	SR		0.9	1.6		V/ μs
Equivalent Input Noise Voltage	V_N	$f=100Hz$		14		nV/ \sqrt{Hz}
		$f=1kHz$		11		\sqrt{Hz}
Equivalent Input Noise Current	I_N	$f=1kHz$		0.13		pA/ \sqrt{Hz}
Total Harmonic Distortion Plus Noise	THD+N	$V_{O(PP)}=4V, R_L=10k\Omega,$ $f=1kHz$	$A_V=1$	0.004		%
			$A_V=10$	0.01		%
			$A_V=100$	0.04		%
Gain-Bandwidth Product		$f=10kHz, C_L=160pF, R_L=10k\Omega$		6.4		MHz
Setting Time	t_s	$V_{(STEP)PP}=2V, R_L=10k\Omega,$ $A_V=-1, C_L=10pF$	0.1%	1.53		μs
			0.01%	1.83		μs
		$V_{(STEP)PP}=2V, R_L=10k\Omega,$ $A_V=-1, C_L=56pF$	0.1%	3.13		μs
			0.01%	3.33		μs
Phase Margin at Unity Gain	Φ_M	$R_L=10k\Omega, C_L=160pF$		45		$^\circ$
Gain Margin				7		dB

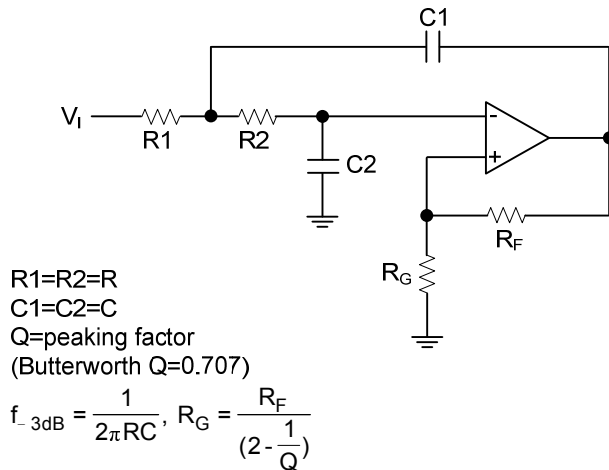
■ TYPICAL APPLICATION CIRCUIT



Driving A Capacitive Load



Single-Pole Low-Pass Filter



2-Pole Low-Pass Sallen-Key Filter

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. UTC reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.