ARM® Cortex®-M4

32-bit Microcontroller

NuMicro® Family
NUC505 Series
Datasheet

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1 GENERAL DESCRIPTION

The NuMicro® NUC505 series 32-bit microcontrollers are embedded with ARM® Cortex®-M4F core for consumer and industrial applications which need high computing power and rich communication interfaces.

The ARM® Cortex®-M4F core within NuMicro® NUC505 series can run up to 100 MHz and support DSP extensions and Floating Point Unit (FPU) function. The NuMicro® NUC505 series supports 128 Kbytes embedded SRAM with zero-wait state and 512 KB/ 2 Mbytes embedded SPI Flash memory, and is equipped with plenty of high performance peripheral devices, such as 24-bit Audio CODEC, USB2.0 High-speed Device, USB2.0 Full-speed Host, and other peripheral.

The NuMicro® NUC505 series is suitable for a wide range of applications such as:

- Audio and Wireless Audio Applications
- Thermal printerDid not find any incorrect format
- GPS Tracker / VTDR (Vehicle Travelling Data Recorder)
- Others high performance or data intensive computing applications

Key Features:

- Core
  - ARM® Cortex®-M4F core running up to 100 MHz (with DSP and FPU)
- Memory
  - 128 KB of SRAM with zero-wait state
  - 512 KB/ 2 MB of SPI Flash
- Security for code protection
  - 128-bit key for code protection against pirating
  - Up to 15 times programming the key
- Clock Control
  - 12 MHz crystal oscillator input
  - Up to two PLLs for system clock and Audio
- Up to 12 Communication interfaces
  - USB 2.0 HS Device interface
  - Up to two USB 2.0 FS Host interfaces
  - Up to three UARTs
  - Up to three SPIs
  - Up to two I²C interfaces (up to 1 MHz)
  - SD Host
- GPIO
  - Supports up to 25/35/52 GPIOs for QFN88/LQFP64/LQFP48 respectively
- Timer
  - Supports four sets of 32-bit timers
  - Supports two watchdog timers (Independent and Window)
- RTC
  - Supports external power pin V_{BAT}
  - 32 bytes spare registers
  - Internal 32.768 kHz RC with calibration
- I^2S
  - Supports Master or Slave mode operation
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports DMA mode
- Audio CODEC
  - Embedded Stereo 24-bit Sigma-Delta CODEC
  - MIC/LINE-In-THDN: -80 dB, Dynamic Range SNR: 90 dB (A-Weighted)
  - Headphone Output-THDN:-60dB, Dynamic Range SNR: 93 dB (A-Weighted)
  - Sample Rate: 8 kHz to 96 kHz
- 12-bit ADC
  - Analog input voltage range: 0~ AV_{DD}
  - Supports single 12-bit SAR ADC conversion
  - Up to 8 channels
  - Up to 1 MSPS conversion with ADC_CH1, and up to 200 kSPS with other channels (except ADC_CH0).
- Built-in LDO with operating voltage 3.3V
- Low Voltage Detector (LVD)
  - With 2 levels: 2.8V / 2.6V
- Low Voltage Reset (LVR)
  - Threshold voltage level: 2.4 V
- Packages
  - LQFP48, LQFP64, QFN88
  - Temperature range: -40℃~+85℃

2 FEATURES

2.1 NUC505 Features

- Core
  - ARM® Cortex®-M4F core running up to 100 MHz
  - Supports DSP extension with hardware divider
  - Supports IEEE 754 compliant Floating Point Unit (FPU)
  - Supports Memory Protection Unit (MPU)
  - One 24-bit system timer
  - Supports Power-down mode by WFI and WFE instructions
  - Single-cycle 32-bit hardware multiplier
  - Supports programmable 16 level priorities of Nested Vectored Interrupt Controller (NVIC)
  - Supports programmable mask-able interrupts
  - Boots from SPI Flash Memory or USB Device
- SRAM Memory
  - 128 KB embedded SRAM with zero-wait state
  - Supports byte-, half-word- and word-access
- SPI Memory Interface Controller
  - Supports external SPI Flash memory
  - Supports code protection
  - Supports DMA mode for code transfer from SPI Flash memory to SRAM
  - Supports CPU direct read from SPI Flash memory.
  - Supports standard (1-bit), dual (2-bit), and quad (4-bit) I/O transfer mode
  - Supports general SPI master interface protocol
- Embedded SPI Flash
  - 512 KB/ 2 MB SPI Flash
  - Configurable program code/data allocation
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports ISP update
  - Supports standard (1-bit), dual (2-bit), and quad (4-bit) I/O transfer mode
  - Supports 100 MHz clock for standard I/O transfer mode
  - Supports 80 MHz clock for dual and quad I/O transfer mode
- Security for code protection
  - 128-bit key for code protection against pirating
  - Up to 15 times programming of the key
- Clock Control
  - Built-in 32.768 kHz internal low speed RC oscillator (LIRC) for RTC function,

Watchdog timer and wake-up operation

- Supports 32.768 kHz external low speed crystal oscillator (LXT) for RTC function and low-power system operation
- Supports 12 MHz external high speed crystal oscillator (HXT) for precise timing operation
- Supports one PLL up to 240 MHz for high performance system operation. The external high speed crystal oscillator (HXT) is used as the clock source for the PLL.

- I^2S
  - Supports Master or Slave mode operation
  - Internal PLL for frequency adjustment
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Supports Mono and Stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Each provides two 16-word FIFO data buffers, one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports DMA mode
  - Interface with internal or external audio CODEC
- Audio CODEC
  - Embedded Stereo 24-bit Sigma-Delta CODEC output
  - ADC-THDN: -80 dB, Dynamic Range SNR: 90 dB (A-Weighted)
  - Headphone Output-THDN:-60dB, Dynamic Range SNR: 93 dB (A-Weighted)
  - Sample Rate: 8 kHz to 96 kHz
- USB 2.0 High-speed device
  - 12 programmable endpoints for Control, Bulk IN/OUT, Interrupt and Isochronous transfers
  - 2K-byte buffer
  - Auto suspend function
  - Remote wake-up capability
- USB 2.0 Full-speed host
  - Fully compliant with USB revision 1.1 specification
  - Open Host Controller Interface (OHCI) revision 1.0 compatible
  - Full-speed (12Mbps) and Low-speed (1.5Mbps) device supported
  - Control, Bulk, Interrupt and Isochronous transfers supported
- SD Host Interface
  - Supports SD (Secure Digital) card and SD_HOST interface
  - Compliant with SD Memory Card Specification Version 2.0

- Supports 1 and 4-bit modes
- Supports 50 MHz to achieve 200 Mbps at 3.3V operation
- Supports DMA master

● Timer

- Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
- Independent clock source for each timer
- Provides One-shot, periodic, toggle and continuous counting operation modes
- Supports event counting function to count the event from external pin
- Supports input capture function to capture or reset counter value

● Watchdog Timer

- Supports multiple clock sources from LIRC (default selection), HXT and LXT
- 8 selectable time-out period from 1.6ms ~ 26.0sec (depending on clock source)
- Interrupt or reset selectable on watchdog time-out

● Window Watchdog Timer

- Supports multiple clock sources from LIRC (default selection), HXT and LXT
- Window set by 6-bit counter with 11-bit prescale
- Interrupt or reset selectable on time-out

● GPIO

- Four I/O modes
- CMOS/Schmitt trigger input selectable
- I/O pin configured as interrupt source with edge trigger setting
- Supports 5V-tolerance function (except PA.7~PA.0 and PD.4~PD.2 only support 3.3 V)
- Supports up to 52/35(34)/25(18) GPIOs for QFN88/LQFP64/LQFP48 respectively

● UART

- Supports up to three UARTs – UART0, UART1 and UART2
- Supports 16-byte FIFOs with programmable level trigger with UART0
- Supports 64-byte FIFOs with programmable level trigger with UART1 and UART2
- Supports auto flow control (nCTS and nRTS) with UART1 and UART2
- Supports IrDA (SIR) function
- Supports RS-485 9-bit mode and direction control
- UART1 and UART2 support LIN function
- Programmable baud-rate generator up to 1/16 system clock
- Supports nCTS and data wake-up function

● SPI

- Supports two sets of SPI controller – SPI0 and SPI1
- Supports Master or Slave mode operation

- Supports 1-bit Transfer mode
- Configurable bit length of a transfer word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports the byte reorder function
- Supports Byte or Word Suspend mode
- Supports 3-wired, no slave select signal, bi-direction interface
- Supports up to 50 MHz

● I^2C

- Supports up to two sets of I^2C devices
- Supports Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Programmable clocks allow versatile rate control
- Supports multiple address recognition (four slave address with mask option)
- Supports SMBus and PMBus
- Supports speed up to 1Mbps
- Supports multi-address Power-down wake-up function

● PWM

- Four 16-bit timers
- Programmable duty control of output waveform (PWM)
- Auto reload mode or one-shot pulse mode
- Capture and compare function

● RTC

- Supports external power pin RTC_VDD33
- Supports 32.768 kHz crystal oscillation circuit
- Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
- Supports Alarm registers (second, minute, hour, day, month, year)
- Supports 32 bytes spare registers
- Wake up from Deep Power-down mode or from Power-down mode
- Supports wake up from Power-down mode by input pin

- Supports chip Power-off by register setting
- Supports Power-on time-out for low battery protection

- Analog to Digital Converter
  - Analog input voltage range: 0~ AV_{DD}
  - Supports single 12-bit SAR ADC conversion
  - 12-bit resolution and 10-bit accuracy is guaranteed
  - Up to 1MSPS conversion with ADC_CH1, and up to 200 kSPS with others (except ADC_CH0).
  - Up to 8 external single-ended analog input channels
  - Supports single ADC interrupt
  - An A/D conversion can be triggered by software control
- Built-in LDO with operating voltage 3.3V
- Low Voltage Detector (LVD)
  - With 2 levels: 2.8V / 2.6V
- Low Voltage Reset (LVR)
  - Threshold voltage level: 2.4 V
- Power Management
  - Advanced power management including Deep Power-down, Power-down, Idle and Normal Operating modes
  - Normal Operating mode
    - CPU runs normally and all clocks on; the current consumption is around 46 mA (at 96 MHz CPU clock)
  - Idle mode
    - CPU clock stop, and all other clocks on
  - Power-down mode
    - All clocks stop, except LXT and LIRC, with SRAM retention; the current consumption is around 700 uA
  - Deep Power-down mode
    - All clocks stop, except LXT and LIRC, without SRAM retention; the current consumption is around 7 uA
- Operating Temperature: -40℃~+85℃
- Packages
  - All Green package (RoHS)
  - QFN 88-pin (10mm x 10mm)
  - LQFP 64-pin (7mm x 7mm)
  - LQFP 48-pin (7mm x 7mm)
  - QFN 48-pin (7mm x 7mm)

3 ABBREVIATIONS

3.1 Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
DMA	Direct Memory Access
FIFO	First In, First Out
FPU	Floating Point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HXT	12 MHz External High Speed Crystal Oscillator
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	32.768 kHz Internal Low Speed RC Oscillator
LXT	32.768 kHz External Low Speed Crystal Oscillator
LVD	Low Voltage Detection
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
SD	Secure Digital
SPI	Serial Peripheral Interface
SPIM	Serial Master Interface Controller
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3.1-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 Selection Guide

4.1.1 NuMicro® NUC505 Base Series Selection Guide

[1]: *√ marked in the table means that only NUC505DS13Y supports Headphone Out.

[2]: The packages are not pin-to-pin compatible even though they are the same packages. LQFP64*: 7x7mm

Part Number	Serial Flash (KB)	SRAM (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity				I²S	USB 2.0 HS Device	USB 2.0 FS Host	PWM (16-Bit)	24-Bit Audio CODEC[1]	DIGITAL MIC	ADC (12-Bit)	RTC	ISP/ICP	Package[2]
						I²C	SD HOST	SPI	UART										
NUC505DLA	512	128	8	18	4	2	-	3	2	1	1	-	-	√	1	5CH	-	√	LQFP48
NUC505DL13Y	2048	128	8	25	4	2	1	3	3	1	1	1	4	-	1	5CH	√	√	LQFP48
NUC505YLA	512	128	8	18	4	2	-	3	2	1	1	-	-	√	1	5CH	-	√	QFN48
NUC505YLA2Y	512	128	8	25	4	2	1	3	3	1	1	1	4	-	1	5CH	√	√	QFN48
NUC505DSA	512	128	8	34	4	2	1	3	3	1	1	1	4	√	1	5CH	-	√	LQFP64*
NUC505DS13Y	2048	128	8	35	4	2	1	3	3	1	1	1	4	√*	1	8CH	√	√	LQFP64*
NUC505YO13Y	2048	128	8	52	4	2	1	3	3	1	1	2	4	√	1	8CH	√	√	QFN88

Table 4.1-1 NuMicro® NUC505 Base Series Selection Guide

4.1.2 NuMicro® NUC505 Base Series Naming Rule

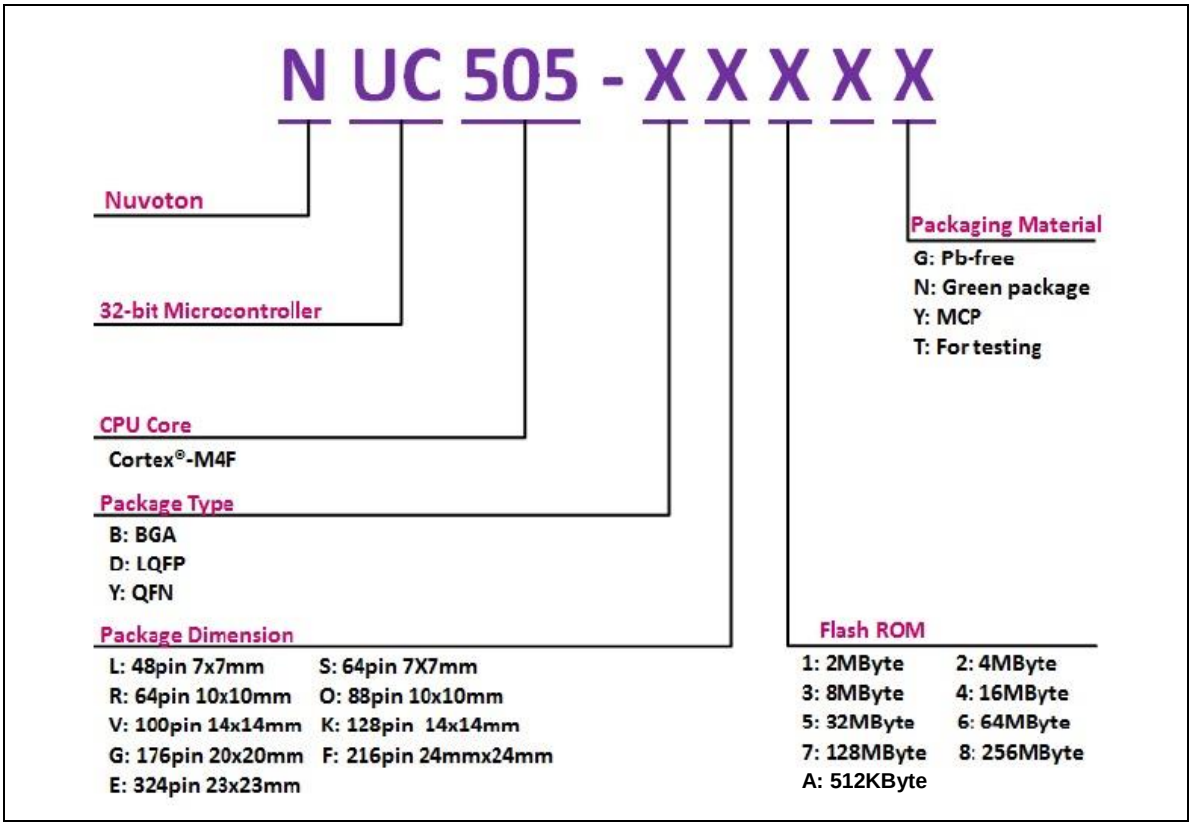


Figure 4.1-1 NuMicro® NUC505 Base Series Selection Code

4.2 Pin Configuration

4.2.1 NuMicro® NUC505DLA LQFP 48-pin

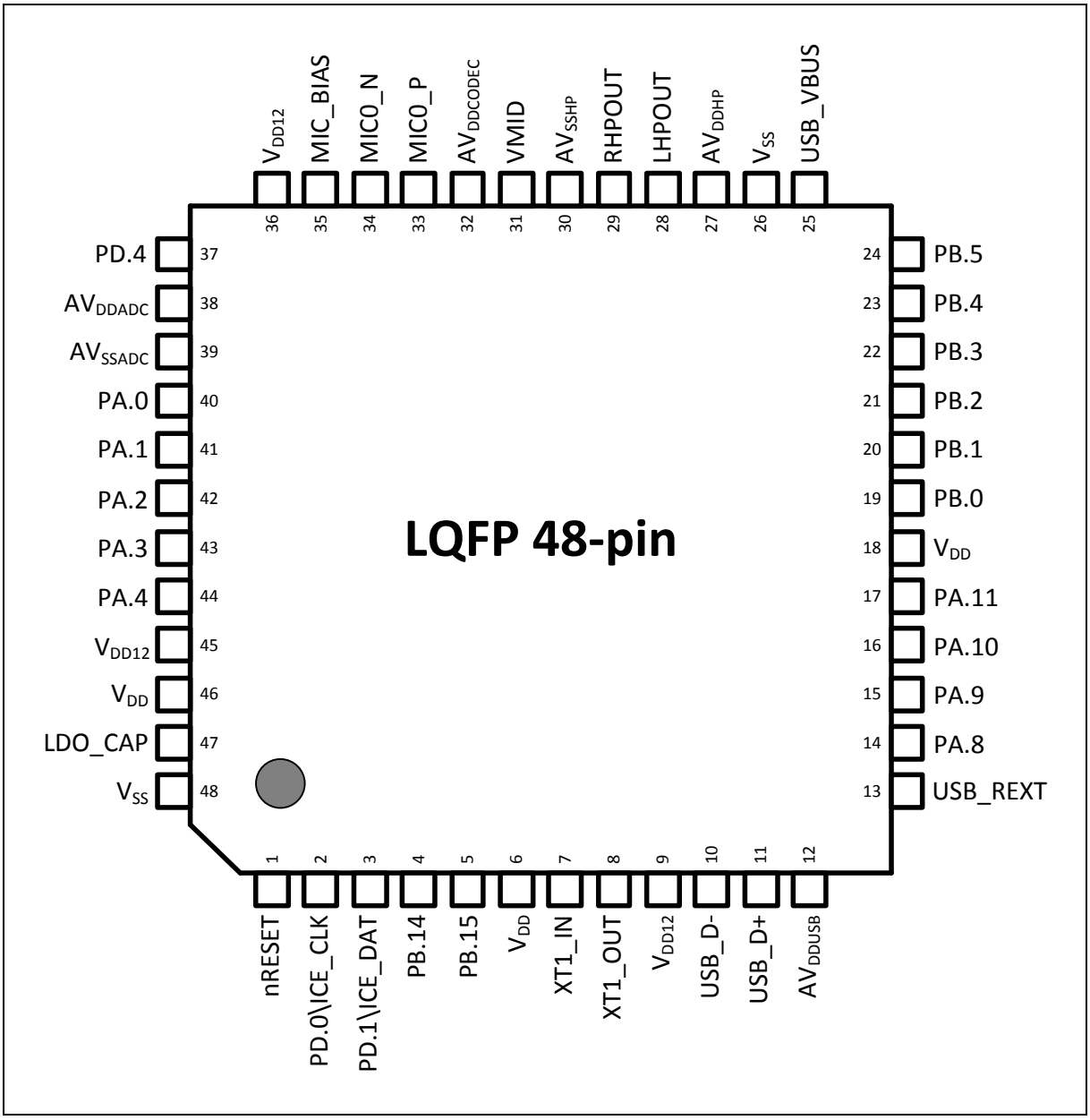


Figure 4.2-1 NuMicro® NUC505DLA LQFP 48-pin Diagram

4.2.2 NuMicro® NUC505DL13Y LQFP 48-pin

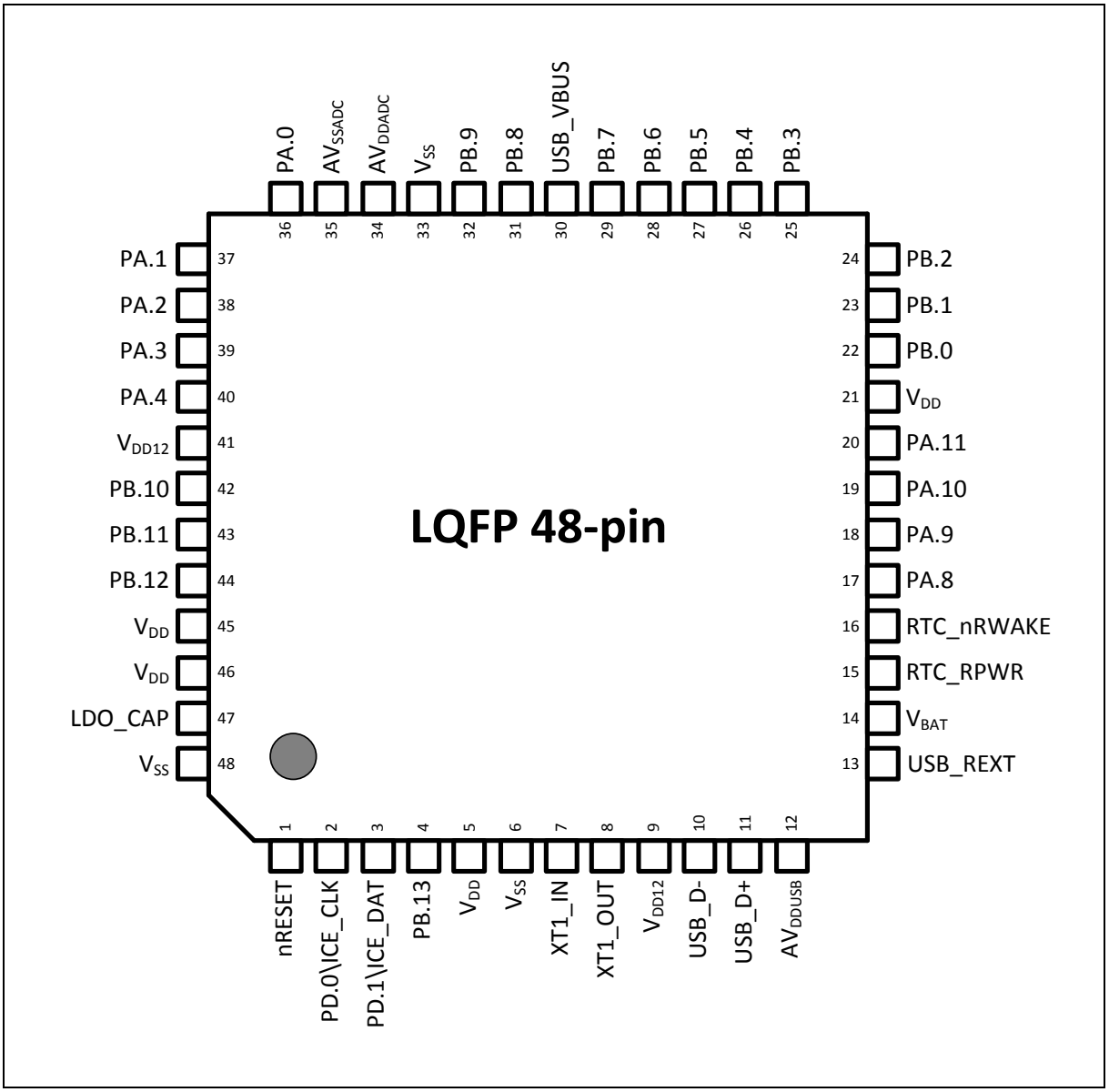


Figure 4.2-2 NuMicro® NUC505DL13Y LQFP 48-pin Diagram

4.2.3 NuMicro® NUC505YLA QFN 48-pin

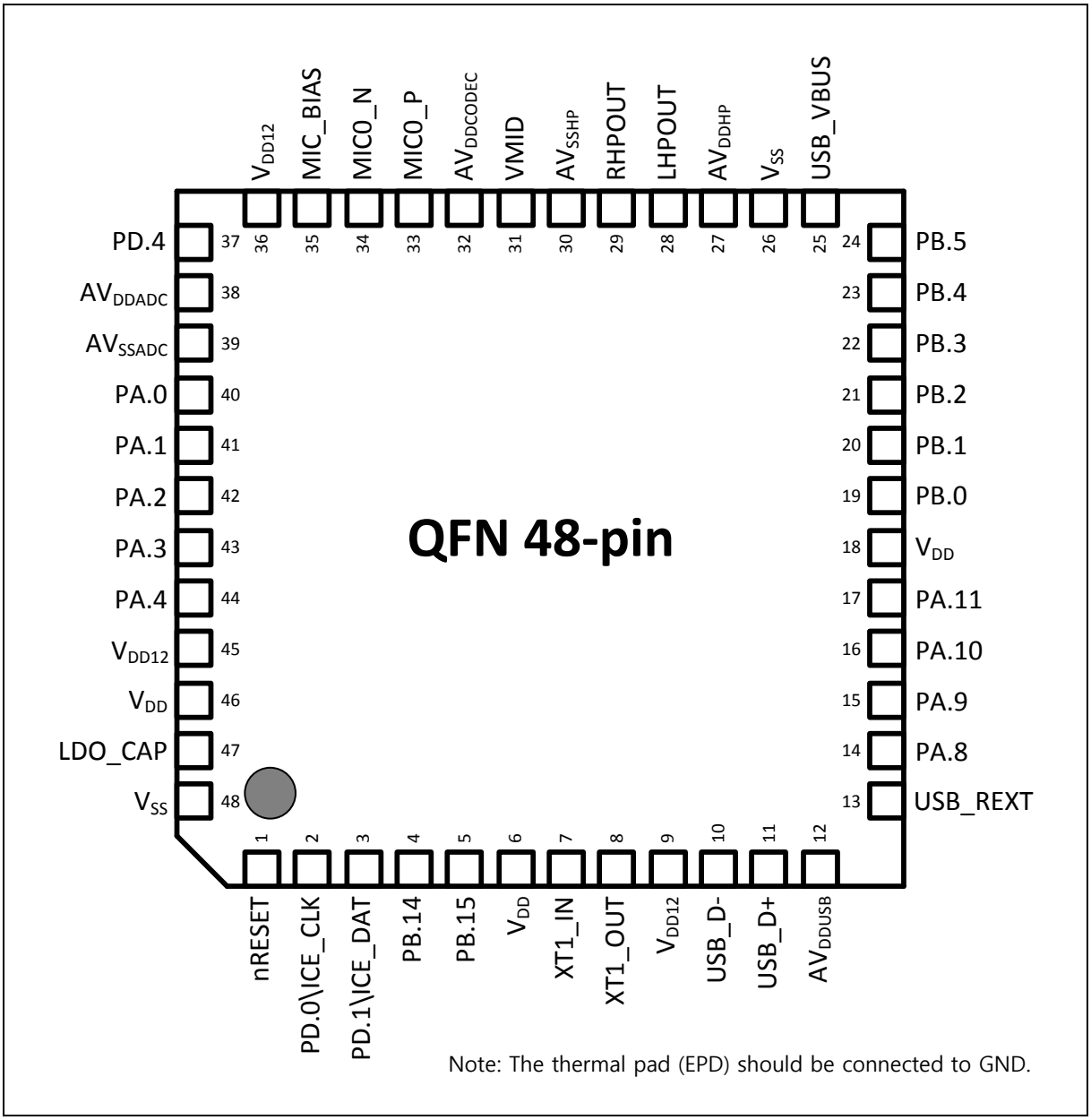
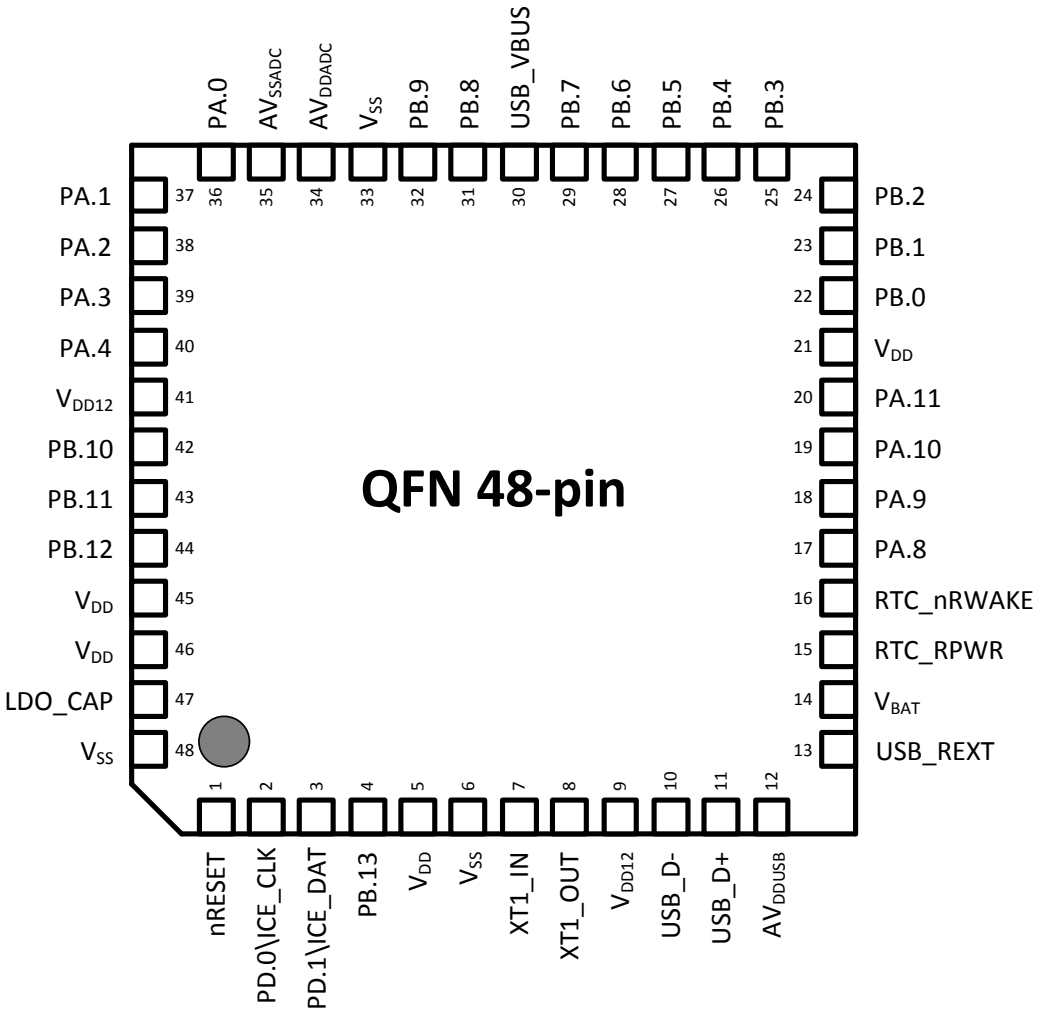


Figure 4.2-3 NuMicro® NUC505YLA QFN 48-pin Diagram

4.2.4 NuMicro® NUC505YLA2Y QFN 48-pin



Note: The thermal pad (EPD) should be connected to GND.

Figure 4.2-4 NuMicro® NUC505YLA2Y QFN 48-pin Diagram

4.2.5 NuMicro® NUC505DSA LQFP 64-pin

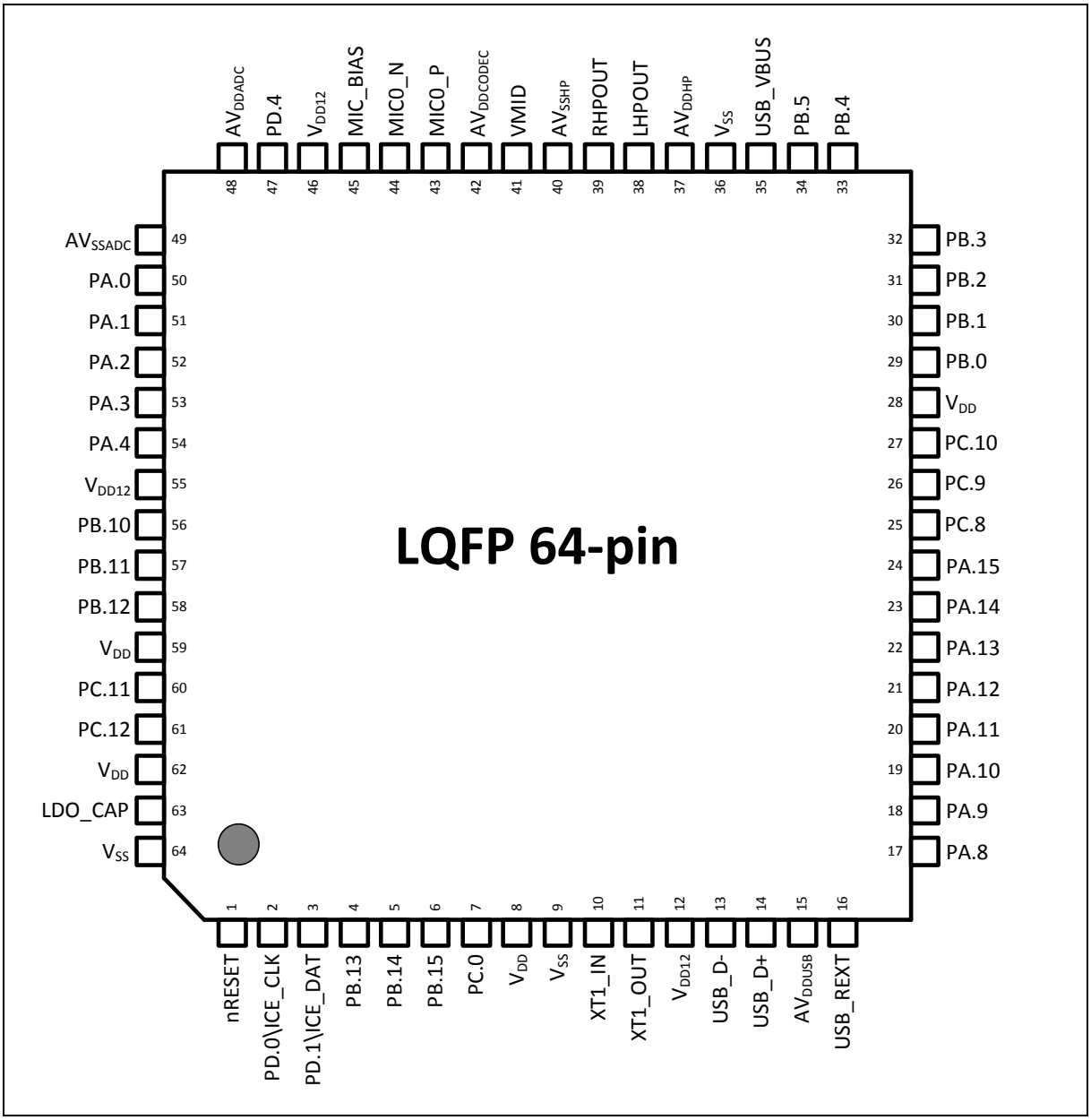


Figure 4.2-5 NuMicro® NUC505DSA LQFP 64-pin Diagram

4.2.6 NuMicro® NUC505DS13Y LQFP 64-pn

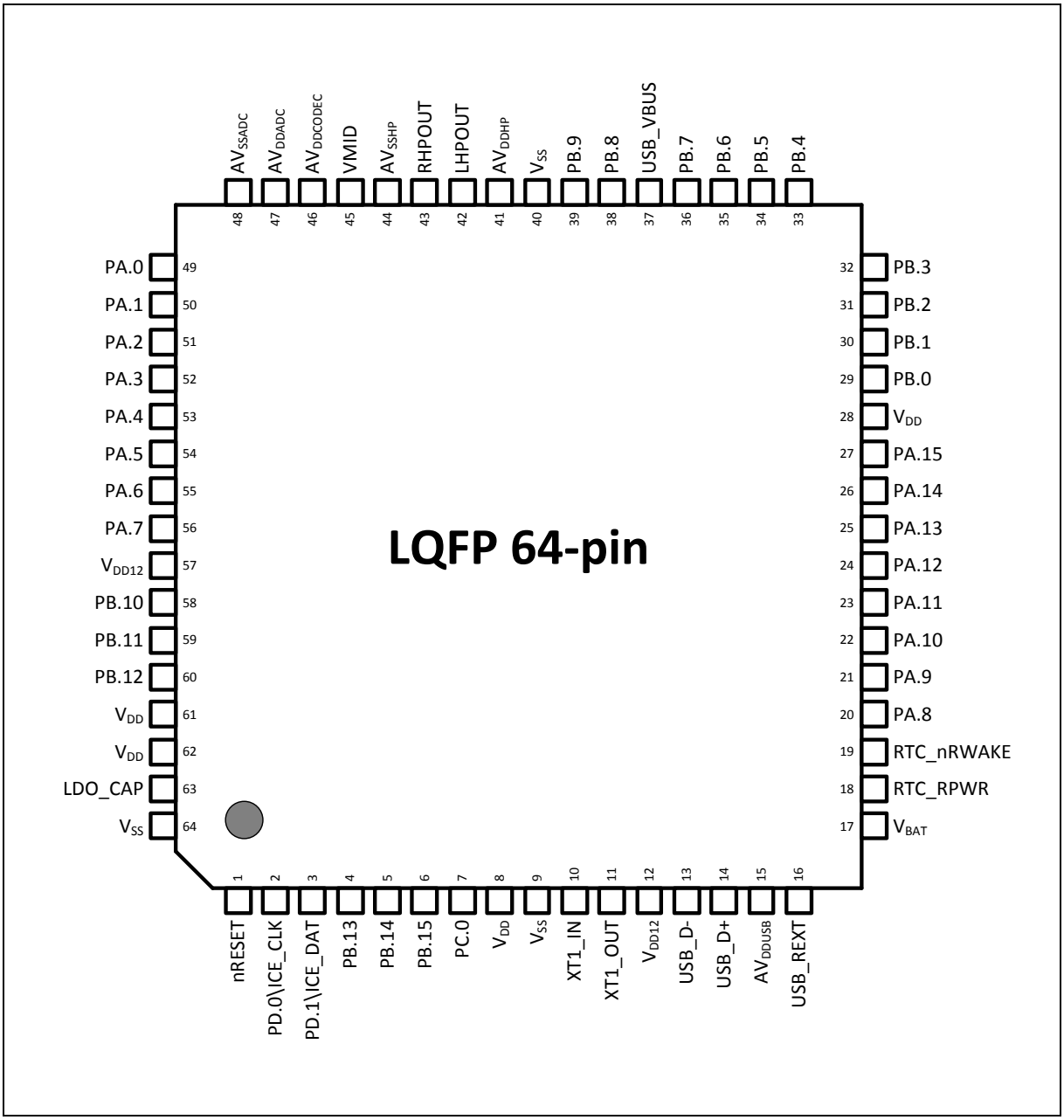
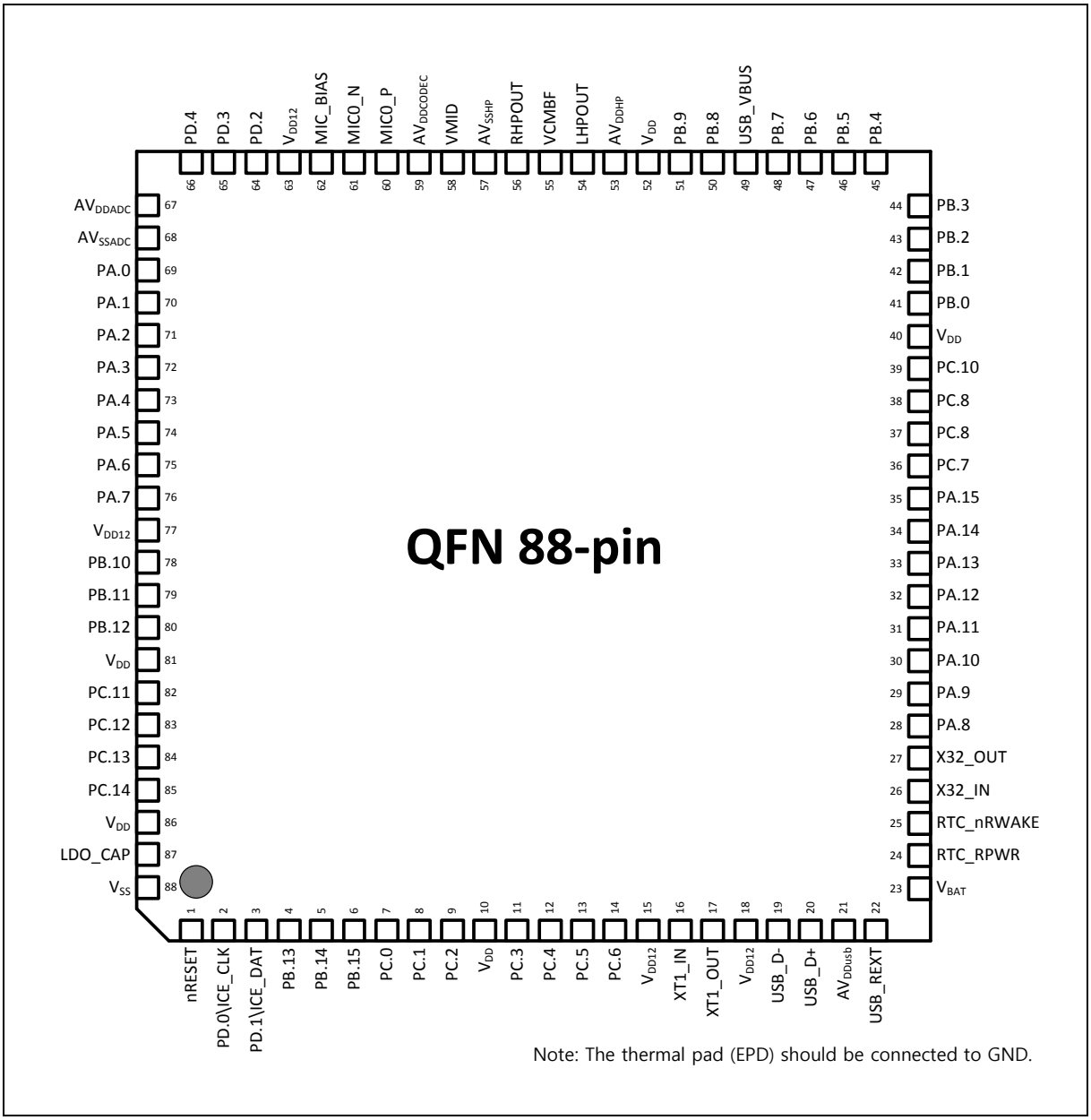


Figure 4.2-6 NuMicro® NUC505DS13Y LQFP 64-pin Diagram

4.2.7 NuMicro® NUC505YO13Y QFN 88-pin



Note: The thermal pad (EPD) should be connected to GND.

Figure 4.2-7 NuMicro® NUC505YO13Y QFN 88-pin Diagram

4.3 Pin Description

4.3.1 NuMicro® NUC505DLA LQFP 48-pin Description

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFPL and SYS_GPx_MFPH)

PA.0 MFP0 means SYS_GPA_MFPL[2:0]=0x0.

PA.9 MFP5 means SYS_GPA_MFPH[6:4]=0x5.

Pin No.	Pin Name	Type	MFP*	Description
1	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
2	ICE_CLK	O	MFP0	Serial wired debugger clock pin. (In ICE mode)
	PD.0	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I^2C0 clock pin.
3	ICE_DAT	I/O	MFP0	Serial wired debugger data pin. (In ICE mode)
	PD.1	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP2	I^2C0 data input/output pin.
4	PB.14	I/O	MFP0	General purpose digital I/O pin.
	USBH1_D+	I/O	MFP1	USB host-lite 1differential signal D+.
	I2C1_SCL	O	MFP2	I2C1 clock pin.
5	PB.15	I/O	MFP0	General purpose digital I/O pin.
	USBH1_D-	I/O	MFP1	USB host-lite 1 differential signal D-.
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
6	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
7	XT1_IN	I	MFP0	External 12 MHz (high speed) crystal input pin.
8	XT1_OUT	O	MFP0	External 12 MHz (high speed) crystal output pin.
9	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
10	USB_D-	A	MFP0	USB differential signal D-.
11	USB_D+	A	MFP0	USB differential signal D+.
12	AV_{DDUSB}	A	MFP0	Power supply for analog USB, DC 3.3V.
13	USB_REXT	A	MFP0	12.1 KΩ used internally for USB circuitry.

14	PA.8	I/O	MFP0	General purpose digital I/O pin.
	SPIM_SS	O	MFP1	SPIM slave select pin.
	I2S_LRCLK	I/O	MFP2	I^2S left right channel clock.
	UART1_TXD	O	MFP3	Data transmitter output pin for UART1.
15	PA.9	I/O	MFP0	General purpose digital I/O pin.
	SPIM_CLK	O	MFP1	SPIM serial clock pin.
	I2S_BCLK	I/O	MFP2	I^2S bit clock pin.
	UART1_RXD	I	MFP3	Data receiver input pin for UART1.
	SYSCFG[0]	I	MFP0	System configuration setting bit 0.
16	PA.10	I/O	MFP0	General purpose digital I/O pin.
	SPIM_MOSI	I/O	MFP1	SPIM MOSI (Master Out, Slave In) pin.
	I2C1_SCL	O	MFP2	I2C1 clock pin.
	SD_CLK	O	MFP4	SD/SDH mode - clock.
	SYSCFG[1]	I	MFP0	System configuration setting bit 1.
17	PA.11	I/O	MFP0	General purpose digital I/O pin.
	SPIM_MISO	I/O	MFP1	SPIM MISO (Master In, Slave Out) pin.
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
	SD_CMD	I	MFP4	SD/SDH mode – command/response.
18	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
19	PB.0	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I2C0 clock pin.
	UART0_TXD	O	MFP3	Data transmitter output pin for UART0.
	SD_DAT2	I/O	MFP4	SD/SDH mode data line bit 2.
20	PB.1	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
	UART0_RXD	I	MFP3	Data receiver input pin for UART0.
	SD_DAT3	I/O	MFP4	SD/SDH mode data line bit 3.

21	PB.2	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS	O	MFP1	SPI0 slave select pin.
	SD_CMD	I	MFP4	SD/SDH mode – command/response.
22	PB.3	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	O	MFP1	SPI0 serial clock pin.
	SD_CLK	O	MFP4	SD/SDH mode – clock.
	SYSCFG[2]	I	MFP0	System configuration setting bit 2.
23	PB.4	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	O	MFP1	SPI0 MOSI (Master Out, Slave In) pin.
	SYSCFG[3]	I	MFP0	System configuration setting bit 3.
24	PB.5	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I	MFP1	SPI0 MISO (Master In, Slave Out) pin.
	SD_nCD	I	MFP4	SD/SDH mode – card detect.
25	USB_VBUS	I	MFP0	Power supply from USB host or HUB.
26	V_{SS}	A	MFP0	Ground
27	AV_{DDHP}	A	MFP0	Power supply for analog CODEC headphone, DC 3.3V.
28	LHPOUT	A	MFP0	Headphone left channel output pin.
29	RHPOUT	A	MFP0	Headphone right channel output pin.
30	AV_{SSHP}	A	MFP0	Ground for analog CODEC headphone.
31	VMID	A	MFP0	Headphone reference power.
32	$AV_{DDCODEC}$	A	MFP0	Power supply for analog CODEC, DC 3.3V.
33	MIC0_P	A	MFP0	Microphone 0 positive input.
34	MIC0_N	A	MFP0	Microphone 0 negative input.
35	MIC_BIAS	A	MFP0	CODEC left line-in channel or Microphone bias.
36	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
37	PD.4	I/O	MFP0	General purpose digital I/O pin.
	RLINEIN	A	MFP1	CODEC right line-in channel.

38	AV_{DDADC}	A	MFP0	Power supply for analog SAR-ADC, DC 3.3V.
39	AV_{SSADC}	A	MFP0	Ground pin for analog SAR-ADC.
40	PA.0	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH0	A	MFP1	ADC channel 0 analog input.
41	PA.1	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH1	A	MFP1	ADC channel 1 analog input.
42	PA.2	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH2	A	MFP1	ADC channel 2 analog input.
	I2S_MCLK	O	MFP2	I^2S master clock output pin.
43	PA.3	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH3	A	MFP1	ADC channel 3 analog input.
	I2S_DI	I	MFP2	I^2S data input.
44	PA.4	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH4	A	MFP1	ADC channel 4 analog input.
	I2S_DO	O	MFP2	I^2S data output.
45	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
46	V_{DD}	A	MFP0	Power supply, DC 3.3V.
47	LDO_CAP	A	MFP0	LDO output pin.
48	V_{SS}	A	MFP0	Ground.

4.3.2 NuMicro® NUC505DL13Y LQFP 48-pin Description

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFPL and SYS_GPx_MFPH)

PA.0 MFP0 means SYS_GPA_MFPL[2:0]=0x0.

PA.9 MFP5 means SYS_GPA_MFPH[6:4]=0x5.

Pin No.	Pin Name	Type	MFP*	Description
1	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
2	ICE_CLK	O	MFP0	Serial wired debugger clock pin. (In ICE mode)
	PD.0	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I^2C0 clock pin.
3	ICE_DAT	I/O	MFP0	Serial wired debugger data pin. (In ICE mode)
	PD.1	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP2	I^2C0 data input/output pin.
4	PB.13	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO	I	MFP1	SPI1 MISO (Master In, Slave Out) pin.
	USBH1_D-	I/O	MFP2	USB host-lite 1 differential signal D-.
	UART2_nRTS	O	MFP3	Request to Send output pin for UART2.
	PWM_CH3	I/O	MFP4	PWM channel3 output/capture input.
5	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
6	V_{SS}	A	MFP0	Ground.
7	XT1_IN	I	MFP0	External 12 MHz (high speed) crystal input pin.
8	XT1_OUT	O	MFP0	External 12 MHz (high speed) crystal output pin.
9	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
10	USB_D-	A	MFP0	USB differential signal D-.
11	USB_D+	A	MFP0	USB differential signal D+.
12	AV_{DDUSB}	A	MFP0	Power supply for analog USB, DC 3.3V.
13	USB_REXT	A	MFP0	12.1 KΩ used internally for USB circuitry.
14	V_{BAT}	A	MFP0	Power supply by batteries for RTC, DC 3.3V.

15	RTC_RPWR	O	MFP0	Enable external power control source when active high.
16	RTC_nRWAKE	I	MFP0	System power enable trigger when active low.
17	PA.8	I/O	MFP0	General purpose digital I/O pin.
	SPIM_SS	O	MFP1	SPIM slave select pin.
	I2S_LRCLK	I/O	MFP2	I^2S left right channel clock.
	UART1_TXD	O	MFP3	Data transmitter output pin for UART1.
18	PA.9	I/O	MFP0	General purpose digital I/O pin.
	SPIM_CLK	O	MFP1	SPIM serial clock pin.
	I2S_BCLK	I/O	MFP2	I^2S bit clock pin.
	UART1_RXD	I	MFP3	Data receiver input pin for UART1.
	SYSCFG[0]	I	MFP0	System configuration setting bit 0.
19	PA.10	I/O	MFP0	General purpose digital I/O pin.
	SPIM_MOSI	I/O	MFP1	SPIM MOSI (Master Out, Slave In) pin.
	I2C1_SCL	O	MFP2	I2C1 clock pin.
	SD_CLK	O	MFP4	SD/SDH mode - clock.
	SYSCFG[1]	I	MFP0	System configuration setting bit 1.
20	PA.11	I/O	MFP0	General purpose digital I/O pin.
	SPIM_MISO	I/O	MFP1	SPIM MISO (Master In, Slave Out) pin.
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
	SD_CMD	I	MFP4	SD/SDH mode – command/response.
21	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
22	PB.0	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I2C0 clock pin.
	UART0_TXD	O	MFP3	Data transmitter output pin for UART0.
	SD_DAT2	I/O	MFP4	SD/SDH mode data line bit 2.
23	PB.1	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.

	UART0_RXD	I	MFP3	Data receiver input pin for UART0.
	SD_DAT3	I/O	MFP4	SD/SDH mode data line bit 3.
24	PB.2	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS	O	MFP1	SPI0 slave select pin.
	SD_CMD	I	MFP4	SD/SDH mode – command/response.
25	PB.3	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	O	MFP1	SPI0 serial clock pin.
	SD_CLK	O	MFP4	SD/SDH mode – clock.
	SYSCFG[2]	I	MFP0	System configuration setting bit 2.
26	PB.4	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	O	MFP1	SPI0 MOSI (Master Out, Slave In) pin.
	SYSCFG[3]	I	MFP0	System configuration setting bit 3.
27	PB.5	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I	MFP1	SPI0 MISO (Master In, Slave Out) pin.
	SD_nCD	I	MFP4	SD/SDH mode – card detect.
28	PB.6	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP3	Data transmitter output pin for UART1.
	SD_DAT0	I/O	MFP4	SD/SDH mode data line bit 0.
29	PB.7	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP3	Data receiver input pin for UART1.
	SD_DAT1	I/O	MFP4	SD/SDH mode data line bit 1.
30	USB_VBUS	I	MFP0	Power supply from USB host or HUB.
31	PB.8	I/O	MFP0	General purpose digital I/O pin.
	USBH_PWEN	O	MFP1	USB host mode to control an external overcurrent source.
	TM1_CNT_OUT	I/O	MFP2	Timer1 event counter input/toggle output.
	UART1_nCTS	I	MFP3	Clear to Send input pin for UART1.
	SD_DAT2	I/O	MFP4	SD/SDH mode data line bit 2.

32	PB.9	I/O	MFP0	General purpose digital I/O pin.
	USBH_OVD	I	MFP1	USB host bus power over voltage detector.
	TM1_EXT	I	MFP2	Timer1 external capture input.
	UART1_nRTS	O	MFP3	Request to Send output pin for UART1.
	SD_DAT3	I/O	MFP4	SD/SDH mode data line bit 3.
33	V_{SS}	A	MFP0	Ground
34	AV_{DDADC}	A	MFP0	Power supply for analog SAR-ADC, DC 3.3V.
35	AV_{SSADC}	A	MFP0	Ground pin for analog SAR-ADC.
36	PA.0	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH0	A	MFP1	ADC channel 0 analog input.
37	PA.1	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH1	A	MFP1	ADC channel 1 analog input.
38	PA.2	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH2	A	MFP1	ADC channel 2 analog input.
	I2S_MCLK	O	MFP2	I^2S master clock output pin.
39	PA.3	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH3	A	MFP1	ADC channel 3 analog input.
	I2S_DI	I	MFP2	I^2S data input.
40	PA.4	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH4	A	MFP1	ADC channel 4 analog input.
	I2S_DO	O	MFP2	I^2S data output.
41	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
42	PB.10	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS	O	MFP1	SPI1 slave select pin.
	I2C1_SCL	O	MFP2	I2C1 clock pin.
	UART2_TXD	O	MFP3	Data transmitter output pin for UART2.
	PWM_CH0	I/O	MFP4	PWM channel0 output/capture input.

43	PB.11	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	O	MFP1	SPI1 serial clock pin.
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
	UART2_RXD	I	MFP3	Data receiver input pin for UART2.
	PWM_CH1	I/O	MFP4	PWM channel1 output/capture input.
44	PB.12	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI	O	MFP1	SPI1 MOSI (Master Out, Slave In) pin.
	USBH1_D+	I/O	MFP2	USB host-lite 1 differential signal D+
	UART2_nCTS	I	MFP3	Clear to send input pin for UART2.
	PWM_CH2	I/O	MFP4	PWM channel2 output/capture input.
45	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
46	V_{DD}	A	MFP0	Power supply, DC 3.3V.
47	LDO_CAP	A	MFP0	LDO output pin.
48	V_{SS}	A	MFP0	Ground.

4.3.3 NuMicro® NUC505YLA QFN 48-pin Description

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFPL and SYS_GPx_MFPH)

PA.0 MFP0 means SYS_GPA_MFPL[2:0]=0x0.

PA.9 MFP5 means SYS_GPA_MFPH[6:4]=0x5.

Pin No.	Pin Name	Type	MFP*	Description
1	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
2	ICE_CLK	O	MFP0	Serial wired debugger clock pin. (In ICE mode)
	PD.0	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I^2C0 clock pin.
3	ICE_DAT	I/O	MFP0	Serial wired debugger data pin. (In ICE mode)
	PD.1	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP2	I^2C0 data input/output pin.
4	PB.14	I/O	MFP0	General purpose digital I/O pin.
	USBH1_D+	I/O	MFP1	USB host-lite 1differential signal D+.
	I2C1_SCL	O	MFP2	I2C1 clock pin.
5	PB.15	I/O	MFP0	General purpose digital I/O pin.
	USBH1_D-	I/O	MFP1	USB host-lite 1 differential signal D-.
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
6	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
7	XT1_IN	I	MFP0	External 12 MHz (high speed) crystal input pin.
8	XT1_OUT	O	MFP0	External 12 MHz (high speed) crystal output pin.
9	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
10	USB_D-	A	MFP0	USB differential signal D-.
11	USB_D+	A	MFP0	USB differential signal D+.
12	AV_{DDUSB}	A	MFP0	Power supply for analog USB, DC 3.3V.
13	USB_REXT	A	MFP0	12.1 KΩ used internally for USB circuitry.
14	PA.8	I/O	MFP0	General purpose digital I/O pin.

	SPIM_SS	O	MFP1	SPIM slave select pin.
	I2S_LRCLK	I/O	MFP2	I^2S left right channel clock.
	UART1_TXD	O	MFP3	Data transmitter output pin for UART1.
15	PA.9	I/O	MFP0	General purpose digital I/O pin.
	SPIM_CLK	O	MFP1	SPIM serial clock pin.
	I2S_BCLK	I/O	MFP2	I^2S bit clock pin.
	UART1_RXD	I	MFP3	Data receiver input pin for UART1.
	SYSCFG[0]	I	MFP0	System configuration setting bit 0.
16	PA.10	I/O	MFP0	General purpose digital I/O pin.
	SPIM_MOSI	I/O	MFP1	SPIM MOSI (Master Out, Slave In) pin.
	I2C1_SCL	O	MFP2	I2C1 clock pin.
	SD_CLK	O	MFP4	SD/SDH mode - clock.
	SYSCFG[1]	I	MFP0	System configuration setting bit 1.
17	PA.11	I/O	MFP0	General purpose digital I/O pin.
	SPIM_MISO	I/O	MFP1	SPIM MISO (Master In, Slave Out) pin.
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
	SD_CMD	I	MFP4	SD/SDH mode – command/response.
18	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
19	PB.0	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I2C0 clock pin.
	UART0_TXD	O	MFP3	Data transmitter output pin for UART0.
	SD_DAT2	I/O	MFP4	SD/SDH mode data line bit 2.
20	PB.1	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
	UART0_RXD	I	MFP3	Data receiver input pin for UART0.
	SD_DAT3	I/O	MFP4	SD/SDH mode data line bit 3.
21	PB.2	I/O	MFP0	General purpose digital I/O pin.

	SPI0_SS	O	MFP1	SPI0 slave select pin.
	SD_CMD	I	MFP4	SD/SDH mode – command/response.
22	PB.3	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	O	MFP1	SPI0 serial clock pin.
	SD_CLK	O	MFP4	SD/SDH mode – clock.
	SYSCFG[2]	I	MFP0	System configuration setting bit 2.
23	PB.4	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	O	MFP1	SPI0 MOSI (Master Out, Slave In) pin.
	SYSCFG[3]	I	MFP0	System configuration setting bit 3.
24	PB.5	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I	MFP1	SPI0 MISO (Master In, Slave Out) pin.
	SD_nCD	I	MFP4	SD/SDH mode – card detect.
25	USB_VBUS	I	MFP0	Power supply from USB host or HUB.
26	V_{SS}	A	MFP0	Ground
27	AV_{DDHP}	A	MFP0	Power supply for analog CODEC headphone, DC 3.3V.
28	LHPOUT	A	MFP0	Headphone left channel output pin.
29	RHPOUT	A	MFP0	Headphone right channel output pin.
30	AV_{SSHP}	A	MFP0	Ground for analog CODEC headphone.
31	VMID	A	MFP0	Headphone reference power.
32	$AV_{DDCODEC}$	A	MFP0	Power supply for analog CODEC, DC 3.3V.
33	MIC0_P	A	MFP0	Microphone 0 positive input.
34	MIC0_N	A	MFP0	Microphone 0 negative input.
35	MIC_BIAS	A	MFP0	CODEC left line-in channel or Microphone bias.
36	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
37	PD.4	I/O	MFP0	General purpose digital I/O pin.
	RLINEIN	A	MFP1	CODEC right line-in channel.
38	AV_{DDADC}	A	MFP0	Power supply for analog SAR-ADC, DC 3.3V.

39	AV_{SSADC}	A	MFP0	Ground pin for analog SAR-ADC.
40	PA.0	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH0	A	MFP1	ADC channel 0 analog input.
41	PA.1	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH1	A	MFP1	ADC channel 1 analog input.
42	PA.2	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH2	A	MFP1	ADC channel 2 analog input.
	I2S_MCLK	O	MFP2	I^2S master clock output pin.
43	PA.3	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH3	A	MFP1	ADC channel 3 analog input.
	I2S_DI	I	MFP2	I^2S data input.
44	PA.4	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH4	A	MFP1	ADC channel 4 analog input.
	I2S_DO	O	MFP2	I^2S data output.
45	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
46	V_{DD}	A	MFP0	Power supply, DC 3.3V.
47	LDO_CAP	A	MFP0	LDO output pin.
48	V_{SS}	A	MFP0	Ground.

Note: The thermal pad (EPD) on the bottom of QFN package should be connected to GND.

4.3.4 NuMicro® NUC505YLA2Y QFN 48-pin Description

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFPL and SYS_GPx_MFPH)

PA.0 MFP0 means SYS_GPA_MFPL[2:0]=0x0.

PA.9 MFP5 means SYS_GPA_MFPH[6:4]=0x5.

Pin No.	Pin Name	Type	MFP*	Description
1	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
2	ICE_CLK	O	MFP0	Serial wired debugger clock pin. (In ICE mode)
	PD.0	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I^2C0 clock pin.
3	ICE_DAT	I/O	MFP0	Serial wired debugger data pin. (In ICE mode)
	PD.1	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP2	I^2C0 data input/output pin.
4	PB.13	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO	I	MFP1	SPI1 MISO (Master In, Slave Out) pin.
	USBH1_D-	I/O	MFP2	USB host-lite 1 differential signal D-.
	UART2_nRTS	O	MFP3	Request to Send output pin for UART2.
	PWM_CH3	I/O	MFP4	PWM channel3 output/capture input.
5	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
6	V_{SS}	A	MFP0	Ground.
7	XT1_IN	I	MFP0	External 12 MHz (high speed) crystal input pin.
8	XT1_OUT	O	MFP0	External 12 MHz (high speed) crystal output pin.
9	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
10	USB_D-	A	MFP0	USB differential signal D-.
11	USB_D+	A	MFP0	USB differential signal D+.
12	AV_{DDUSB}	A	MFP0	Power supply for analog USB, DC 3.3V.
13	USB_REXT	A	MFP0	12.1 KΩ used internally for USB circuitry.
14	V_{BAT}	A	MFP0	Power supply by batteries for RTC, DC 3.3V.

15	RTC_RPWR	O	MFP0	Enable external power control source when active high.
16	RTC_nRWAKE	I	MFP0	System power enable trigger when active low.
17	PA.8	I/O	MFP0	General purpose digital I/O pin.
	SPIM_SS	O	MFP1	SPIM slave select pin.
	I2S_LRCLK	I/O	MFP2	I^2S left right channel clock.
	UART1_TXD	O	MFP3	Data transmitter output pin for UART1.
18	PA.9	I/O	MFP0	General purpose digital I/O pin.
	SPIM_CLK	O	MFP1	SPIM serial clock pin.
	I2S_BCLK	I/O	MFP2	I^2S bit clock pin.
	UART1_RXD	I	MFP3	Data receiver input pin for UART1.
	SYSCFG[0]	I	MFP0	System configuration setting bit 0.
19	PA.10	I/O	MFP0	General purpose digital I/O pin.
	SPIM_MOSI	I/O	MFP1	SPIM MOSI (Master Out, Slave In) pin.
	I2C1_SCL	O	MFP2	I2C1 clock pin.
	SD_CLK	O	MFP4	SD/SDH mode - clock.
	SYSCFG[1]	I	MFP0	System configuration setting bit 1.
20	PA.11	I/O	MFP0	General purpose digital I/O pin.
	SPIM_MISO	I/O	MFP1	SPIM MISO (Master In, Slave Out) pin.
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
	SD_CMD	I	MFP4	SD/SDH mode – command/response.
21	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
22	PB.0	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I2C0 clock pin.
	UART0_TXD	O	MFP3	Data transmitter output pin for UART0.
	SD_DAT2	I/O	MFP4	SD/SDH mode data line bit 2.
23	PB.1	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.

	UART0_RXD	I	MFP3	Data receiver input pin for UART0.
	SD_DAT3	I/O	MFP4	SD/SDH mode data line bit 3.
24	PB.2	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS	O	MFP1	SPI0 slave select pin.
	SD_CMD	I	MFP4	SD/SDH mode – command/response.
25	PB.3	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	O	MFP1	SPI0 serial clock pin.
	SD_CLK	O	MFP4	SD/SDH mode – clock.
	SYSCFG[2]	I	MFP0	System configuration setting bit 2.
26	PB.4	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	O	MFP1	SPI0 MOSI (Master Out, Slave In) pin.
	SYSCFG[3]	I	MFP0	System configuration setting bit 3.
27	PB.5	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I	MFP1	SPI0 MISO (Master In, Slave Out) pin.
	SD_nCD	I	MFP4	SD/SDH mode – card detect.
28	PB.6	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP3	Data transmitter output pin for UART1.
	SD_DAT0	I/O	MFP4	SD/SDH mode data line bit 0.
29	PB.7	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP3	Data receiver input pin for UART1.
	SD_DAT1	I/O	MFP4	SD/SDH mode data line bit 1.
30	USB_VBUS	I	MFP0	Power supply from USB host or HUB.
31	PB.8	I/O	MFP0	General purpose digital I/O pin.
	USBH_PWEN	O	MFP1	USB host mode to control an external overcurrent source.
	TM1_CNT_OUT	I/O	MFP2	Timer1 event counter input/toggle output.
	UART1_nCTS	I	MFP3	Clear to Send input pin for UART1.
	SD_DAT2	I/O	MFP4	SD/SDH mode data line bit 2.

32	PB.9	I/O	MFP0	General purpose digital I/O pin.
	USBH_OVD	I	MFP1	USB host bus power over voltage detector.
	TM1_EXT	I	MFP2	Timer1 external capture input.
	UART1_nRTS	O	MFP3	Request to Send output pin for UART1.
	SD_DAT3	I/O	MFP4	SD/SDH mode data line bit 3.
33	V_{SS}	A	MFP0	Ground
34	AV_{DDADC}	A	MFP0	Power supply for analog SAR-ADC, DC 3.3V.
35	AV_{SSADC}	A	MFP0	Ground pin for analog SAR-ADC.
36	PA.0	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH0	A	MFP1	ADC channel 0 analog input.
37	PA.1	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH1	A	MFP1	ADC channel 1 analog input.
38	PA.2	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH2	A	MFP1	ADC channel 2 analog input.
	I2S_MCLK	O	MFP2	I^2S master clock output pin.
39	PA.3	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH3	A	MFP1	ADC channel 3 analog input.
	I2S_DI	I	MFP2	I^2S data input.
40	PA.4	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH4	A	MFP1	ADC channel 4 analog input.
	I2S_DO	O	MFP2	I^2S data output.
41	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
42	PB.10	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS	O	MFP1	SPI1 slave select pin.
	I2C1_SCL	O	MFP2	I2C1 clock pin.
	UART2_TXD	O	MFP3	Data transmitter output pin for UART2.
	PWM_CH0	I/O	MFP4	PWM channel0 output/capture input.

43	PB.11	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	O	MFP1	SPI1 serial clock pin.
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
	UART2_RXD	I	MFP3	Data receiver input pin for UART2.
	PWM_CH1	I/O	MFP4	PWM channel1 output/capture input.
44	PB.12	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI	O	MFP1	SPI1 MOSI (Master Out, Slave In) pin.
	USBH1_D+	I/O	MFP2	USB host-lite 1 differential signal D+
	UART2_nCTS	I	MFP3	Clear to send input pin for UART2.
	PWM_CH2	I/O	MFP4	PWM channel2 output/capture input.
45	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
46	V_{DD}	A	MFP0	Power supply, DC 3.3V.
47	LDO_CAP	A	MFP0	LDO output pin.
48	V_{SS}	A	MFP0	Ground.

Note: The thermal pad (EPD) on the bottom of QFN package should be connected to GND.

4.3.5 NuMicro® NUC505DSA LQFP 64-pin Description

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFPL and SYS_GPx_MFPH)

PA.0 MFP0 means SYS_GPA_MFPL[2:0]=0x0.

PA.9 MFP5 means SYS_GPA_MFPH[6:4]=0x5.

Pin No.	Pin Name	Type	MFP	Description
1	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
2	ICE_CLK	O	MFP0	Serial wired debugger clock pin. (In ICE mode)
	PD.0	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I2C0 clock pin.
3	ICE_DAT	I/O	MFP0	Serial wired debugger data pin. (In ICE mode)
	PD.1	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
4	PB.13	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO	I	MFP1	SPI1 MISO (Master In, Slave Out) pin.
	USBH1_D-	I/O	MFP2	USB host-lite 1 differential signal D-.
	UART2_nRTS	O	MFP3	Request to Send output pin for UART2.
	PWM_CH3	I/O	MFP4	PWM channel3 output/capture input.
5	PB.14	I/O	MFP0	General purpose digital I/O pin.
	USBH1_D+	I/O	MFP1	USB host-lite 1 differential signal D+.
	I2C1_SCL	O	MFP2	I2C1 clock pin.
6	PB.15	I/O	MFP0	General purpose digital I/O pin.
	USBH1_D-	I/O	MFP1	USB host-lite 1differential signal D-.
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
7	PC.0	I/O	MFP0	General purpose digital I/O pin.
	SD_CMD	I	MFP1	SD/SDH mode – command/response.
8	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
9	V_{SS}	A	MFP0	Ground

10	XT1_IN	I	MFP0	External 12 MHz (high speed) crystal input pin.
11	XT1_OUT	O	MFP0	External 12 MHz (high speed) crystal output pin.
12	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
13	USB_D-	A	MFP0	USB differential signal D-.
14	USB_D+	A	MFP0	USB differential signal D+.
15	AV_{DDUSB}	A	MFP0	Power supply for analog USB, DC 3.3V.
16	USB_REXT	A	MFP0	12.1 KΩ used internally for USB circuitry.
17	PA.8	I/O	MFP0	General purpose digital I/O pin.
	SPIM_SS	O	MFP1	SPIM slave select pin.
	I2S_LRCLK	I/O	MFP2	I^2S left right channel clock.
	UART1_TXD	O	MFP3	Data transmitter output pin for UART1.
18	PA.9	I/O	MFP0	General purpose digital I/O pin.
	SPIM_CLK	O	MFP1	SPIM serial clock pin.
	I2S_BCLK	I/O	MFP2	I^2S bit clock pin.
	UART1_RXD	I	MFP3	Data receiver input pin for UART1.
	SYSCFG[0]	I	MFP0	System configuration setting bit 0.
19	PA.10	I/O	MFP0	General purpose digital I/O pin.
	SPIM_MOSI	I/O	MFP1	SPIM MOSI (Master Out, Slave In) pin. (Data 0 pin for Quad Mode I/O).
	I2C1_SCL	O	MFP2	I2C1 clock pin.
	SD_CLK	O	MFP4	SD/SDH mode – clock.
	SYSCFG[1]	I	MFP0	System configuration setting bit 1.
20	PA.11	I/O	MFP0	General purpose digital I/O pin.
	SPIM_MISO	I/O	MFP1	SPIM MISO (Master In, Slave Out) pin. (Data 1 pin for Quad Mode I/O).
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
	SD_CMD	I	MFP4	SD/SDH mode – command/response.
21	PA.12	I/O	MFP0	General purpose digital I/O pin.

	SPIM_D2	I/O	MFP1	SPIM data 2 pin for Quad Mode I/O.
	TM0_CNT_OUT	I	MFP2	Timer0 event counter input/toggle output.
22	PA.13	I/O	MFP0	General purpose digital I/O pin.
	SPIM_D3	I/O	MFP1	SPIM data 3 pin for Quad Mode I/O.
	TM0_EXT	I	MFP2	Timer0 external capture input.
	SD_nCD	I	MFP4	SD/SDH mode – card detect.
23	PA.14	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I2C0 clock pin.
	SD_DAT0	I/O	MFP4	SD/SDH mode data line bit 0.
24	PA.15	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
	SD_DAT1	I/O	MFP4	SD/SDH mode data line bit 1.
25	PC.8	I/O	MFP0	General purpose digital I/O pin.
	I2S_MCLK	O	MFP1	I^2S master clock output pin.
26	PC.9	I/O	MFP0	General purpose digital I/O pin.
	I2S_DI	I	MFP1	I^2S data input.
	TM2_CNT_OUT	I/O	MFP2	Timer2 event counter input/toggle output.
	PWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
27	PC.10	I/O	MFP0	General purpose digital I/O pin.
	I2S_DO	O	MFP1	I^2S data output.
	TM2_EXT	I	MFP2	Timer2 external capture input.
	PWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
28	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
29	PB.0	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I2C0 clock pin.
	UART0_TXD	O	MFP3	Data transmitter output pin for UART0.
	SD_DAT2	I/O	MFP4	SD/SDH mode data line bit 2.

30	PB.1	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
	UART0_RXD	I	MFP3	Data receiver input pin for UART0.
	SD_DAT3	I/O	MFP4	SD/SDH mode data line bit 3.
31	PB.2	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS	O	MFP1	SPI0 slave select pin.
	SD_CMD	I	MFP4	SD/SDH mode – command/response.
32	PB.3	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	O	MFP1	SPI0 serial clock pin.
	SD_CLK	O	MFP4	SD/SDH mode – clock.
	SYSCFG[2]	I	MFP0	System configuration setting bit 2.
33	PB.4	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	O	MFP1	SPI0 MOSI (Master Out, Slave In) pin.
	SYSCFG[3]	I	MFP0	System configuration setting bit 3.
34	PB.5	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I	MFP1	SPI0 MISO (Master In, Slave Out) pin.
	SD_nCD	I	MFP4	SD/SDH mode – card detect.
35	USB_VBUS	I	MFP0	Power supply from USB host or HUB.
36	V_{SS}	A	MFP0	Ground.
37	AV_{DDHP}	AP	VDD	Power supply for analog CODEC headphone, DC 3.3V.
38	LHPOUT	A	MFP0	Headphone left channel output pin.
39	RHPOUT	A	MFP0	Headphone right channel output pin.
40	AV_{SSHP}	A	MFP0	Ground for analog CODEC headphone.
41	VMID	A	MFP0	Headphone reference power.
42	$AV_{DDCODEC}$	A	MFP0	Power supply for analog CODEC, DC 3.3V.
43	MIC0_P	A	MFP0	Microphone 0 positive input.
44	MIC0_N	A	MFP0	Microphone 0 negative input.

45	MIC_BIAS	A	MFP0	CODEC left line-in channel or Microphone bias.
46	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
47	PD.4	I/O	MFP0	General purpose digital I/O pin.
	RLINEIN	A	MFP1	CODEC right line-in channel.
48	AV_{DDADC}	A	MFP0	Power supply for analog SAR-ADC, DC 3.3V.
49	AV_{SSADC}	A	MFP0	Ground pin for analog SAR-ADC.
50	PA.0	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH0	A	MFP1	ADC channel 0 analog input.
51	PA.1	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH1	A	MFP1	ADC channel 1 analog input.
52	PA.2	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH2	A	MFP1	ADC channel 2 analog input.
	I2S_MCLK	O	MFP2	I^2S master clock output pin.
53	PA.3	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH3	A	MFP1	ADC channel 3 analog input.
	I2S_DI	I	MFP2	I^2S data input.
54	PA.4	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH4	A	MFP1	ADC channel 4 analog input.
	I2S_DO	O	MFP2	I^2S data output.
55	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
56	PB.10	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS	O	MFP1	SPI1 slave select pin.
	I2C1_SCL	O	MFP2	I2C1 clock pin.
	UART2_TXD	O	MFP3	Data transmitter output pin for UART2.
	PWM_CH0	I/O	MFP4	PWM channel0 output/capture input.
57	PB.11	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	O	MFP1	SPI1 serial clock pin.

	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
	UART2_RXD	I	MFP3	Data receiver input pin for UART2.
	PWM_CH1	I/O	MFP4	PWM channel1 output/capture input.
58	PB.12	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI	O	MFP1	SPI1 MOSI (Master Out, Slave In) pin.
	USBH1_D+	I/O	MFP2	USB host-lite 1 differential signal D+
	UART2_nCTS	I	MFP3	Clear to Send input pin for UART2.
	PWM_CH2	I/O	MFP4	PWM channel2 output/capture input.
59	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
60	PC.11	I/O	MFP0	General purpose digital I/O pin.
	I2S_LRCLK	I/O	MFP1	I^2S left right channel clock.
	TM3_CNT_OUT	I/O	MFP2	Timer3 event counter input/toggle output.
	PWM_CH2	I/O	MFP3	PWM channel2 output/capture input.
61	PC.12	I/O	MFP0	General purpose digital I/O pin.
	I2S_BCLK	I/O	MFP1	I^2S bit clock pin.
	TM3_EXT	I	MFP2	Timer3 external capture input.
	PWM_CH3	I/O	MFP3	PWM channel3 output/capture input.
62	V_{DD}	A	MFP0	Power supply, DC 3.3V.
63	LDO_CAP	A	MFP0	LDO output pin.
64	V_{SS}	A	MFP0	Ground.

4.3.6 NuMicro® NUC505DS13Y LQFP 64-pin Description

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFPL and SYS_GPx_MFPH)

PA.0 MFP0 means SYS_GPA_MFPL[2:0]=0x0.

PA.9 MFP5 means SYS_GPA_MFPH[6:4]=0x5.

Pin No.	Pin Name	Type	MFP	Description
1	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
2	ICE_CLK	O	MFP0	Serial wired debugger clock pin. (In ICE mode)
	PD.0	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I2C0 clock pin.
3	ICE_DAT	I/O	MFP0	Serial wired debugger data pin. (In ICE mode)
	PD.1	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
4	PB.13	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO	I	MFP1	SPI1 MISO (Master In, Slave Out) pin.
	USBH1_D-	I/O	MFP2	USB host-lite 1 differential signal D-.
	UART2_nRTS	O	MFP3	Request to Send output pin for UART2.
	PWM_CH3	I/O	MFP4	PWM channel3 output/capture input.
5	PB.14	I/O	MFP0	General purpose digital I/O pin.
	USBH1_D+	I/O	MFP1	USB host-lite 1 differential signal D+.
	I2C1_SCL	O	MFP2	I2C1 clock pin.
6	PB.15	I/O	MFP0	General purpose digital I/O pin.
	USBH1_D-	I/O	MFP1	USB host-lite 1differential signal D-.
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
7	PC.0	I/O	MFP0	General purpose digital I/O pin.
	SD_CMD	I	MFP1	SD/SDH mode – command/response.
8	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
9	V_{SS}	A	MFP0	Ground

10	XT1_IN	I	MFP0	External 12 MHz (high speed) crystal input pin.
11	XT1_OUT	O	MFP0	External 12 MHz (high speed) crystal output pin.
12	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
13	USB_D-	A	MFP0	USB differential signal D-.
14	USB_D+	A	MFP0	USB differential signal D+.
15	AV_{DDUSB}	A	MFP0	Power supply for analog USB, DC 3.3V.
16	USB_REXT	A	MFP0	12.1 KΩ used internally for USB circuitry.
17	V_{BAT}	A	MFP0	Power supply by batteries for RTC, DC 3.3V.
18	RTC_RPWR	O	MFP0	Enable external power control source when active high.
19	RTC_nRWAKE	I	MFP0	System power enable trigger when active low.
20	PA.8	I/O	MFP0	General purpose digital I/O pin.
	SPIM_SS	O	MFP1	SPIM slave select pin.
	I2S_LRCLK	I/O	MFP2	I^2S left right channel clock.
	UART1_TXD	O	MFP3	Data transmitter output pin for UART1.
21	PA.9	I/O	MFP0	General purpose digital I/O pin.
	SPIM_CLK	O	MFP1	SPIM serial clock pin.
	I2S_BCLK	I/O	MFP2	I^2S bit clock pin.
	UART1_RXD	I	MFP3	Data receiver input pin for UART1.
	SYSCFG[0]	I	MFP0	System configuration setting bit 0.
22	PA.10	I/O	MFP0	General purpose digital I/O pin.
	SPIM_MOSI	I/O	MFP1	SPIM MOSI (Master Out, Slave In) pin. (Data 0 pin for Quad Mode I/O).
	I2C1_SCL	O	MFP2	I2C1 clock pin.
	SD_CLK	O	MFP4	SD/SDH mode – clock.
	SYSCFG[1]	I	MFP0	System configuration setting bit 1.
23	PA.11	I/O	MFP0	General purpose digital I/O pin.
	SPIM_MISO	I/O	MFP1	SPIM MISO (Master In, Slave Out) pin. (Data 1 pin for Quad Mode I/O).

	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
	SD_CMD	I	MFP4	SD/SDH mode – command/response.
24	PA.12	I/O	MFP0	General purpose digital I/O pin.
	SPIM_D2	I/O	MFP1	SPIM data 2 pin for Quad Mode I/O.
	TM0_CNT_OUT	I	MFP2	Timer0 event counter input/toggle output.
25	PA.13	I/O	MFP0	General purpose digital I/O pin.
	SPIM_D3	I/O	MFP1	SPIM data 3 pin for Quad Mode I/O.
	TM0_EXT	I	MFP2	Timer0 external capture input.
	SD_nCD	I	MFP4	SD/SDH mode – card detect.
26	PA.14	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I2C0 clock pin.
	SD_DAT0	I/O	MFP4	SD/SDH mode data line bit 0.
27	PA.15	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
	SD_DAT1	I/O	MFP4	SD/SDH mode data line bit 1.
28	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
29	PB.0	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I2C0 clock pin.
	UART0_TXD	O	MFP3	Data transmitter output pin for UART0.
	SD_DAT2	I/O	MFP4	SD/SDH mode data line bit 2.
30	PB.1	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
	UART0_RXD	I	MFP3	Data receiver input pin for UART0.
	SD_DAT3	I/O	MFP4	SD/SDH mode data line bit 3.
31	PB.2	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS	O	MFP1	SPI0 slave select pin.
	SD_CMD	I	MFP4	SD/SDH mode – command/response.

32	PB.3	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	O	MFP1	SPI0 serial clock pin.
	SD_CLK	O	MFP4	SD/SDH mode – clock.
	SYSCFG[2]	I	MFP0	System configuration setting bit 2.
33	PB.4	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	O	MFP1	SPI0 MOSI (Master Out, Slave In) pin.
	SYSCFG[3]	I	MFP0	System configuration setting bit 3.
34	PB.5	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I	MFP1	SPI0 MISO (Master In, Slave Out) pin.
	SD_nCD	I	MFP4	SD/SDH mode – card detect.
35	PB.6	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP3	Data transmitter output pin for UART1.
	SD_DAT0	I/O	MFP4	SD/SDH mode data line bit 0.
36	PB.7	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP3	Data receiver input pin for UART1.
	SD_DAT1	I/O	MFP4	SD/SDH mode data line bit 1.
37	USB_VBUS	I	MFP0	Power supply from USB host or HUB.
38	PB.8	I/O	MFP0	General purpose digital I/O pin.
	USBH_PWEN	O	MFP1	USB host mode to control an external overcurrent source.
	TM1_CNT_OUT	I/O	MFP2	Timer1 event counter input/toggle output.
	UART1_nCTS	I	MFP3	Clear to Send input pin for UART1.
	SD_DAT2	I/O	MFP4	SD/SDH mode data line bit 2.
39	PB.9	I/O	MFP0	General purpose digital I/O pin.
	USBH_OVD	I	MFP1	USB host bus power over voltage detector.
	TM1_EXT	I	MFP2	Timer1 external capture input.
	UART1_nRTS	O	MFP3	Request to Send output pin for UART1.
	SD_DAT3	I/O	MFP4	SD/SDH mode data line bit 3.

40	V_{SS}	A	MFP0	Ground.
41	AV_{DDHP}	AP	VDD	Power supply for analog CODEC headphone, DC 3.3V.
42	LHPOUT	A	MFP0	Headphone left channel output pin.
43	RHPOUT	A	MFP0	Headphone right channel output pin.
44	AV_{SSHP}	A	MFP0	Ground for analog CODEC headphone.
45	VMID	A	MFP0	Headphone reference power.
46	$AV_{DDCODEC}$	A	MFP0	Power supply for analog CODEC, DC 3.3V.
47	AV_{DDADC}	A	MFP0	Power supply for analog SAR-ADC, DC 3.3V.
48	AV_{SSADC}	A	MFP0	Ground pin for analog SAR-ADC.
49	PA.0	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH0	A	MFP1	ADC channel 0 analog input.
50	PA.1	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH1	A	MFP1	ADC channel 1 analog input.
51	PA.2	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH2	A	MFP1	ADC channel 2 analog input.
	I2S_MCLK	O	MFP2	I^2S master clock output pin.
52	PA.3	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH3	A	MFP1	ADC channel 3 analog input.
	I2S_DI	I	MFP2	I^2S data input.
53	PA.4	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH4	A	MFP1	ADC channel 4 analog input.
	I2S_DO	O	MFP2	I^2S data output.
54	PA.5	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH5	A	MFP1	ADC channel 5 analog input.
55	PA.6	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH6	A	MFP1	ADC channel 6 analog input.
56	PA.7	I/O	MFP0	General purpose digital I/O pin.

	ADC_CH7	A	MFP1	ADC channel 7 analog input.
57	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
58	PB.10	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS	O	MFP1	SPI1 slave select pin.
	I2C1_SCL	O	MFP2	I2C1 clock pin.
	UART2_TXD	O	MFP3	Data transmitter output pin for UART2.
	PWM_CH0	I/O	MFP4	PWM channel0 output/capture input.
59	PB.11	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	O	MFP1	SPI1 serial clock pin.
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
	UART2_RXD	I	MFP3	Data receiver input pin for UART2.
	PWM_CH1	I/O	MFP4	PWM channel1 output/capture input.
60	PB.12	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI	O	MFP1	SPI1 MOSI (Master Out, Slave In) pin.
	USBH1_D+	I/O	MFP2	USB host-lite 1 differential signal D+
	UART2_nCTS	I	MFP3	Clear to Send input pin for UART2.
	PWM_CH2	I/O	MFP4	PWM channel2 output/capture input.
61	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
62	V_{DD}	A	MFP0	Power supply, DC 3.3V.
63	LDO_CAP	A	MFP0	LDO output pin.
64	V_{SS}	A	MFP0	Ground.

4.3.7 NuMicro® NUC505YO13Y QFN 88-pin Description

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFPL and SYS_GPx_MFPH)

PA.0 MFP0 means SYS_GPA_MFPL[2:0]=0x0.

PA.9 MFP5 means SYS_GPA_MFPH[6:4]=0x5.

Pin No.	Pin Name	Type	MFP	Description
1	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
2	ICE_CLK	O	MFP0	Serial wired debugger clock pin. (In ICE mode)
	PD.0	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I2C0 clock pin.
3	ICE_DAT	I/O	MFP0	Serial wired debugger data pin. (In ICE mode)
	PD.1	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
4	PB.13	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO	I	MFP1	SPI1 MISO (Master In, Slave Out) pin.
	USBH1_D-	I/O	MFP2	USB host-lite 1 differential signal D-.
	UART2_nRTS	O	MFP3	Request to Send output pin for UART2.
	PWM_CH3	I/O	MFP4	PWM channel3 output/capture input.
5	PB.14	I/O	MFP0	General purpose digital I/O pin.
	USBH1_D+	I/O	MFP1	USB host-lite 1differential signal D+.
	I2C1_SCL	O	MFP2	I2C1 clock pin.
6	PB.15	I/O	MFP0	General purpose digital I/O pin.
	USBH1_D-	I/O	MFP1	USB host-lite 1 differential signal D-.
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
7	PC.0	I/O	MFP0	General purpose digital I/O pin.
	SD_CMD	I	MFP1	SD/SDH mode – command/response.
8	PC.1	I/O	MFP0	General purpose digital I/O pin.
	SD_CLK	O	MFP1	SD/SDH mode – clock.

Pin No.	Pin Name	Type	MFP	Description
9	PC.2	I/O	MFP0	General purpose digital I/O pin.
	SD_nCD	I	MFP1	SD/SDH mode – card detect.
10	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
11	PC.3	I/O	MFP0	General purpose digital I/O pin.
12	PC.4	I/O	MFP0	General purpose digital I/O pin.
	SD_DAT0	I/O	MFP1	SD/SDH mode data line bit 0.
13	PC.5	I/O	MFP0	General purpose digital I/O pin.
	SD_DAT1	I/O	MFP1	SD/SDH mode data line bit 1.
14	PC.6	I/O	MFP0	General purpose digital I/O pin.
	SD_DAT2	I/O	MFP1	SD/SDH mode data line bit 2.
15	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
16	XT1_IN	I	MFP0	External 12 MHz (high speed) crystal input pin.
17	XT1_OUT	O	MFP0	External 12 MHz (high speed) crystal output pin.
18	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
19	USB_D-	A	MFP0	USB differential signal D-.
20	USB_D+	A	MFP0	USB differential signal D+.
21	AV_{DDUSB}	A	MFP0	Power supply for analog USB, DC 3.3V.
22	USB_REXT	A	MFP0	12.1 KΩ used internally for USB circuitry.
23	V_{BAT}	A	MFP0	Power supply by batteries for RTC, DC 3.3V.
24	RTC_RPWR	O	MFP0	Enable external power control source when active high.
25	RTC_nRWAKE	I	MFP0	System power enable trigger when active low.
26	X32_IN	I	MFP0	External 32.768 kHz (low speed) crystal input pin.
27	X32_OUT	O	MFP0	External 32.768 kHz (low speed) crystal output pin.
28	PA.8	I/O	MFP0	General purpose digital I/O pin.
	SPIM_SS	O	MFP1	SPIM slave select pin.
	I2S_LRCLK	I/O	MFP2	I^2S left right channel clock.

Pin No.	Pin Name	Type	MFP	Description
	UART1_TXD	O	MFP3	Data transmitter output pin for UART1.
29	PA.9	I/O	MFP0	General purpose digital I/O pin.
	SPIM_CLK	O	MFP1	SPIM serial clock pin.
	I2S_BCLK	I/O	MFP2	I^2S bit clock pin.
	UART1_RXD	I	MFP3	Data receiver input pin for UART1.
	SYSCFG[0]	I	MFP0	System configuration setting bit 0.
30	PA.10	I/O	MFP0	General purpose digital I/O pin.
	SPIM_MOSI	I/O	MFP1	SPIM MOSI (Master Out, Slave In) pin. (Data 0 pin for Quad Mode I/O).
	I2C1_SCL	O	MFP2	I2C1 clock pin.
	SD_CLK	O	MFP4	SD/SDH mode – clock.
	SYSCFG[1]	I	MFP0	System configuration setting bit 1.
31	PA.11	I/O	MFP0	General purpose digital I/O pin.
	SPIM_MISO	I/O	MFP1	SPIM MISO (Master In, Slave Out) pin. (Data 1 pin for Quad Mode I/O).
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
	SD_CMD	I	MFP4	SD/SDH mode – command/response.
32	PA.12	I/O	MFP0	General purpose digital I/O pin.
	SPIM_D2	I/O	MFP1	SPIM data 2 pin for Quad Mode I/O.
	TM0_CNT_OUT	I/O	MFP2	Timer0 event counter input/toggle output.
33	PA.13	I/O	MFP0	General purpose digital I/O pin.
	SPIM_D3	I/O	MFP1	SPIM data 3 pin for Quad Mode I/O.
	TM0_EXT	I	MFP2	Timer0 external capture input.
	SD_nCD	I	MFP4	SD/SDH mode – card detect.
34	PA.14	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I2C0 clock pin.
	SD_DAT0	I/O	MFP4	SD/SDH mode data line bit 0.

Pin No.	Pin Name	Type	MFP	Description
35	PA.15	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP2	I2C0 data input/output pin.
	SD_DAT1	I/O	MFP4	SD/SDH mode data line bit 1.
36	PC.7	I/O	MFP0	General purpose digital I/O pin.
	SD_DAT3	I/O	MFP1	SD/SDH mode data line bit 3.
37	PC.8	I/O	MFP0	General purpose digital I/O pin.
	I2S_MCLK	O	MFP1	I^2S master clock output pin.
38	PC.9	I/O	MFP0	General purpose digital I/O pin.
	I2S_DI	I	MFP1	I^2S data input.
	TM2_CNT_OUT	I/O	MFP2	Timer2 event counter input/toggle output.
	PWM_CH0	I/O	MFP3	PWM channel0 output/capture input.
39	PC.10	I/O	MFP0	General purpose digital I/O pin.
	I2S_DO	O	MFP1	I^2S data output.
	TM2_EXT	I	MFP2	Timer2 external capture input.
	PWM_CH1	I/O	MFP3	PWM channel1 output/capture input.
40	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
41	PB.0	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	O	MFP2	I2C0 clock pin.
	UART0_TXD	O	MFP3	Data transmitter output pin for UART0.
	SD_DAT2	I/O	MFP4	SD/SDH mode data line bit 2.
42	PB.1	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	FMP2	I2C0 data input/output pin.
	UART0_RXD	I	FMP3	Data receiver input pin for UART0.
	SD_DAT3	I/O	MFP4	SD/SDH mode data line bit 3.
43	PB.2	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS	O	MFP1	SPI0 slave select pin.

Pin No.	Pin Name	Type	MFP	Description
	SD_CMD	I	MFP4	SD/SDH mode – command/response.
44	PB.3	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	O	MFP1	SPI0 serial clock pin.
	SD_CLK	O	MFP4	SD/SDH mode – clock.
	SYSCFG[2]	I	MFP0	System configuration setting bit 2.
45	PB.4	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	O	MFP1	SPI0 MOSI (Master Out, Slave In) pin.
	SYSCFG[3]	I	MFP0	System configuration setting bit 3.
46	PB.5	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I	MFP1	SPI0 MISO (Master In, Slave Out) pin.
	SD_nCD	I	MFP4	SD/SDH mode – card detect.
47	PB.6	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP3	Data transmitter output pin for UART1.
	SD_DAT0	I/O	MFP4	SD/SDH mode data line bit 0.
48	PB.7	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP3	Data receiver input pin for UART1.
	SD_DAT1	I/O	MFP4	SD/SDH mode data line bit 1.
49	USB_VBUS	I	MFP0	Power supply from USB host or HUB.
50	PB.8	I/O	MFP0	General purpose digital I/O pin.
	USBH_PWEN	O	MFP1	USB host mode to control an external overcurrent source.
	TM1_CNT_OUT	I/O	MFP2	Timer1 event counter input/toggle output.
	UART1_nCTS	I	MFP3	Clear to Send input pin for UART1.
	SD_DAT2	I/O	MFP4	SD/SDH mode data line bit 2.
51	PB.9	I/O	MFP0	General purpose digital I/O pin.
	USBH_VOD	I	MFP1	USB host bus power over voltage detector.
	TM1_EXT	I	MFP2	Timer1 external capture input.

Pin No.	Pin Name	Type	MFP	Description
	UART1_nRTS	O	MFP3	Request to Send output pin for UART1.
	SD_DAT3	I/O	MFP4	SD/SDH mode data line bit 3.
52	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
53	AV_{DDHP}	A	MFP0	Power supply for analog CODEC headphone, DC 3.3V.
54	LHPOUT	A	MFP0	Headphone left channel output pin.
55	VCMBF	A	MFP0	VCM buffer output pin for headphone driver capless application.
56	RHPOUT	A	MFP0	Headphone right channel output pin.
57	AV_{SSHP}	A	MFP0	Ground for analog CODEC headphone.
58	VMID	A	MFP0	Headphone reference power.
59	$AV_{DDCODEC}$	A	MFP0	Power supply for analog CODEC, DC 3.3V.
60	MIC0_P	A	MFP0	Microphone 0 positive input.
61	MIC0_N	A	MFP0	Microphone 0 negative input.
62	MIC_BIAS	A	MFP0	CODEC left line-in channel or Microphone bias.
63	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
64	PD.2	I/O	MFP0	General purpose digital I/O pin.
	MIC1_P	A	MFP1	Microphone 1 positive input.
65	PD.3	I/O	MFP0	General purpose digital I/O pin.
	MIC1_N	A	MFP1	Microphone 1 negative input.
66	PD.4	I/O	MFP0	General purpose digital I/O pin.
	RLINEIN	A	MFP1	CODEC right line-in channel.
67	AV_{DDADC}	A	MFP0	Power supply for analog SAR-ADC, DC 3.3V.
68	AV_{SSADC}	A	MFP0	Ground pin for analog SAR-ADC.
69	PA.0	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH0	A	MFP1	ADC channel 0 analog input.
70	PA.1	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH1	A	MFP1	ADC channel 1 analog input.

Pin No.	Pin Name	Type	MFP	Description
71	PA.2	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH2	A	MFP1	ADC channel 2 analog input.
	I2S_MCLK	O	MFP2	I^2S master clock output pin.
72	PA.3	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH3	A	MFP1	ADC channel 3 analog input.
	I2S_DI	I	MFP2	I^2S data input.
73	PA.4	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH4	A	MFP1	ADC channel 4 analog input.
	I2S_DO	O	MFP2	I^2S data output.
74	PA.5	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH5	A	MFP1	ADC channel 5 analog input.
75	PA.6	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH6	A	MFP1	ADC channel 6 analog input.
76	PA.7	I/O	MFP0	General purpose digital I/O pin.
	ADC_CH7	A	MFP1	ADC channel 7 analog input.
77	V_{DD12}	A	MFP0	Power supply for I/O ports, DC 1.2V
78	PB.10	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS	O	MFP1	SPI1 slave select pin.
	I2C1_SCL	O	MFP2	I2C1 clock pin.
	UART2_TXD	O	MFP3	Data transmitter output pin for UART2.
	PWM_CH0	I/O	MFP4	PWM channel0 output/capture input.
79	PB.11	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	O	MFP1	SPI1 serial clock pin.
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin.
	URAT2_RXD	I	MFP3	Data receiver input pin for UART2.
	PWM_CH1	I/O	MFP4	PWM channel1 output/capture input.

Pin No.	Pin Name	Type	MFP	Description
80	PB.12	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI	O	MFP1	SPI1 MOSI (Master Out, Slave In) pin.
	USBH1_D+	I/O	MFP2	USB host-lite 1 differential signal D+.
	UART2_nCTS	I	MFP3	Clear to Send input pin for UART2.
	PWM_CH2	I/O	MFP4	PWM channel2 output/capture input.
81	V_{DD}	A	MFP0	Power supply for I/O ports, DC 3.3V.
82	PC.11	I/O	MFP0	General purpose digital I/O pin.
	I2S_LRCLK	I/O	MFP1	I^2S left right channel clock.
	TM3_CNT_OUT	I/O	MFP2	Timer3 event counter input/toggle output.
	PWM_CH2	I/O	MFP3	PWM channel2 output/capture input.
83	PC.12	I/O	MFP0	General purpose digital I/O pin.
	I2S_BCLK	I/O	MFP1	I^2S bit clock pin.
	TM3_EXT	I	MFP2	Timer3 external capture input.
	PWM_CH3	I/O	MFP3	PWM channel3 output/capture input.
84	PC.13	I/O	MFP0	General purpose digital I/O pin.
	USBH2_D+	I/O	MFP1	USB host-lite 2 differential signal D+.
85	PC.14	I/O	MFP0	General purpose digital I/O pin.
	USBH2_D-	I/O	MFP1	USB host-lite 2 differential signal D-.
86	V_{DD}	A	MFP0	Power supply, DC 3.3V.
87	LDO_CAP	A	MFP0	LDO output pin.
88	V_{SS}	A	MFP0	Ground.

Note: The thermal pad (EPD) on the bottom of QFN package should be connected to GND.

4.3.8 Summary GPIO Multi-function Pin Description

MPF0	MPF1	MPF2	MPF3	MPF4	Other	Driving
PA.0	ADC_CH0					2~16mA
PA.1	ADC_CH 1					2~16mA
PA.2	ADC_CH 2					2~16mA
PA.3	ADC_CH 3					2~16mA
PA.4	ADC_CH 4					2~16mA
PA.5	ADC_CH 5					2~16mA
PA.6	ADC_CH 6					2~16mA
PA.7	ADC_CH 7					2~16mA
PA.8	SPIM_SS	I2S_LRCLK	UART1_TXD			8mA
PA.9	SPIM_CLK	I2S_BCLK	UART1_RXD		SYSCFG[0]	8mA
PA.10	SPIM_MOSI	I2C1_SCL		SD_CLK	SYSCFG[1]	8mA
PA.11	SPIM_MISO	I2C1_SDA		SD_CMD		8mA
PA.12	SPIM_D2	TM0_CNT_OUT				8mA
PA.13	SPIM_D3	TM0_EXT		SD_nCD		8mA
PA.14		I2C0_SCL		SD_DAT0		4mA
PA.15		I2C0_SDA		SD_DAT1		4mA
PB.0		I2C0_SCL	UART0_TXD	SD_DAT2		4mA
PB.1		I2C0_SDA	UART0_RXD	SD_DAT3		4mA
PB.2	SPI0_SS			SD_CMD		4mA
PB.3	SPI0_CLK			SD_CLK	SYSCFG[2]	4mA
PB.4	SPI0_MOSI				SYSCFG[3]	4mA
PB.5	SPI0_MISO			SD_nCD		4mA
PB.6			UART1_TXD	SD_DAT0		4mA
PB.7			UART1_RXD	SD_DAT1		4mA
PB.8	USBH_PWEN	TM1_CNT_OUT	UART1_nCTS	SD_DAT2		4mA
PB.9	USBH_OVD	TM1_EXT	UART1_nRTS	SD_DAT3		4mA
PB.10	SPI1_SS	I2C1_SCL	UART2_TXD	PWM_CH0		4mA
PB.11	SPI1_CLK	I2C1_SDA	UART2_RXD	PWM_CH1		4mA
PB.12	SPI1_MOSI	USBH1_D+	UART2_nCTS	PWM_CH2		8mA
PB.13	SPI1_MISO	USBH1_D-	UART2_nRST	PWM_CH3		8mA
PB.14	USBH1_D+	I2C1_SCL				8mA
PB.15	USBH1_D-	I2C1_SDA				8mA

PC.0	SD_CMD					8mA
PC.1	SD_CLK					8mA
PC.2	SD_nCD					8mA
PC.3						8mA
PC.4	SD_DAT0					8mA
PC.5	SD_DAT1					8mA
PC.6	SD_DAT2					8mA
PC.7	SD_DAT3					8mA
PC.8	I2S_MCLK					4mA
PC.9	I2S_DI	TM2_CNT_OUT	PWM_CH0			4mA
PC.10	I2S_DO	TM2_EXT	PWM_CH1			4mA
PC.11	I2S_LRCLK	TM3_CNT_OUT	PWM_CH2			4mA
PC.12	I2S_BCLK	TM3_EXT	PWM_CH3			4mA
PC.13	USBH2_D+					8mA
PC.14	USBH2_D-					8mA
PD.0		I2C0_SCL			ICE_CLK	4mA
PD.1		I2C0_SDA			ICE_DAT	4mA
PD.2					MIC1_P	2~16mA
PD.3					MIC1_N	2~16mA
PD.4					RLINEIN	2~16mA

4.3.9 GPIO Multi-function Pin Summary

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFPL and SYS_GPx_MFPH)

PA.0 MFP0 means SYS_GPA_MFPL[2:0]=0x0.

PA.9 MFP5 means SYS_GPA_MFPH[6:4]=0x5.

Group	Pin Name	GPIO	MFP*	Type	Description
ADC	ADC_CH0	PA.0	MFP1	A	ADC0 analog input.
	ADC_CH1	PA.1	MFP1	A	ADC1 analog input.
	ADC_CH2	PA.2	MFP1	A	ADC2 analog input.
	ADC_CH3	PA.3	MFP1	A	ADC3 analog input.
	ADC_CH4	PA.4	MFP1	A	ADC4 analog input.
	ADC_CH5	PA.5	MFP1	A	ADC5 analog input.
	ADC_CH6	PA.6	MFP1	A	ADC6 analog input.
	ADC_CH7	PA.7	MFP1	A	ADC7 analog input.
CODEC	MIC1_P	PD.2	MFP1	A	Audio MIC1 analog positive input pin
	MIC1_N	PD.3	MFP1	A	Audio MIC1 analog negative input pin
	RLINEIN	PD.4	MFP1	A	Audio right line-in analog pin.
I2C0	I2C0_SCL	PA.14	MFP2	I/O	I2C0 clock pin.
	I2C0_SCL	PB.0	MFP2	I/O	I2C0 clock pin.
	I2C0_SCL	PD.0	MFP2	I/O	I2C0 clock pin.
	I2C0_SDA	PA.15	MFP2	I/O	I2C0 data input/output pin.
	I2C0_SDA	PB.1	MFP2	I/O	I2C0 data input/output pin.
	I2C0_SDA	PD.1	MFP2	I/O	I2C0 data input/output pin.
I2C1	I2C1_SCL	PA.10	MFP2	I/O	I2C1 clock pin.
	I2C1_SCL	PB.10	MFP2	I/O	I2C1 clock pin.
	I2C1_SCL	PB.14	MFP2	I/O	I2C1 clock pin.
	I2C1_SDA	PA.11	MFP2	I/O	I2C1 data input/output pin.
	I2C1_SDA	PB.11	MFP2	I/O	I2C1 data input/output pin.
	I2C1_SDA	PB.15	MFP2	I/O	I2C1 data input/output pin.
I^2S	I2S_MCLK	PA.2	MFP2	O	I^2S master clock output pin.
	I2S_MCLK	PC.8	MFP1	O	I^2S master clock output pin.
	I2S_BCLK	PA.9	MFP2	I/O	I^2S bit clock pin.
	I2S_BCLK	PC.12	MFP1	I/O	I^2S bit clock pin.
	I2S_LRCLK	PA.8	MFP2	I/O	I^2S left right channel pin.
	I2S_LRCLK	PC.11	MFP1	I/O	I^2S left right channel pin.

Group	Pin Name	GPIO	MFP*	Type	Description
	I2S_DO	PA.4	MFP2	O	I^2S data output.
	I2S_DO	PC.10	MFP1	O	I^2S data output.
	I2S_DI	PA.3	MFP2	I	I^2S data input.
	I2S_DI	PC.9	MFP1	I	I^2S data input.
ICE	ICE_CLK	PD.0	MFP0	I	Serial wired debugger clock pin
	ICE_DAT	PD.1	MFP0	I/O	Serial wired debugger data pin
PWM	PWM_CH0	PB.10	MFP4	I/O	PWM output/capture input.
	PWM_CH0	PC.9	MFP3	I/O	PWM output/capture input.
	PWM_CH1	PB.11	MFP4	I/O	PWM output/capture input.
	PWM_CH1	PC.10	MFP3	I/O	PWM output/capture input.
	PWM_CH2	PB.12	MFP4	I/O	PWM output/capture input.
	PWM_CH2	PC.11	MFP3	I/O	PWM output/capture input.
	PWM_CH3	PB.13	MFP4	I/O	PWM output/capture input.
	PWM_CH3	PC.12	MFP3	I/O	PWM output/capture input.
SPIM	SPIM_SS	PA.8	MFP1	O	SPIM slave select pin.
	SPIM_CLK	PA.9	MFP1	O	SPIM serial clock pin.
	SPIM_MOSI	PA.10	MFP1	I/O	SPIM MOSI (Master Out, Slave In) pin.
	SPIM_MISO	PA.11	MFP1	I/O	SPIM MISO (Master In, Slave Out) pin.
	SPIM_D2	PA.12	MFP1	I/O	SPIM data-2 bit in quad mode.
	SPIM_D3	PA.13	MFP1	I/O	SPIM data-3 bit in quad mode.
SPI0	SPI0_SS	PB.2	MFP1	O	SPI0 slave select pin.
	SPI0_CLK	PB.3	MFP1	O	SPI0 serial clock pin.
	SPI0_MOSI	PB.4	MFP1	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_MISO	PB.5	MFP1	I/O	SPI0 MISO (Master In, Slave Out) pin.
SPI1	SPI1_SS	PB.10	MFP1	O	SPI1 slave select pin.
	SPI1_CLK	PB.11	MFP1	O	SPI1 serial clock pin.
	SPI1_MOSI	PB.12	MFP1	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_MISO	PB.13	MFP1	I/O	SPI1 MISO (Master In, Slave Out) pin.
Timer	TM0_CNT_OUT	PA.12	MFP2	I/O	Timer0 event counter input / toggle output.
	TM0_EXT	PA.13	MFP2	I	Timer0 external counter input
	TM1_CNT_OUT	PB.8	MFP2	I/O	Timer1 event counter input / toggle output.
	TM1_EXT	PB.9	MFP2	I	Timer1 external counter input
	TM2_CNT_OUT	PC.9	MFP2	I/O	Timer2 event counter input / toggle output.

Group	Pin Name	GPIO	MFP*	Type	Description
	TM2_EXT	PC.10	MFP2	I	Timer2 external counter input
	TM3_CNT_OUT	PC.11	MFP2	I/O	Timer3 event counter input / toggle output.
	TM3_EXT	PC.12	MFP2	I	Timer3 external counter input
UART0	UART0_RXD	PB.1	MFP3	I	Data receiver input pin for UART0.
	UART0_TXD	PB.0	MFP3	O	Data transmitter output pin for UART0.
UART1	UART1_RXD	PA.9	MFP3	I	Data receiver input pin for UART1.
	UART1_RXD	PB.7	MFP3	I	Data receiver input pin for UART1.
	UART1_TXD	PA.8	MFP3	O	Data transmitter output pin for UART1.
	UART1_TXD	PB.6	MFP3	O	Data transmitter output pin for UART1.
	UART1_nCTS	PB.8	MFP3	I	Clear to Send input pin for UART1.
	UART1_nRTS	PB.9	MFP3	O	Request to Send output pin for UART1.
UART2	UART2_RXD	PB.11	MFP3	I	Data receiver input pin for UART2.
	UART2_TXD	PB.10	MFP3	O	Data transmitter output pin for UART2.
	UART2_nCTS	PB.12	MFP3	I	Clear to Send input pin for UART2.
	UART2_nRTS	PB.13	MFP3	O	Request to Send output pin for UART2.
USB Host Lite	USBH_PWEN	PB.8	MFP1	O	USB host to control an external overcurrent source.
	USBH_VOD	PB.9	MFP1	I	USB host lite over voltage detector
	USBH2_D+	PC.13	MFP1	A	USB host lite 2 differential signal D+.
	USBH2_D-	PC.14	MFP1	A	USB host lite 2 differential signal D-.
	USBH1_D+	PB.12	MFP2	A	USB host lite 1 differential signal D+.
	USBH1_D+	PB.14	MFP1	A	USB host lite 1 differential signal D+.
	USBH1_D-	PB.13	MFP2	A	USB host lite 1 differential signal D-.
	USBH1_D-	PB.15	MFP1	A	USB host lite 1 differential signal D-.
SDH	SD_CLK	PA.10	MFP4	O	SD/SDH mode - clock
	SD_CLK	PB.3	MFP4	O	SD/SDH mode – clock
	SD_CLK	PC.1	MFP1	O	SD/SDH mode – clock
	SD_CMD	PA.11	MFP4	O	SD/SDH mode – command/response
	SD_CMD	PB.2	MFP4	O	SD/SDH mode – command/response
	SD_CMD	PC.0	MFP1	O	SD/SDH mode – command/response
	SD_nCD	PA.13	MFP4	I	SD/SDH mode – card detect.
	SD_nCD	PB.5	MFP4	I	SD/SDH mode – card detect.
	SD_nCD	PC.2	MFP1	I	SD/SDH mode – card detect.
	SD_DAT0	PA.14	MFP4	I/O	SD/SDH mode data line bit 0.

Group	Pin Name	GPIO	MFP*	Type	Description
	SD_DAT0	PB.6	MFP4	I/O	SD/SDH mode data line bit 0.
	SD_DAT0	PC.4	MFP1	I/O	SD/SDH mode data line bit 0.
	SD_DAT1	PA.15	MFP4	I/O	SD/SDH mode data line bit 1.
	SD_DAT1	PB.7	MFP4	I/O	SD/SDH mode data line bit 1.
	SD_DAT1	PC.5	MFP1	I/O	SD/SDH mode data line bit 1.
	SD_DAT2	PB.0	MFP4	I/O	SD/SDH mode data line bit 2.
	SD_DAT2	PB.8	MFP4	I/O	SD/SDH mode data line bit 2.
	SD_DAT2	PC.6	MFP1	I/O	SD/SDH mode data line bit 2.
	SD_DAT3	PB.1	MFP4	I/O	SD/SDH mode data line bit 3.
	SD_DAT3	PB.9	MFP4	I/O	SD/SDH mode data line bit 3.
	SD_DAT3	PC.7	MFP1	I/O	SD/SDH mode data line bit 3.

Table 4.3-1 NUC505 GPIO Multi-function Table

5 BLOCK DIAGRAM

5.1 NuMicro® NUC505 Series Block Diagram

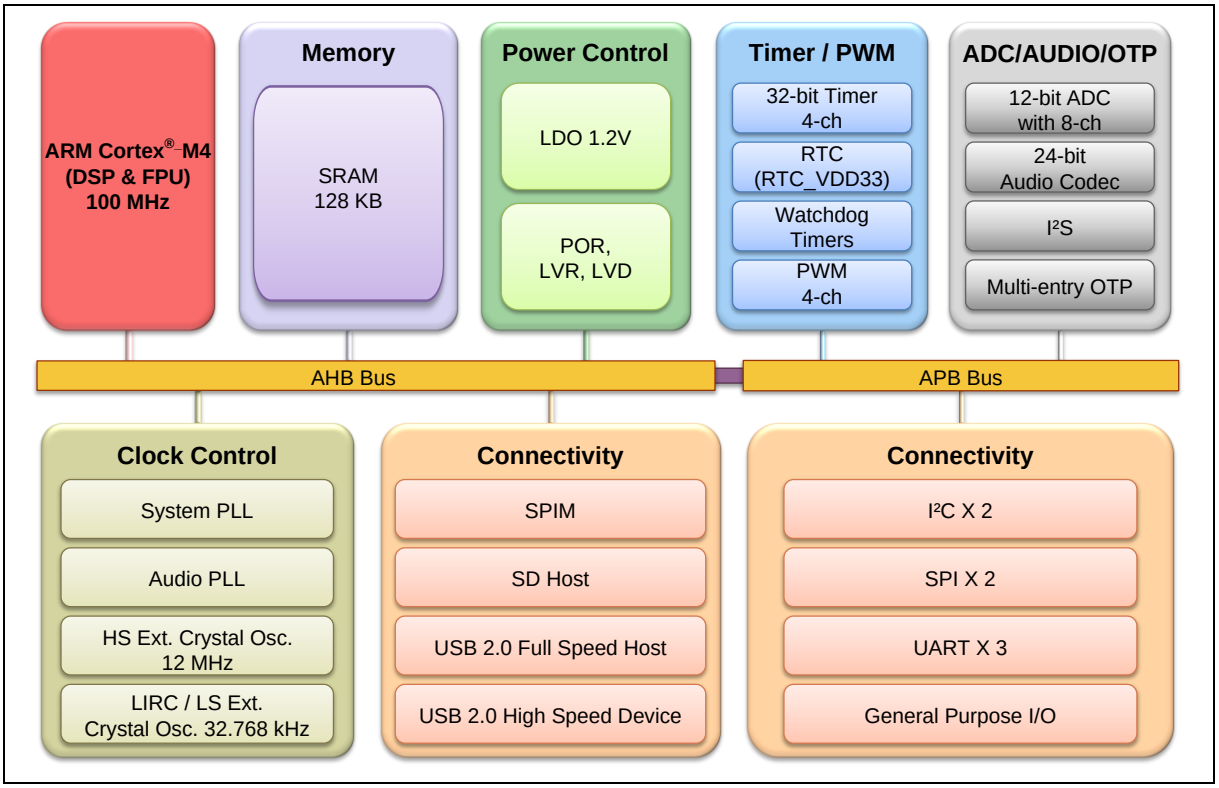


Figure 5.1-1 NuMicro® NUC505 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M4 Core

The Cortex®-M4 processor, a configurable, multistage, 32-bit RISC processor, has three AMBA AHB-Lite interfaces for best parallel performance and includes a NVIC component. The processor has optional hardware debug functionality, which can execute Thumb code, and is compatible with other Cortex®-M profile processors. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The Cortex®-M4F is a processor with the same capability as the Cortex®-M4 processor and includes floating point arithmetic functionality. The NUC505 is embedded with Cortex®-M4F processor. Throughout this document the name Cortex®-M4 refers to both Cortex®-M4 and Cortex®-M4F processors. The following figure shows the functional controller of the processor.

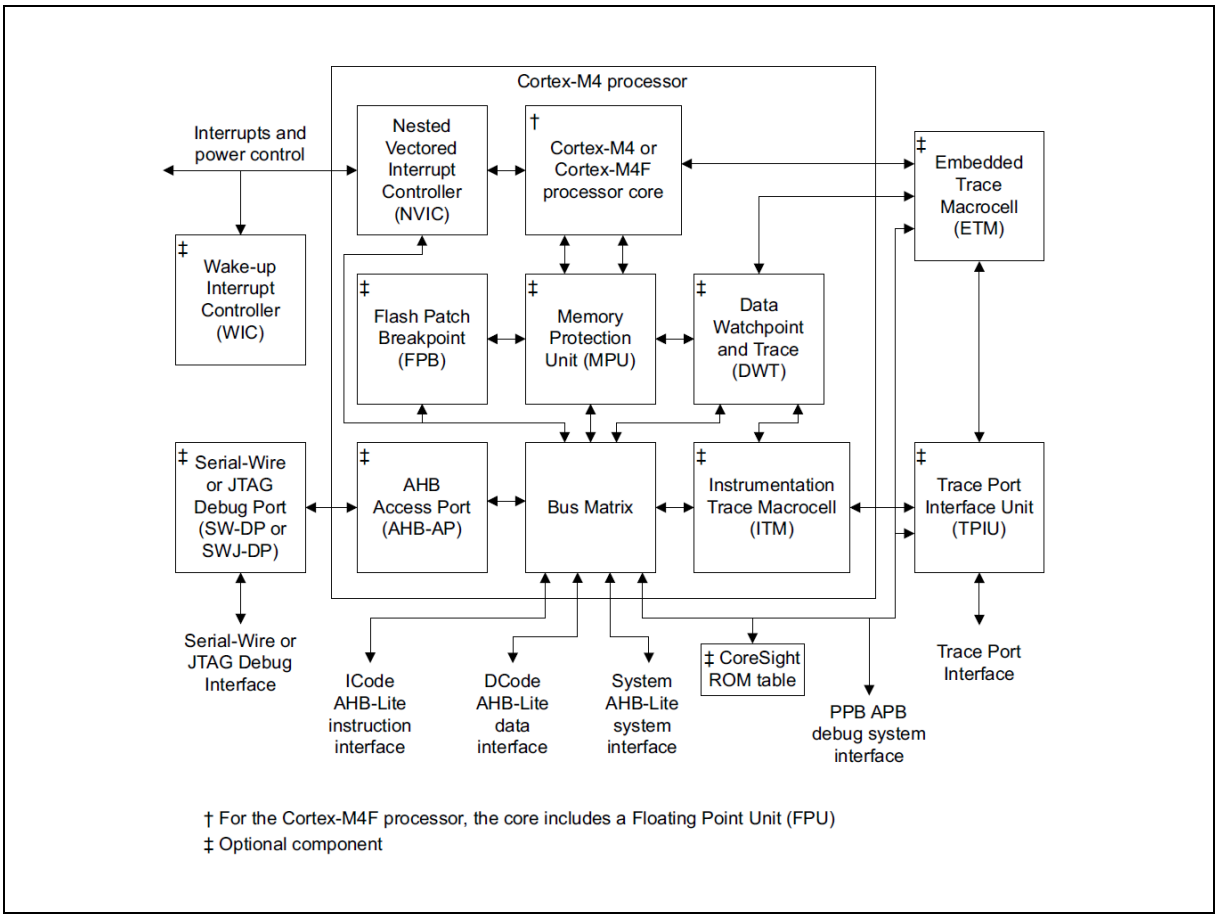


Figure 6.1-1 Cortex®-M4 Block Diagram

Cortex®-M4 processor features:

- A low gate count processor core, with low latency interrupt processing that has:
  - A subset of the Thumb instruction set, defined in the ARMv7-M Architecture Reference Manual.

- Banked Stack Pointer (SP).
- Hardware integer divide instructions, SDIV and UDIV.
- Handler and Thread modes.
- Thumb and Debug states.
- Support for interruptible-continued instructions LDM, STM, PUSH, and POP for low interrupt latency.
- Automatic processor state saving and restoration for low latency Interrupt Service Routine (ISR) entry and exit.
- Support for ARMv6 big-endian byte-invariant or little-endian accesses.
- Support for ARMv6 unaligned accesses.

- Floating Point Unit (FPU) in the Cortex®-M4F processor providing:
  - 32-bit instructions for single-precision (C float) data-processing operations.
  - Combined Multiply and Accumulate instructions for increased precision (Fused MAC).
  - Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root.
  - Hardware support for denormals and all IEEE rounding modes.
  - 32 dedicated 32-bit single precision registers, also addressable as 16 double-word registers.
  - Decoupled three-stage pipeline.
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Features include:
  - External interrupts. Configurable from 1 to 240; the NUC505 has been configured with 32 interrupts.
  - Bits of priority, configurable from bit 3 to bit 7.
  - Dynamic reprioritization of interrupts.
  - Supports priority grouping which enables selection of preempting interrupt levels and non-preempting interrupt levels.
  - Supports tril-chaining and late arrival of interrupts, which enables back-to- back interrupt processing without the overhead of state saving and restoration between interrupts.
  - Processor state automatically saved on interrupt entry, and restored on interrupt exit with on instruction overhead.
  - Supports Wake-up Interrupt Controller (WIC) with Power-down mode.
- Memory Protection Unit (MPU). An optional MPU for memory protection, including:
  - Eight memory regions.
  - Sub Region Disable (SRD), enabling efficient use of memory regions.
  - The ability to enable a background region that implements the default memory map attributes.
- Low-cost debug solution that features:

- Debug access to all memory and registers in the system, including access to memory mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted.
- Serial Wire Debug Port (SW-DP) or Serial Wire JTAG Debug Port (SWJ-DP) debug access. But NUC505 only supports SW-DP.
- Optional Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches.
- Optional Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling.
-

- Bus interfaces:
  - Three Advanced High-performance Bus-Lite (AHB-Lite) interfaces: ICode, Dcode, and System bus interfaces.

  Private Peripheral Bus (PPB) based on Advanced Peripheral Bus (APB) interface.
  - Bit-band support that includes atomic bit-band write and read operations.
  - Memory access alignment.
  - Write buffer for buffering of write data.
  - Exclusive access transfers for multiprocessor systems.

6.2 System Manager

6.2.1 Overview

The following functions are included in system manager section

- System reset
- System memory map
- Bus arbitration algorithm
- Global control registers
- System Timer (Systick)
- Nested Vectored Interrupt Control (NVIC)
- System control register map and description

6.2.2 System Reset

- Hardware Reset
  - Power-on Reset (POR)
  - Low level on the nRESET Pin (nRST)
  - Watchdog time-out reset (WDT)
  - Low voltage reset (LVR)
- Software Reset
  - SYSRESETREQ (AIRCR[2])
  - CPU Reset (SYS_IPRST0[0])
  - CHIPRST (SYS_IPRST0 [1])

Note1: SYSRESETREQ (AIRCR[2]) reset the whole chip including all peripherals, but does not reset SPIM function, vector map module parameter setting, and PA.8~PA.15 multi-function setting.

Note2: CPU Rest (SYS_IPRST0[0]) only resets the CPU function.

Note3: CHIPRST (SYS_IPRST0[1]) reset the whole chip including all peripherals.

6.2.3 System Power-on Setting

The power-on setting is used to configure the chip to enter the specified state when the chip is powered up or reset. Since each pin of power-on setting has an internal pulled-up resistor during reset period, if the application needs to set the configuration to “0”, the proper pull-down must be added for the corresponding configuration pins.

PB.4	PB.3	PA.10	PA.9	Description	Register Mapping
1	1	1	1	Boot from Internal MCP SPI Flash	SYS_BOOTSET[3:0]
1	1	1	0	Boot from USB	SYS_BOOTSET[3:0]
1	1	0	1	Boot from External SPI Flash	SYS_BOOTSET[3:0]
1	0	1	1	Boot from ICP Mode	SYS_BOOTSET[3:0]
0	1	1	1	SWD/ICE Mode with Internal SPI Flash	SYS_BOOTSET[3:0]
0	1	1	0	SWD/ICE Mode with External SPI Flash	SYS_BOOTSET[3:0]

Table 6.2-1 System Power-on Setting Guide

6.2.4 System Power Distribution

In this chip, power distribution is divided into five segments:

- Audio CODEC power from $AV_{DDCODEC}$, AV_{DDHP}, and AV_{SSHP} provides the power for audio CODEC operation.
- Analog-to-Digital converter (ADC) power from AV_{DDADC} and AV_{SSADC} provides the power for ADC operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.2 V power for digital operation and I/O pins.
- USB transceiver power from USB_VBUS offers the power for operating the USB transceiver.
- RTC power from V_{BAT} provides the power for RTC and 80 bytes backup registers.

The outputs of internal voltage regulators, LDO and V_{DD}, require an external capacitor which should be located close to the corresponding pin. Analog power ($AV_{DDCODEC}$ and AV_{DDADC}) should be the same voltage level of the digital power (V_{DD}). The following figure shows the power distribution of the NuMicro® NUC505.

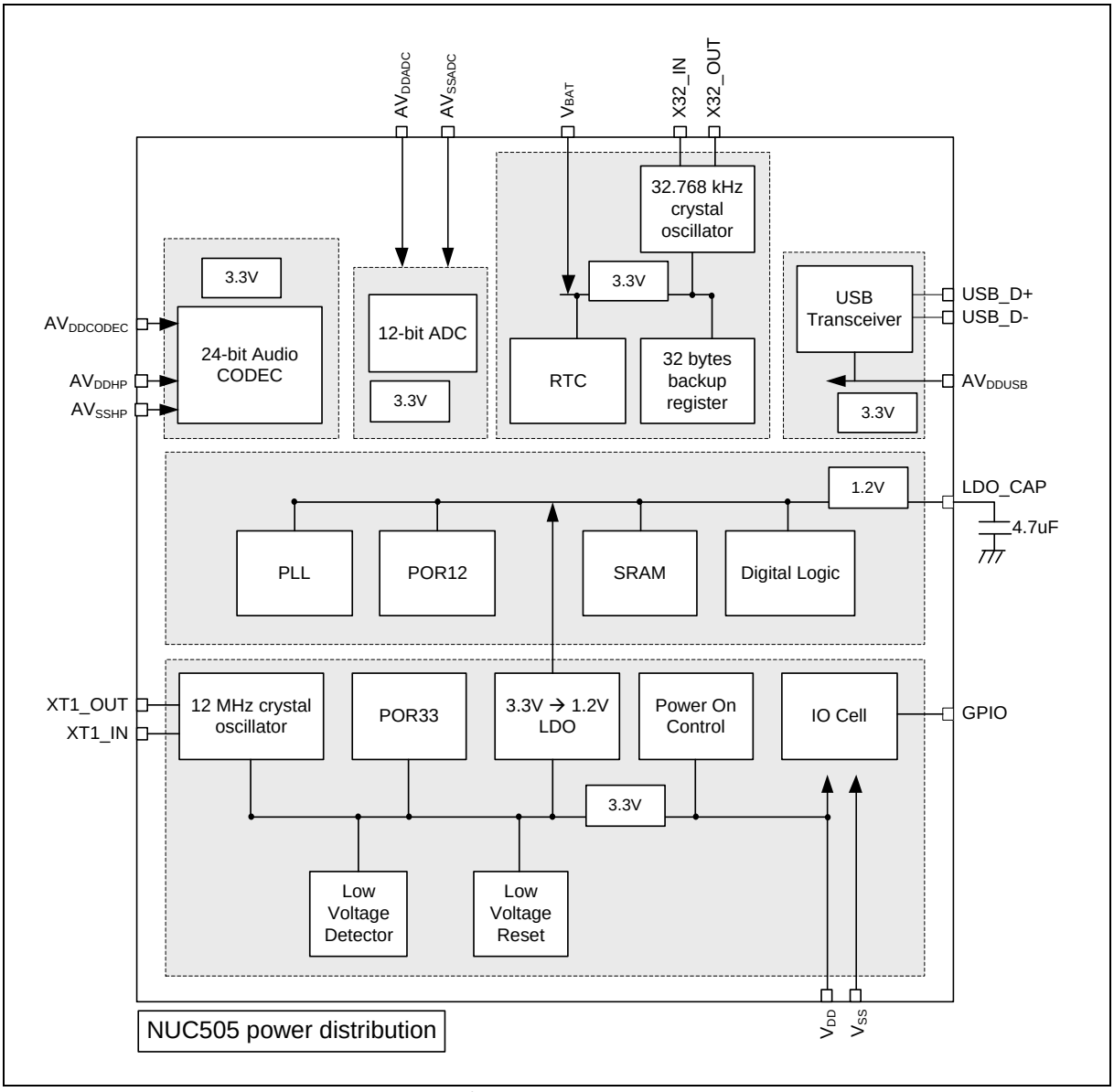


Figure 6.2-1 NuMicro® NUC505 Power Distribution Diagram

6.2.5 System Memory Mapping

The NUC505 provides a 4G-byte address space for programmers. The memory locations assigned to each on-chip modules are shown in Table 6.2-2. The detailed registers and memory addressing or programming will be described in the following sections for individual on-chip modules. The NUC505 only supports little-endian data format.

Address Space	Token	Modules
Memory Space		
0x1FFF_0000 – 0x1FFF_7FFF	IBR_BA	Internal Boot ROM (IBR) Memory Space

0x2000_0000 – 0x2000_7FFF	SRAM1_BA	SRAM1 Memory Space (32K Bytes)
0x2000_8000 – 0x2000_FFFF	SRAM2_BA	SRAM2 Memory Space (32K Bytes)
0x2001_0000 – 0x2001_7FFF	SRAM3_BA	SRAM3 Memory Space (32K Bytes)
0x2001_8000 – 0x2001_FFFF	SRAM4_BA	SRAM4 Memory Space (32K Bytes)
0x0000_0000 – 0x0FFF_FFFF	FLASH_BA	SPI Flash/ROM Memory Space
AHB Controllers Space (0x4000_0000 ~0x4000FFFF)		
0x4000_0000 – 0x4000_01FF	GCR_BA	Global Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers
0x4000_7000 – 0x4000_7FFF	SPIM_BA	SPIM Control Register
0x4000_9000 – 0x4000_9FFF	USBD_BA	USB Device Controller Registers
0x4000_A000 – 0x4000_AFFF	SDH_BA	SDH Control Register
0x4000_B000 – 0x4000_BFFF	USBH_BA	USB Host Controller Registers
APB Controllers Space (0x400E_0000~0x400E_FFFF)		
0x400E_1000 – 0x400E_1FFF	SPI1_BA	SPI1 Master/Slave Controller Registers (SPI1)
0x400E_2000 – 0x400E_2FFF	ADC_BA	ADC Controller Registers
0x400E_3000 – 0x400E_3FFF	GPIO_BA	GPIO Controller Registers
0x400E_4000 – 0x400E_4FFF	I2C0_BA	I2C0 Interface Control Registers
0x400E_5000 – 0x400E_5FFF	I2C1_BA	I2C1 Interface Control Registers
0x400E_6000 – 0x400E_6FFF	PWM_BA	PWM Controller Registers
0x400E_7000 – 0x400E_7FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x400E_8000 – 0x400E_8FFF	I2S_BA	Inter-IC Sound (I^2S) Control Register
0x400E_9000 – 0x400E_9FFF	SPI0_BA	SPI0 Master/Slave Controller Registers (SPI0)
0x400E_A000 – 0x400E_AFFF	Timer01_BA	Timer0/Timer1 Control Registers
0x400E_B000 – 0x400E_BFFF	Timer23_BA	Timer2/Timer3 Control Registers
0x400E_C000 – 0x400E_CFFF	UART0_BA	UART0 Control Registers (Normal Speed)
0x400E_D000 – 0x400E_DFFF	UART1_BA	UART1 Control Registers (High Speed)
0x400E_E000 – 0x400E_EFFF	UART2_BA	UART2 Control Registers (High Speed)
0x400E_F000 – 0x400E_FFFF	WDT_BA	WDT Interface Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-2 Address Space Assignments for On-Chip Controllers

6.2.6 SRAM Memory Organization

The NUC505 supports embedded SRAM with a total of 128 Kbytes and the SRAM organization is separated to four banks: SRAM bank0, SRAM bank1, SRAM bank2, and SRAM bank3. Each of these four banks has 32 Kbytes address space and can be accessed simultaneously.

- Supports a total of 128 Kbytes SRAM
- Supports byte / half word / word write
- Supports fixed 32 Kbytes SRAM banks for independent access
- Supports remap address to 0x1FF0_0000
- Supports remap arbitrary memory block of 128 Kbytes SRAM to 0x0000_0000 by using vector map module

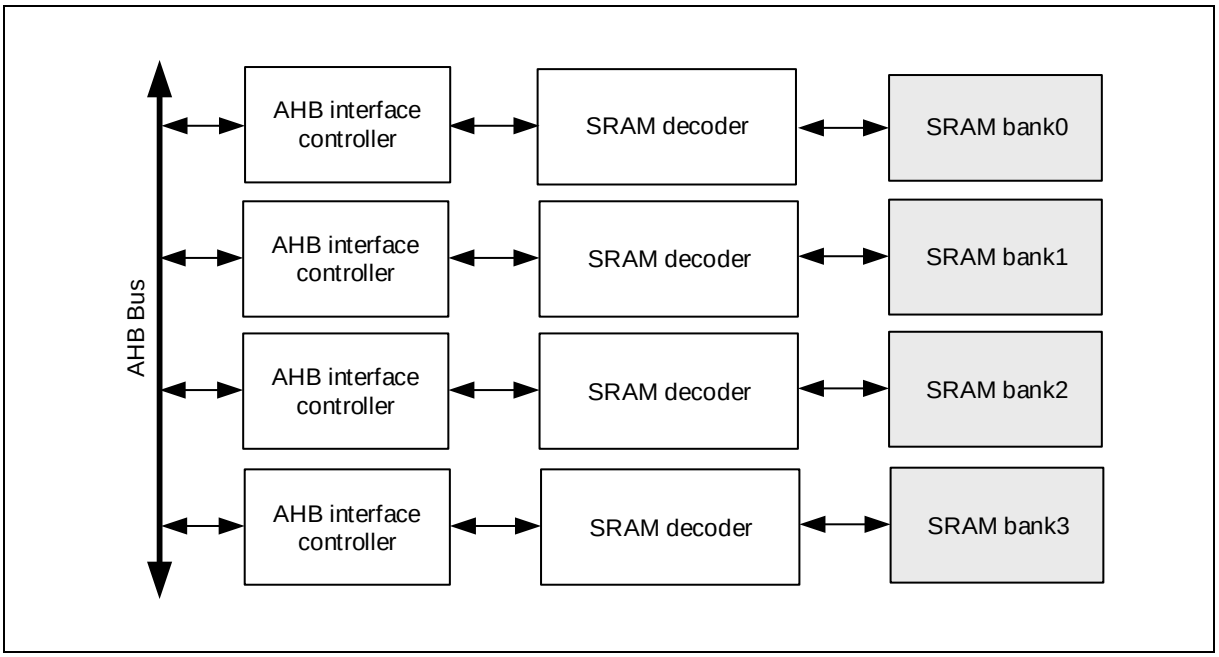


Figure 6.2-2 SRAM Block Diagram

Figure 6.2-3 shows the SRAM organization of NUC505. There are four SRAM banks in NUC505 and each bank is addressed to 32 Kbytes. The bank0 address space is from 0x2000_0000 to 0x2000_7FFF. The bank1 address space is from 0x2000_8000 to 0x2000_FFFF. The bank2 address space is from 0x2001_0000 to 0x2001_7FFF. The bank3 address space is from 0x2001_8000 to 0x2001_FFFF.

The address of each bank is remapping from 0x2000_0000 to 0x1FF0_0000. CPU can access SRAM bank0 through 0x2000_0000 to 0x2000_7FFF or 0x1FF0_0000 to 0x1FF0_7FFF, SRAM bank1 through 0x2000_8000 to 0x2000_FFFF or 0x1FF0_8000 to 0x1FF0_FFFF, SRAM bank2 through 0x2001_0000 to 0x2001_7FFF or 0x1FF1_0000 to 0x1FF1_7FFF, and SRAM bank3 through 0x2001_8000 to 0x2001_FFFF or 0x1FF1_8000 to 0x1FF1_FFFF.

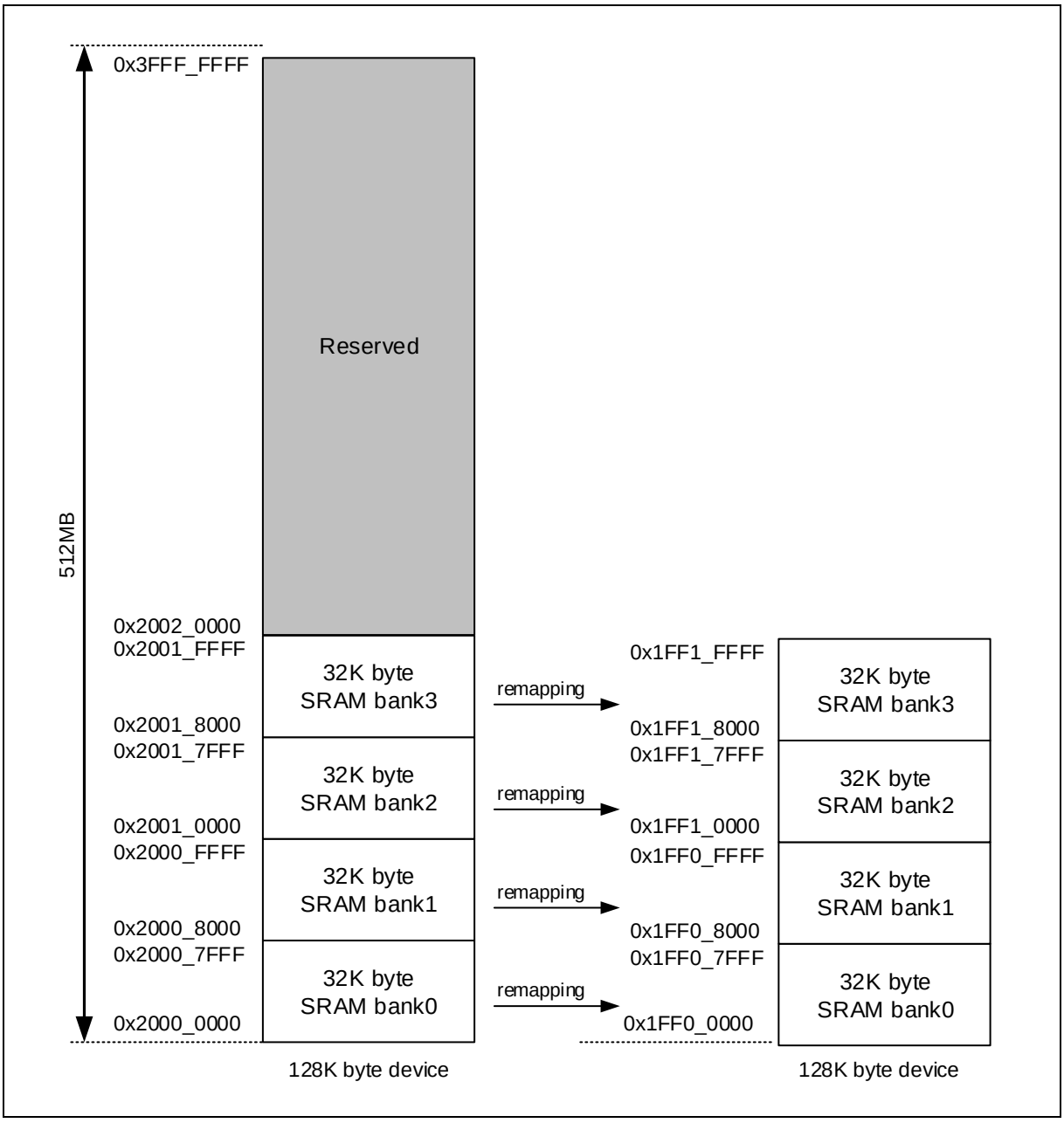


Figure 6.2-3 SRAM Memory Organization

Figure 6.2-4 shows the vector map module diagram. Arbitrary memory block in 128 Kbytes SRAM can be remapped to the SPI flash block and its start address is 0x0000_0000. The location and size with the memory block are controlled by the register SYS_RVMPADDR[31:0] and the register SYS_RVMPLEN[31:24]. The SYS_RVMPADDR indicates the start address of the memory block and SYS_RVMPLEN describes about the size of the memory block (the unit is 1 Kbyte).

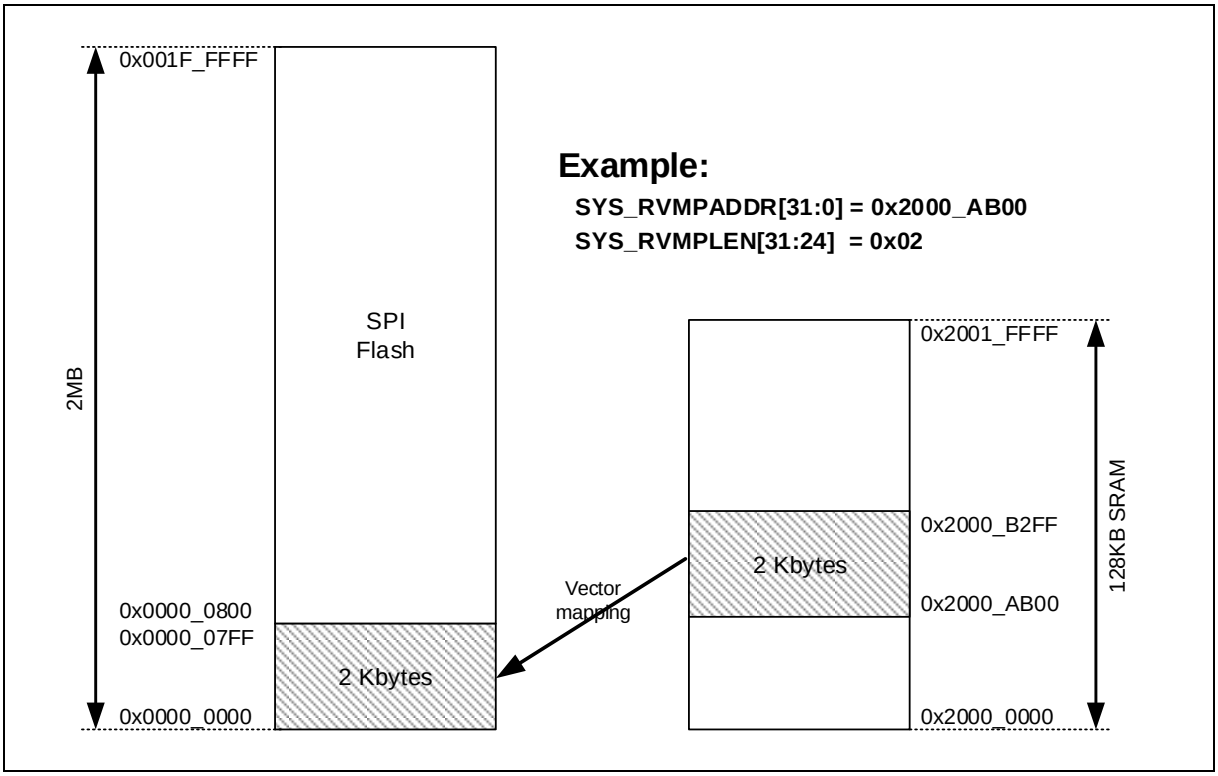


Figure 6.2-4 Vector Map Module Block

6.2.7 AHB Bus Arbitration

The internal bus of NUC505 is an AHB-Compliant Bus and supports to connect with the standard AHB master or slave. The NUC505 AHB arbiter provides a choice of two arbitration algorithms for simultaneous requests. These two arbitration algorithms are the Fixed-priority mode and the Round-robin- priority (rotate) mode. The selection of modes and types is determined in the **PRISEL** field of the ***SYS_AHBCTL*** control register.

6.2.7.1 Fixed Priority Mode

Fixed priority mode is selected if **PRISEL** = 0. The order of priorities on the AHB mastership among the on-chip master modules are listed in Table 6.2-3.

Priority Sequence (PRISEL = 0)	AHB Bus Priority
1 (Lowest)	Cortex-M4 I
2	Cortex-M4 D
3	Cortex-M4 System
4	SPIM
5	USBD

6	USBH
6	SDH
8 (Highest)	I^2S

Table 6.2-3 AHB Bus Priority Order in Fixed Priority Mode If two or more master modules request to access AHB bus at the same time, the higher priority request will get the permission to access AHB bus.

Priority Sequence (PRISEL = 0)	**AHB Bus Priority**
1 (Lowest)	Cortex-M4 I
2	Cortex-M4 D
3	Cortex-M4 System
4	SPIM
5	USBD
6	USBH
6	SDH
8 (Highest)	I^2S

Table 6.2-3 AHB Bus Priority Order in Fixed Priority Mode

The SPI flash controller normally has the lowest priority (except CPU interface) under the fixed priority mode. The NUC505 provides a mechanism to raise the priority of CPU request to the highest. If the **CPUHPRI** bit (bit-4 of ***SYS_AHBCTL*** *control register*) is set to 1, the **PRISTS** bit (bit-5 of ***SYS_AHBCTL*** *control register*) will be automatically set to 1 while an unmasked external IRQ occurs. Under this circumstance, the ARM core will become the highest priority to access AHB bus.

The programmer can recover the original priority order by directly writing "1" to clear the **PRISTS** bit. For example, this can be done that at the end of an interrupt service routine. Note that **PRISTS** only can be automatically set to 1 by an external interrupt when **CPUHPRI** = 1. It will not take effect for a programmer to directly write 1 to **PRISTS** to raise ARM core's AHB priority.

6.2.7.2 Round Robin Priority Mode

Round-robin priority mode is selected if **PRISEL** = 1. The AHB bus arbiter uses a round robin arbitration scheme for every master module to gain the bus ownership in turn. That is the requestor having the highest priority becomes the lowest-priority requestor after it has been granted access.

6.2.7.3 Rotate rule Example

In the default sequence of AHB Master Bus, the priority is I^2S>SDH > USBH > USBD >SPIM >M4(S) > M4(D) > M4(I).

6.2.8 System Timer (Systick)

The Cortex®-M4 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “ARM® Cortex®-M4 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.2.9 Nested Vectored Interrupt Control (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. Users can only fully access the NVIC from privileged mode, but this may cause interrupts to enter a pending state in user mode if enabling the Configuration and Control Register. Any other user mode access causes a bus fault. Users can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

- An implementation-defined number of interrupts, in the range 1-240 interrupts.
- A programmable priority level of 0-16 for each interrupts. A higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC, providing Power-down mode support.

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.2.9.1 Exception Model and System Interrupt Map

The following table lists the exception model supported by NUC505 series. Software can set 16 levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0x00” and the lowest priority is denoted as “0xF0” (The 4-LSB always 0). The default priority of all the user-configurable interrupts is “0x00”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR to relocate the vector table start address to a different memory location, in the range 0x00000080 to 0x3FFFFF80,

The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Exception Type	Vector Number	Vector Address	Priority
Reset	1	0x00000004	-3
NMI	2	0x00000008	-2
Hard Fault	3	0x0000000C	-1
Memory Manager Fault	4	0x00000010	Configurable
Bus Fault	5	0x00000014	Configurable
Usage Fault	6	0x00000018	Configurable
Reserved	7 ~ 10		Reserved
SVCall	11	0x0000002C	Configurable
Debug Monitor	12	0x00000030	Configurable
Reserved	13		Reserved
PendSV	14	0x00000038	Configurable
SysTick	15	0x0000003C	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	0x00000000 + (Vector Number)*4	Configurable

Table 6.2-4 Exception Model

Vector Number	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	PWR_INT	Power On Interrupt
17	1	WDT_INT	Watch Dog Timer interrupt
18	2	Reserved	Reserved
19	3	I2S_INT	I^2S interrupt
20	4	EINT0_INT	External GPIO Group 0 interrupt
21	5	EINT1_INT	External GPIO Group 1 interrupt
22	6	EINT2_INT	External GPIO Group 2 interrupt
23	7	EINT3_INT	External GPIO Group 3 interrupt
24	8	SPIM_INT	SPIM interrupt
25	9	USBD_INT	USB Device 20 interrupt
26	10	TM0_INT	Timer0 interrupt
27	11	TM1_INT	Timer1 interrupt
28	12	TM2_INT	Timer2 interrupt

29	13	TM3_INT	Timer3 interrupt
30	14	SDH_INT	SDH interrupt
31	15	PWM0_INT	PWM0 interrupt
32	16	PWM1_INT	PWM1 interrupt
33	17	PWM2_INT	PWM2 interrupt
34	18	PWM3_INT	PWM3 interrupt
35	19	RTC_INT	Real Time Clock interrupt
36	20	SPI0_INT	SPI0 interrupt
37	21	I2C1_INT	I2C1 interrupt
38	22	I2C0_INT	I2C0 interrupt
39	23	UART0_INT	UART0 interrupt
40	24	UART1_INT	UART1 interrupt
41	25	ADC_INT	ADC interrupt
42	26	wwdt_INT	Window Watch Dog Timer interrupt
43	27	USBH_INT	USB Host 1.1 interrupt
44	28	UART2_INT	UART2 interrupt
45	29	LVD_INT	Low Voltage Detection interrupt
46	30	SPI1_INT	SPI1 interrupt
47	31	Reserved	Reserved

Table 6.2-5 Interrupt Number Table

6.2.9.2 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts, and each interrupt uses MSB 4 bits of the 8-bit field).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip. The clocks include AHB, APB and engine clocks for all of devices like USB device, USB host, UART and so on. There are two PLL clocks, PLL and APLL, derived from external HXT clock input. The PLL clock allows the processor to operate at a high internal clock frequency. Also, the APLL is used to generate more accuracy frequency for audio CODEC. They also implement the power control function, include the individually clock on or off control register, clock source selector and divider. These functions minimize the extra power consumption and the chip runs on the just right condition. In Power-down mode, the controller turns off the crystal oscillator to minimize the chip power consumption.

6.3.2 Clock Diagram

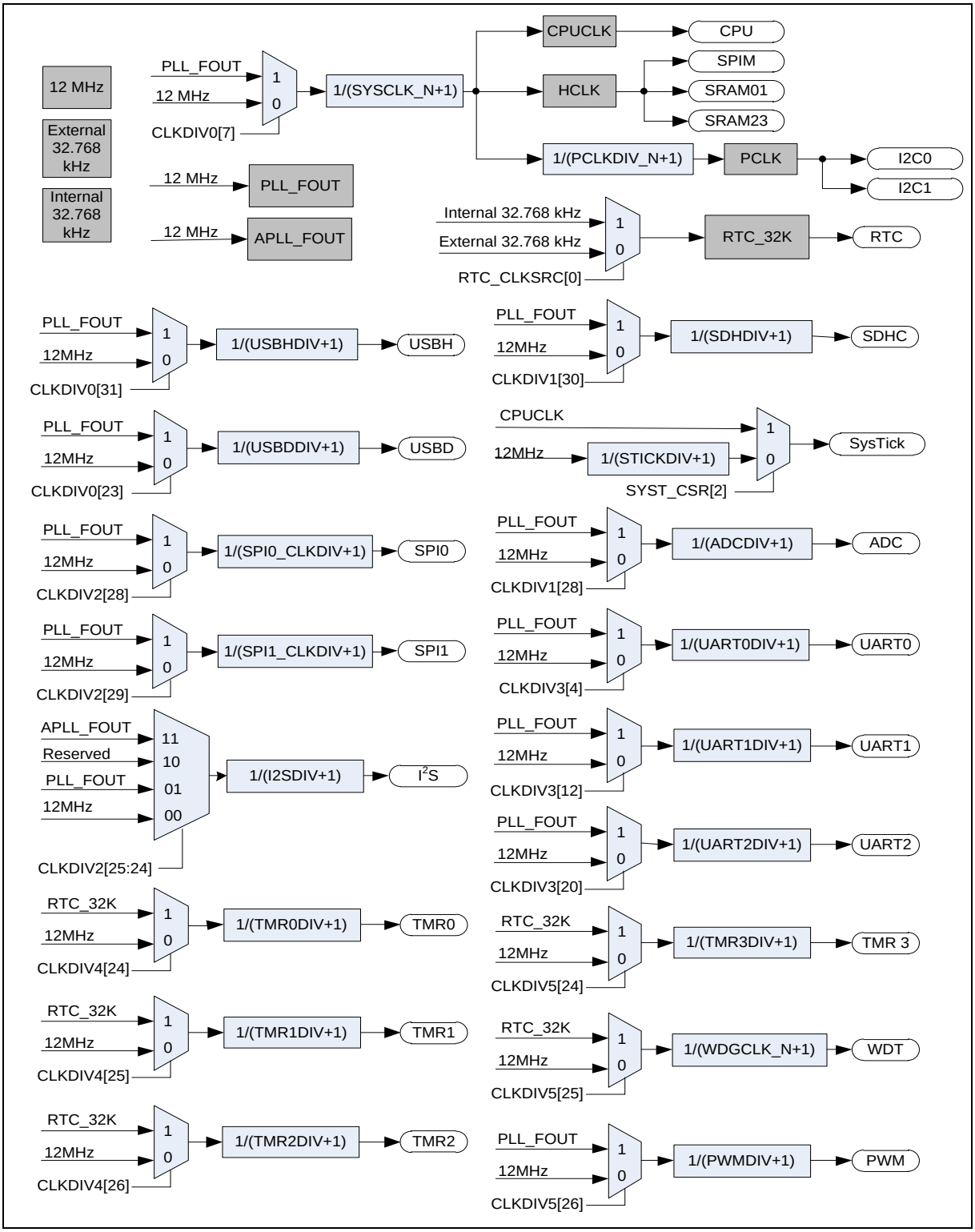


Figure 6.3-1 Clock Generator Global View Diagram

6.3.3 Clock Generator

The clock generator consists of 4 clock sources, which are listed below:

- Real-time clock (RTC_CLK) source can be selected from external 32.768 kHz external low speed crystal oscillator (LXT) or 32.768 kHz internal low speed RC oscillator (LIRC)
- 12 MHz external high speed crystal oscillator (HXT)
- Programmable System PLL output clock frequency (PLL_FOUT)
- Programmable Audio PLL output clock frequency (APLL_FOUT)

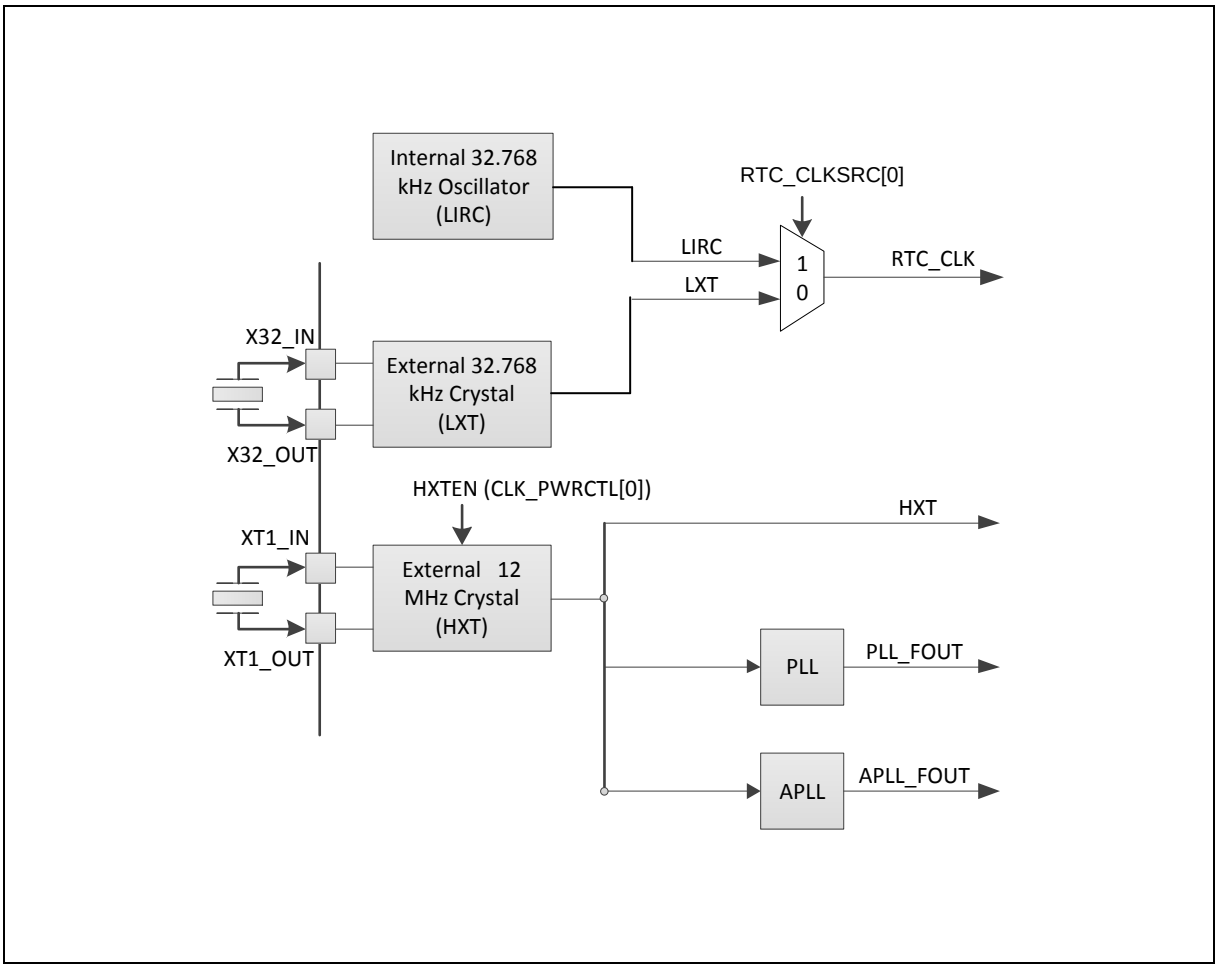


Figure 6.3-2 Clock Generator Block Diagram

The external crystal oscillator and two capacitors are connected to the pad “XT1_IN / X32_IN” and pad “XT1_OUT / X32_OUT”. The capacitance value of the two capacitors may be changed for differential crystal oscillator from different vender. The load capacitance values and resistance values must be adjusted according to the selected oscillator. The recommended load capacitance values and resistance values as

Crystal Oscillator	Capacitance Values	Resistance Values

12 MHz	20pF	1 MΩ
32.768 kHz	33pF	10 MΩ

Table 6.3-1 Recommended Load Capacitance Values and Resistance Values.

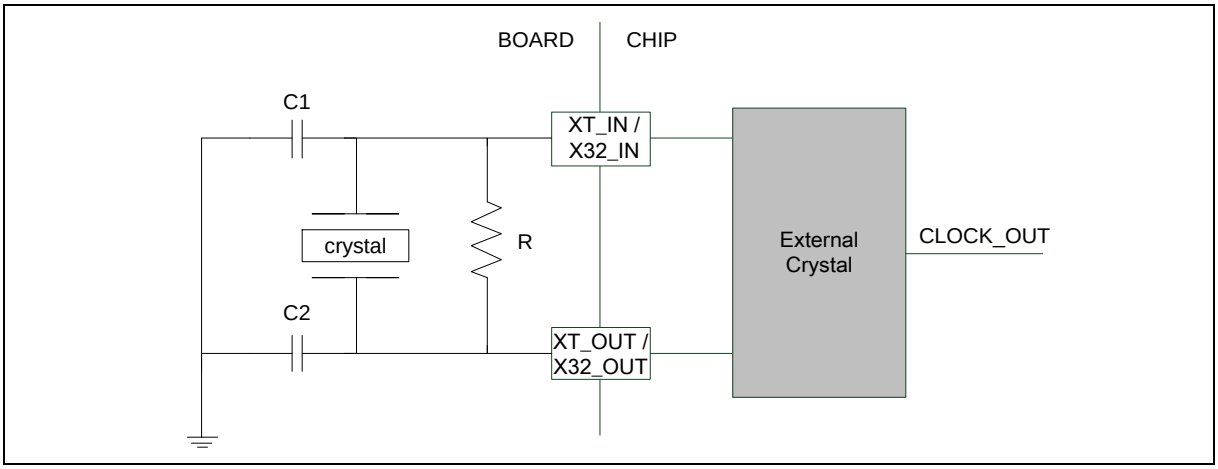


Figure 6.3-3 Crystal Oscillator Circuit

6.3.4 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

The clocks which still keep active are listed below:

- Clock Generator
  - 32.768 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock

In Power-down mode, If the woke-up even occurred, the disabled clocks will be regenerated after PDWKPSC (CLK_PWRCTL[23:8]) x 256 HXT cycle.

6.4 General Purpose I/O (GPIO)

6.4.1 Overview

The NUC505 series has up to 52 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. The 52 pins are arranged in 4 ports named as PA, PB, PC, and PD. PA and PB have 16 pins on port, PC has 15 pins on port, and PD has 5 pins on port. Each of the 52 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each I/O pins can be configured by software individually as Input or Push-pull output mode. After the chip is reset, the I/O mode of all pins is input mode with no pull-up and pull-down enable (except PB.2, it is pull-up enable). Each I/O pin has an individual pull-up and pull-down resistor which is about 40 kΩ ~ 50 kΩ for VDD and Vss. User can set Px_PUEN to control I/O pins to pull-up or pull-down.

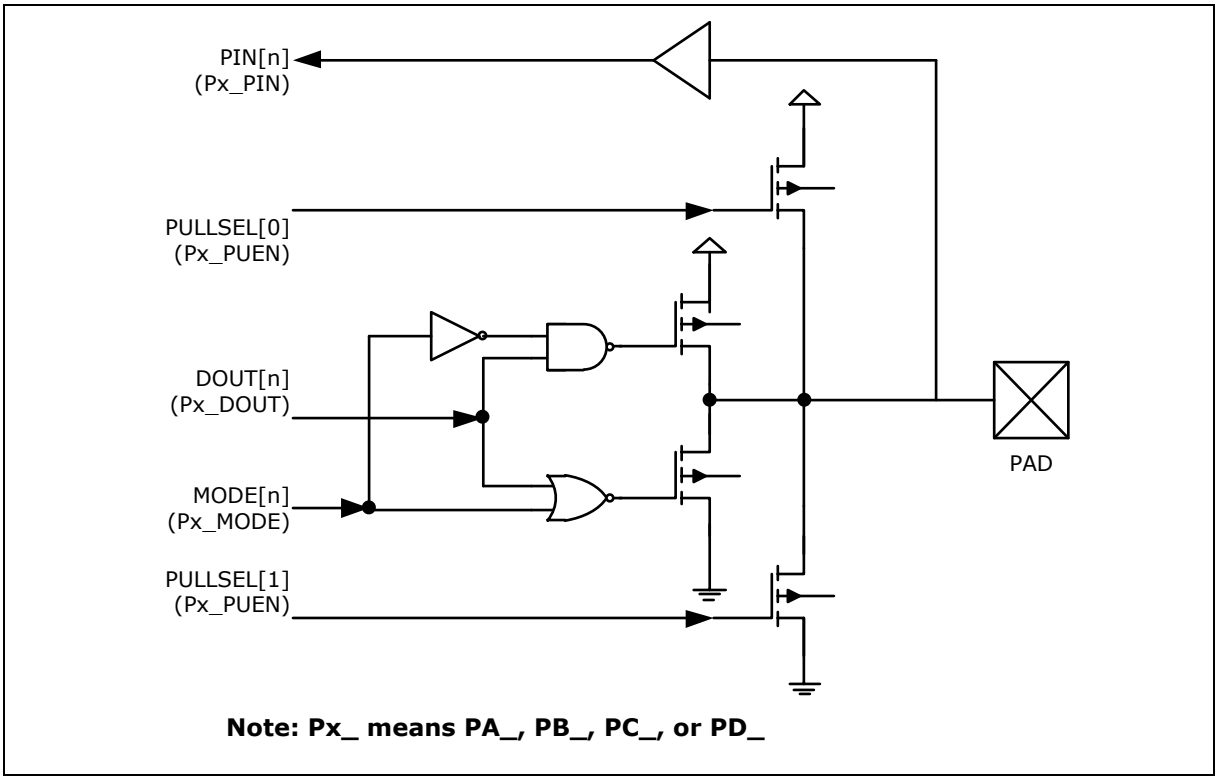


Figure 6.4-1 I/O Pin Block Diagram

6.4.2 Features

- Two I/O modes:
  - Push-Pull Output mode
  - Input only with high impendence mode
- CMOS/Schmitt trigger input selectable (refers SYS_GPAIBE register on TRM)
- I/O pin can be configured as interrupt source with edge setting

- I/O pin has individual internal pull-up resistor and pull-down resistor
- Enabling the pin interrupt function will also enable the wake-up function

6.5 Timer Controller (TIMER)

6.5.1 Overview

The Timer Controller includes four 32-bit timers, TIMER0 ~ TIMER3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.5.2 Features

- Four sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides One-shot, Periodic, Toggle and Continuous Counting operation modes
- Time-out period = (Period of timer clock input) * (8-bit prescale counter+1) * CMPDAT (TIMERx_CMP[23:0])
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit up counter value is readable through TIMERx_CNT (Timer Data Register)
- Supports event counting function to count the event from external pin (TM0_CNT_OUT~TM3_CNT_OUT)
- Supports external capture pin (TM0_EXT~TM3_EXT) for interval measurement
- Supports external capture pin (TM0_EXT~TM3_EXT) to reset 24-bit up counter
- Supports chip wake-up from Idle mode, Power-down mode and Deep Power-down mode, if a timer interrupt signal is generated.

6.6 PWM Generator and Capture Timer (PWM)

6.6.1 Overview

The NUC505 series has one PWM generator that can support four channels PWM output or four channels input capture sharing the same pins (PWM_CH0/ PWM_CH1/PWM_CH2/PWM_CH3).

The PWM generator has a 16-bit PWM counter and comparator, and the PWM generator supports two standard PWM output modes: Independent output mode and Complementary output mode with 8-bit Dead-time generator. Each mode can be used as a timer and issues interrupt independently. In addition, It also has an 8-bit prescaler and clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16) to support wide range clock frequency of PWM counter. For PWM output control unit, it supports polarity output function.

The PWM generator also supports input capture function. It supports latch PWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

After the capture feature is enabled, the capture always latches PWM-counter to RCAPDATn when input channel has a rising transition and latched PWM-counter to FCAPDATn when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CRLIEN0 (PWM_CAPCTL01[1]) (Rising latch Interrupt enable) and CFLIEN0 (PWM_CAPCTL01[2]) (Falling latch Interrupt enable) to determine the condition of interrupt occur. Capture channel 1 has the same feature by setting CRLIEN1 (PWM_CAPCTL01[17]) and CFLIEN1 (PWM_CAPCTL01[18]). The capture channel 2 & 3 has the same feature by setting CRLIEN2 (PWM_CAPCTL23[1]),CFLIEN2 (PWM_CAPCTL23[2]) and CRLIEN3 (PWM_CAPCTL23[17]), CFLIEN3 (PWM_CAPCTL23[18]) respectively. Whenever Capture issues Interrupt 0/1/2/3, the PWM counter 0/1/2/3 will be reload at this moment.

There are only four interrupts from PWM. PWM 0 and Capture 0 share the same interrupt; PWM 1 and Capture 1 share the same interrupt and so on. Therefore, PWM function and Capture function in the same channel cannot be used at the same time.

6.6.2 Features

6.6.2.1 PWM function features

- Supports 4 PWM output channels with 16-bit resolution
- Supports 8-bit prescaler and clock divider
- Supports 4 PWM interrupts
- Supports One-shot or Auto-reload PWM counter operation mode
- Supports 8-bit Dead-time

6.6.2.2 Capture function features

- Supports 4 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports 4 Capture interrupts

6.7 Watchdog Timer (WDT)

6.7.1 Overview

The Watchdog Timer is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, the Watchdog Timer supports the function to wake up system from Power-down mode.

6.7.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval.
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycle and the time-out interval period is 32.5 ms ~ 8.224 s if WDT_CLK = 32 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable Watchdog Timer reset delay period, including 1026、130 、18 or 3 WDT_CLK reset delay period.
- Supports Watchdog Timer time-out wake-up function when Watchdog Timer clock source is selected as 32 kHz low-speed oscillator.

6.8 Window Watchdog Timer (WWDT)

6.8.1 Overview

The Window Watchdog Timer is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.8.2 Features

- 6-bit down counter CNTDAT (WWDT_CNT[5:0]) and 6-bit compare value CMPDAT (WWDT_CTL[21:16]) to make the window period flexible
- Selectable maximum 11-bit WWDT clock prescale PSCSEL (WWDT_CTL[11:8]) to make WWDT time-out interval variable

6.9 Real Time Clock (RTC)

6.9.1 Overview

The Real Time Clock (RTC) block can be operated by independent power supply while the system power is off. The RTC uses a 32.768 kHz external crystal (LXT) or internal oscillator (LIRC), and offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate the frequency accuracy of external crystal oscillator (LXT) or internal oscillator (LIRC).

The RTC controller also offers 32 bytes spare registers to store user's important information.

The wake-up signal is used to wake the system from Idle mode, Power-down mode and Deep Power-down mode.

6.9.2 Features

- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register
- Supports Leap Year indication in RTC_LEAPYEAR register
- Supports Day of the Week counter in RTC_WEEKDAY register
- Frequency of RTC clock source compensate by RTC_FREQADJ register
- All time and calendar message expressed in BCD format
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports RTC Time Tick and Alarm Match interrupt
- Supports chip wake-up from Idle mode, Power-down mode and Deep Power-down mode while a RTC interrupt signal is generated
- Supports 32 bytes spare registers and these registers values are preserved when RTC power domain is existed

6.10 UART Interface Controller (UART)

6.10.1 Overview

The NUC505 series provides three channels of Universal Asynchronous Receiver/Transmitters (UART). The UART Controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART Controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, RS-485, auto-flow control function and auto-baud rate measuring function.

6.10.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16(UART0) / 64/64(UART1 and UART2) bytes entry FIFO for data payloads
- Supports hardware auto-flow control (nCTS and nRTS) with UART1 and UART2
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS and data wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface features
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART1 /UART2 with LIN function)
  - Supports LIN Master/Slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detection function for receiver
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction

6.11 I²C Serial Interface Controller (Master/Slave)

6.11.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more details about I²C Bus Timing.

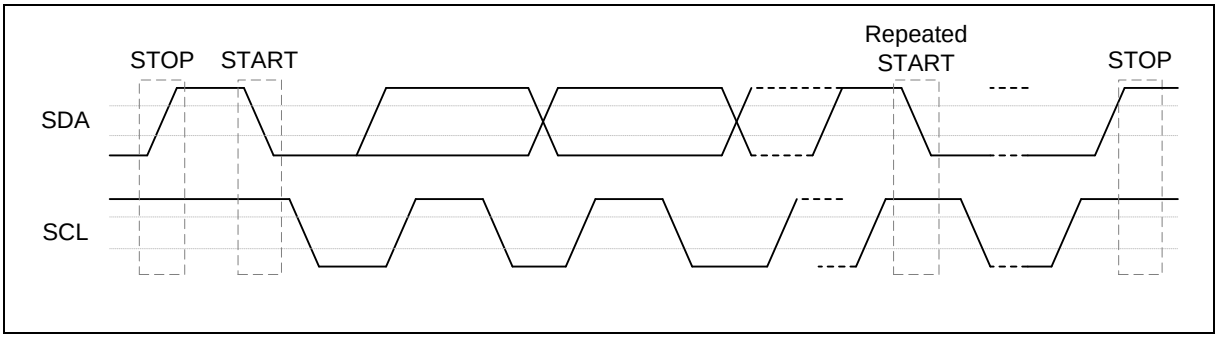


Figure 6.11-1 I²C Bus Timing

The device on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit I2CEN (I2C_CTL[6]) should be set to '1'. The I²C H/W interfaces to the I²C bus via two pins: SDA and SCL. Pull up resistor is needed for I²C operation as these are open drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

6.11.2 Features

The NUC505 series provides two channels of I^2C. The I^2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus include:

- Master/Slave mode and General Call Mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to stretch and un-stretch serial transfer
- Built-in a 14-bit time-out counter will request the I^2C interrupt if the I^2C bus hangs up and time-out counter overflows.
- Programmable divider allowing for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave addresses with mask option)
- Supports address match wake-up function

6.12 Serial Peripheral Interface (SPI)

6.12.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol that operates in full duplex mode. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The NUC505 series contains one set of SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Also, the SPI controller can be configured as a master or a slave device.

6.12.2 Features

- Supports Master or Slave mode operation
- Configurable bit length of a transfer word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports byte reorder function
- Supports Byte or Word Suspend mode
- Supports 3-wire, no slave select signal, bi-direction interface
- Up to 2 sets of SPI controllers

6.13 SPI Memory Interface Controller (SPIM)

6.13.1 Overview

The SPI Memory Interface Controller performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data received from CPU. This controller can drive up to 2 external peripherals (embedded SPI Flash or external SPI Flash) and act as a SPI master. It can generate an interrupt signal when data transfer is finished and can be cleared by writing 1 to the interrupt flag. The active level of device/slave select signal can be chosen to low active or high active, which depends on the peripheral. Writing a divisor into the SPIM_CTL1 register can program the frequency of serial clock output to the peripheral. This controller contains four 32-bit transmit/receive buffers, and can provide 1 to 4 burst mode operation. The number of bits in each transaction can be 8, 16, 24, or 32; data can be transmitted/received up to four successive transactions in one transfer.

6.13.2 Features

- Supports SPI master mode
- Supports DMA mode (DMA Write and DMA Read), Direct Memory Map (DMM) mode, and I/O mode
- 8-, 16-, 24-, and 32-bit length of transaction
- Supports standard (1-bit), dual (2-bit), and quad (4-bit) I/O transfer mode
- Provides burst mode operation, which can transmit/receive data up to four successive transactions in one transfer
- Two slave/device select lines (embedded SPI Flash or external SPI Flash)
- Fully static synchronous design with one clock domain

6.14 I²S Controller with Internal Audio CODEC (I²S)

6.14.1 Overview

The I²S controller consists of I²S protocol interface to internal audio CODEC and supports to use external audio CODEC. The I²S controller includes two 16 words FIFO for transfer path and receiver path respectively and is capable of handling 8, 16, 24, or 32 bits word sizes sample.

The structure of internal audio CODEC is a delta-sigma 24-bit CODEC with microphone input, audio line-in input, and headphone output.

6.14.2 Features

I²S Controller

- Supports Master mode and Slave mode
- Capable of handling 8-, 16-, 24- and 32-bit word sizes sample
- Supports Mono and Stereo audio data
- Supports I²S and most significant bit (MSB) justified data format
- Supports PCM-A and PCM-B data format
- Provides two 16 words FIFO, one for transmitting and the other for receiving
- Generates interrupt requests when FIFO levels cross a programmable boundary
- Supports TX DMA function for transmitting and RX DMA function receiving
- Supports RX Data Power Measurement
- Supports connecting to external audio CODEC

Internal CODEC

- Supports mono microphone input and stereo audio line-in input
- Supports stereo headphone output
- Supports stereo and mono mode
- Features of ADC
  - Total-Harmonic-Distortion with Noise (THD+N): -80 dB
  - Dynamic-Range (DR) and Signal-to-Noise ratio (SNR): 90 dB (A-Weighted)
- Features of DAC (headphone out with 32Ω loading)
  - Total-Harmonic-Distortion with Noise (THD+N): -60 dB
  - Dynamic-Range (DR) and Signal-to-Noise ratio (SNR): 93 dB (A-Weighted)
- Supports sampling rate with 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, and 96 kHz

6.15 USB 2.0 Device Controller (USBD)

6.15.1 Overview

The USB device controller interfaces the AHB bus and the UTMI bus. The USB controller contains both the AHB master interface and AHB slave interface. CPU programs the USB controller registers through the AHB slave interface. For IN or OUT transfer, the USB device controller needs to write data to memory or read data from memory through the AHB master interface. The USB device controller is complaint with USB 2.0 specification and it contains 12 configurable endpoints in addition to control endpoint. These endpoints could be configured to BULK, INTERRUPT or ISO. The USB device controller has a built-in DMA to relieve the load of CPU.

6.15.2 Features

- USB Specification reversion 2.0 compliant
- Supports 12 configurable endpoints in addition to Control Endpoint
- Each of the endpoints can be Isochronous, Bulk or Interrupt and either IN or OUT direction
- Three different operation modes of an in-endpoint – Auto Validation mode, Manual Validation mode, Fly mode
- Supports DMA operation
- 2048 Bytes Configurable RAM used as endpoint buffer
- Supports Endpoint Maximum Packet Size up to 1024 bytes

6.16 USB 1.1 Host Controller (USBH)

6.16.1 Overview

The NUC505 series is equipped with one USB 1.1 Host Controller (USBH) that supports Open Host Controller Interface (OpenHCI, OHCI) Specification and register-level description of a host controller to manage the devices and data transfer of Universal Serial Bus (USB).

The USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port overcurrent detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting overcurrent of attached USB devices.

6.16.2 Features

- Supports Universal Serial Bus (USB) Specification Revision 1.1.
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports both full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt and Isochronous transfers.
- Supports an integrated Root Hub.
- Supports one USB host port in LQFP48 or LQFP64 and two USB host ports in QFN88
- Supports port power control and port overcurrent detection.
- Supports DMA for real-time data transfer.

6.17 Secure-Digital Host Controller (SDHC)

6.17.1 Overview

The Secure-Digital Host Controller (SDH Controller) includes a DMAC (Direct Memory Access Controller) unit and a SD unit. The DMAC unit provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer (128 bytes), and the SD unit controls the interface of SD/SDHC/MMC. The SD HOST controller can support SD/SDHC/MMC with DMAC to provide a fast data transfer between system memory and cards.

6.17.2 Features

- Supports single DMA channel.
- Supports hardware Scatter-Gather function.
- Using single 128 Bytes shared buffer for data exchange between system memory and cards.
- Interface with DMAC for register read/write and data transfer.
- Supports SD/SDHC/MMC card.
- The frequency of HCLK should be higher than the frequency of peripheral clock.

6.18 12-bit Analog-to-Digital Converter (ADC)

6.18.1 Overview

The NUC505 series contains one 12-bit successive approximation analog-to-digital converter (ADC) with 8 single-end external input channels (ADC_CH0, ADC_CH1, … ADC_CH7). The ADC_CH0 has an internal 10 kΩ resistor divider for battery detection. The ADC_CH2 also supports key pad comparator function. User can control the A/D conversion by setting the SWTRG (ADC_CTL[0]).

6.18.2 Features

- Analog input voltage range: 0~AV_{DDADC}.
- 12-bit resolution and 10-bit accuracy guaranteed.
- Up to 8 single-end analog input channels.
- ADC clock frequency up to 16 MHz.
- Up to 1 MSPS conversion rate when using in ADC_CH1 channel.
- Up to 200 kSPS conversion rate when using in ADC_CH2, …ADC_CH7 channels.
- Configurable ADC internal sampling time.
- Supports key pad comparator (ADC_CH2).
- Built-in 10 kΩ resistor divider for battery detection (ADC_CH0).

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{DD} - V_{SS}$	DC Power Supply	-0.3	+4.0	V
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V
$1/t_{CLCL}$	Oscillator Frequency		12	MHz
T_A	Operating Temperature	-40	+85	℃
T_{ST}	Storage Temperature	-55	+150	℃
I_{DD}	Maximum Current into V_{DD}	-	160	mA
I_{SS}	Maximum Current out of V_{SS}		160	mA
I_{IO}	Maximum Current sunk by a I/O pin		I/O pin[*2, 3, 4]	mA
	Maximum Current sourced by a I/O pin		I/O pin[*2, 3, 4]	mA
	Maximum Current sunk by total I/O pins		100	mA
	Maximum Current sourced by total I/O pins		100	mA

Note:

1. Exposure to conditions beyond those listed under absolute maximum ratings may adversely affect the lift and reliability of the device.
2. 4mA: PA.14, PA.15, PB.0, PB.1, PB.2, PB.3, PB.4, PB.5, PB.6, PB.7, PB.8, PB.9, PB.10, PB.11, PC.8, PC.9, PC.10, PC.11, PC.12, PD.0, PD.1
3. 8mA: PA.8, PA.9, PA.10, PA.11, PA.12, PA.13, PB.12, PB.13, PB.14, PB.15, PC.0, PC.1, PC.2, PC.3, PC.4, PC.5, PC.6, PC.7, PC.13, PC.14
4. Can setting strength for 2mA, 6.5mA, 8.7mA, 13mA, 15.2mA, 19.5mA, 21.7mA, 26.1mA: PA.0, PA.1, PA.2, PA.3, PA.4, PA.5, PA.6, PA.7, PD.2, PD.3, PD.4

7.2 DC Characteristics

(V_{DD} - V_{SS} = 3 ~ 3.6 V, T_A = 25°C)

SYMBOL	PARAMETER	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
V_{DD}	Operation Voltage	3	3.3	3.6	V	
V_{SS} AV_{SS}	Power Ground	-0.3	-	-	V	
V_{DD12}	Core Logic and I/O Buffer Pre-Driver Voltage	1.08	1.2	1.32	V	
V_{BAT}	RTC Power Supply	2	-	3.6	V	
I_{BAT_EX}	External crystal RTC Supply Current	-	4	-	uA	
I_{BAT_IN}	Internal RC RTC Supply Current	0.1	0.6	0.9	uA	
F_{INT_RC}	Internal RC frequency	15	32	90	Khz	
V_{OH}	High Level Output Voltage	2.4	-	-	V	
V_{OL}	Low Level Output Voltage	-	-	0.4	V	
V_{IH}	Input High Voltage	2.0	-	-	V	
V_{IL}	Input Low Voltage	-	-	0.8	V	
V_{TH}	Switch Threshold	0.87	1.05	1.2	V	Schmitt-falling-trigger
		1.65	1.9	2.1	V	Schmitt-rising-trigger
R_{PU}	Input Pull-up Resist	32	53	120	kΩ	V_{IN} = V_{ss}

SYMBOL	PARAMETER	SPECIFICATION				TEST CONDITIONS				
		MIN.	TYP.	MAX.	UNIT					
R_{PD}	Input Pull-down Resistance	37	49	120	kΩ	$V_{IN} = V_{DD}$				
I_L	Input Leakage Current	-10	-	10	uA					
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA					
I_{OL1}	Low level sink current [*1]	4	-	-	mA	$V_{OL} = 0.4V$				
I_{OL2}		8	-	-	mA					
I_{OL3}		2、6.5、8.7、13、15.2、19.5、21.7、26.1	-	-	mA					
I_{OH1}	High level source current [*2]	4	-	-	mA	$V_{OH} = 2.4V$				
I_{OH2}		8	-	-	mA					
I_{OH3}		2、6.5、8.7、13、15.2、19.5、21.7、26.1	-	-	mA					
I_{DD1}	V_{DD}= 3.3V, Operating current Normal Run Mode while(1){} executed from SPI flash or RAM	-	18.83	-	mA	HXT 12Mhz	LXT	PLL 96Mhz	All digital module	Code
						✔	×	✔	×	SPI
I_{DD2}		-	27.33	-		✔	×	✔	✔	SPI
I_{DD3}		-	25.38	-		✔	×	✔	×	RAM
I_{DD4}		-	32.13	-		✔	×	✔	✔	RAM
I_{DD5}		-	4.53			✔	×	×	×	SPI
I_{DD6}		-	6.47			✔	×	×	✔	SPI
I_{DD7}			5.23			✔	×	×	×	RAM
I_{DD8}			5.94			✔	×	×	✔	RAM

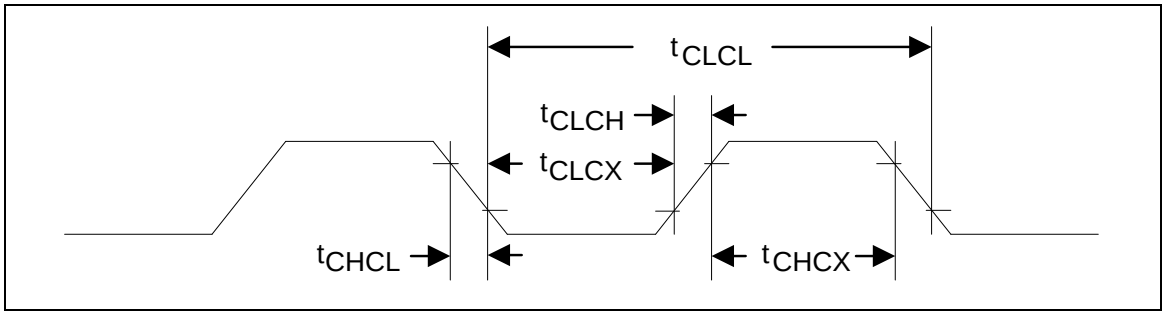
SYMBOL	PARAMETER	SPECIFICATION				TEST CONDITIONS			
		MIN.	TYP.	MAX.	UNIT				
I_{IDLE1}	V_{DD}= 3.3V, Operating Current Idle Mode at 12 MHz	-	17	-	mA	HXT	RTC	PLL	All digital module
						✔	×	×	✔
I_{IDLE2}		-	12.3	-		✔	×	×	×
I_{PWD}	V_{DD} =3.3V, Standby current Power-down (Deep Sleep)mode	700	-	-	uA	HXT	RTC	PLL	RAM retention
						×	×	×	✔

Note:

1. 4mA: PA.14, PA.15, PB.0, PB.1, PB.2, PB.3, PB.4, PB.5, PB.6, PB.7, PB.8, PB.9, PB.10, PB.11, PC.8, PC.9, PC.10, PC.11, PC.12, PD.0, PD.1
2. 8mA: PA.8, PA.9, PA.10, PA.11, PA.12, PA.13, PB.12, PB.13, PB.14, PB.15, PC.0, PC.1, PC.2, PC.3, PC.4, PC.5, PC.6, PC.7, PC.13, PC.14
3. Can setting strength for 2mA, 6.5mA, 8.7mA, 13mA, 15.2mA, 19.5mA, 21.7mA, 26.1mA: PA.0, PA.1, PA.2, PA.3, PA.4, PA.5, PA.6, PA.7, PD.2, PD.3, PD.4

7.3 AC Electrical Characteristics

7.3.1 External 12 MHz Crystal



Note: Duty cycle is 50%.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITION
Clock High Time	t_{CHCX}	-	41.6	-	nS	
Clock Low Time	t_{CLCX}	-	41.6	-	nS	
Clock Rise Time	t_{CLCH}	-	-	25	nS	
Clock Fall Time	t_{CHCL}	-	-	25	nS	

7.3.2 External 12 MHz High Speed Oscillator

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
f_{HXT}	Input clock frequency	External crystal for X_{IN}		12		MHz
T_A	Temperature	-	-40	-	85	℃
V_{HXT}	V_{DD}	-		3.3		V
I_{HXT}	Operating current	12 MHz@ V_{DD} = 3.3V	-	3	-	mA

7.3.3 Typical Crystal Application Circuits

Crystal Oscillator	Capacitance Values	Resistance Values
12 MHz	20pF	1 MΩ
32.768 kHz	33pF	10 MΩ

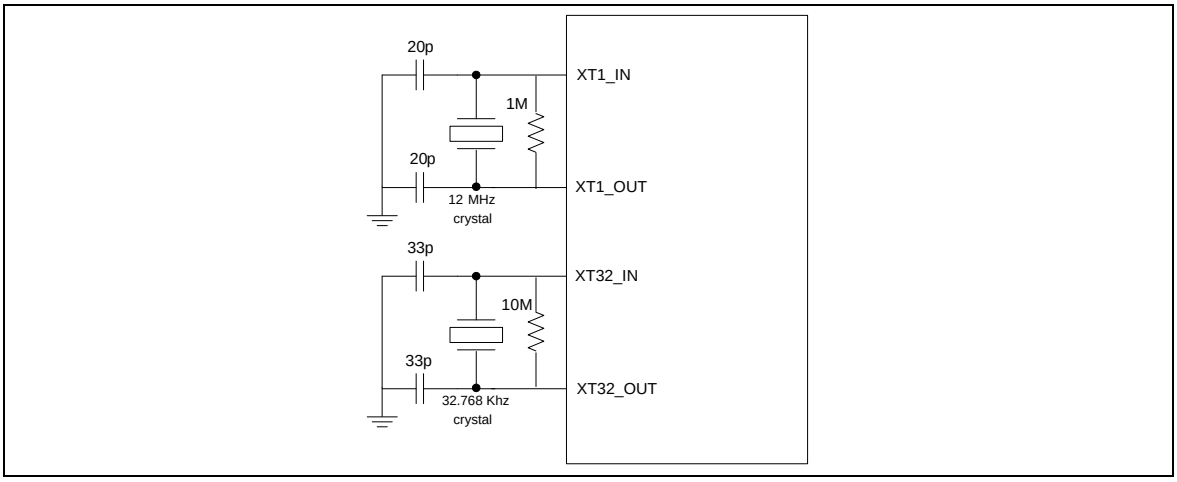


Figure 7.3-1 Typical Crystal Application Circuit

7.3.4 Internal 32 kHz Low Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage	-	3	-	3.6	V
Center Frequency	-	-	32	-	kHz
Operating current	V_{DD} =3.3V	-	0.5	-	uA

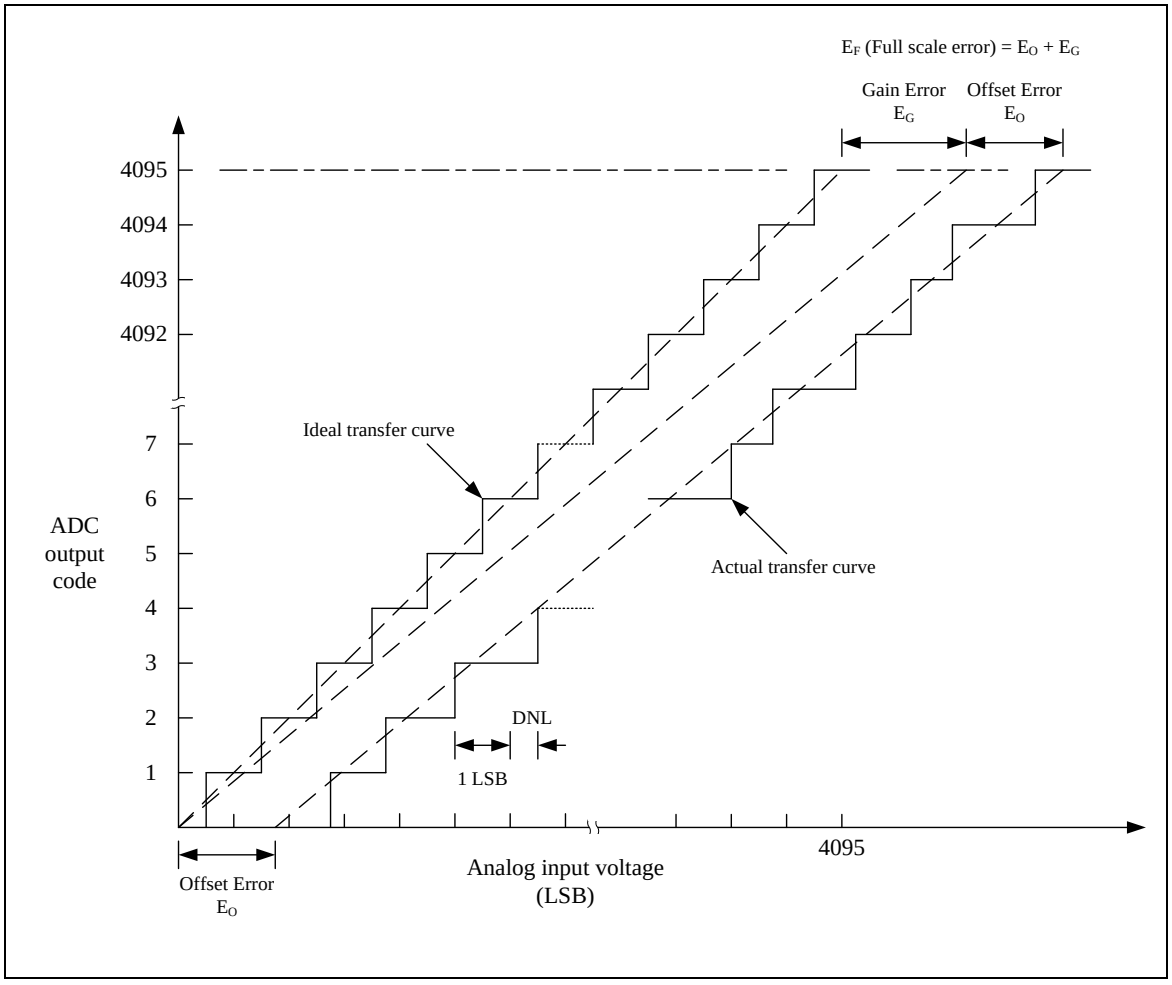
7.4 Analog Characteristics

7.4.1 Specifications of 12-bit SARADC

Symbol	PARAMETER	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
A_{VDD_ADC}	Operating Voltage	2.7	3.3	3.6	V	
R_{ADC}	Resolution	-	-	12	bit	
V_{REF}	Reference Voltage	2	-	A_{VDD_ADC}	V	
V_{IN}	ADC input Voltage	0	-	V_{REF}	V	
R_{IN}	Analog input impedance	2			MΩ	
F_{SPS}	Sampling Rate	-	-	1M	Hz	ADC Clock = 16MHz Free Running Conversion(ADC_CH1)
		-	-	200k	Hz	ADC Clock = 3.2MHz Free Running Conversion(ADC_CH2, ADC_CH3, ADC_CH4, ADC_CH5, ADC_CH6, ADC_CH7)
E_Q	Gain Error (Transfer Gain)	-	-2	-4	LSB	
E_A	Absolute Error	-	3	-	LSB	
INL	Integral Non-linearity Error	-	±3	-	LSB	
DNL	Differential Non-linearity Error	-1	-	+1.5	LSB	
E_O	Offset Error		±1	±3	LSB	
SNR	S/N	-	62	-	dB	
-	Total Harmonic Distortion	-	62	-	dB	

Note:

1. The performance measurement is in ADC only condition (all other module are in reset statue).
2. Design by guarantee, no test in production.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

7.4.2 Specifications of 24-bit Delta-Sigma CODEC

Symbol	Parameter	Specifications				Test Conditions
		Min.	Typ	Max.	Unit	
Reference						
	VMID	-	0.5*A_{VDD_CODEC}	-	V	
Microphone Bias						
	Bias Voltage	-	0.75*A_{VDD_CODEC}	-	V	
	Maximum Output Current	-	-	3	mA	
	Capacitive Load	-	-	50	pF	
Line Input						
	Resolution	-	24	-	Bit	
THD	Total Harmonic Distortion	-	-80	-70	dB	
DR	Dynamic Range	80	90	-	dB	-60dB input, A-Weighted
SNR	S/N	80	90	-	dB	
	Channel Separation	-	100	-	dB	
	Channel Matching	-	0.2	-	dB	
VFS	Full Scale Output Voltage	-	0.93* A_{VDD_CODEC}/ 3.3	-	dB	
	Input Impedance	10	-	-	kΩ	
	Input Capacitor	-	10	-	pF	
Headphone Output						
THD	Total Harmonic Distortion	-	-80	-	dB	RL = 0 Ω, Po = 10mW
THD	Total Harmonic Distortion	-	-60	-	dB	RL = 32 Ω, Po = 10mW
SNR	S/N	90	93	-	dB	A-Weighted
Power Supply Current (No PLL, No Loading)						
	A_{VDD_CODEC}	-	8	-	mA	

Symbol	Parameter	Specifications				Test Conditions
		Min.	Typ	Max.	Unit	
	A_{VDD_HP}	-	4	-	mA	

Note: The performance measurement is in CODEC only condition (All other module are in reset statue).

7.4.3 Specification of LDO

Symbol	Parameter	Min.	Typ	Max.	Unit	Note
V_{DD}	Input Voltage	1.62	3.3	3.6	V	A_{VDD_LDO} input voltage
V_{LDO}	Output Voltage	-10%	1.2	+10%	V	
T_A	Temperature	-40	25	85	℃	
E_{CAP}	External Capacitor	-	4.7	-	μF	

Notes:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 4.7μF or higher capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

7.4.4 Specification of Low Voltage Reset

Symbol	Parameter	Min.	Typ	Max.	Unit	Test Condition
V_{DD}	Supply Voltage	0	-	3.6	V	
T_A	Temperature	-40	25	85	℃	
I_{LVR}	Quiescent Current	-	25	40	uA	V_{DD}=3.3V
V_{LVR}	Threshold Voltage	2.16	2.4	2.64	V	T_A=-45 ~ 85℃

7.4.5 Specifications of Power-on Reset

Symbol	Parameter	Min.	Typ	Max.	Unit	Test Condition
T_A	Temperature	-40	25	85	℃	
I_{POR}	Quiescent Current	-	33	50	uA	V_{DD}>Reset voltage
V_{POR}	Reset Voltage	1.6	2	2.4	V	T_A=-40 ~ 85℃
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	-	-	100	mV	
RPV_{DD}	V_{DD} Raising Rate to Ensure Power-on Reset	0.025	-	-	V/ms	
t_{POR}	Minimum Time for VDD Stays at VPOR to Ensure Power-on Reset	0.5	-	-	ms	

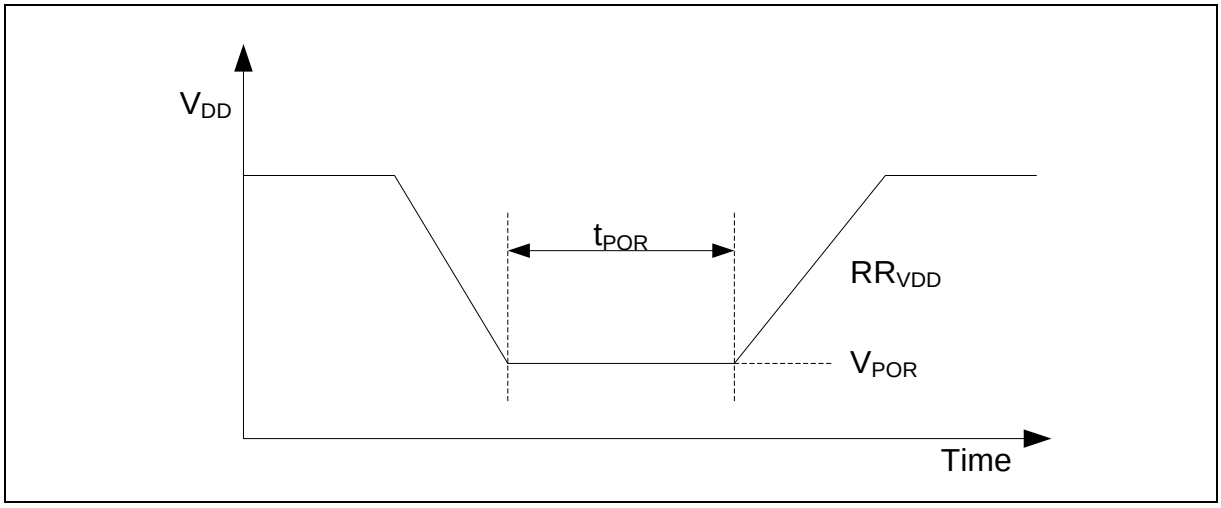


Figure 7.4-1 Power-up Ramp Condition

7.4.6 USB PHY Specifications

7.4.6.1 USB DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
V_{IH}	Input high (driven)		2.0	-	-	V
V_{IL}	Input low		-	-	0.8	V
V_{DI}	Differential input sensitivity	USB_DP-USB_DM	0.2	-	-	V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8	-	2.5	V
V_{SE}	Single-ended receiver threshold		0.8	-	2.0	V
	Receiver hysteresis		-	400	-	mV
V_{OL}	Output low (driven)		0	-	0.3	V
V_{OH}	Output high (driven)		2.8	-	3.6	V
V_{CRS}	Output signal cross voltage		1.3	-	2.0	V
R_{PU}	Pull-up resistor		1.425	-	1.575	kΩ
V_{TRM}	Pull-down resistor		14.25	-	15.75	kΩ
Z_{DRV}	Termination Voltage for upstream port pull up (RPU)		3.0	-	3.6	V
C_{IN}	Driver output resistance	Steady state drive*	28	-	49.5	Ω
V_{IH}	Transceiver capacitance	Pin to V_{SS}	-	-	20	pF

Note: Driver output resistance does not include series resistor resistance.

7.4.6.2 USB Full-Speed Driver Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
T_{FR}	Rising time	CL = 50p	4	-	20	ns
T_{FF}	Falling time	CL = 50p	4	-	20	ns
T_{FRFF}	Rising and falling time matching	$T_{FRFF} = T_{FR} / T_{FF}$	90	-	111.11	%

7.4.6.3 USB High-Speed Driver Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
T_{FR}	Rising time	CL = 5p	500			ns
T_{FF}	Falling time	CL = 5p	500			ns
T_{FRFF}	Rising and falling time matching	$T_{FRFF} = T_{FR} / T_{FF}$	90		111	%

7.4.7 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min.	Max.	Min.	Max.	
t_{LOW}	SCL low period	4.7	-	1.2	-	uS
t_{HIGH}	SCL high period	4	-	0.6	-	uS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	20+0.1Cb	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by design, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

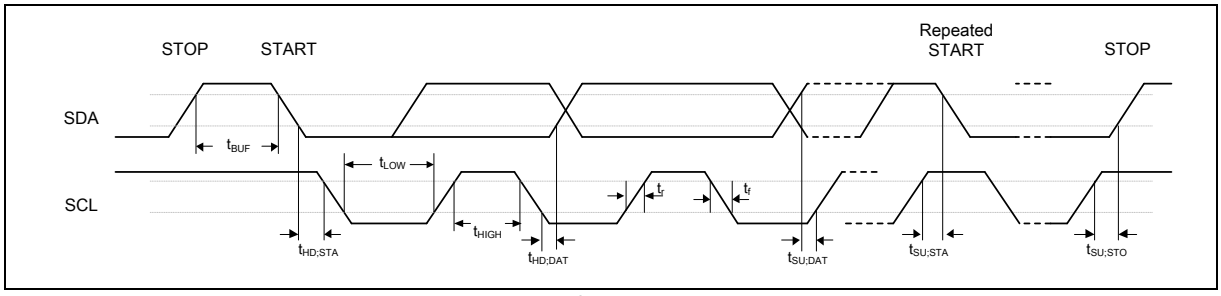


Figure 7.4-2 I²C Timing Diagram

7.4.8 SPI Dynamic Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
SPI Master Mode (V_{DD} = 3.0 V ~ 3.6 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4.5	-	-	ns
t_V	Data output valid time	-	2	4	ns
SPI Slave Mode (V_{DD} = 3.0 V ~ 3.6 V, 0 pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4.5	-	-	ns
t_V	Data output valid time	-	18	24	ns

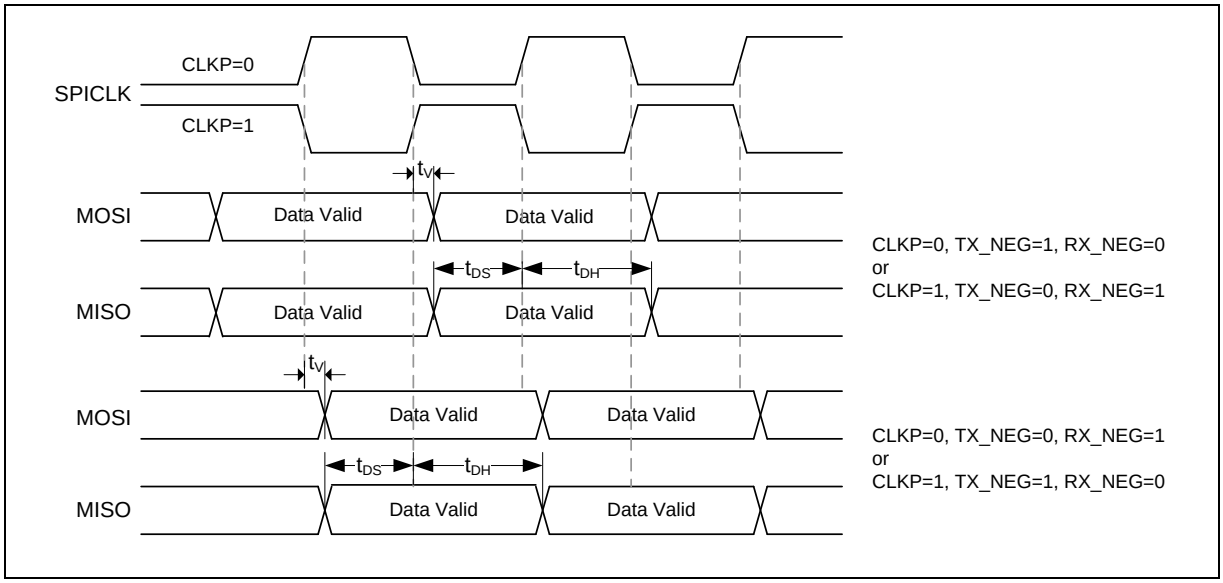


Figure 7.4-3 SPI Master Mode Timing Diagram

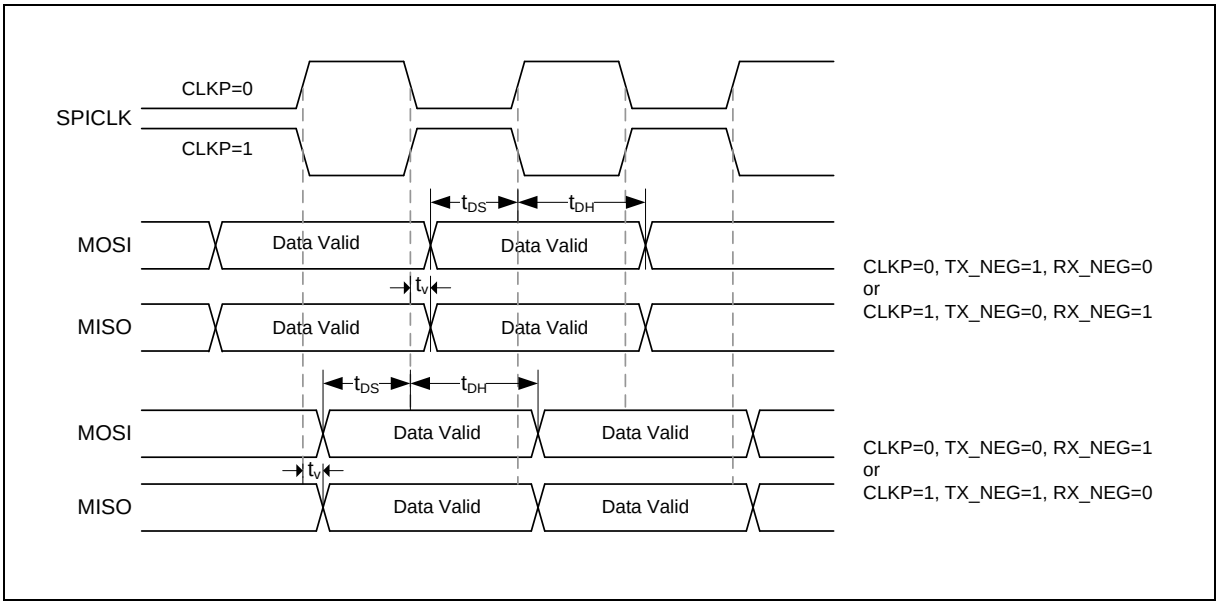


Figure 7.4-4 SPI Slave Mode Timing Diagram

7.4.9 I²S Dynamic Characteristics

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
$t_{h(WS)}$	I2S clock high time	42	-	ns	Master fPCLK = 12.288 MHz, data: 24 bits, audio frequency = 48 kHz
$t_{su(WS)}$	I2S clock low time	37	-		
$t_{h(WS)}$	LRCLK valid time	7	-		Master mode
$DuCy_{(SCK)}$	LRCLK hold time	1	-		Master mode
$t_{su(SD_MR)}$	LRCLK setup time	34	-		Slave mode
$t_{su(SD_SR)}$	LRCLK hold time	0	-		Slave mode
$t_{h(SD_MR)}$	I2S slave input clock duty cycle	25	75	%	Slave mode
$t_{h(SD_SR)}$	Data input setup time	0	-	ns	Master receiver
$t_{v(SD_ST)}$		0	-		Slave receiver
$t_{h(SD_ST)}$	Data input hold time	0	-		Master receiver
$t_{v(SD_MT)}$		0	-		Slave receiver
$t_{h(SD_MT)}$	Data output valid time	-	32		Slave transmitter (after enable edge)
$t_{h(WS)}$	Data output hold time	16	-		Slave transmitter (after enable edge)
$t_{su(WS)}$	Data output valid time	-	5		Master transmitter (after enable edge)
$t_{h(WS)}$	Data output hold time	0	-		Master transmitter (after enable edge)

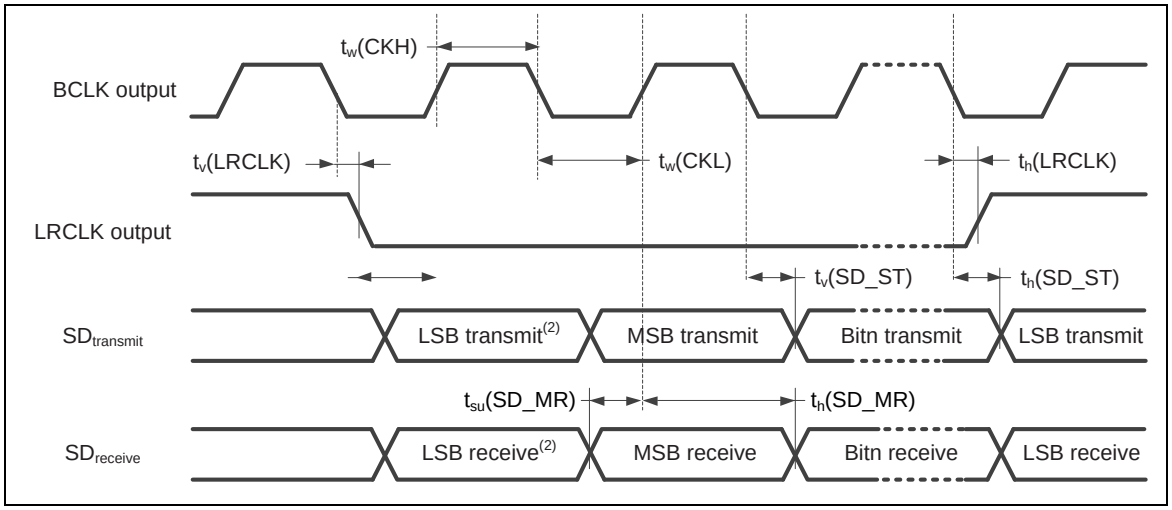


Figure 7.4-5 I2S Master Mode Timing Diagram

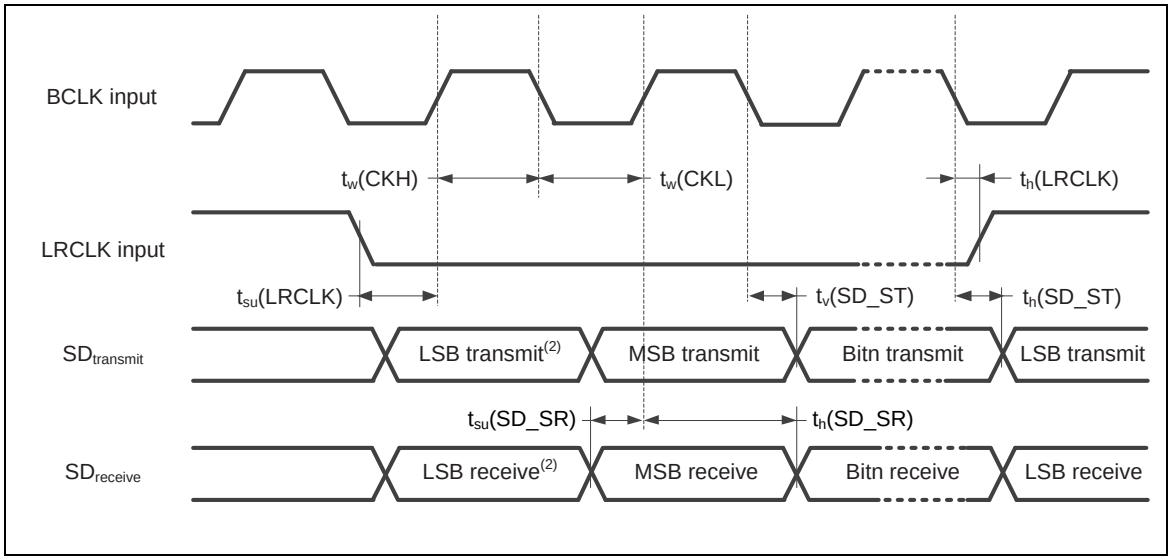
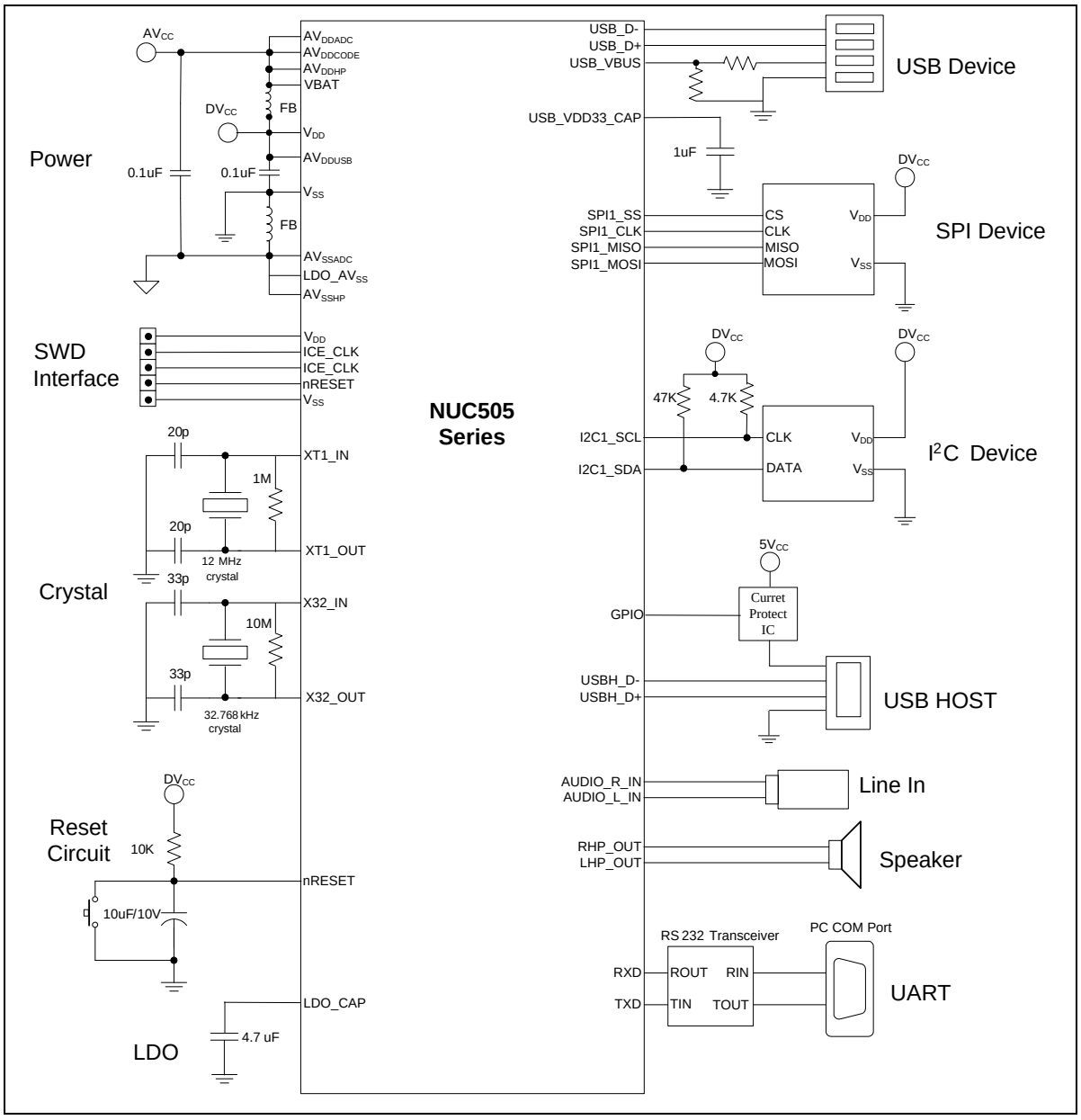


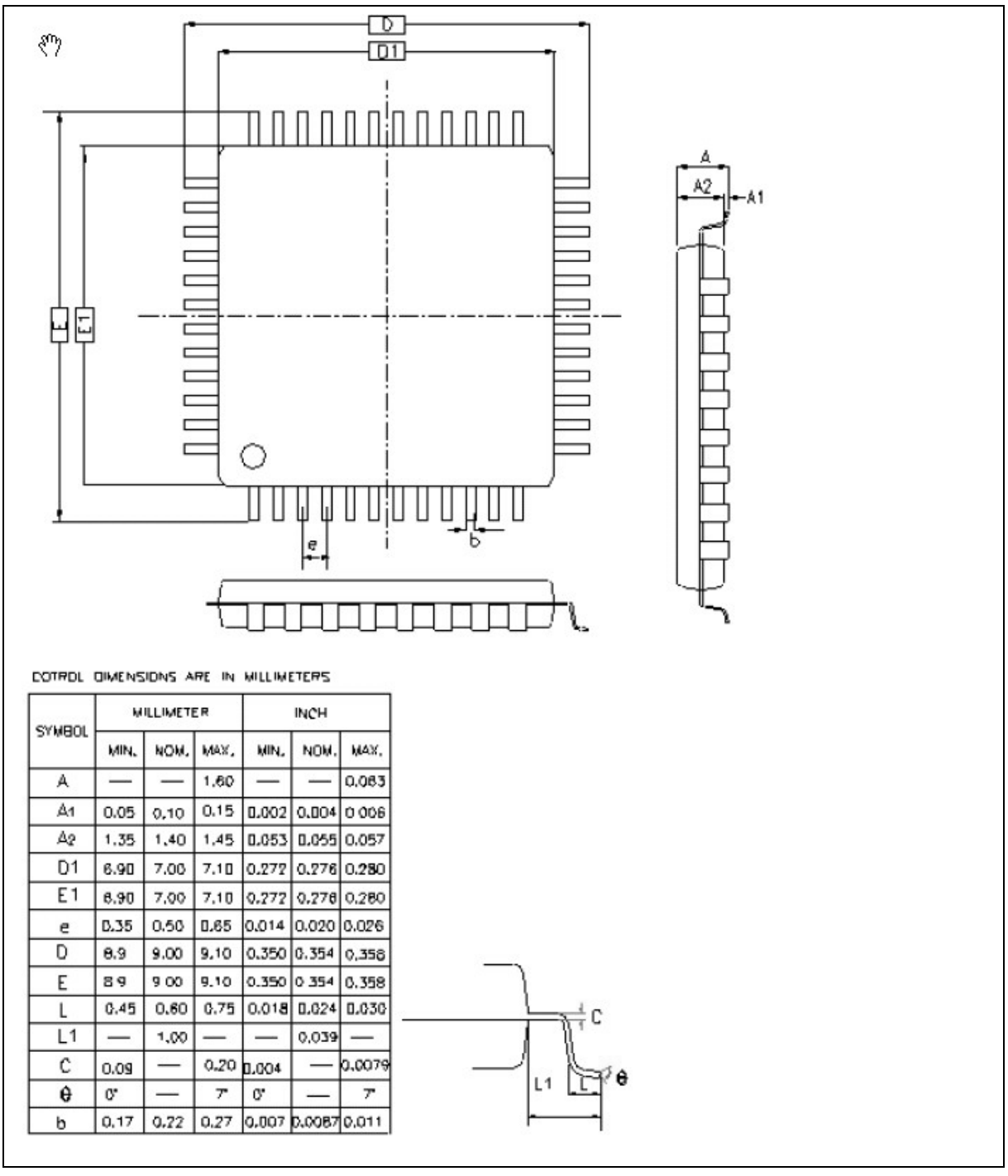
Figure 7.4-6 I^2S Slave Mode Timing Diagram

8 APPLICATION CIRCUIT



9 PACKAGE DIMENSIONS

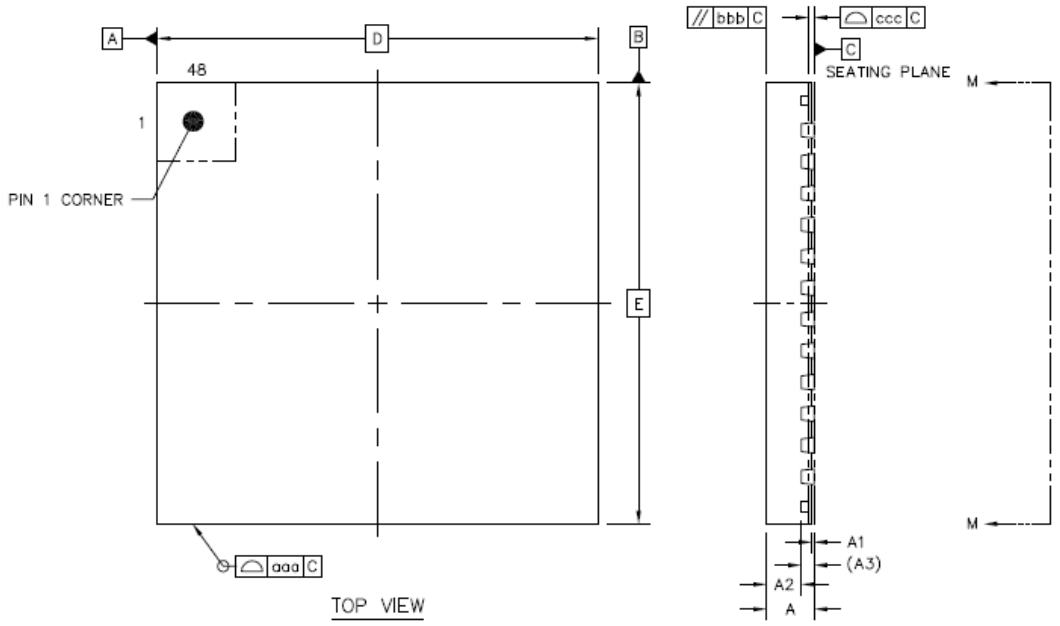
9.1 LQFP 48L (7x7x1.4mm footprint 2.0mm)

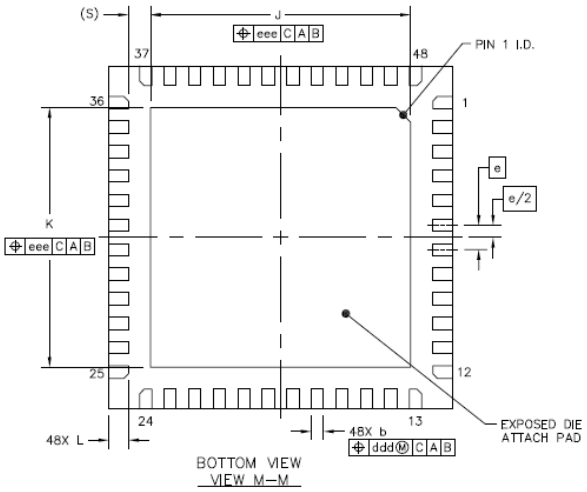


CONTROL DIMENSIONS ARE IN MILLIMETERS

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.026
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.004	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

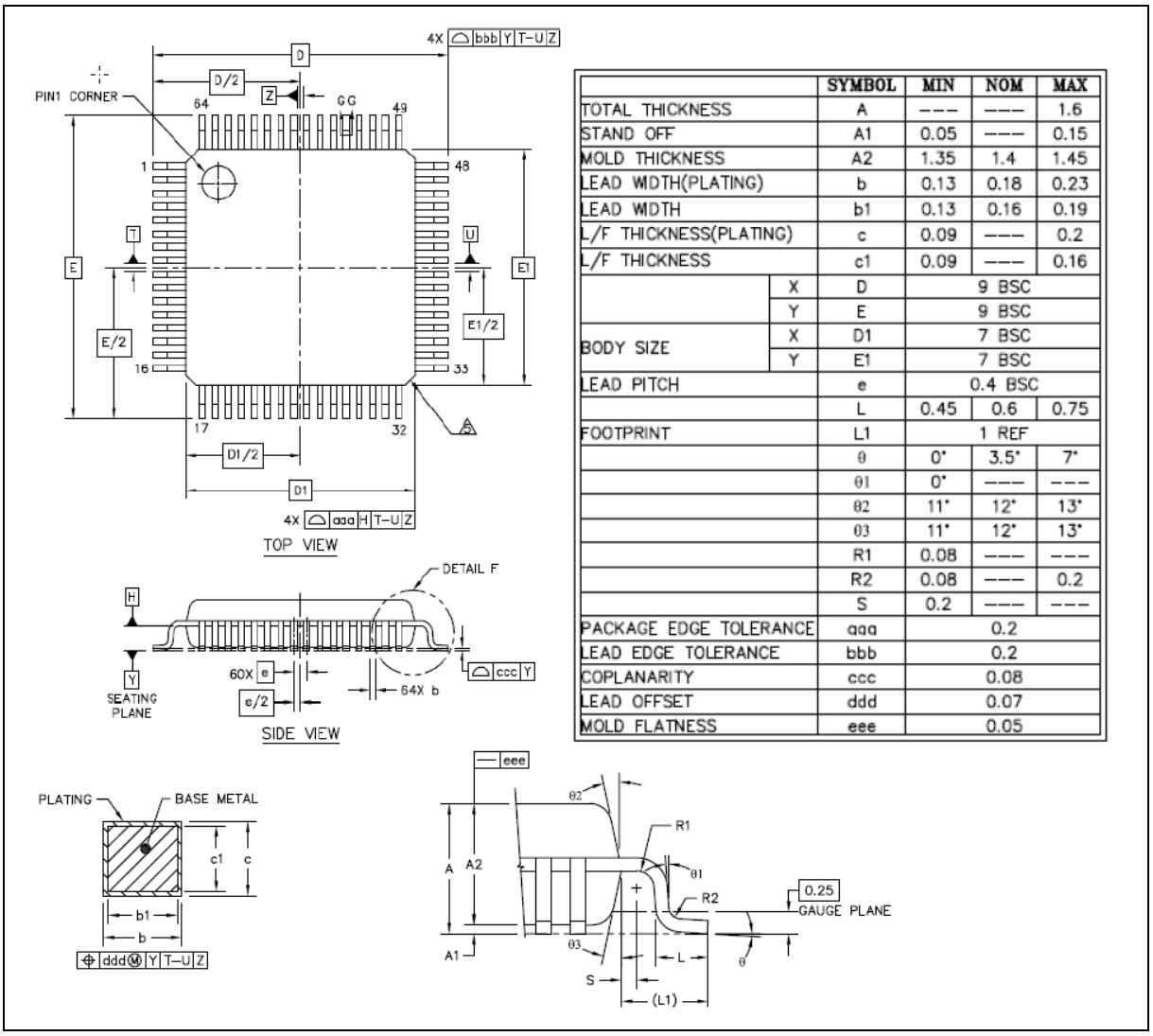
9.2 QFN 48 (7x7x0.8mm)





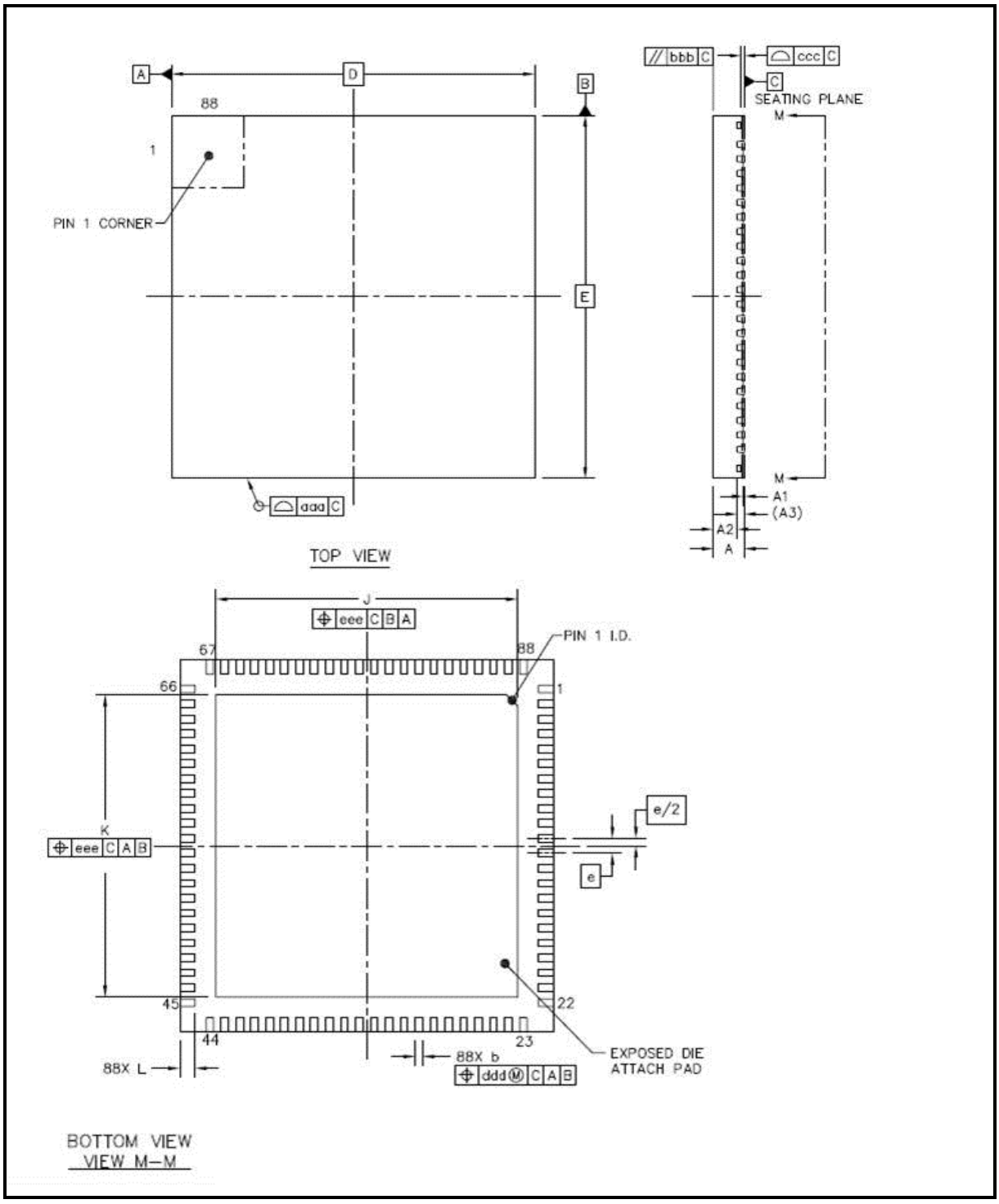
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	5.2	5.3	5.4
	Y	K	5.2	5.3	5.4
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	
		S		0.45 REF	

9.3 LQFP 64L (7x7x1.4mm footprint 2.0mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	9 BSC		
	Y	E	9 BSC		
BODY SIZE	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

9.4 QFN 88 (10x10x0.9mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		10 BSC	
	Y	E		10 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	8	8.1	8.2
	Y	K	8	8.1	8.2
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

10 REVISION HISTORY

Date	Revision	Description
2014.04.23	1.01	Preliminary version
2015.05.28	1.02	1. Added new part number: NUC505DLA, NUC505YLA, and NUC505DSA in Chapter 4. 2. Updated embedded SPI Flash memory size to 512 KB for new part number.
2015.11.04	1.04	1. Added a note to indicate that NUC505DS13Y only supports Headphone Out in section 4.1.1. 2. Added a note to indicate the packages are not pin-to-pin compatible in section 4.1.1. 3. Added section 9.2 QFN 48 (7x7x0.8mm) package specification. 4. Added part number NUC505YLA2Y in section 4.1.1, 4.2.4, and 4.3.4. 5. Replaced power mode name of Sleep mode and Deep-sleep mode with Idle mode and Power-down mode respectively.
2016.05.09	1.05	1. Added a note to Pin Diagram and Pin Description for QFN 48/88-pin packages.
2016.06.30	1.06	1. Corrected the typo in the Pin Configuration section 4.2.4/4.2.5/4.2.6 and Pin Description section 4.3.5.

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