

3.6W Constant Output Power Class-D Audio Amplifier with Class-G Boost Converter

Features

- **Operating Voltage: 3V-5.2V**
- **3.6W into 4W Load from 3.6V Supply at 1%THD+N (WLCSP1.5x2-12)**
- **3W into 4W Load from 3.6V Supply at 1%THD+N (TQFN4x4-16)**
- **Integrated Class-G Boost Converter-Increases Efficiency at Low Output Power**
- **Low Quiescent Current of 3.5 mA from 3.6 V**
- **Thermal and Short-Circuit Protection with Auto Recovery**
- **20dB Fixed Gain**
- **Lead Free and Green Device Available (RoHS Compliant)**
- **Power Enhanced Packages**
 - WLCSP 1.5x2-12
 - TQFN 4x4-16

General Description

The APA2018 is a mono, high efficiency, filter-free Class-D audio amplifier and is available in WLCSP1.5x2-12 and TQFN4x4-16 Package.

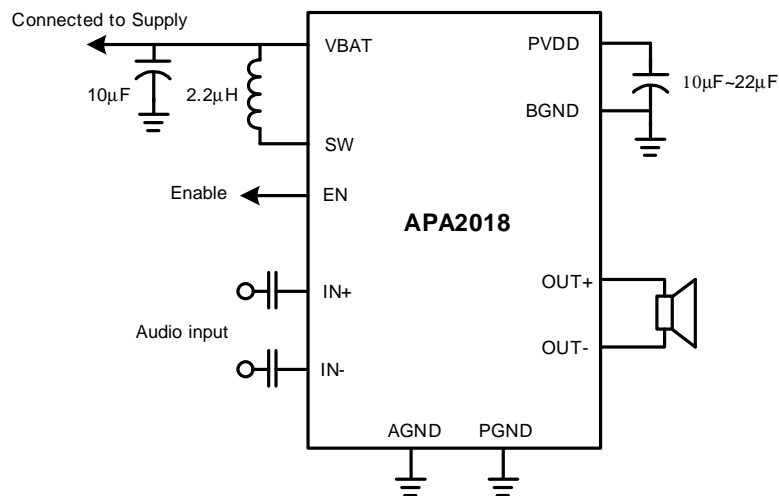
The APA2018 is a high efficiency Class-D audio power amplifier with an integrated Class-G boost converter that enhances efficiency at low output power. It drives up to 3.6W into an 4Ω speaker (1%THD+N). With 85% typical efficiency, the APA2018 helps extend battery life when playing audio.

The built-in boost converter generates a 5.75V supply voltage for the Class-D amplifier when high output power is required. This provides a louder audio output than a stand-alone amplifier directly connected to the battery. During low audio output power periods, the boost converter deactivates and connects VBAT directly to the Class-D amplifier supply, PVDD. This improves overall efficiency. The APA2018 has an integrated low-pass filter to improve the RF rejection and reduce DAC out-of-band noise, increasing the signal-to-noise ratio(SNR).

Applications

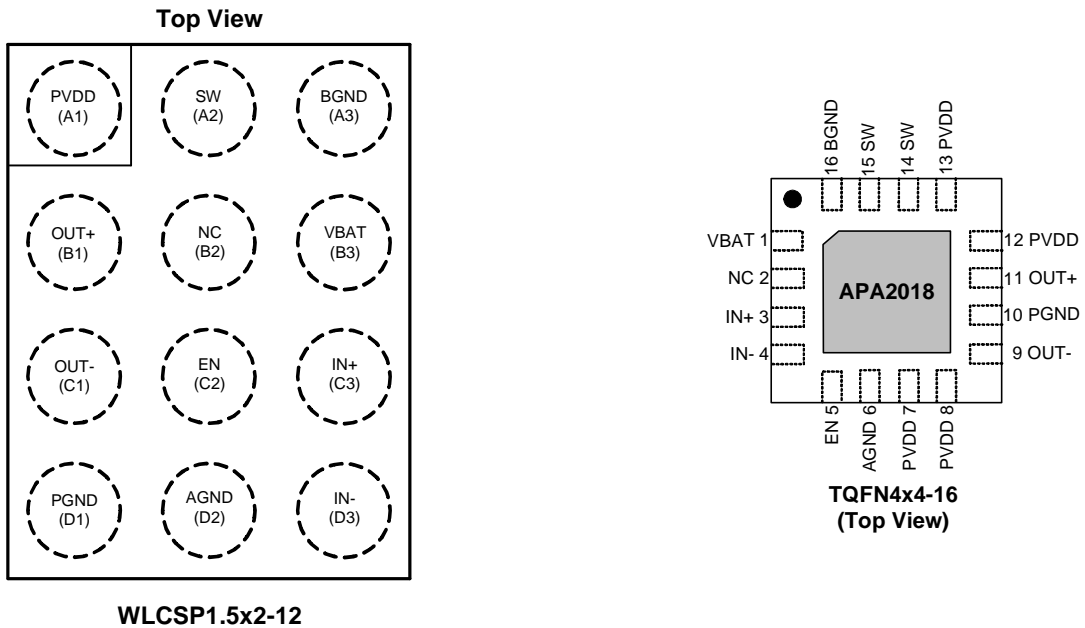
- **Cell Phones**
- **GPS**
- **Portable multimedia devices**

Simplified Application Circuit

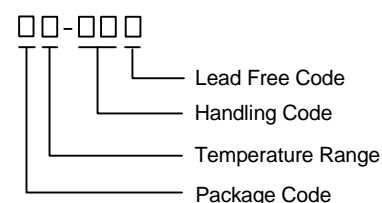




ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Pin Configuration



Ordering and Marking Information

<p>APA2018</p>  <p>Lead Free Code Handling Code Temperature Range Package Code</p>	<p>Package Code HA : WLCSP1.5x2-12 QB : TQFN4x4-16 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Lead Free Code G : Halogen and Lead Free Device</p>
<p>APA2018 HA :</p> 	<p>X - Date Code</p>
<p>APA2018 QB :</p> 	<p>XXXXX - Date Code</p>

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V _{BAT}	Supply Voltage (VBAT to GND)	-0.3 to 6	V
	Input Voltage (IN+, IN- to GND)	-0.3 to V _{BAT} +0.3	
	Input Voltage (EN to GND)	-0.3 to V _{BAT} +0.3	
T _J	Maximum Junction Temperature	150	°C
T _{STG}	Storage Temperature Range	-65 to +150	
T _{SDR}	Maximum Soldering Temperature Range, 10 Seconds	260	
P _D	Power Dissipation	Internally Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics (Note 2,3)

Symbol	Parameter	Value	Unit
θ _{JA}	Thermal Resistance -Junction to Ambient ^(Note2)	WLCSP1.5x2-12	97
		TQFN4x4-16	60
θ _{JC}	Thermal Resistance -Junction to Case ^(Note3)	WLCSP1.5x2-12	36
		TQFN4x4-16	12

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Note 3: The case temperature is measured at the center of the PGND PIN on the underside of the WLCSP1.53x1.98-12 and TQFN4x4-16 package.

Recommended Operating Conditions

Symbol	Parameter		Range		Unit
			Min.	Max.	
V _{BAT}	Supply Voltage		3	5.2	V
V _{IH}	High Level Threshold Voltage	EN	1.3	-	
V _{IL}	Low Level Threshold Voltage	EN	-	0.6	
V _{ICM}	Common Mode Input Voltage		1	V _{DD} -1	°C
T _A	Ambient Temperature Range		-40	85	
T _J	Junction Temperature Range		-40	150	
R _L	Speaker Resistance,		4	-	Ω

Electrical Characteristics

$V_{BAT}=3.6V$, $V_{GND}=0V$, $R_L=8\Omega+33\mu H$, $T_A=25^\circ C$ (unless otherwise noted)

Symbol	Parameter	Test Condition	APA2018			Unit
			Min.	Typ.	Max.	
V_{BAT}	Supply voltage range		3		5.2	V
	Class-D supply voltage range	EN=VBAT.boost converter active		5.75		V
		Boost converter disabled(in bypass mode)	3	-	5.2	
	Supply under voltage shutdown		-	2.8	-	
$V_{ThresholdV}$	Control pin threshold	EN	1.3	-	-	
	Control pin threshold Hysteresis		-	0.2	-	
I_{DD}	Operating quiescent current	EN = VBAT = 3.6 V	-	3.5	6	mA
I_{SD}	Shutdown quiescent current	VBAT = 2.5 V to 5.2 V, EN = GND	-	0.2	1	μA
	Input common-mode voltage range	IN+,IN-	0.6	-	1.3	V
$T_{START-UP}$	Start-up time		-	6	10	ms
BOOST CONVERTER						
PVDD	Boost converter output voltage range	$I_{BOOST}=0mA$	5.4	5.8	6.4	V
		$I_{BOOST}=700mA$	-	5.6	-	
I_L	Boost converter input current limit	Power supply current	-	2700	-	mA
	Boost converter start-up current limit	Boost converter starts up from IL full shutdown	-	600	-	
		Boost converter wakes up from auto-pass through mode	-	1000	-	
f_{BOOST}	Boost converter frequency		-	1.2	-	MHz
CLASS-D AMPLIFIER						
P_O	Output power	THD=1%, VBAT=3.0V, f=1kHz (WLCSP1.5x2-12)	-	2	-	W
		THD=1%, VBAT=3.6V, f=1kHz (WLCSP1.5x2-12)	-	2	-	
		THD=1%, VBAT=3.0V, f=1kHz, RL=4 Ω +33 μ H (WLCSP1.5x2-12)	-	3.6	-	
		THD=1%, VBAT=3.6V, f=1kHz, RL=4 Ω +33 μ H (WLCSP1.5x2-12)	-	3.7	-	
		THD=1%, VBAT=3.6V, f=1kHz, RL=4 Ω +33 μ H (TQFN4x4-16)	-	3	-	
A_V	Voltage gain		19.5	20	20.5	dB
V_{OS}	Output offset voltage		-	2	10	mV

Electrical Characteristics

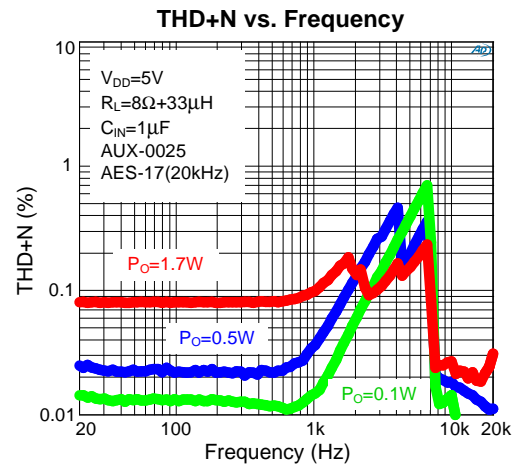
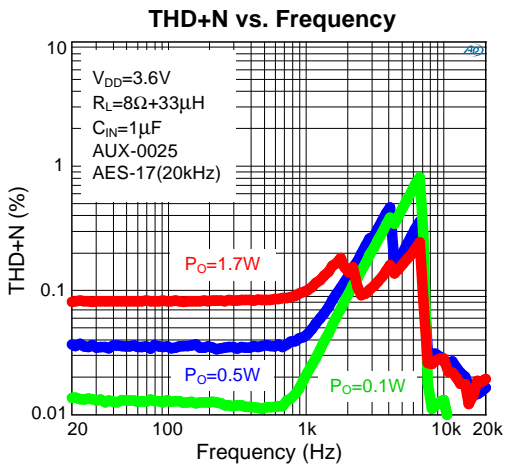
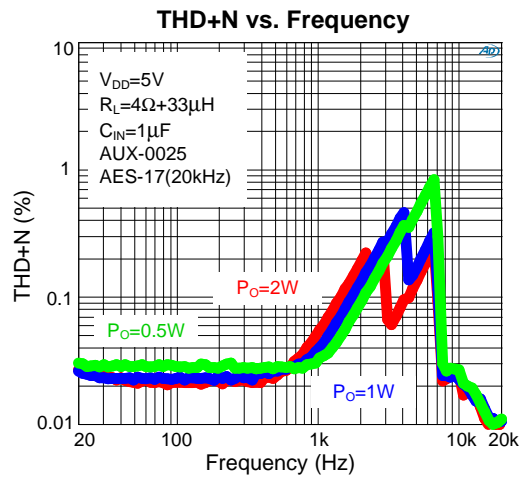
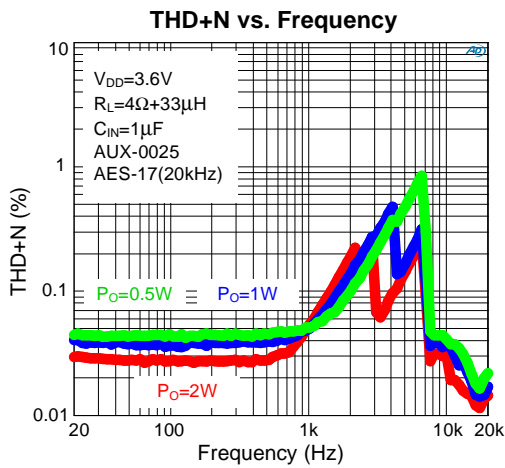
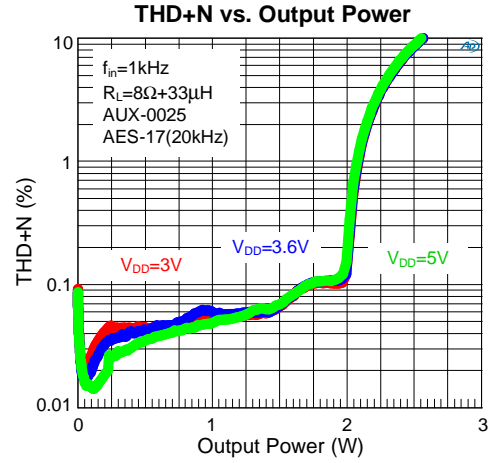
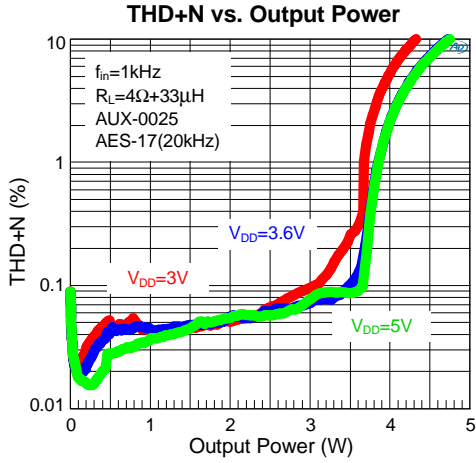
$V_{BAT}=3.6V$, $V_{GND}=0V$, $R_L=8\Omega+33\mu H$, $T_A=25^\circ C$ (unless otherwise noted)

Symbol	Parameter	Test Condition	APA2018			Unit
			Min.	Typ.	Max.	
CLASS-D AMPLIFIER						
OCP	Short-circuit protection threshold current		-	2	-	A
R_{IN}	Input impedance (per input pin)		-	24	-	k Ω
	Input impedance in shutdown(per input pin)	EN=0V	-	1300	-	
Z_O	Output impedance in shutdown		-	2	-	k Ω
	Maximum input voltage swing	EN=0V	-	2	-	V_{RMS}
	Boost converter auto-pass through threshold	Class-D output voltage threshold when boost converter automatically turns on	-	2	-	V_{PK}
$f_{CLASS-D}$	Class-D switching frequency		275	300	325	kHz
η	Class-D and boost combined efficiency	$P_O=500mW$, $V_{BAT}=3.6V$	-	90	-	%
V_N	Noise output voltage	A-weighted	-	49	-	μV_{RMS}
		Unweighted	-	65	-	
SNR	Signal-to-noise ratio	1.7W, $R_L=8\Omega+33\mu H$. A-weighted	-	97.5	-	dB
		1.7W, $R_L=8\Omega+33\mu H$. Unweighted	-	95	-	
		2W, $R_L=4\Omega+33\mu H$. A-weighted	-	95	-	
		2W, $R_L=4\Omega+33\mu H$. Unweighted	-	93	-	
THD+N	Total harmonic distortion plus noise	$P_O=100mW$, $f=1kHz$	-	0.06	-	%
		$P_O=500mW$, $f=1kHz$	-	0.07	-	
		$P_O=1.7W$, $f=1kHz$, $R_L=8\Omega+33\mu H$	-	0.07	-	
		$P_O=2W$, $f=1kHz$, $R_L=4\Omega+33\mu H$	-	0.15	-	
PSRR	AC-Power supply ripple rejection(output referred)	200mV _{PP} square ripple, $V_{BAT}=3.8V$, $f=217Hz$	-	70	-	dB
		200mV _{PP} square ripple, $V_{BAT}=3.8V$, $f=1kHz$	-	70	-	
CMRR	AC-Common mode rejection ratio (output referred)	200mV _{PP} square ripple, $V_{BAT}=3.8V$, $f=217Hz$	-	71	-	
		200mV _{PP} square ripple, $V_{BAT}=3.8V$, $f=1kHz$	-	71	-	

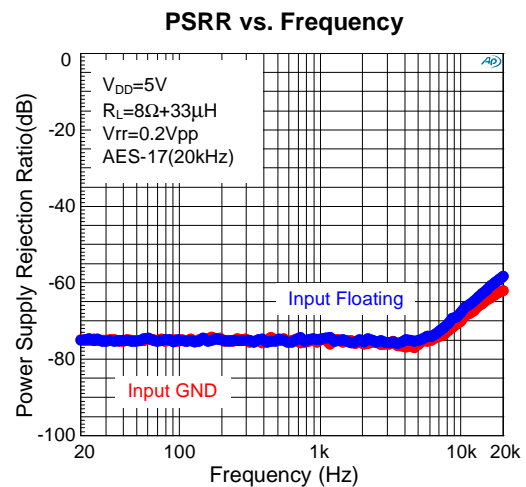
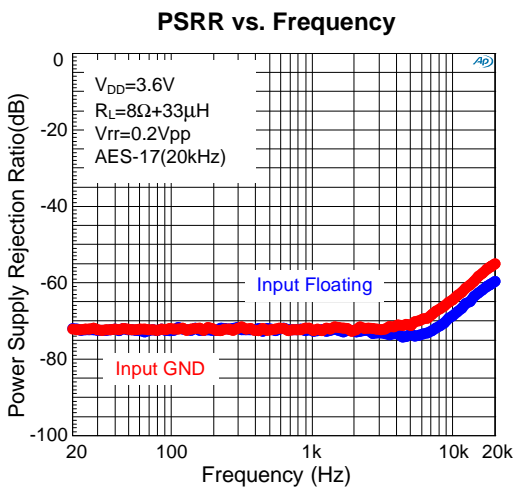
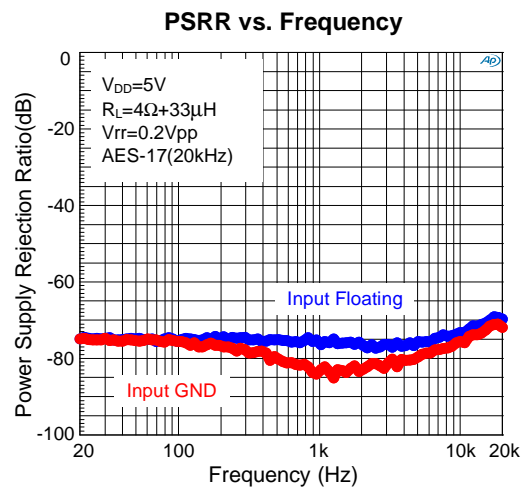
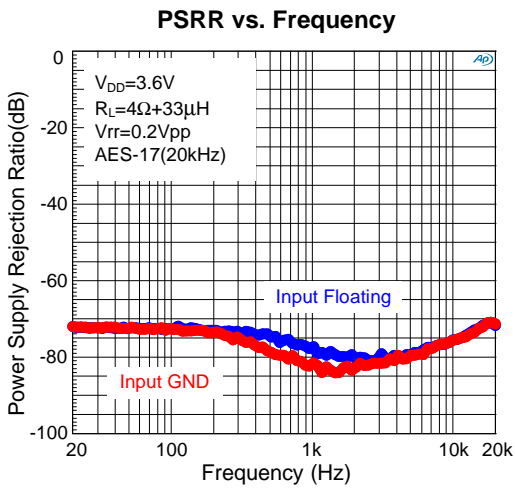
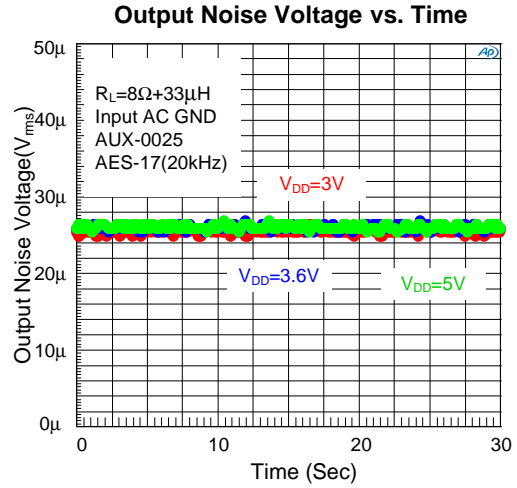
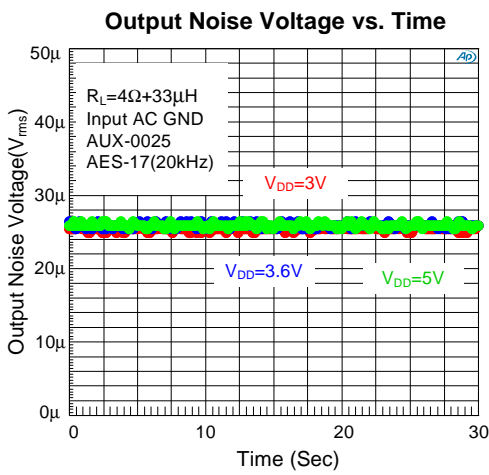
Pin Description

Pin		Name	I/O/P	Function Description
NO.				
WLCSP	TQFN			
A1	7,8,12,13	PVDD	O	Boost converter output and Class-D power stage supply voltage.
A2	14,15	SW	I	Boost converter switch input; connect boost inductor between VBAT and SW.
A3	16	BGND	P	Boost converter power ground.
B1	11	OUT+	O	Positive audio output.
B2	2	NC	I	NC
B3	1	VBAT	P	Supply voltage.
C1	9	OUT-	O	Negative audio output.
C2	5	EN	I	Device enable; set to logic high to enable.
C3	3	IN+	I	Positive audio input.
D1	10	PGND	P	Class-D power ground.
D2	6	AGND	P	Analog ground.
D3	4	IN-	I	Negative audio input.

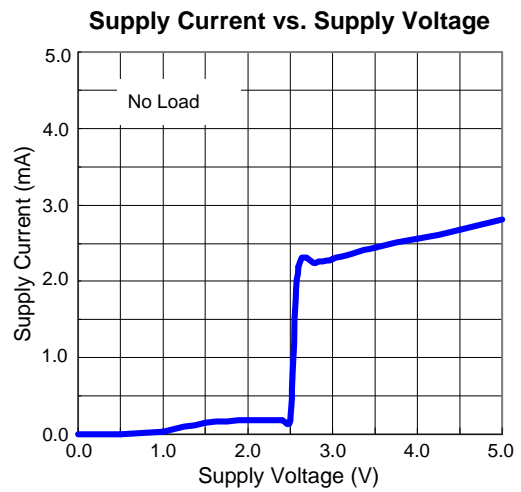
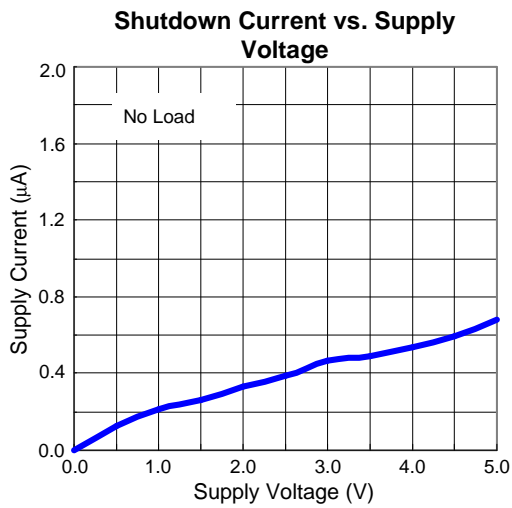
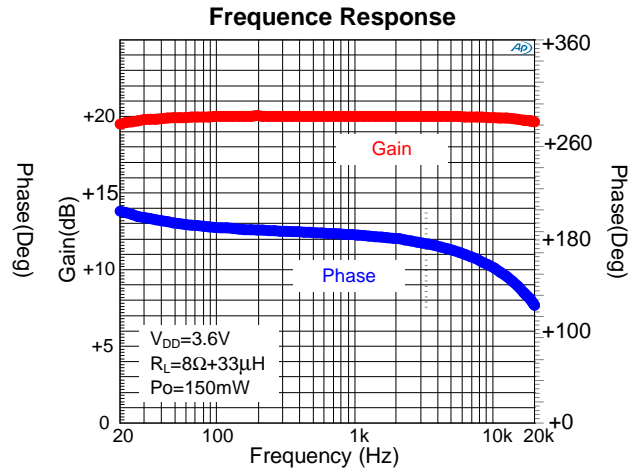
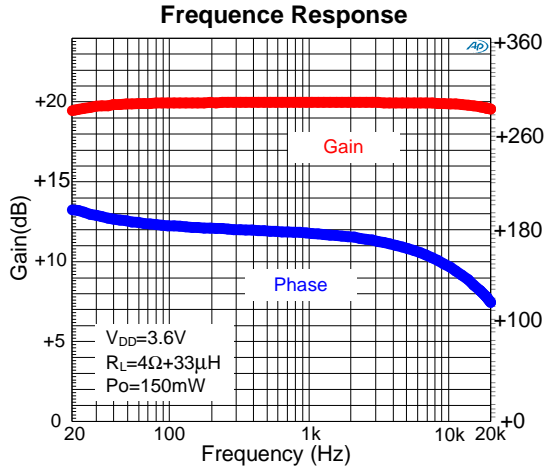
Typical Operating Characteristics



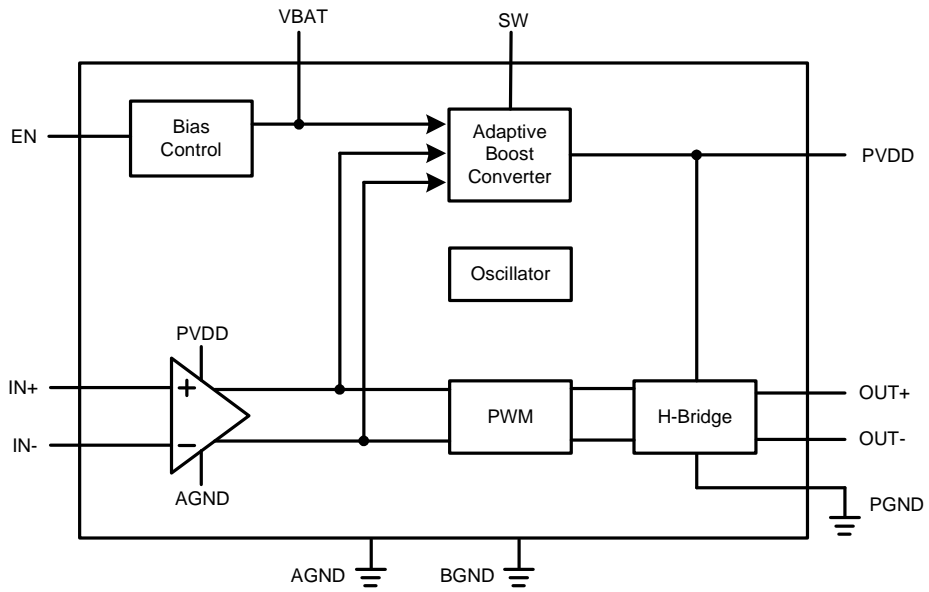
Typical Operating Characteristics



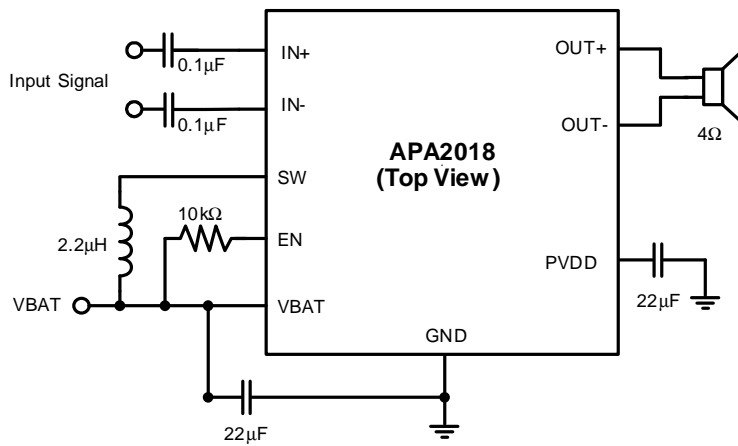
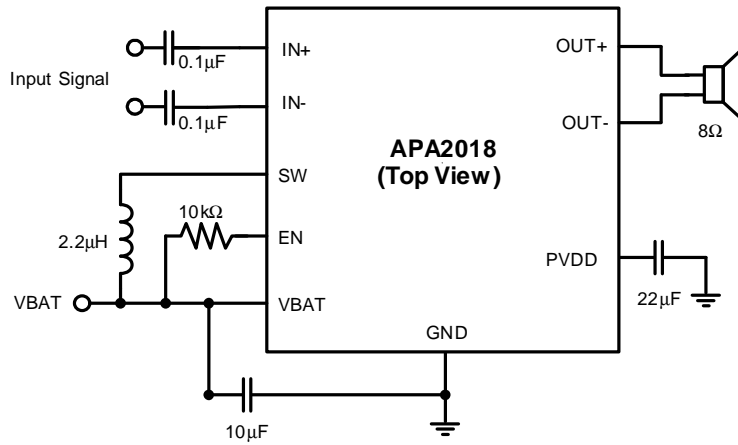
Typical Operating Characteristics



Block Diagram



Typical Application Circuit



Function Descriptions

Boost Converter Auto Pass Through (APT)

The APA2018 consists of a Class-G boost converter and a Class-D amplifier. The boost converter operates from the supply voltage, VBAT, and generates a higher output voltage PVDD at 5.75 V. PVDD drives the supply voltage of the Class-D amplifier. This improves loudness over non-boosted solutions. The boost converter has a “Pass Through” mode in which it turns off automatically and PVDD is directly connected to VBAT through an internal bypass switch.

The boost converter is adaptive and operates between pass through mode and boost mode depending on the output audio signal amplitude. When the audio output amplitude exceeds the “auto pass through” (APT) threshold, the boost converter is activated automatically and goes to boost mode. The transition time from normal mode to boost mode is fast enough to prevent clipping large transient audio signals. APA2018’s APT threshold is fixed at $2 V_{PEAK}$. When the audio output signal is below APT threshold, the boost converter is deactivated and goes to pass through mode. The adaptive boost converter maximizes system efficiency at lower audio output levels.

The Class-G boost converter is designed to drive the Class-D amplifier only. Do not use the boost converter to drive external devices.

Boost Converter Auto Pass Through (APT)

The critical external components are summarized in the following table:

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Boost converter inductor	At 30% rated DC bias current of the inductor	1.5	2.2	4.7	μH
Boost converter input capacitor		4.7		22	μF
Boost converter output capacitor	Working capacitance biased at boost output voltage, if 4.7μH inductor is chosen, then minimum capacitance is 10μF	10		22	μF

Boost Converter Component Section

The following is a list of terms and definitions used in the boost equations found later in this document.

C - Minimum boost capacitance required for a given ripple voltage on PVDD.

L - Boost inductor

f_{BOOST} - Switching frequency of the boost converter.

i_{PVDD} - Current pulled by the Class-D amplifier from the boost converter.

I_L - Average current through the boost inductor.

PVDD - Supply voltage for the Class-D amplifier. (Voltage generated by the boost converter output)

VBAT - Supply voltage to the IC.

ΔI_L - Ripple current through the inductor.

ΔV - Ripple voltage on PVDD.

Inductor Equations

Inductor current rating is determined by the requirements of the load. The inductance is determined by two factors: the minimum value required for stability and the maximum ripple current permitted in the application. Use Equation 1 to determine the required current rating. Equation 1 shows the approximate relationship between the average inductor current, I_L , to the load current, load voltage, and input voltage (IPVDD, PVDD, and VBAT, respectively). Insert IPVDD, PVDD, and VBAT into Equation 1 and solve for I_L . The inductor must maintain at least 90% of its initial inductance value at this current.

$$I_L = I_{PVDD} \times \left(\frac{PVDD}{VBAT \times 0.8} \right)$$

Ripple current, ΔI_L , is peak-to-peak variation in inductor current. Smaller ripple current reduces core losses in the inductor and reduces the potential for EMI. Use Equation 2 to determine the value of the inductor, L. Equation 2 shows the relationship between inductance L, VBAT, PVDD, the switching frequency, f_{BOOST} , and ΔI_L . Insert the maximum acceptable ripple current into Equation 2 and solve for L.

$$L = \left(\frac{VBAT \times (PVDD - VBAT)}{\Delta I_L \times f_{BOOST} \times PVDD} \right)$$

Function Descriptions

ΔIL is inversely proportional to L . Minimize ΔIL is as much as necessary for a specific application. Increase the inductance to reduce the ripple current. Do not use greater than $4.7\mu H$, as this prevents the boost converter from responding to fast output current changes properly. If using above $3.3\mu H$, and then use at least $10\mu F$ capacitance on PVDD to ensure boost converter stability.

The typical inductor value range for the APA2018 is $2.2\mu H$ to $3.3\mu H$. Select an inductor with less than 0.5Ω dc resistance, DCR. Higher DCR reduces total efficiency due to an increase in voltage drop across the inductor.

Boost Converter Capacitor Selection

The value of the boost capacitor is determined by the minimum value of working capacitance required for stability and the maximum voltage ripple allowed on PVDD in the application. Working capacitance refers to the available capacitance after derating the capacitor value for DC bias, temperature, and aging. Do not use any component with a working capacitance less than $6.8\mu F$. This corresponds to a $10\mu F/16V$ capacitor or a $10\mu F/10V$ capacitor.

Do not use above $22\mu F$ capacitance as it will reduce the boost converter response time to large output current transients.

Equation 3 shows the relationship between the boost capacitance, C , to load current, load voltage, ripple voltage, input voltage, and switching frequency (I_{PVDD} , $PVDD$, ΔV , V_{BAT} , and f_{BOOST} respectively).

Insert the maximum allowed ripple voltage into Equation 3 and solve for C . The 1.5 multiplier accounts for capacitance loss due to applied dc voltage and temperature for X5R and X7R ceramic capacitors.

$$C = 1.5 \times \frac{I_{PVDD} \times (PVDD - V_{BAT})}{\Delta V \times f_{BOOST} \times PVDD}$$

Short Circuit Auto-recovery

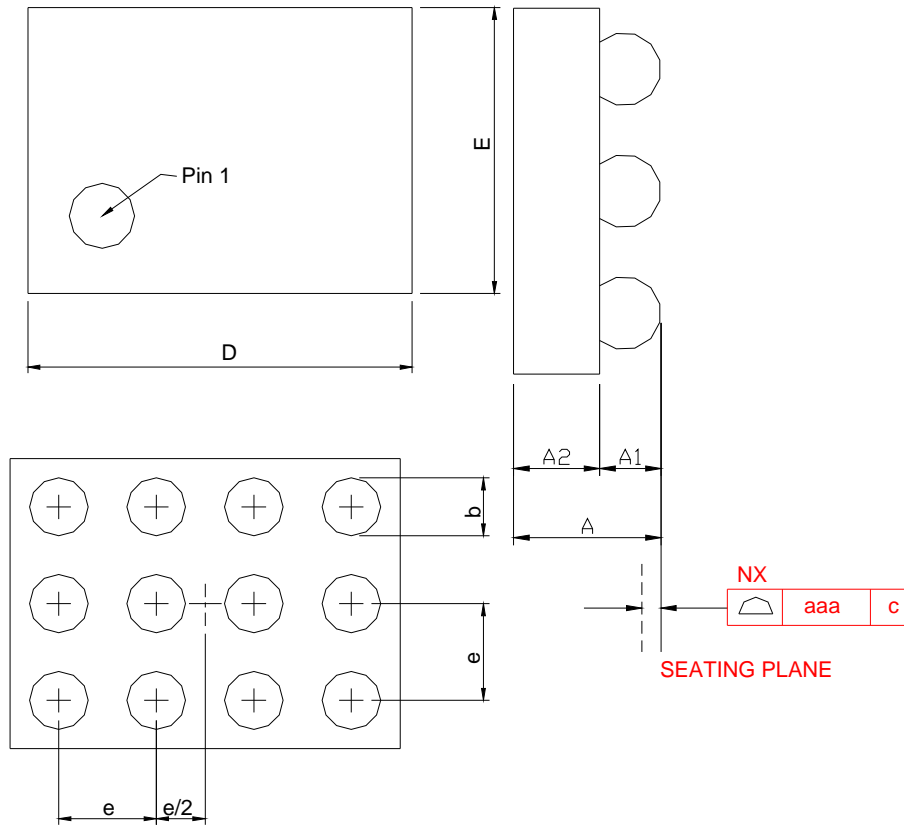
When a short circuit event happens, the APA2018 goes to low duty cycle mode and tries to reactivate itself every 1.8 seconds. The auto-recovery will continue until the short circuit event stops. This feature protects the device without affecting the device's long term reliability.

Thermal protection

The over-temperature circuit limits the junction temperature of the APA2018. When the junction temperature exceeds $T_J = +170^\circ C$, a thermal sensor turns off the output buffer, allowing the devices to cool. The thermal sensor allows the amplifier to start-up after the junction temperature down about $140^\circ C$. The thermal protection designed with a $30^\circ C$ hysteresis lowers the average T_J during continuous thermal overload conditions, increasing lifetime of the IC.

Package Information

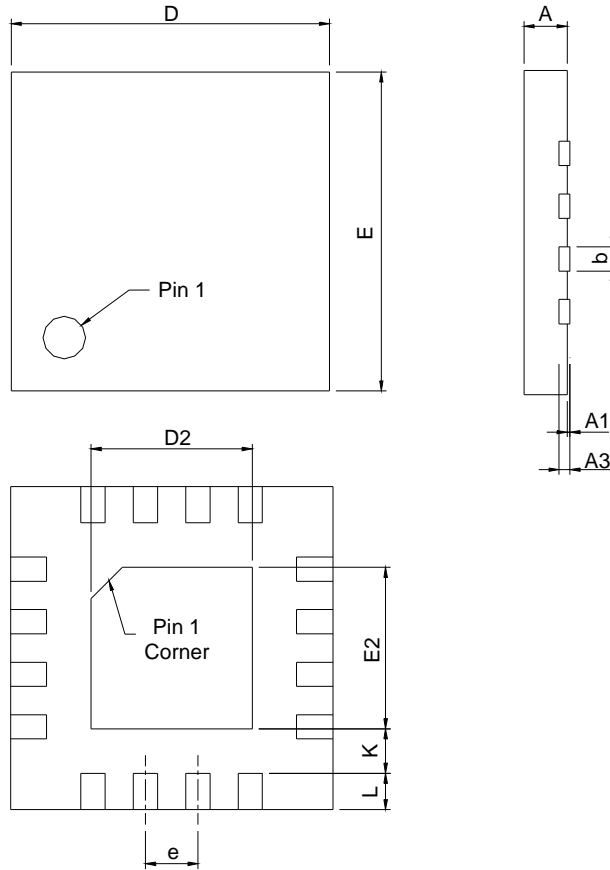
WLCSP1.50x2.0-12



SYMBOL	WLCSP1.50x2.0-12			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.49	0.62	0.019	0.024
A1	0.21	0.28	0.008	0.011
A2	0.28	0.34	0.011	0.013
b	0.28	0.34	0.011	0.013
D	1.95	2.01	0.077	0.080
E	1.50	1.56	0.059	0.061
e	0.50 BSC		0.020 BSC	
aaa	0.05		0.002	

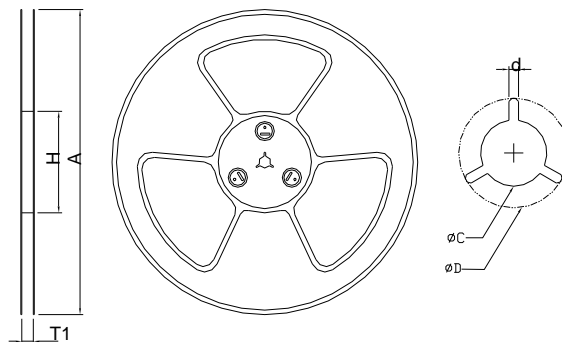
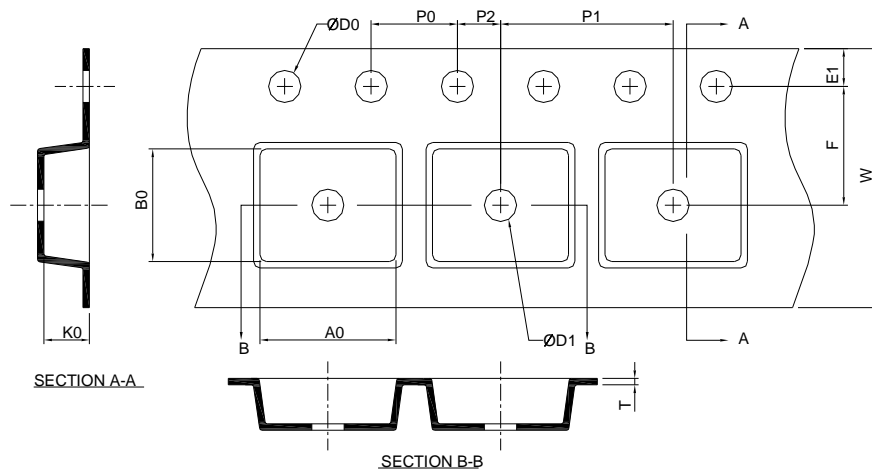
Package Information

TQFN4x4-16



SYMBOL	TQFN4x4-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.25	0.35	0.010	0.014
D	3.90	4.10	0.154	0.161
D2	1.90	2.10	0.075	0.083
E	3.90	4.10	0.154	0.161
E2	1.90	2.10	0.075	0.083
e	0.65 BSC		0.026 BSC	
L	0.40	0.50	0.016	0.020
K	0.20		0.008	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN4x4-16	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.00±0.20

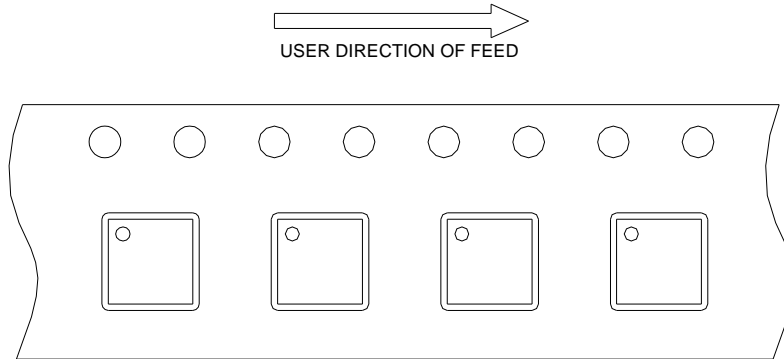
(mm)

Devices Per Unit

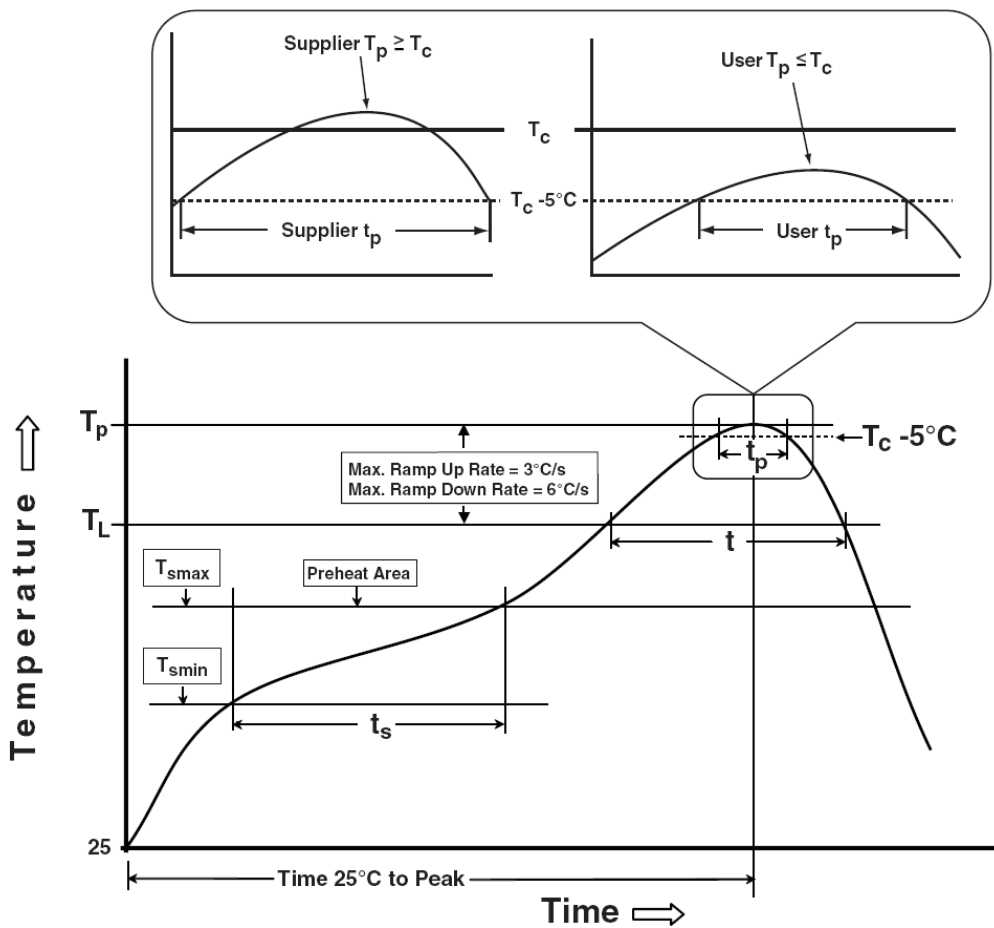
Package Type	Unit	Quantity
TQFN4x4-16	Tape & Reel	3000

Taping Direction Information

TQFN4x4-16



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^\circ\text{C}$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM ≥ 2KV
MM	JESD-22, A115	VMM ≥ 200V
Latch-Up	JESD 78	10ms, $1_{tr} \geq 100\text{mA}$

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