DS2.1, 2003-08-04

DELIC-LC/DELIC-PB

DSP Embedded Line and Port Interface Controller

PEB 20570/PEB 20571/PEF 20570/PEF 20571 Version 3.1

1 Addendum to “DELIC Clock System Synchronization”

The DELIC Clock System Synchronization is described in the DELIC-LC PEB 20570/ DELIC-PB PEB 20571 Data Sheet, independent of the version (2.1 .. 3.1).

As an addendum to chapter **“DELIC Clock System Synchronization”** of the DELIC-LC/DELIC-PB Data Sheet the following describes the system behaviour when using the VIP PEB 20590 or PEB 20591 in **LT-T mode**, for example when synchronizing to the Central Office.

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Revision History:	Previous Version:	Addendum	DS2, 2002-08-09

Major Changes:
- Chapter 3: New PEF version of DELIC-LC/DELIC-PB is available
- Chapter 4: DELIC Strap Option Configuration
- Trademarks changed

1.1 Clocking the VIP in LT-T Mode by DELIC Layer 1 Clock

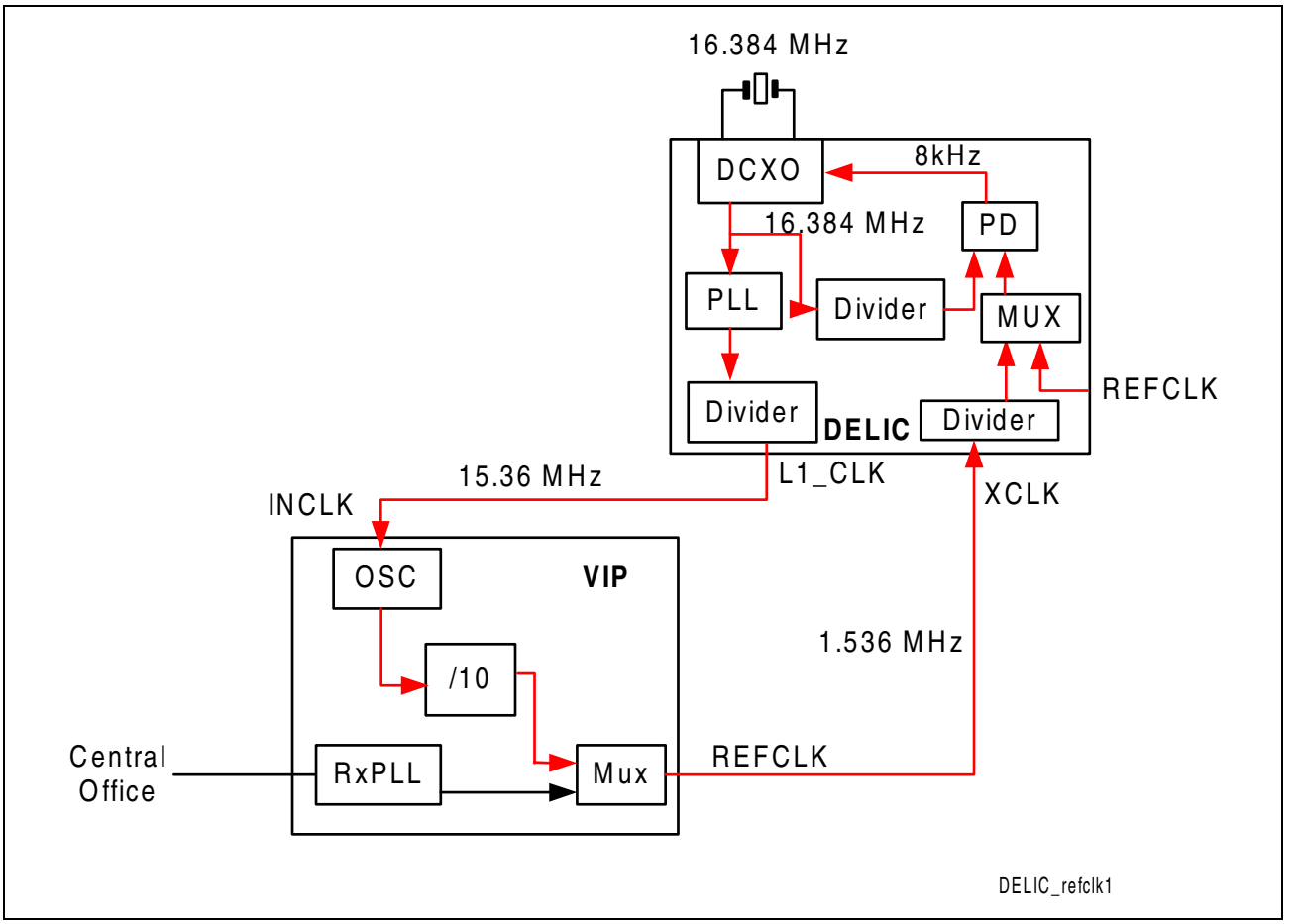


Figure 1 Clocking the VIP by using DELIC Layer 1 Clock

When the Central Office is activated, its clock signal is retrieved by the RxPLL of the VIP and a 1.536 MHz reference signal is generated and used as input signal for the DELIC DCXO (pin XCLK). This signal is divided down to 8 kHz and used as input for the DCXO phase detector (PD). The second input to PD is another 8 kHz signal which originates from the 16.384 MHz output of the DCXO.

The DELIC PLL multiplies the 16.384 MHz DCXO signal up to 61.44 MHz. A divider generates the 15.36 MHz layer 1 clock which is used to clock the VIP.

When the Central Office is deactivated, the VIP takes its oscillator signal of 15.36 MHz (the DELIC Layer 1 clock) divided by 10 and uses this signal as DELIC XCLK input as replacement of the Central Office clock.

As a consequence, the DELIC DCXO gets its own signal as input for the PD. Since the second PD input is also generated by the DCXO, the PLL system is unstable. This results in the DCXO and the PLL running to its respective corner frequency. Therefore, the 100 ppm clock accuracy, required by ITU-T I.430, cannot be guaranteed during this time. When switching to another clock source (REFCLK), the DELIC DCXO will work properly again.

The time within the DELIC DCXO guarantees the 100 ppm clock accuracy varies, depending on various conditions. When the central office deactivates, the user will be notified by the DELIC. It is up to the user to provide another clock source (for example REFCLK) for the DCXO as soon as possible.

1.2 VIP clocked in LT-T Mode by an external Crystal

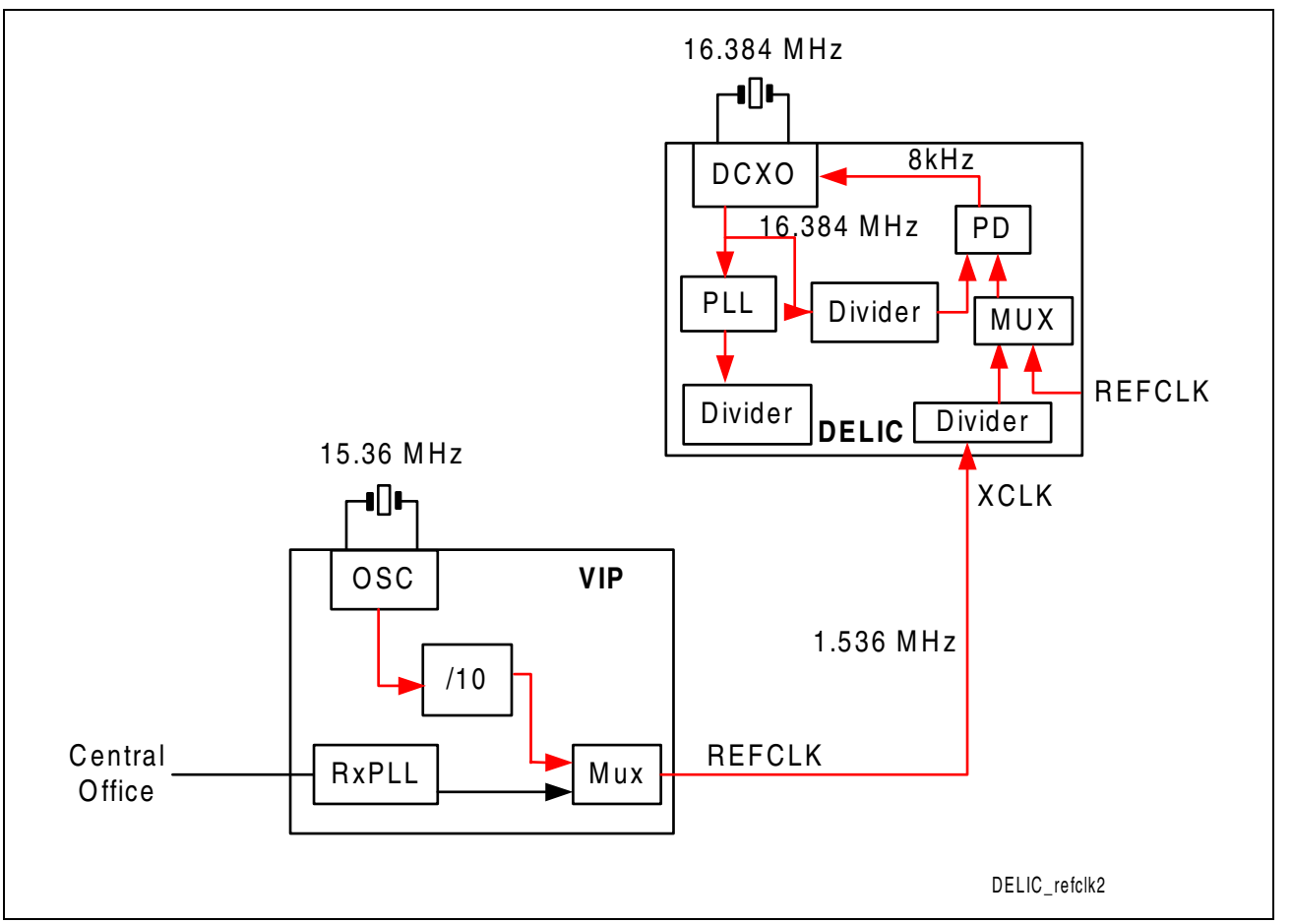


Figure 2 Clocking the VIP by using external Crystal

As shown in **Figure 2** no unstable system can occur by using an external crystal rather than the DELIC Layer 1 clock as VIP clock source in LT-T mode. When the central office line is deactivated, the VIP takes the 15.36 MHz oscillator signal and divides it by 10. This signal is used as XCLK input of the DELIC DCXO. Since the VIP 15.36 MHz signal is entirely independent from the DELIC clocking system no unstable system can occur.

Note: In LT-T mode it is recommended to use an external crystal to clock the VIP.

2 Corrections to “Recommended 16.384 MHZ Crystal Parameters”

The following table and figures should be taken as an replacement of the **“Recommended 16.384 MHz Crystal Parameters”** of the DELIC-LC PEB 20570/PEF 20570 and DELIC-PB PEB 20571/PEF 20571.

The DELIC PLL pulls the external crystal by adding/substracting capacitors (internal). By default, half of the internal capacitors are switched on at each pin (CLK16_XI and CLK_16XO).

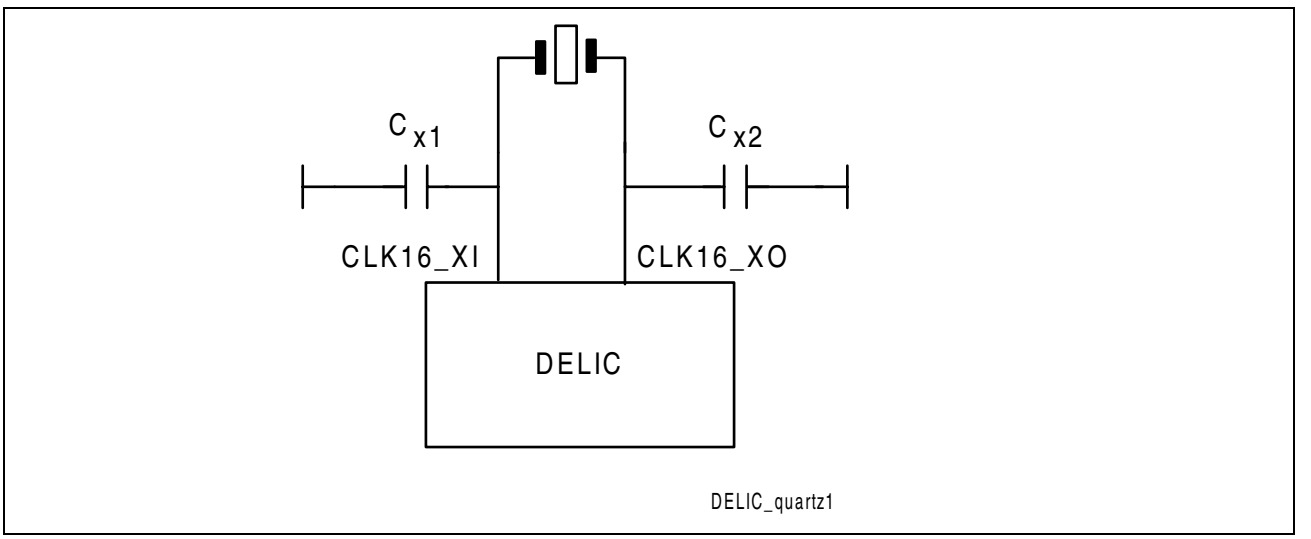


Figure 3 Connecting the Crystal to the DELIC

Attention: On the DELIC Evaluation Board (SMART 2057, Infineon) C_{x1} and C_{x2} are 3.3 pF each. This value can be used as reference, but depends on the respective board design (for example layout).

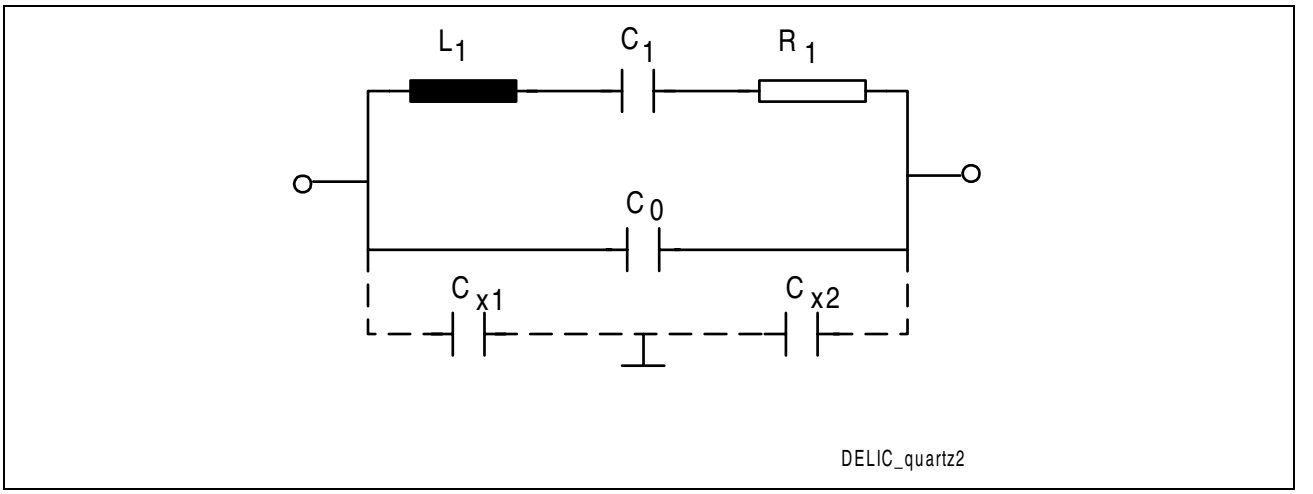


Figure 4 Equivalent Circuit Diagram of the Crystal

Table 1 Recommend Crystal Parameters

Parameter	Symbol	Values	Unit
Motional Capacitance	C_1	≥ 25	fF
Shunt Capacitance	C_0	≤7	pF
External Load Capacitance	C_L	15	pF
Resonance Resistance	R_1	≤30	Ω
Frequency Calibration Tolerance		≤150	ppm

3 Extended Temperature Range

The DELIC-LC and DELIC-PB, Version 3.1, are now available as PEF version. The PEF version is compliant to the device description in the "**DELIC-LC PEB 20570/DELIC-PB PEB 20571 Data Sheet, Version 3.1**" but extends the operating conditions to the extended temperature range of -40°C to +85°C. The ordering code is:

Table 2 DELIC-LC/DELIC-PB PEF Version Ordering Code

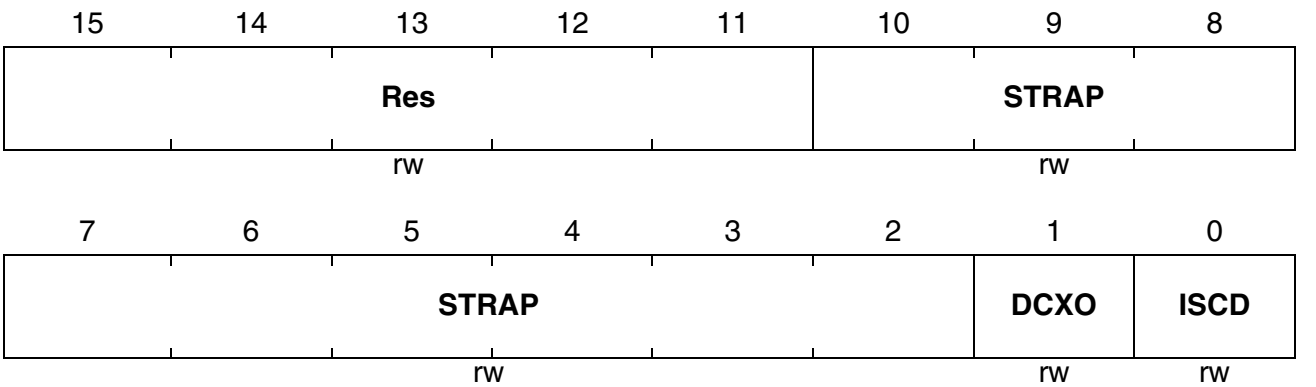
Device Name	Version	Type	Ordering Code
DELIC-LC	Version 3.1	PEF 20570	Q67237-H1442
DELIC-PB	Version 3.1	PEF 20571	Q67237-H1441

4 DELIC Strap Option Configuration

The DELIC "**Strap Status Register (CSTRAP)**" is described in the DELIC-LC PEB 20570/DELIC-PB PEB 20571 Data Sheet, independent of the version (2.1 .. 3.1). The register description (see updated register **CSTRAP**) of the Data Sheet is misleading concerning bit 0 and 1. They are **not** configured by strap option. For a stable DCXO synchronization it is recommended to proceed as follows:

1. After Boot read register CSTRAP to detect the value
2. Set only bit CSTRAP:**DCXO** to '**0**' and set the others as detected before

CSTRAP
Strap Status Register **($D08F_H$) Reset Value: 0000 0xxx xxxx xx10_B**



Field	Bits	Type	Description
Res	[15:11]	rw	**Reserved** Returns 0 upon read; must be written with 0.
STRAP	[10:2]	rw	**STRAP Pin Definition** This register enables the OAK® to read the strap values sampled during reset. Bit Function 10 PCM Clock Master Strap 9:7 Test Mode Strap 6 Emulation Boot Strap 5 PLL Bypass Strap 4 DSP PLL Power-Down Strap 3 Boot Strap 2 Reset counter Bypass Strap
DCXO	1	rw	**DCXO Synchronization Config** 0 Linear (slow) synchronization 1 Fast synchronization (default)

Field	Bits	Type	Description
ISCD	0	rw	**Internal Source Clock Delay** 0 PFS, PDC, DCL, FSC, DCL2000 are delayed by some ns (default) 1 PFS, PDC, DCL, FSC, DCL2000 are not delayed