M21012/M21011/M21001

Quad Multi-Rate CDR (42 Mbps - 3.2 Gbps)

The M21012 is a high-performance quad multi-rate clock and data recovery (CDR) array, optimized for multi-lane telecom, and datacom applications. Each channel has an independent multi-rate CDR capable of operating at data-rates between 42 Mbps and 3.2 Gbps, allowing maximum flexibility in system design. The M21011 is rated for operation in the range of 1 Gbps to 3.2 Gbps. The M21001 is rated for operation in the range of 42 Mbps to 800 Mbps. Aside from the difference in supported signal data-rates, the M21012, M21011, and M21001 are identical. Signal conditioning features include input equalization and output pre-emphasis, allowing robust reception and transmission of signals to other devices up to 60" away. User-selectable input interface types allow DC-coupled input to CML, LVDS, and LVPECL. The outputs can also be DC-coupled to CML and LVDS. Frequency acquisition is accomplished with an external reference clock. The built-in frequency synthesizer allows multi-rate operation, while operating with a single reference clock. The device can be controlled either through hardwired pins or an I^2C -compatible interface. The hardwired mode eliminates the need for an external micro-controller, while allowing control of the key features of the device. The I^2C-compatible interface allows complete control of the device features.

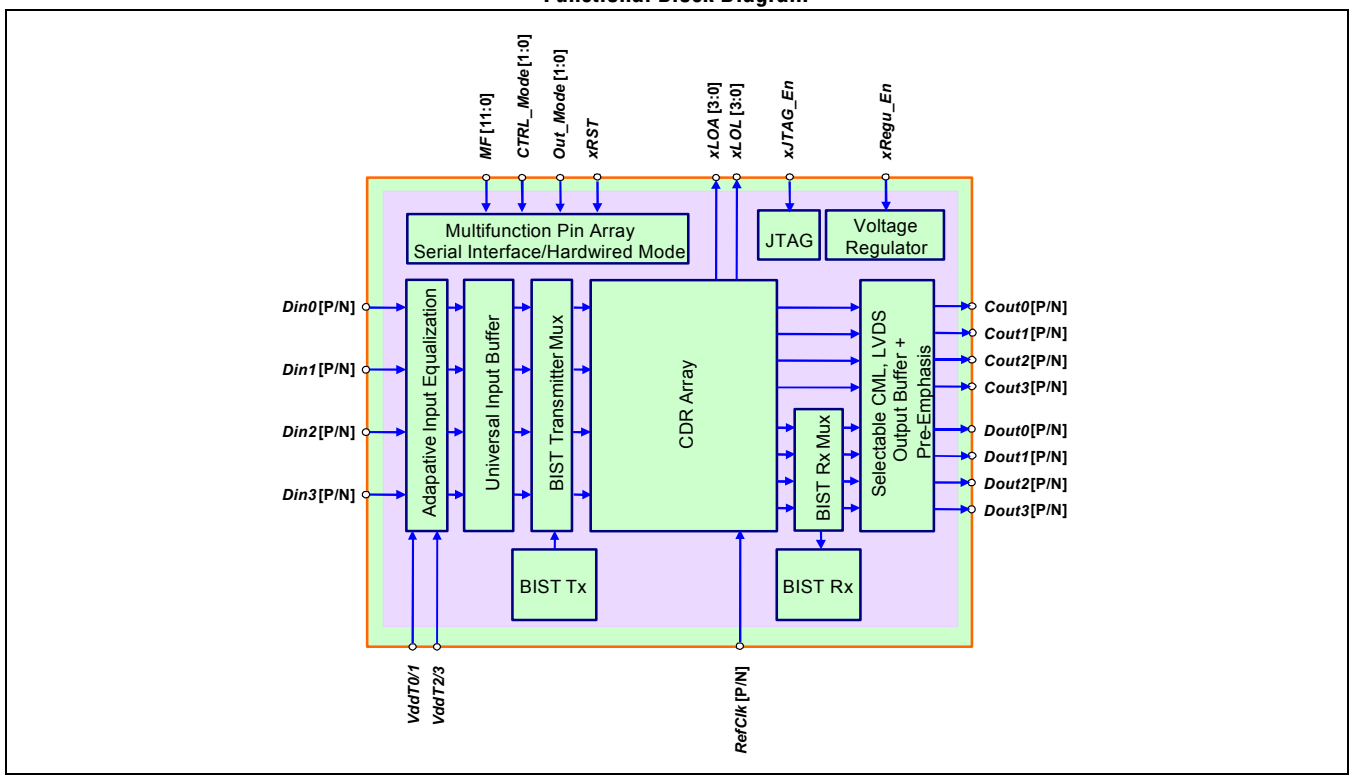
Applications

- Backplane reach extension
- SONET OC-48, OC-48 with FEC systems and modules
- Fibre Channel systems
- Gigabit Ethernet systems
- 10GBASE-CX4 systems and modules
- Clock Synthesizer

Features

- M21012 has four independent Multi-Rate CDRs capable of running between 42 Mbps and 3.2 Gbps
- M21011 has four independent Multi-Rate CDRs capable of running between 1 Gbps and 3.2 Gbps
- M21001 has four independent Multi-Rate CDRs capable of running between 42 Mbps and 800 Mbps
- Flexible DC-Coupled input interface to CML, LVPECL, and LVDS
- Flexible Control through I^2C-compatible interface or hardwired pins
- Jitter generation 4.5 mUI rms, Jitter Tolerance 0.625 UI typical
- Signal conditioning features for superior performance on FR4 trace lengths of up to 60", twinaxial cable lengths of up to 25m
- Typical Total Power Consumption as low as 400 mW with all channels running
- Built-in pattern generator and receiver for module and system testing

Functional Block Diagram



Ordering Information

Part Number	Package	Operating Data Rate
M21012-12	72-terminal, 10mm, MLF	42 Mbps - 3.2 Gbps
M21012G-12(1)	72-terminal, 10mm, MLF (RoHS compliant)	42 Mbps - 3.2 Gbps
M21011-12	72-terminal, 10mm, MLF	1 Gbps - 3.2 Gbps
M21011G-12(1)	72-terminal, 10mm, MLF (RoHS compliant)	1 Gbps - 3.2 Gbps
M21001-12	72-terminal, 10mm, MLF	42 Mbps - 800 Mbps
M21001G-12(1)	72-terminal, 10mm, MLF (RoHS compliant)	42 Mbps - 800 Mbps

NOTES:

1. The letter "G" designator after the part number indicates that the device is RoHS-compliant. Refer to www.mindspeed.com for additional information.
2. M21012, M21011, M21001 are the base device numbers, and -12 is the device revision number.
3. These devices are shipped in trays.

Revision History

Revision	Level	Date	Description
D	Release	November 2005	• Discontinued support for LVPECL output interface. • Added note about reserved two-wire serial interface addresses 00001xx. • Updated Table 2-1 with absolute maximum ratings for high-speed signal, control, interface, and alarm pins.
C	Release	July 2005	• Added RoHS compliant part numbers to the ordering information. • Table 2-2 note 4 updated to reflect $0°C \le T_a \le 70°C$ for $F_{VCO} > 2.666$ GHz. • Added Section 1.2.15 to provide details on supported ambient temperature range as a function of data-rate. • Included figure "Definition of Pre-Emphasis Levels" in Section 1.2.11 • Inserted eye diagrams in Section 1.2.10 showing input equalization performance.

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- Backplane reach extension
- SONET OC-48, OC-48 with FEC systems and modules
- Fibre Channel systems
- Gigabit Ethernet systems
- 10GBASE-CX4 systems and modules
- Clock Synthesizer

Figure 1-1. Module Application

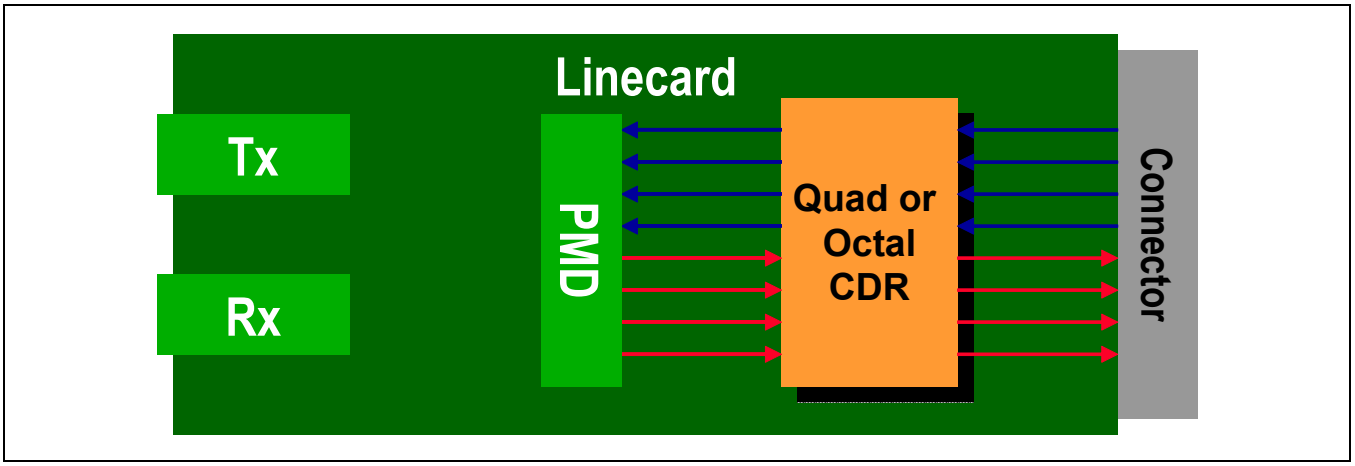


Figure 1-2. Backplane Application

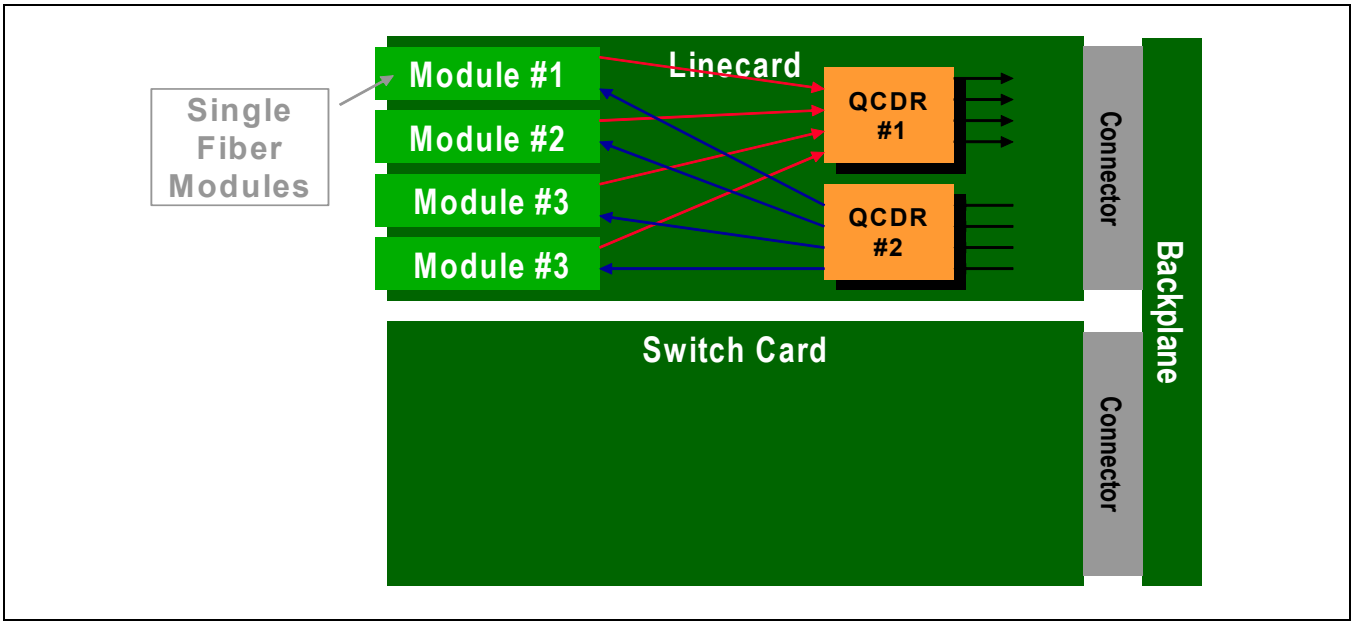
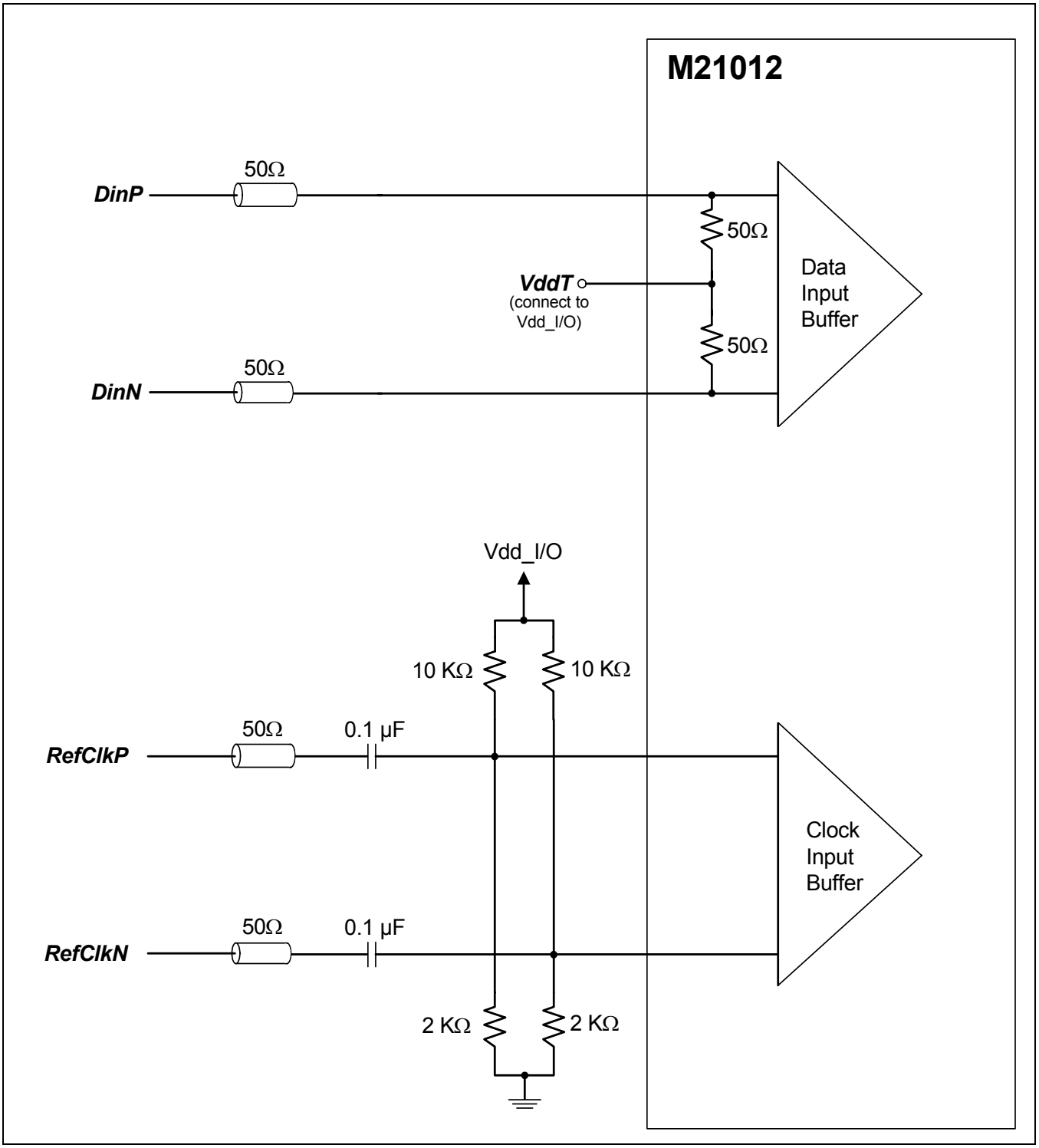


Figure 1-3. Recommended Data and Reference Clock Input Coupling Circuitry



1.2 Detailed Feature Descriptions

1.2.1 Conventions

Throughout this data sheet, physical pins will be denoted in ***bold italic*** print. An array of pins can be called by each individual pin name (e.g. ***MF0***, ***MF1***, ***MF2***, ***MF3***, and ***MF6***) or as an array (e.g. ***MF*** [6,3:0]). The M21012 control is accessed through registers that employ an 8-bit address and an 8-bit data scheme. Registers are denoted in italic print, (e.g. *TestRegister)* and individual bits within the register will be called out as *TestRegister* [4:3] to denote the 4th and 3rd bit where bit 0 is the LSB and bit 7 is the MSB. Many features of the device are bit mapped within a register; if the status of the other bits are uncertain, it is recommended that the user reads the value from the register before writing, to assure only the desired bits change. Writing in the same value to the bits within a register does not cause glitches to the unchanged features. The addresses for the registers as well as their functions can be found in detail in Chapter 3.0. The purpose of the text description is to highlight the features of the registers. For redundant items, such as the channel number, the registers will have a nomenclature of *TestReg*_0 for channel 0, *TestReg*_1 for channel 1, *TestReg*_2 for channel 2, *TestReg*_3 for channel 3. For general reference, the text will denote such registers as *TestReg*_N where N can vary from 0 to 3. Individual CDR and LOA circuits are mapped to input channels.

1.2.2 Reset

Upon application of power, the M21012 automatically generates a master reset. At any time, forcing ***xRST*** = L causes the M21012 to enter the master reset state. A master reset can also be initiated through the registers in the two-wire interface control mode by writing AAh to *Mastreset*. Once a master reset is initiated, all registers are returned to the default values, the internal state machines cleared, and all CDR/BIST reset to the out-of-lock condition. After a reset, the register *Mastreset* will automatically return to the default value of 00h.

Each individual CDR can be soft reset by setting *CDR_ctrlA*_N [7] = 1 where N = 0 for CDR 0, N = 1 for CDR 1 and so on. The bit should be returned to 0b for normal operation. After a soft reset, the registers that determine the CDR operation options such as data-rate, window sizes, etc., remain unchanged and only the CDR state-machine is reset, resulting in an out-of lock condition.

1.2.3 Internal Voltage Regulator

The digital and analog core are designed to run at 1.2V, however, for operation from 1.8V to 3.3V, an internal linear voltage regulator is provided. ***xRegu_En*** = L enables the voltage regulator which uses ***AVdd_I/O*** and ***DVdd_I/O*** to generate the required 1.2V for ***AVdd_Core*** and ***DVdd_Core***. In this mode, the ***AVdd_Core*** and ***DVdd_Core*** pins should be connected to a floating DC low inductance PCB plane and AC bypassed to ***Vss*** using standard decoupling techniques. If desired, ***AVdd_Core*** and ***DVdd_Core*** can be separated into individual planes. If 1.2V is available, it can be connected directly to ***AVdd_Core*** and ***DVdd_Core,*** to save power, by bypassing the internal linear regulator with ***xRegu_En*** = H. In this case, it is recommended that the ***AVdd_Core*** and ***DVdd_Core*** pins be tied together to a common PCB plane, and bypassed to ***Vss*** with standard decoupling techniques.

1.2.4 High-Speed Input/Output Pins

The high-speed input data interface is Universal High-Speed (UHS), which can support PCML, LVDS, and LVPECL with no external components (DC coupled), while 5V PECL or –5.2V ECL would require AC coupling capacitors (internal 50Ω input pull-ups). The high-speed serial differential data (42 Mbps to 3200 Mbps) enters the device via ***Din*** [3:0,P/N]. Inputs 0 and 1 are internally terminated with 50Ω to ***VddT0/1*** and inputs 2 and 3 are terminated with 50Ω to ***VddT2/3***. For different applications ***VddT*** may be terminated to other DC voltages to minimize DC currents.

For other input interfaces, DC coupling is permitted if the input level meets the input swing and common-mode requirements by terminating ***VddT*** to a DC voltage that keeps the DC current draw within specifications. If this DC voltage is not readily available, ***VddT*** can be decoupled to ground with high frequency capacitors. In all cases, ***VddT*** must be a low-impedance node since it is shared between inputs, which requires either a low impedance plane or bypass capacitors.

Table 1-1. Typical AVdd_I/O and VddT Supply Levels for Different Input Interfaces

Interface	Logic High Range (V)	Common Mode Range (V)	Logic Swing Range (mVpp Diff)	*AVdd_I/O* Range (V)	*VddT* Supply
PCML	***AVdd_I/O***	***AVdd_I/O*** - Swing/2	100 - 2000	1.8 - 3.3	***AVdd_I/O***
LVDS	1.4	1.2	100 - 700	1.8 - 3.3	Decoupled
AC-Coupled	N/A	N/A	100 - 2000	1.8 - 3.3	***AVdd_I/O***

NOTE: Table for standard interfacing applications. Non-standard interfacing applications must meet I/O specifications.

The M21012 supports multiple high-speed output modes. The output modes are selectable with hardwired pins only. The I/O interface is set with ***Out_Mode*** [1:0] and the output level with ***MF*** [9:8] as shown in Table 1-2. In the two-wire interface mode, the *Out_ctrl*_N [7:6] register is used to set the data level, and ***Out_Mode*** [1:0] is used to set the interface type. In the two-wire interface mode, the data output can be enabled with *Out_ctrl*_N [2] = 1b (default) and the output data polarity can be flipped by setting *Out_ctrl*_N [3] = 1b (default: no inversion). Output data polarity flip is an internal function that would have the same effect as switching the P and N terminals. The recommended ***AVdd_I/O*** for the different output interfaces is shown in Table 1-3. The PCML+ mode is the same as the PCML mode except that higher output swing levels are provided for applications that may require them.

Table 1-2. Output Interface and Level Mapping (For both hardwired and software modes)

Multifunction Pins & Register ***MF*** [9:8] *Out_ctrl*_N [7:6]	PCML Mode ***Out_Mode*** [1:0] = 00b	LVDS Mode ***Out_Mode*** [1:0] = 01b	PCML+ Mode ***Out_Mode*** [1:0] = 11b
00b	Off	Off	Off
01b	600 mV	RRL at 450 mV	1000 mV
10b	1000 mV	GPL at 650 mV	1300 mV
11b	1300 mV	1000 mV	1600 mV

Table 1-3. Output Interface and Recommended AVdd_I/O Range

Output Logic	*AVdd_I/O* Range (V)
Off	1.8 - 3.3
PCML at 600 mV	1.8 - 3.3
PCML at 1V	1.8 - 3.3
PCML at 1.3V	1.8 - 3.3
PCML+ at 1.6V	1.8 - 3.3
LVDS GPL	1.8 - 3.3
LVDS RRL	1.8 - 3.3

1.2.5 CDR Reference Frequency

The CDR frequency acquisition requires the use of an external reference clock. An external reference clock is applied to ***RefClk***[P/N] to enable frequency reference acquisition (FRA) in the CDR. PCML, CMOS are examples of the wide variety of interfaces supported for the reference clock. The inputs contain a DC-coupled 100Ω differential termination between ***RefClkP*** and ***RefClkN*** along with a 100 KΩ pull-down on each terminal to ***Vss***. After this termination/pull-down block, the inputs are AC coupled internally. The common-mode and allowable voltage swings are specified in Table 2-10. The ***RefClk*** common-mode must be above 250 mV, which may require external pull-ups.

1.2.6 Multifunction Pins Overview

The M21012 is designed to be an extremely versatile device, with many user selectable options in the CDR and I/O, to optimize performance. All of these options can be accessed and controlled through the I^2C-compatible two-wire serial interface. The I^2C-compatible serial interface I/O pins and address pins are mapped to the multifunction pins ***MF*** [11:0]. A subset of the key features for most applications, such as standard data-rates, I/O levels, etc., can be selected through ***MF*** [11:0] in the hardwired mode. The hardwired mode does not require the use of a serial interface. In this mode, upon power up (auto reset on power up), the M21012 function is determined by the status of the hardwired pins. During operation, the hardwired pins can change states, which would cause the CDR to follow with the appropriate action. Another feature of the multifunction pins is to support JTAG testing of this device during PCB manufacturing.

The various control and test modes of this device are selected with three pins: ***CTRL_Mode*** [1:0]**,** and ***xJTAG_En***. ***xJTAG_En*** = L overrides ***CTRL_Mode*** [1:0]**,** and puts the device in JTAG test mode, while ***xJTAG_En*** = H allows ***CTRL_Mode*** [1:0] to determine the M21012 control mode, as summarized in Table 1-4.

Table 1-4. Mode Select Pins

Pin	JTAG Test Mode	Hardwired Mode	Two-Wire Serial Mode
xJTAG_En	L	H	H
CTRL_Mode [1:0]	no impact	11b	01b

1.2.7 Multifunction Pins Defined for Hardwired Mode

In the hardwired mode, a subset of options in the M21012 can be accessed with hardwired physical pins, as defined in Table 1-5. The hardwired data-rates along with the default reference clock frequency are shown in Table 1-6.

Table 1-5. Multifunction Pins for Hardwired Mode

Pin	Function	Description
MF0	Data-rate selection	CDR data-rate select (see Table 1-6 for description)
MF1	Data-rate selection	CDR data-rate select (see Table 1-6 for description)
MF2	Data-rate selection	CDR data-rate select (see Table 1-6 for description)
MF3	Data-rate selection	CDR data-rate select (see Table 1-6 for description)
MF4	Pre-emphasis control	L = Pre-emphasis enable H = Pre-emphasis disable
MF5	Clock output control	L = Clock outputs enable H = Clock outputs disable
MF6	Clock polarity flip	L = Clock polarity flip H = Standard clock polarity
MF7	Data polarity flip	L = Data polarity flip H = Standard data polarity
MF8	Output level selection	00b: All outputs disabled 01b: 600 mV (CML) 10b: 1V (CML) 11b: 1.3V (CML) See Table 1-2 for the other output interface modes.
MF9	Output level selection	
MF10	Equalization control	L = Input equalization enabled H = Input equalization disabled
MF11	CDR bypass control	L = All CDRs bypassed and powered down H = All CDRs enabled

Table 1-6. Hardwired Data-Rates and Associated Reference Clock Frequencies

Pins *MF* [3:0]	Application	Signal Data-Rate (Mbps)	Reference Frequency (MHz)
0000	10x Fibre Channel - XAUI	3187.5	159.375
0001	10 Gigabit Ethernet - XAUI	3125	156.25
0010	STS-48 + FEC	2666	19.44
0011	STS-48	2488.32	19.44
0101	2x Fibre Channel	2125	106.25
0110	Gigabit Ethernet	1250	125
0111	1x Fibre Channel	1062.5	106.25
1000	STS-12	622.08	19.44
1001	STS-3	155.52	19.44
1010	STS-1	51.84	19.44
1011	ESCON	200	10
1100	FE	125	12.5
1101	STS-48	2488.32	155.52

1.2.8 Two-Wire Serial Interface

The two-wire serial interface is compatible with the I^2C standard. The M21012 supports the read/write slave-only mode, 7-bit device address field width, and supports the standard rate of 100 Kbps, fast mode of 400 Kbps, and high-speed mode of 3.4 Mbps. The 7-bit address for the device is determined with ***MF*** [6:0], which allows for a maximum of 124 unique addresses for this device. The four addresses 00001xx (4, 5, 6, 7) are reserved and should not be used. SDA (***MF11***) and SCL (***MF10***) can drive a maximum of 500 pF each at the maximum rate. During the write mode from the master to the M21012, data is latched into the internal M21012 registers on the rising edge of SCL, during the acknowledge phase (ACK) of communication. Table 1-7 summarizes the multifunction pins for the two-wire serial interface mode. For further information on timing, please see the I ^2C bus specification standard.

Table 1-7. Multifunction Pins for Two-Wire Interface

Pin	Function	Description
MF0	Address bit 0	7-bit device address; address bit 0 is LSB, address bit 6 is MSB
MF1	Address bit 1	
MF2	Address bit 2	
MF3	Address bit 3	
MF4	Address bit 4	
MF5	Address bit 5	
MF6	Address bit 6	
MF10	SCL	Clock input
MF11	SDA	Data input/output (open drain)

1.2.9 JTAG

The M21012 supports JTAG external boundary scan, which includes all of the high-speed I/O, as well as the traditional digital I/O. Table 1-8 shows the multifunction pins signal mapping for JTAG testing.

Table 1-8. Multifunction Pins for JTAG

Pin	Function	Description
MF8	TMS	Test select
MF9	TDI	Test data input
MF10	TCK	Test clock
MF11	TDO	Test data output

1.2.10 Input Deterministic Jitter Attenuators

Each of the four input channels contains an independent input equalizer (IE). For the IE, the address N is mapped to the input channel. In the hardwired mode, there is the option to set input equalization on or off. In the two-wire serial interface control mode, the default state allows for configurable input equalization settings using *Ineq_ctrl*_N [2:0], for which the setting of 100b is optimized for trace lengths between 10 - 46 inches.

The input equalization settings have been optimized for a variety of backplane and connectivity applications, such as board traces and twinaxial cables. For board traces on FR4, such as the Tyco Electronics Hm-Zd legacy backplane, the input equalizer can drive trace-lengths of up to 60” at 3.1875 Gbps, and up to 72” at 2.125 Gbps. The equalizer has similar high performance on Nelco-13, Arlon 25, Rogers 3003, 4003C, 4340, GeTek PCB materials, and twinaxial cables. The input equalizer was designed to compensate for the deterministic jitter accumulation effects of typical backplane interconnects, which have bandwidths of hundreds of MHz to a few GHz. The equalizers are not expected to make a significant difference in performance with signal data-rates less than 1 Gbps.

Another component of input deterministic jitter is inter-symbol interference (ISI) due to DC offsets. By default, a DC servo-like circuit is enabled to correct for this type of deterministic jitter, and can be disabled by setting *Ineq_ctrl*_N [4] = 0b. The DC servo can also be used to track changes in the common mode, for single-ended operation.

Figure 1-4. STS-48 waveform after transmission through 76” of PCB traces (input to M21012)

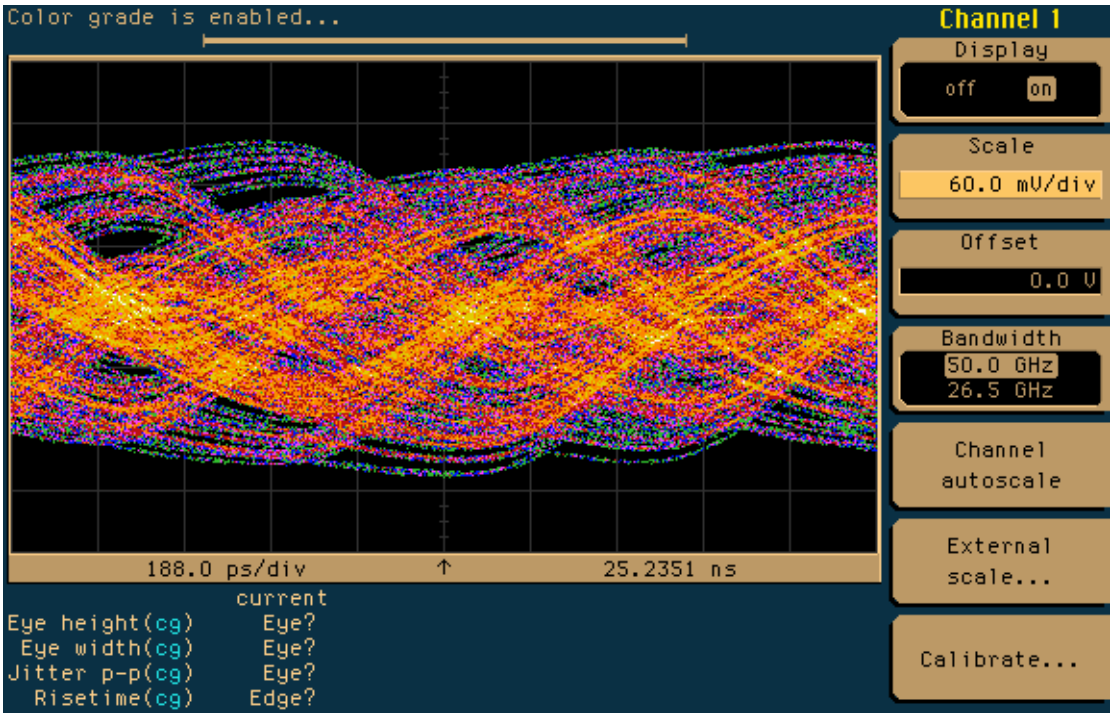
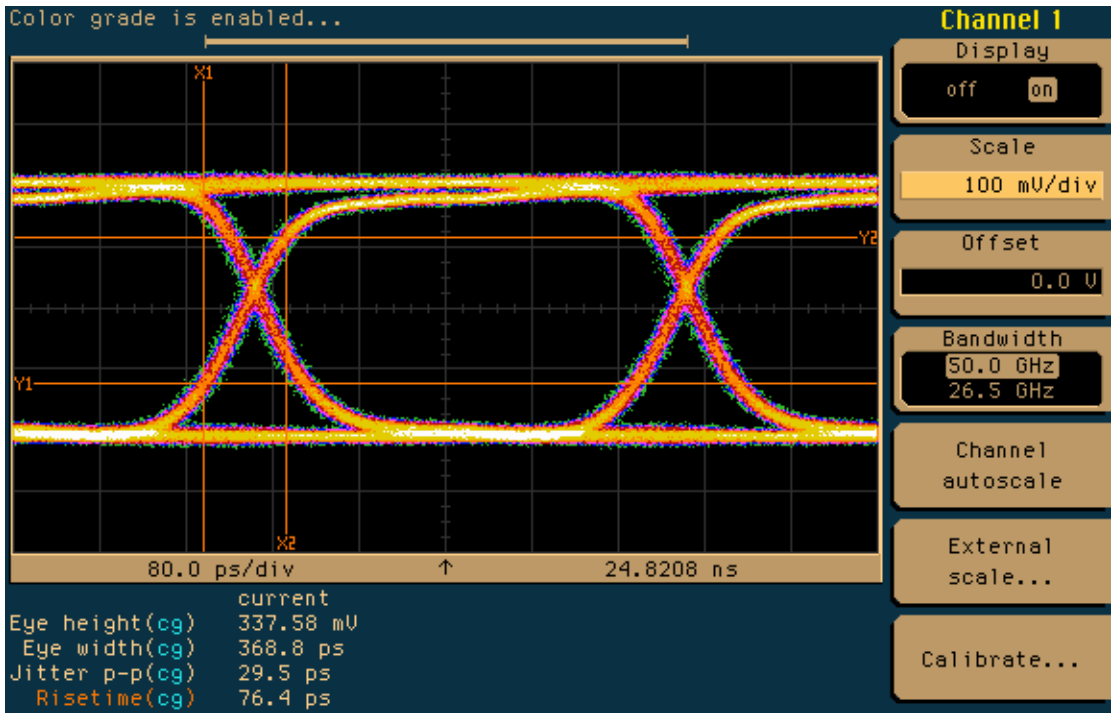


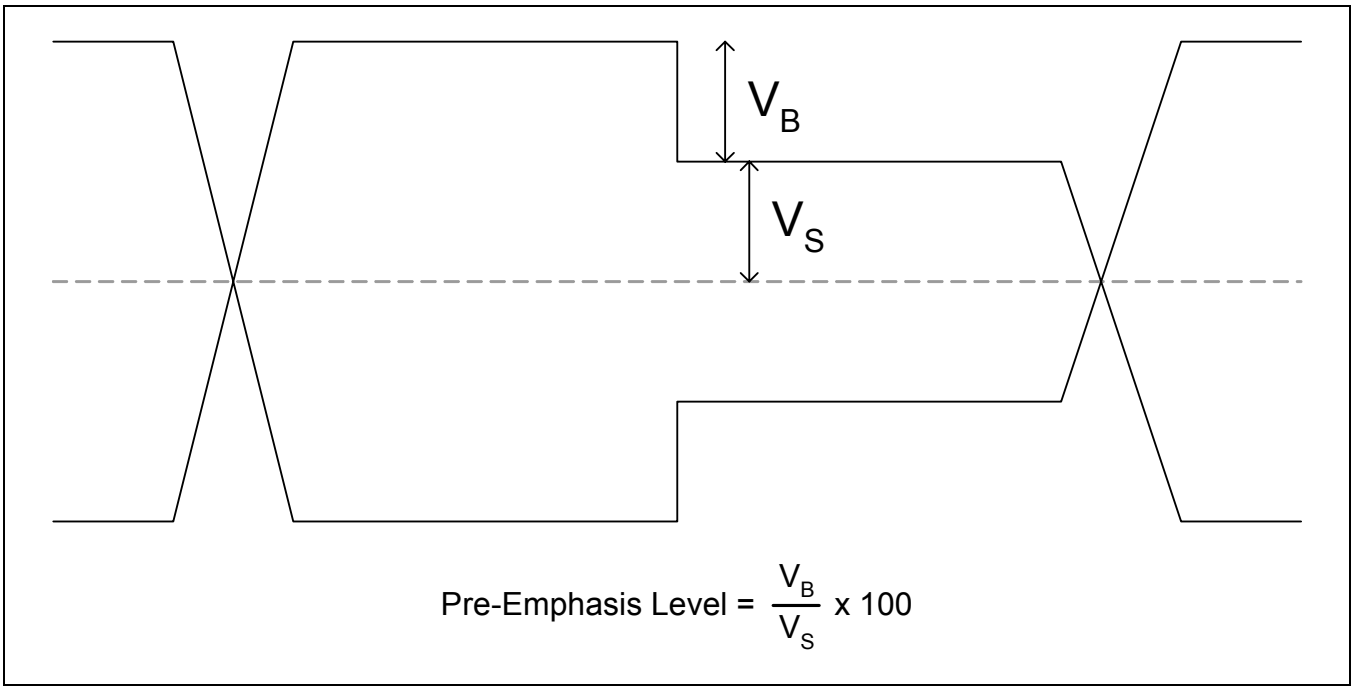
Figure 1-5. STS-48 waveform at M21012 output with input shown in Figure 1-4



1.2.11 Output Pre-Emphasis

Each of the four output channels contains an independent output pre-emphasis circuit that can be used to select the optimal pre-emphasis level. The pre-emphasis settings have been optimized for a variety of backplane and connectivity applications. For board traces on FR4, such as the Tyco Electronics Hm-Zd legacy backplane, the pre-emphasis circuit can drive trace-lengths of up to 40” at 3.1875 Gbps, and up to 60” at 2.125 Gbps. Like the input equalizer settings, the output pre-emphasis circuit has similar high performance on Nelco-13, Arlon 25, Rogers 3003, 4003C, 4340, GeTek PCB materials, and twinaxial cables. The digital pre-emphasis level is selected, for each output channel, with *Preemp_ctrl*_N [2:0], and the default value of 000b corresponds to pre-emphasis disabled. The pre-emphasis circuit tracks the signal data-rate throughout the multi-rate range, however, like the input equalizer, it is designed to compensate for the bandwidth limitations of the interconnect, and may not have the desired effects at the low end of the multi-rate range. The output pre-emphasis function is available for all data interfaces and levels.

Figure 1-6. Definition of Pre-Emphasis Levels



1.2.12 CDR Features

The M21012 contains four multi-rate CDRs, that can each operate at independent data-rates. When the CDR achieves phase lock onto the incoming data stream, the CDR removes the incoming random jitter above its loop bandwidth, as well as any deterministic jitter remaining from the two input deterministic jitter attenuators (IE & DC servo). The M21012 output data has extremely low jitter, due to retiming with a very low jitter generation CDR. The output pre-emphasis option allows for compensation of interconnect deterministic jitter, generated up to the next downstream device.

Each CDR is capable of multi-rate operation which is achieved by a combination of built in VCO frequency dividers (VCD), Data Rate Dividers (DRD), and a wide VCO tuning range (F_{min} = 2.0 GHz, F_{max} = 3.2 GHz). As a result, the allowed input data range is F_{min} / DRD_{max} to F_{max} / DRD_{min}. Although the ranges are not continuous, the ranges are deliberately chosen to cover all typical applications.

By default, the loop-bandwidth is set to pass SONET STS-48 specifications, with DRD = 1 and F_{vco} = 2.48832 GHz, with less than 0.1 dB of jitter peaking, and approximate bandwidth of 2 MHz. Within a given VCO frequency

range, the bandwidth will scale proportionately. For example, if the loop bandwidth (F_{LBW}) is 2 MHz at 2.48332 GHz, then at 3.125 GHz the F_{LBW} will be 2.5 MHz, and peaking will be less than 0.1 dB. When DRD is not equal to 1, the bandwidth at DRD = 1 scales by the DRD divide ratio. For example, if the F_{LBW} is 2 MHz at STS-48 with DRD = 1, then if DRD = 4 for STS-12 operation, the F_{LBW} will be 500 KHz. In the hardwired mode, the F_{LBW} will be properly set for the hardwired data-rates. In the two-wire serial interface mode, the default bandwidth scales automatically with the input signal data-rate. The loop bandwidth (F_{LBW}) can also be tuned through the registers.

The CDR needs to achieve frequency lock before it can achieve phase lock and re-time the input data. Frequency reference acquisition (FRA) requires an external frequency source to be connected to the ***RefClk*** [P/N] pins.

Frequency acquisition is accomplished with two key sections. The first section is a secondary frequency lock loop (FLL) that drives the VCO towards the desired frequency. The second section is the loss-of-lock circuitry (LOLCir), that turns on or off the secondary FLL. Both loss of lock (LOL) and loss of activity (LOA) have register bits (*Alarm_LOA* and *Alarm_LOL*) which are active high, and pins (***xLOA*** [3:0] and ***xLOL*** [3:0]) which are active low. ***xLOA*** [3:0] and ***xLOL*** [3:0] can be wired OR externally. In general context, they will be referred to as LOL or LOA which is active H. Frequency acquisition takes place when the LOLCir determines an out of lock condition (LOL = H) for each CDR, when the VCO frequency exceeds a given range (window). The LOLCir enables the secondary FLL to drive the VCO close to the desired frequency (the input signal data-rate). When the VCO falls within a given frequency range where the CDR loop can acquire phase lock, the LOLCir turns off the secondary FLL and sets LOL = L, allowing the CDR to achieve phase lock. During this time, the LOLCir continues to monitor the frequency difference and will signal a LOL = H, to start the acquisition routine again, if the frequency falls out of range. The LOLCir range is fixed in the hardwired mode, and programmable in the two-wire interface mode. The frequency threshold (window) for LOL = H-to-L and LOL = L-to-H are different, to prevent LOL from toggling when the frequency is near one of the windows. These registers also control the frequency acquisition time. Suggested values are given in this document for general robust operation, and are used as register defaults, however, the programmability of the registers allow for optimization based on a given application (e.g. faster lock times).

Each CDR contains an independent loss of activity (LOA) detector that determines if there is valid data, by comparison with the transition density of the reference clock; this assumes a 50% transition density for the data. Fixed window detectors compare the data transition density with the reference frequency. If the data transition density falls outside of the 50% +/- 12.5% window, a loss of activity condition is signaled. When LOA goes high, it (just like LOL) forces the FLL to turn on, so that the VCO will be forced to the desired frequency range. When LOA goes low again, phase lock will occur.

All of the CDRs are reset upon ***xRST*** = L, *Mastreset* = AAh, or upon power up. A soft reset through *CDR_ctrlA*_N [7] = 1b resets the individual CDR state machine, and presets the CDR to an out-of-lock condition, however, the register contents that are related to CDR setup are unchanged. It is required to force a soft-reset if the signal data-rate is dynamically changed. The soft reset register bit needs to be cleared for proper operation. A reset during operation will cause bit errors, until the CDR achieves phase lock.

By default, all of the CDRs are active and powered up for normal operation. By setting *CDR_ctrlB*_N [7:6] = 11b, a CDR can be bypassed and powered down, to allow for non-standard data-rates, or to save power when the CDR is not required at lower data-rates. When *CDR_ctrlB*_N [7:6] = 01b, the CDR is bypassed but active (VCO locked to the input data), the output data is not re-timed. In the last mode with *CDR_ctrlB*_N [7:6] = 10b, the CDR is powered down and the input and output paths are also powered down. In this case the input signal does not reach the output, so this setting should only be used to power down unused channels.

The on-chip loop filter automatically scales with the VCO data-rate divider selection. For operation with a fixed DRD setting, the loop bandwidth scales proportionally to the new data-rate, from the standard SONET operating frequency. From the default setting, the bandwidth can be reduced to 80% with *Phadj_ctrl*_N [5:4] = 00b, and increased to 400% with *Phadj_ctrl*_N [5:4] = 10b.

To prevent the propagation of noise in the case where there is a LOL/LOA condition, the CDR contains an auto-inhibit feature, which is enabled by default. When either LOA or LOL is active, the output of the CDR is fixed at a logic high state (***DoutP*** = H, ***DoutN*** = L). This feature can be disabled by setting *CDR_ctrlA*_N [3] = 0b, which allows *CDR_ctrlA*_N [5] to either force an inhibit (1b) or to never inhibit (0b).

In some optical module and backplane applications, the optimal data sampling point is not in the middle of the data eye. By default, the CDR achieves phase lock very near the center of the eye. For optimal performance (jitter tolerance), the actual sampling point can be adjusted with *Phadj_ctrl*_N [3:0]. The adjustment range is from –122.5 mUI to +122.5 mUI with 17.5 mUI steps.

1.2.13 Multi-Rate CDR Data-Rate Selection

For multi-rate operation, the first step is to determine the desired data-rate range. The input data range must be bracketed by $DF_{min} = F_{vco,min}/DRD_{max}$ to $DF_{max} = F_{vco,max}/DRD_{min}$. $DF_{max/min}$ are the maximum/minimum input data-rate frequencies, $DRD_{max/min}$ are the maximum/minimum data-rate divider settings using *CDR_ctrlB*_N [3:0], and $F_{vco,min}/F_{vco,max}$ are the minimum/maximum VCO frequencies, which are 2.0 GHz and 3.2 GHz respectively. The valid data-rates are shown in Table 1-9.

Table 1-9. Valid Input Data Ranges

Parameter	DF_{min}	DF_{max}	Units
Data-rate divider (DRD = 1): *CDR_ctrlB*_N [3:0] = 0000b	2.0	3.2	GHz
Data-rate divider (DRD = 2): *CDR_ctrlB*_N [3:0] = 0001b	1.0	1.6	GHz
Data-rate divider (DRD = 4): *CDR_ctrlB*_N [3:0] = 0010b	500	800	MHz
Data-rate divider (DRD = 8): *CDR_ctrlB*_N [3:0] = 0011b	250	400	MHz
Data-rate divider (DRD = 12): *CDR_ctrlB*_N [3:0] = 0100b	166.7	266.66	MHz
Data-rate divider (DRD = 16): *CDR_ctrlB*_N [3:0] = 0101b	125	200	MHz
Data-rate divider (DRD = 24): *CDR_ctrlB*_N [3:0] = 0110b	83.33	133.33	MHz
Data-rate divider (DRD = 32): *CDR_ctrlB*_N [3:0] = 0111b	62.5	100	MHz
Data-rate divider (DRD = 48): *CDR_ctrlB*_N [3:0] = 1000b	42	66.66	MHz

It is important to note the difference between the VCO frequency (F_{vco}), and the data-rate frequency (DF). F_{vco} is always between 2 GHz to 3.2 GHz, while DF is the divided down F_{vco} that matches the input data-rate.

1.2.14 Frequency Reference Acquisition (FRA)

When an external reference is applied to ***RefClk***, the FRA mode is selected in either the hardwired or two-wire serial interface mode. Frequency acquisition is enabled by the LOLCir when LOL = H (*Alarm_LOL* = H or ***xLOL*** = L). A secondary FLL attempts to lock the VCO to a frequency derived from the external reference. When the frequency is close to the desired frequency, LOLCir sets LOL = L and disables the secondary FLL, thus, the main CDR PLL is free to phase lock to the incoming data. Although the main CDR PLL can achieve frequency lock, the VCO frequency tuning range typically exceeds the CDR PLL inherent acquisition range. This implies that the FLL needs to get the VCO within the CDR PLL range. The loss of lock circuitry (LOLCir) is used to determine when the secondary FLL is active. The LOLCir consists of window detectors that constantly compare a scaled VCO frequency, to a frequency related to the external reference. When LOL = H the loop is out of lock, the FLL is activated until the frequency difference is within the narrow reference window (NRW). When LOL = L, the FLL is not engaged until the frequency exceeds the wide reference window (WRW). If a signal is not present, the FLL circuit will drive the VCO frequency to the NRW and turn off. Without data present, the VCO would then drift until the frequency difference exceeds the WRW, and repeat this cycle. To prevent this, by default, the FLL is activated with LOL = H, or LOA = H and the FLL is not de-activated unless both LOL = L and LOA = L.

Figure 1-7. Block Diagram of FRA Mode

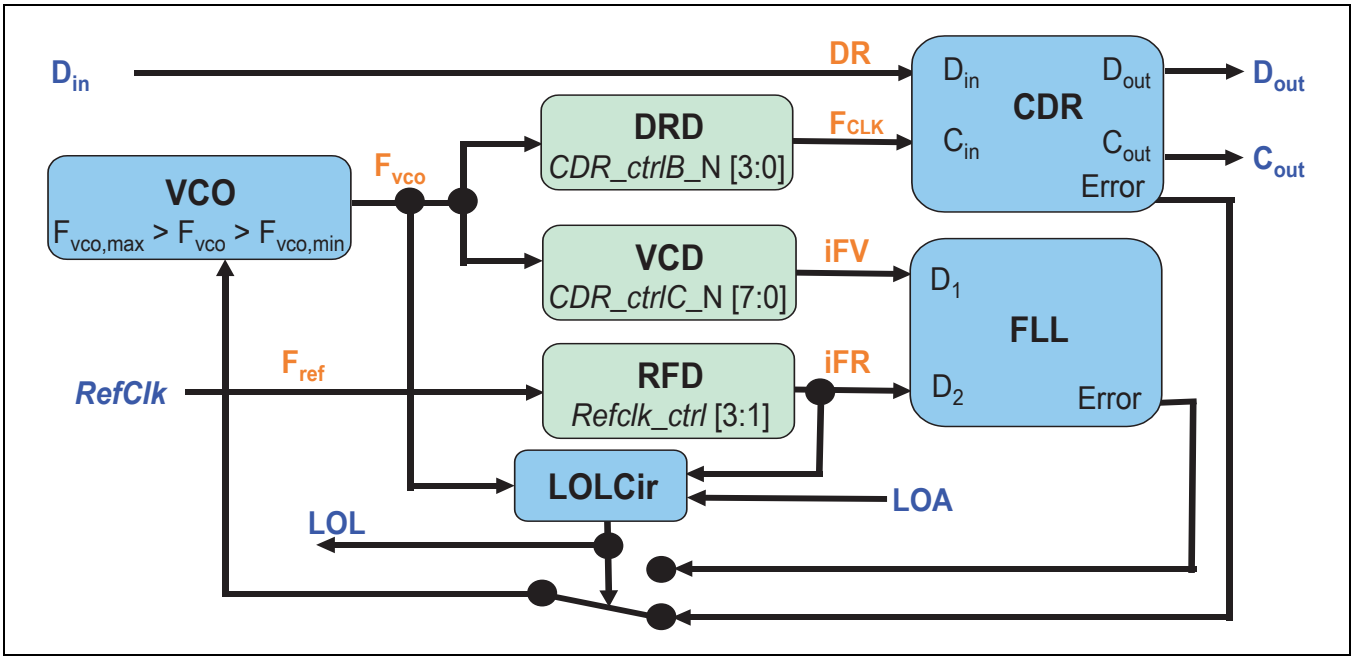


Figure 1-7 shows a block diagram of the FRA mode. The secondary FLL for the FRA mode compares a scaled version of the internal VCO frequency (iFV) with a scaled version of the reference clock frequency (iFR); iFR and iFV are limited to between 10 MHz and 25 MHz. The external reference clock frequency (F_{ref}) is applied to the ***RefClk*** [P/N] terminals. This reference frequency is scaled to the iFR by the reference frequency divider (RFD) [*Refclk_ctrl* [3:1]], which allows for an external reference clock in the range of 10 MHz to 800 MHz. The RFD level is a globally set value that applies to all CDRs. Table 1-10 gives the divider ratio, along with the minimum and maximum F_{ref} values.

Table 1-10. Reference Clock Frequency Ranges

RFD Value	Minimum F_{ref} (MHz)	Maximum F_{ref} (MHz)
RFD (*Refclk_ctrl* [3:1] = 000b): divide by 1	10	25
RFD (*Refclk_ctrl* [3:1] = 001b): divide by 2	20	50
RFD (*Refclk_ctrl* [3:1] = 010b): divide by 4	40	100
RFD (*Refclk_ctrl* [3:1] = 011b): divide by 8	80	200
RFD (*Refclk_ctrl* [3:1] = 100b): divide by 12	120	300
RFD (*Refclk_ctrl* [3:1] = 101b): divide by 16	160	400
RFD (*Refclk_ctrl* [3:1] = 110b): divide by 32	320	800

The VCO frequency is scaled to the iFV by the VCO comparison divider (VCD) [*CDR_ctrlC*_N [7:0]]. Table 1-11 provides DRD, RFD, and VCD values for common applications. For applications that only deal with SONET/SDH data-rates, a 19.44 MHz reference clock frequency must be used. For applications where a combination of SONET/SDH and other data-rates are used, a 25 MHz reference clock frequency must be used. If either of these reference clock frequencies is not available, please contact Mindspeed Technologies Applications Engineering for other options.

Table 1-11. DRD/RFD/VCD Settings for Different Data-Rates and Reference Frequencies

Application	DR (Mbps)	Fref (MHz)	DRD	RFD	VCD	Notes
10GE - XAUI	**3125**	**156.25**	**1**	**8**	**160**	**1**
10GE-XAUI	3125	25	1	2	250	
10GFC - XAUI	**3187.5**	**159.375**	**1**	**8**	**160**	**1**
10GFC-XAUI	3187.5	25	1	2	255	2
STS-48+FEC	**2666.06**	**19.44**	**1**	**1**	**137**	**1, 2**
STS-48 + FEC	2666.06	25	1	2	213	2
STS-48	**2488.32**	**155.52**	**1**	**8**	**128**	**1**
STS-48	**2488.32**	**19.44**	**1**	**1**	**128**	**1**
STS-48	2488.32	25	1	2	199	2
2GFC	**2125**	**106.25**	**1**	**8**	**160**	**1**
2GFC	2125	25	1	2	170	
GE	**1250**	**125**	**2**	**8**	**160**	**1**
GE	1250	25	2	2	200	
FC	**1062.5**	**106.25**	**2**	**8**	**160**	**1**
FC	1062.5	25	2	2	170	2
STS-12	**622.08**	**19.44**	**4**	**1**	**128**	**1**
STS-12	622.08	25	4	2	199	2
FC	531	25	4	2	170	2
FC	266	25	12	2	255	2
ESCON	**200**	**10**	**12**	**1**	**240**	**1**
ESCON	200	25	12	2	192	
STS-3	**155.52**	**19.44**	**16**	**1**	**128**	**1**
STS-3	155.52	25	16	2	199	2
FC	133	25	24	2	255	2
FE	**125**	**12.5**	**16**	**1**	**160**	**1**
FE	125	25	24	2	240	
STS-1	51.84	25	48	2	199	2
STS-1	**51.84**	**19.44**	**48**	**1**	**128**	**1, 2**
DS3	44.736	25	48	2	172	2

NOTES:

1. Bold text denotes standard hardwired rates.
2. Set *LOL_ctrl*_N[0] = 1b, all other bits at default values.

The FLL drives the iFV to iFR, and it is the primary function of the LOLCir to determine when to turn off the FLL, so the CDR can achieve phase lock. The LOLCir uses the frequency difference between iFV and iFR to switch LOL, which turns on and off the secondary FLL. The thresholds where LOL makes a transition are defined as windows. These windows are fixed in the hardwired mode, and programmable in the two-wire interface mode. To prevent LOL from toggling at the thresholds, two windows are used for hysteresis. When LOL = L and the frequency difference exceeds the larger window (WRW), LOL L-to-H occurs to signal an out of lock case. When LOL = H (and LOA = L), the frequency difference is brought within the narrow reference window (NRW), after which LOL makes a H-to-L transition signaling in-lock. If LOA = H when LOL = L, the FLL remains on to keep the VCO locked to the reference, until a signal is present. N_{acq} is defined with *LOL_ctrl*_N [7:5], N_{narrow} is defined with *LOL_ctrl*_N [4:1], and N_{wide} is defined with *LOL_ctrl*_N [0]. The LOLCir averages a large number of transitions before making an LOL decision. This averaging time is referred to as the LOL decision time or DT_{LOL}.

Table 1-12 shows various window sizes for different applications, including the default value in both the hardwired and two-wire serial interface modes.

Table 1-12. LOL Window Size and Decision Time Examples

Condition	N_{acq}	N_{narrow}	N_{wide}	Narrow Window (ppm)	Wide Window (ppm)	Decision Time (µs)
Hardwired mode default	101b	0100b	0b	±1955	±2930	420
Two-wire serial interface mode default	101b	0100b	0b	±1955	±2930	420
iFV = iFR	111b	0010b	1b	±245	±975	1685
Fast lock	010b	0001b	0b	±5860	±7800	56

NOTES:

1. Decision time is calculated with iFR = 19.44 MHz; will scale proportionally with iFR range from 10 to 25 MHz.
2. Above are examples showing ability to tailor windows for data-rates, reference frequencies, and acquisition times.

1.2.15 Ambient Temperature Range Limitations

Table 1-13 summarizes the supported ambient temperature range as a function of data-rate, and indicates when it is required to center the VCO.

Table 1-13. Supported Ambient Temperature Range by Data-Rate

F_{VCO} (GHz)	DR (Gbps)	T_a (°C)	VCO Centering Requirement
2.0 - 2.666	2.0/DRD - 2.666/DRD	-40 - 85	N
2.7 - 2.97	2.7/DRD - 2.97/DRD	0 - 70	N
2.7 - 2.97	2.7/DRD - 2.97/DRD	-40 - 85	Y
3.0 - 3.2	3.0/DRD - 3.2/DRD	0 - 70	Y

F_{VCO} is the VCO frequency, which always lies in the range 2.0 - 3.2 GHz. DR is the data-rate of the input signal, and DRD is the data-rate divider (1, 2, 4, 8, 12, 16, 24, 32, 48) set with *CDR_ctrlB*_N[3:0]. T_a is the ambient temperature supported, which decreases for F_{VCO} > 2.666 GHz. As an example, if the data-rate is 800 Mbps DRD should be set to 4; to lock to this signal the VCO needs to operate at 3.2 GHz. Under these conditions the ambient temperature range supported is 0°C - 70°C, and it is necessary to center the VCO in each of the four lanes.

The VCO tuning range is roughly the same bandwidth as the variation in VCO center frequency between the extremes of the operating temperature range. This issue can be resolved by centering the VCO frequency during the in-circuit testing (ICT) phase prior to shipment of the customer systems.

1. The CDR must be powered up and configured at 25°C - 40°C ambient temperature during ICT.
2. Power up the device and configure the registers via the two-wire interface with the appropriate settings for the application of interest.
3. Read and store the VCO trim code from register MBh[4:0].
4. Every time the device is powered up, this trim code must be forced by setting M0h[0] = 0b then writing the code to MAh[4:0]. This can be done during the same write cycle as when the other registers are configured.

It should be noted that it is not possible to center the VCO in the hardwired mode, it is necessary to program the CDR using the two-wire interface.

1.2.16 Loss of Activity

By default, the LOA detector is enabled and can be disabled by setting *CDR_ctrlA*_N [1] = 0b, where N is the channel number. Loss of activity measures the transition density of data to determine if the data is valid. With SONET data, the transition density is typically 50%, averaged over long periods. During small time intervals, data transition density variations are due to data content, packet headers, stress patterns, etc. In some applications, when data is not present, noise produces rail-to-rail transitions that cause problems with level based detectors. These applications include cascaded CDRs, high-gain crosspoints, as well as modules with optical amplifiers. The data transition density based LOA detector can separate data from random noise, determine false lock at the wrong integer and non-integer data-rate, signal stuck high/low conditions, and determine false lock to re-timed noise. Unlike level based detectors, it cannot determine false lock onto low amplitude data, which is a condition that does not typically occur with backplane applications, and can be handled by the limiting amplifier or pre-amplifier in modules. The LOA window is fixed at ±12.5% from 50%; or alternatively if data with 50% transition density is present, the data-rate frequency can vary by ±12.5% before an LOA L-to-H transition occurs. If the data transition density of valid data falls outside the 37.5 - 62.5% window, the LOA detector must be disabled.

1.2.17 Built-In Self Test (BIST) Overview

The M21012 contains a BIST test pattern generator as well as a test pattern receiver. Both the BIST transmitter (BIST Tx), and BIST receiver (BIST Rx) are designed to operate with fixed patterns. For SONET operation, the PRBS 2^7-1, 2^{15}-1, 2^{23}-1, and 2^{31}-1 test patterns are provided. For 8b/10b testing, the fibre channel CRPAT and CJTPAT standard patterns are supported. In addition, an 8b/10b countdown pattern is also provided; this is the 8b/10b representation of a binary count from 255 to 0, while maintaining 8b/10b running disparity requirements. User programmable 16 bit (SONET) and 20 bit (8b/10b) patterns are also provided; they are typically used to generate short patterns for debug, such as 1100b, as well as 8b/10b idle or control characters. The BIST is designed to reduce system development time, as well as product test costs, and can be used by both the equipment provider as well as the equipment end user.

When enabled, the BIST Rx allows one input from the CDR to enter the BIST receiver. The desired channel to monitor is selected through a control register. The BIST Rx uses the recovered clock and data from the selected CDR to drive the pattern checker. Every time a bit error is received, the error register is incremented. The maximum number of errors is FFh, and all subsequent errors will not be counted. At any time, the error register can be cleared. By keeping track of the time between a clear and a read, a rough BER number can be obtained.

When enabled, the BIST Tx can broadcast the output test pattern to channels 0 and 1 (the BIST Tx and Rx can be used at the same time). The BIST Tx contains an internal clock multiplier (PLL), that can take its input from either the external reference frequency, or from the same CDR that is driving the BIST Rx (only in full-rate mode, DRD = 1).

1.2.18 BIST Test Patterns

The test pattern is selected with *BISTtx_ctrl* [5:2] for the transmitter, and *BISTrx_ctrl* [5:2] for the receiver.

The PRBS patterns generated by the unit are ITU-T 0.151 compliant, and summarized in Table 1-14.

Table 1-14. BIST PRBS Patterns

BISTtx_ctrl **[5:2]** / *BISTrx_ctrl* **[5:2]**	**Pattern**	**Polynomial**
0000b	PRBS 2^7-1	2^7+2^6+1
0001b	PRBS 2^{15}-1	$2^{15}+2^{14}+1$
0010b	PRBS 2^{23}-1	$2^{23}+2^{18}+1$
0011b	PRBS 2^{31}-1	$2^{31}+2^{28}+1$

For 8b/10b data, three patterns are available. The CJTPAT and CRPAT comply with the Fibre Channel T11.2/ Project 1230/Rev10 specifications.

Table 1-15. BIST 8b/10b Patterns

BISTtx_ctrl **[5:2]** / *BISTrx_ctrl* **[5:2]**	**Pattern**
0100b	CJTPAT
0101b	CRPAT
0110b	Countdown

Two user programmable patterns that are 16 bits long (*BISTtx_ctrl* [5:2] = *BISTrx_ctrl* [5:2] = 0111b) and 20 bits long (*BISTtx_ctrl* [5:2] = *BISTrx_ctrl* [5:2] = 1000b) are determined with *BIST_pattern0*, *BIST_pattern1, BIST_pattern2*. Note that the contents of these registers are used by both the BIST Tx and the BIST Rx, if they are setup in this mode.

1.2.19 BIST Receiver (BIST Rx) Operation

The BIST Rx is powered up and enabled by setting *BISTrx_ctrl* [1] = 1b (off by default), resetting the BIST Rx block with *BISTrx_ctrl* [0] = 1b (default), and selecting a pattern with *BISTrx_ctrl* [5:2]. The signal to the BIST Rx is routed from the input of the device, and the BIST Rx can only check one channel at a time. The desired channel to monitor is selected with *BISTrx_chsel* [2:0]. The BIST Rx uses the recovered clock from the CDR to drive the BIST state-machine, thus the CDR must be enabled and locked to data for proper operation. When the data is valid, *BISTrx_ctrl* [6] = 1b is used to clear the error register, and all subsequent errors can be read back through *BISTrx_error*. The BIST Rx automatically synchronizes the input data with the pattern.

1.2.20 BIST Transmitter (BIST Tx) Operation

The BIST Tx is powered up and enabled by setting *BISTtx_ctrl* [1] = 1b (off by default), resetting the BIST Tx block with *BISTtx_ctrl* [0] = 1b (default), and selecting a pattern with *BISTtx_ctrl* [5:2]. The BIST Tx can multicast the test pattern to channels 0 and 1 selected with *BISTtx_chsel* [1:0]. The high-speed clock of the BIST Tx is generated from its own frequency multiplier PLL, that uses a selectable frequency reference determined by *BISTtx_ctrl* [6]. With *BISTtx_ctrl* [6] = 0b (default), the external reference clock is used and typically gives the lowest jitter output. With *BISTtx_ctrl* [6] = 1b the reference clock is derived from the same CDR used to drive the BIST Rx (this feature only works with DRD = 1 for that CDR). In this mode, the BIST Tx output is synchronous with the CDR used in the BIST Rx, however, it contains the low-frequency jitter from the input data. In either case, the BIST Tx PLL needs to

be configured for the proper data-rate. When the PLL is properly configured and locked to the reference, the LOL flag should be low (*BISTtx_alarm* [7]). A bit error can be intentionally inserted into the BIST Tx output, by providing a 0b, 1b, 0b sequence to *BISTtx_ctrl* [7].

The BIST Tx PLL setup is similar to the CDR FRA mode, thus, the description of similar registers for the CDR also applies and will not be repeated here. The desired output data-rate is set with the DRD register (*BISTtx_PLL_ctrlB* [3:0]) and with the VCD register (*BISTtx_PLL_ctrlC* [7:0]). The input reference frequency iFR is the same as for the main CDRs, since the same external reference and reference dividers are used. In the internal CDR case, iFR is $F_{vco,rxcdr}/128$, where $F_{vco,rxcdr}$ is the VCO frequency of the CDR selected by *BISTrx_chsel* [2:0]. Unlike the CDR, the Tx PLL always makes iFR equal to iFV, and *BISTtx_alarm* [7] is used to determine if the Tx PLL is in lock. Like the CDRs, if the output data-rate of the BIST Tx needs to be changed, the BIST Tx requires a soft reset.

1.2.21 Junction Temperature Monitor

An internal junction temperature monitor with a range of –40°C to 130°C is integrated into the M21012. On the low end, the temperature monitor (Tmon) is set to measure –40°C to 10°C in six 10°C steps, and on the high end, 80°C to 130°C in six 10°C steps. The typical temperature resolution is 3°C. The temperature monitor is enabled with *Temp_mon* [1] = 1b. When enabled, the temperature measurement cycle is achieved by providing a rising edge for *Temp_mon* [0]. Afterwards, the correct temperature can be read from *Temp_value* [3:0]. Table 1-16 shows the mapping of the temperature to *Temp_value* [3:0]. Enabling and strobing the temperature in the same write cycle will not yield reliable results.

Table 1-16. Junction Temperature Monitor

Junction Temperature	*Temp_value* [3:0]	Condition
$T_j \geq 130°C$	1100b	High-alarm
$130°C > T_j \geq 120°C$	1011b	High-alarm
$120°C > T_j \geq 110°C$	1010b	High-warning
$110°C > T_j \geq 100°C$	1001b	Normal
$100°C > T_j \geq 90°C$	1000b	Normal
$90°C > T_j \geq 80°C$	0111b	Normal
$80°C > T_j \geq 10°C$	0110b	Normal
$10°C > T_j \geq 0°C$	0101b	Normal
$0°C > T_j \geq -10°C$	0100b	Normal
$-10°C > T_j \geq -20°C$	0011b	Normal
$-20°C > T_j \geq -30°C$	0010b	Low-warning
$-30°C > T_j \geq -40°C$	0001b	Low-alarm
$-40°C > T_j$	0000b	Low-alarm

1.2.22 IC Identification / Revision Code

The IC identification can be read back from *Chipcode,* and the revision of the device can be read back from *Revcode*. The assigned IC identification for the M21012 is 12h, for the M21011 is 11h, for the M21001 is 10h, and the revision code is 20h.

1.3 Pin Definitions

Table 1-17. Power Pins

Pin Name	Function	Type
Vss	IC ground	Power
AVdd_I/O	Analog I/O positive supply	Power
AVdd_Core	Analog core positive supply	Power
DVdd_I/O	Digital I/O positive supply	Power
DVdd_Core	Digital core positive supply	Power

NOTES:

1. If internal regulator is enabled, connect all of the ***AVdd_Core*** and/or ***DVdd_Core*** pins together to a common floating plane and bypass to ***Vss***.
2. If internal regulator is NOT enabled, it is recommended that all ***AVdd_Core*** pins be tied to a plane at 1.2V, that is bypassed to ground. ***DVdd_Core*** can be tied to this plane or separately decoupled.
3. IC ground (***Vss***) is established by contact with exposed pad on underside of package; there are no ***Vss*** pins.

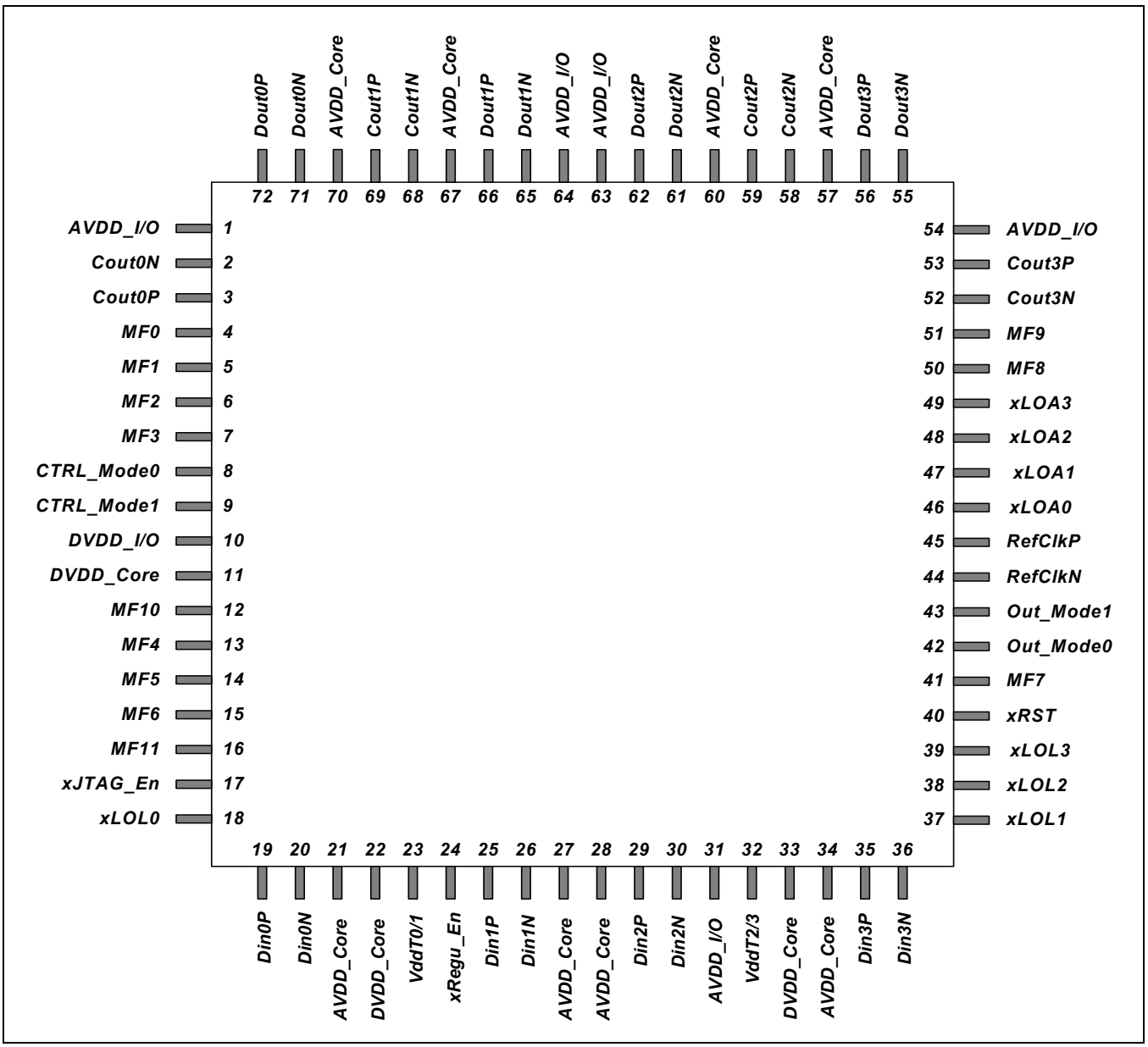
Table 1-18. High-Speed Signal Pins

Pin Name	Function	Termination	Type
Din0P	Serial positive data input for channel 0	50Ω pull up to ***VddT0/1***	I - universal
Din0N	Serial negative data input for channel 0	50Ω pull up to ***VddT0/1***	I - universal
Din1P	Serial positive data input for channel 1	50Ω pull up to ***VddT0/1***	I - universal
Din1N	Serial negative data input for channel 1	50Ω pull up to ***VddT0/1***	I - universal
Din2P	Serial positive data input for channel 2	50Ω pull up to ***VddT2/3***	I - universal
Din2N	Serial negative data input for channel 2	50Ω pull up to ***VddT2/3***	I - universal
Din3P	Serial positive data input for channel 3	50Ω pull up to ***VddT2/3***	I - universal
Din3N	Serial negative data input for channel 3	50Ω pull up to ***VddT2/3***	I - universal
VddT0/1	Termination pin for ***Din*** [1:0]	Terminate to ***AVdd_I/O***	I - termination
VddT2/3	Termination pin for ***Din*** [3:2]	Terminate to ***AVdd_I/O***	I - termination
Dout0P	Serial positive data output for channel 0	50Ω pull up to ***AVdd_I/O***	O - CML/LVDS
Dout0N	Serial negative data output for channel 0	50Ω pull up to ***AVdd_I/O***	O - CML/LVDS
Dout1P	Serial positive data output for channel 1	50Ω pull up to ***AVdd_I/O***	O - CML/LVDS
Dout1N	Serial negative data output for channel 1	50Ω pull up to ***AVdd_I/O***	O - CML/LVDS
Dout2P	Serial positive data output for channel 2	50Ω pull up to ***AVdd_I/O***	O - CML/LVDS
Dout2N	Serial negative data output for channel 2	50Ω pull up to ***AVdd_I/O***	O - CML/LVDS
Dout3P	Serial positive data output for channel 3	50Ω pull up to ***AVdd_I/O***	O - CML/LVDS
Dout3N	Serial negative data output for channel 3	50Ω pull up to ***AVdd_I/O***	O - CML/LVDS
Cout0P	Serial positive clock output for channel 0	50Ω pull up to ***AVdd_I/O***	O - CML/LVDS
Cout0N	Serial negative clock output for channel 0	50Ω pull up to ***AVdd_I/O***	O - CML/LVDS
Cout1P	Serial positive clock output for channel 1	50Ω pull up to ***AVdd_I/O***	O - CML/LVDS
Cout1N	Serial negative clock output for channel 1	50Ω pull up to ***AVdd_I/O***	O - CML/LVDS
Cout2P	Serial positive clock output for channel 2	50Ω pull up to ***AVdd_I/O***	O - CML/LVDS
Cout2N	Serial negative clock output for channel 2	50Ω pull up to ***AVdd_I/O***	O - CML/LVDS
Cout3P	Serial positive clock output for channel 3	50Ω pull up to ***AVdd_I/O***	O - CML/LVDS
Cout3N	Serial negative clock output for channel 3	50Ω pull up to ***AVdd_I/O***	O - CML/LVDS
RefClkP	Reference clock positive input	Internal pull down	I - AC coupled
RefClkN	Reference clock negative input	Internal pull down	I - AC coupled

Table 1-19. Control, Interface, and Alarm Pins

Pin Name	Function	Default	Type
MF0	Multifunction pin for hardwired mode, and serial interface	Internal pull up	I - CMOS
MF1	Multifunction pin for hardwired mode, and serial interface	Internal pull up	I - CMOS
MF2	Multifunction pin for hardwired mode, and serial interface	Internal pull up	I - CMOS
MF3	Multifunction pin for hardwired mode, and serial interface	Internal pull up	I - CMOS
MF4	Multifunction pin for hardwired mode, and serial interface	Internal pull up	I - CMOS
MF5	Multifunction pin for hardwired mode, and serial interface	Internal pull up	I - CMOS
MF6	Multifunction pin for hardwired mode, and serial interface	Internal pull up	I - CMOS
MF7	Multifunction pin for hardwired mode	Internal pull up	I - CMOS
MF8	Multifunction pin for hardwired mode, and JTAG	Internal pull up	I - CMOS
MF9	Multifunction pin for hardwired mode, and JTAG	Internal pull up	I - CMOS
MF10	Multifunction pin for hardwired mode, serial interface, and JTAG	Internal pull up	I - CMOS
MF11	Multifunction pin for hardwired mode, serial interface, and JTAG	Internal pull up	I - CMOS
CTRL_Mode0	Hardwired or two-wire serial interface mode control pin	Internal pull up	I - CMOS
CTRL_Mode1	Hardwired or two-wire serial interface mode control pin	Internal pull up	I - CMOS
Out_Mode0	Output data interface control pin	Internal pull down	I - CMOS
Out_Mode1	Output data interface control pin	Internal pull down	I - CMOS
xRST	Reset pin (L = reset)	Internal pull up	I - CMOS
xJTAG_En	JTAG testing control pin (L = enable)	Internal pull up	I - CMOS
xRegu_En	Internal voltage regulator control pin (L = enable)	Internal pull up	I - CMOS
xLOA0	Loss of activity alarm pin for channel 0 (L = LOA)	No internal pull up/down	O - open drain
xLOA1	Loss of activity alarm pin for channel 1 (L = LOA)	No internal pull up/down	O - open drain
xLOA2	Loss of activity alarm pin for channel 2 (L = LOA)	No internal pull up/down	O - open drain
xLOA3	Loss of activity alarm pin for channel 3 (L = LOA)	No internal pull up/down	O - open drain
xLOL0	Loss of lock alarm pin for CDR at channel 0 (L = LOL)	No internal pull up/down	O - open drain
xLOL1	Loss of lock alarm pin for CDR at channel 1 (L = LOL)	No internal pull up/down	O - open drain
xLOL2	Loss of lock alarm pin for CDR at channel 2 (L = LOL)	No internal pull up/down	O - open drain
xLOL3	Loss of lock alarm pin for CDR at channel 3 (L = LOL)	No internal pull up/down	O - open drain

Figure 1-8. M21012 Pinout Diagram (Top View)



2.0 Product Specifications

2.1 Absolute Maximum Ratings

These are the absolute maximum ratings beyond which the device can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not warranted.

Table 2-1. Absolute Maximum Ratings

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DVdd_I/O	Digital I/O power		0	1.8/2.5/3.3	3.6	V
AVdd_I/O	Analog I/O power		0	1.8/2.5/3.3	3.6	V
AVdd_Core	Analog core power	2	0	1.2	1.5	V
DVdd_Core	Digital core power	2	0	1.2	1.5	V
—	High-speed signal pins	3	***Vss*** - 0.5	—	***AVdd_I/O*** + 0.5	V
—	Control, interface, and alarm pins	4	***Vss*** - 0.5	—	***DVdd_I/O*** + 0.5	V
T_{st}	Storage temperature		–65	—	+150	°C
ESD	Human body model (low-speed)		2000	—	—	V
ESD	Human body model (high-speed)		1000	—	—	V
ESD	Charged device model		100	—	—	V

NOTES:

1. No damage under typical conditions.
2. Apply voltage to core pins if internal regulator is disabled. If enabled, pins should be floating with by-pass to ***Vss***.
3. High-speed signal pins are shown in Table 1-18.
4. Control, interface, and alarm pins are shown in Table 1-19.

2.2 Recommended Operating Conditions

Table 2-2. Recommended Operating Conditions

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DVdd_I/O	Digital I/O power	2	—	1.8/2.5/3.3	—	V
AVdd_I/O	Analog I/O power	2	—	1.8/2.5/3.3	—	V
AVdd_Core	Analog core power	1, 2	—	1.2	—	V
DVdd_Core	Digital core power	1, 2	—	1.2	—	V
T_a	Ambient temperature	4	- 40	—	85	°C
θ_{ja}	Junction to ambient thermal resistance	3	—	24	—	°C/W

NOTES:

1. Needed only if ***AVdd_Core*** or ***DVdd_Core*** are provided from external source (internal regulator disabled ***xRegu_En*** = H).
2. Typical value +/- 5% is acceptable.
3. With forced convection of 1 m/s and 2.5 m/s, θ_{ja} is decreased to 18°C/W and 16°C/W respectively.
4. This temperature range is supported when the VCO operates between 2.0 - 2.666 GHz, or for data rates between 2.0/DRD - 2.666/DRD Gbps, where DRD = data-rate divider. For higher data-rates, T_a is supported in the range 0°C - 70°C and the device should be powered up and configured at room temperature. For details, see Section 1.2.15.

2.3 Power Dissipation

Table 2-3. DC Power Electrical Specifications (1 of 2)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
Idd	Case 1: current consumption for output swing = 600 mV CML, internal regulator = on, clock outputs = off	1	—	310	365	mA
Pdiss	Power dissipation at 1.8V	—	—	560	660	mW
Pdiss	Power dissipation at 3.3V	2	—	1.02	1.2	W
Idd	Case 2: current consumption for output swing = 600 mV CML, internal regulator = on, clock outputs = on	1	—	370	435	mA
Pdiss	Power dissipation at 1.8V	—	—	670	780	mW
Pdiss	Power dissipation at 3.3V	2	—	1.22	1.44	W
Idd	Case 3: current consumption for output swing = 1V CML, internal regulator = on, clock outputs = off	1	—	340	400	mA
Pdiss	Power dissipation at 1.8V	—	—	610	720	mW
Pdiss	Power dissipation at 3.3V	2	—	1.12	1.32	W
Idd	Case 4: current consumption for output swing = 1V CML, internal regulator = on, clock outputs = on	1	—	420	490	mA
Pdiss	Power dissipation at 1.8V	—	—	760	880	mW
Pdiss	Power dissipation at 3.3V	2	—	1.39	1.62	W

Table 2-3. DC Power Electrical Specifications (2 of 2)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
	Case 5: output swing = 600 mV CML, internal regulator = off, clock outputs = off	1				
Idd_core	Core current consumption	—	—	260	300	mA
Idd_io	Input/Output buffers current consumption	—	—	50	70	mA
Pdiss	Power dissipation at 1.2V core, 1.8V I/O	—	—	400	490	mW
Pdiss	Power dissipation at 1.2V core, 3.3V I/O	—	—	480	590	mW
	Case 6: output swing = 600 mV CML, internal regulator = off, clock outputs = on	1				
Idd_core	Core current consumption	—	—	285	330	mA
Idd_io	Input/Output buffers current consumption	—	—	100	125	mA
Pdiss	Power dissipation at 1.2V core, 1.8V I/O	—	—	520	620	mW
Pdiss	Power dissipation at 1.2V core, 3.3V I/O	—	—	670	810	mW
Idd	Case 7: current consumption for output swing = 450 mV LVDS, internal regulator = on, clock outputs = off	1	—	320	380	mA
Pdiss	Power dissipation at 1.8V	—	—	580	680	mW
Pdiss	Power dissipation at 3.3V	2	—	1.06	1.25	W
Idd	Case 8: current consumption for output swing = 1.6V PCML+, internal regulator = on, clock outputs = off	1	—	410	470	mA
Pdiss	Power dissipation at 1.8V	—	—	740	850	mW
Pdiss	Power dissipation at 3.3V	2	—	1.35	1.55	W

NOTES:

1. Specified at recommended operating conditions – see Table 2-2.
2. Thermal design such as thermal pad vias on PCB must be considered for this case.

2.4 Input/Output Specifications

Table 2-4. Two-Wire Serial Interface CMOS I/O Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
V_{OH}	Output logic high I_{OH} = –3 mA	2	0.8 x ***DVdd_I/O***	***DVdd_I/O***	—	V
V_{OL}	Output logic low I_{OL} = 24 mA	2	—	0.0	0.2 x ***DVdd_I/O***	V
I_{OL}	Output current (logic low)	—	10	—	—	mA
V_{IH}	Input logic high	—	0.75 x ***DVdd_I/O***	—	3.6	V
V_{IL}	Input logic low	—	0	—	0.25 x ***DVdd_I/O***	V
I_{IH}	Input current (logic high)	—	–100	—	100	µA
I_{IL}	Input current (logic low)	—	–100	—	100	µA
t_r	Output rise time (20-80%)	—	—	—	5	ns
t_f	Output fall time (20-80%)	—	—	—	5	ns
C2wire	Input capacitance of ***MF10*** & ***MF11*** in two-wire serial mode	3	—	—	10	pF

NOTES:

1. Specified at recommended operating conditions – see Table 2-2.
2. ***DVdd_I/O*** can be chosen independently from ***AVdd_I/O***.
3. Two-wire serial output mode can drive 500 pF.

Table 2-5. Universal High-Speed (UHS) Input Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{IN}	Input signal data-rate	3	42	—	3200	Mbps
V_{ID}	Input differential voltage (P-P)	4,5	100	—	2000	mV
V_{ICM}	Input common-mode voltage	—	***Vss***	—	***AVdd_I/O***	mV
V_{IH}	Maximum input high voltage	—	—	—	***AVdd_I/O*** + 400	mV
V_{IL}	Minimum input low voltage	—	***Vss*** - 400	—	—	mV
—	Maximum voltage difference between common-mode voltage and ***VddT***	—	—	—	600	mV
R_{IN}	Input termination to ***VddT***	7	45	50	65	Ω
S_{11}	Input return loss (40 MHz to 2.5 GHz)	—	—	–15.0	—	dB
S_{11}	Input return loss (2.5 GHz to 5 GHz)	—	—	–5.0	—	dB
—	Maximum DC input current	6	—	—	25	mA

NOTES:

1. Specified at recommended operating conditions – see Table 2-2.
2. Designed for seamless interface to PCML.
3. Designed for SONET and 8b/10b data.
4. Example 1200 mV_{pp} differential = 600 mV_{pp} for each single-ended terminal.
5. Minimum input level defined as error free operation at 10^{-12} BER.
6. Computed as the current through 50Ω from the voltage difference between the input voltage common mode and ***VddT.***
7. See Figure 2-1 for input termination circuit.

Figure 2-1. Data Input Internal Circuitry

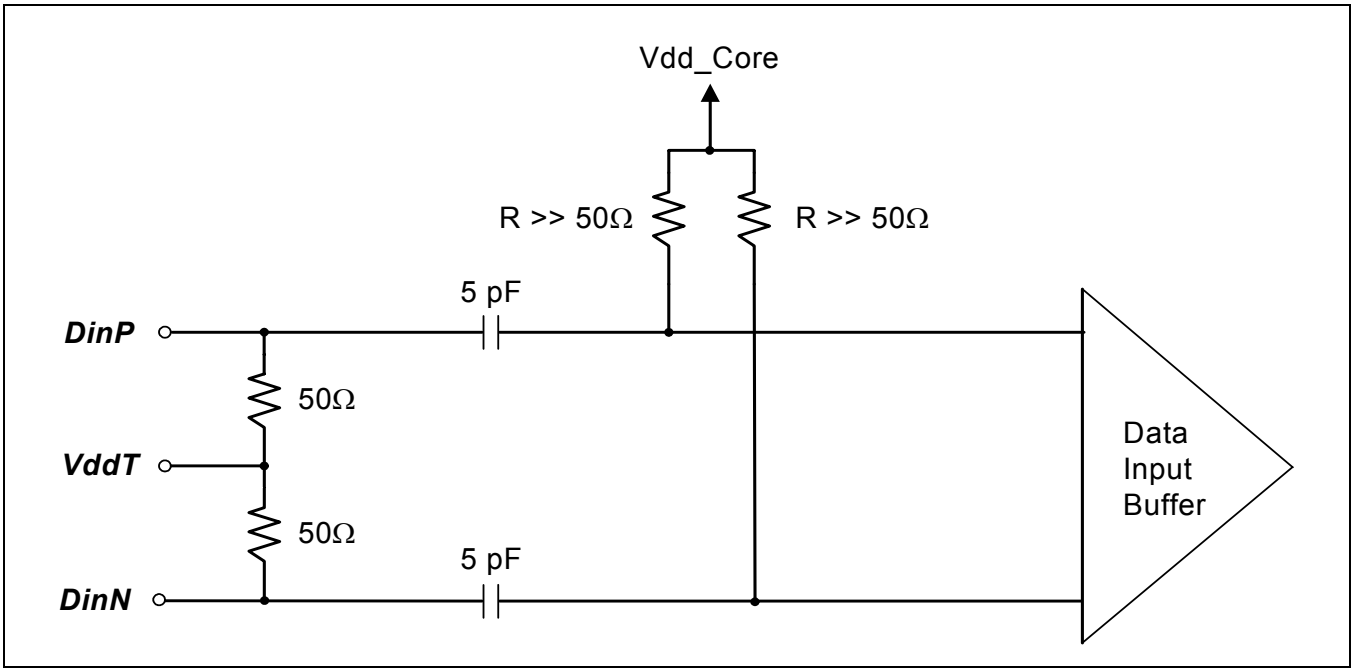


Table 2-6. PCML (Positive Current Mode Logic) Output Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{OUT}	Output signal data-rate	—	42	—	3200	Mbps
t_r/t_f	Rise/Fall time (20-80%) for all levels	—	—	75	130	ps
V_{OH}	Low swing: output logic high (single-ended)	—	***AVdd_I/O*** – 25	—	***AVdd_I/O***	mV
V_{OL}	Low swing: output logic low (single-ended)	—	***AVdd_I/O*** – 370	—	***AVdd_I/O*** – 260	mV
V_{OD}	Low swing: differential swing	2	500	600	700	mV
V_{OH}	Medium swing: output logic high (single-ended)	—	***AVdd_I/O*** – 30	—	***AVdd_I/O***	mV
V_{OL}	Medium swing: output logic low (single-ended)	—	***AVdd_I/O*** – 600	—	***AVdd_I/O*** – 440	mV
V_{OD}	Medium swing: differential swing	2	800	1000	1200	mV
CV_{OD}	Clock output differential swing: medium setting	2	640	—	—	mV
V_{OH}	High swing: output logic high (single-ended)	—	***AVdd_I/O*** – 30	—	***AVdd_I/O***	mV
V_{OL}	High swing: output logic low (single-ended)	—	***AVdd_I/O*** – 770	—	***AVdd_I/O*** – 550	mV
V_{OD}	High swing: differential swing	2	1000	1300	1500	mV
V_{OH}	PCML+ swing: output logic high (single-ended)	—	***AVdd_I/O*** – 35	—	***AVdd_I/O***	mV
V_{OL}	PCML+ swing: output logic low (single-ended)	—	***AVdd_I/O*** – 1000	—	***AVdd_I/O*** – 700	mV
V_{OD}	PCML+ swing: differential swing	2	1300	1600	2000	mV
R_{OUT}	Output termination to ***AVdd_I/O***	—	45	50	65	Ω
S_{22}	Output return loss (40 MHz to 2.5 GHz)	—	—	–15.0	—	dB
S_{22}	Output return loss (2.5 GHz to 5 GHz)	—	—	–5.0	—	dB

NOTES:

1. Specified at recommended operating conditions – see Table 2-2.
2. Example 1200 mV $_{P-P}$ differential = 600 mV $_{P-P}$ for each single-ended terminal.
3. All output swings defined with pre-emphasis off.
4. Clock output swing is typically 20% less than data output swing, and clock output rise/fall time is typically 30% less than data output rise/fall time.

Table 2-7. LVDS (Low Voltage Differential Signal) Output Electrical Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{OUT}	Output signal data-rate	—	42	—	800	Mbps
V_{OCM}	Output average common mode range	2	1125	—	1275	mV
t_r/t_f	GPL: rise/fall time (20-80%)	—	—	75	130	ps
V_{OD}	GPL: differential output (P-P)	3	500	650	800	mV
V_{OD}	RRL: differential output (P-P)	—	300	450	550	mV
R_{OUT}	Output termination (differential)	—	90	100	130	Ω
S_{22}	Output return loss (40 MHz to 2.5 GHz)	—	—	–15.0	—	dB
S_{22}	Output return loss (2.5 GHz to 5 GHz)	—	—	–5.0	—	dB

NOTES:

1. Specified at recommended operating conditions - see Table 2-2.
2. Computed as average (average positive output and average negative output).
3. Conforms to IEEE Std 1596.3-1996 for GPL. All values specified for 50Ω single-ended back-match, 100Ω differential load.
4. All output swings defined with pre-emphasis off.
5. Clock output swing is typically 10% less than data output swing, and clock output rise/fall time is typically 20% less than data output rise/fall time.

Table 2-8. Input Equalization Performance Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{IN}	Input signal data-rate	—	42	—	3200	Mbps
—	Maximum error-free distance at 3.1875 Gbps	2, 3, 6	—	—	60	in
—	Maximum error-free distance at 2.125 Gbps	2, 3, 6	—	—	72	in

NOTES:

1. Specified at recommended operating conditions – see Table 2-2.
2. Performance measured on standard FR4 backplane such as standards provided by TYCO for 10GE XAUI.
3. Measured with PCML driver without output pre-emphasis at a minimum launch voltage of 1 Vpp output swing at beginning of line.
4. Combined input equalization + output pre-emphasis performance will be better than individual performance, but less than the sum of the two lengths.
5. Input equalization has greatest effect for data-rates higher than 1 Gbps.
6. Default setting optimized for driving 10 - 46 in of PCB trace length. Equalizer can be configured for longer reach using two-wire interface.
7. Test setup: pattern generator → test backplane → DUT → error detector.

Table 2-9. Output Pre-Emphasis Performance Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{OUT}	Output signal data-rate	—	42	—	3200	Mbps
—	Maximum error-free distance at 3.1875 Gbps	2	—	—	40	in
—	Maximum error-free distance at 2.125 Gbps	2	—	—	60	in

NOTES:

1. Specified at recommended operating conditions – see Table 2-2.
2. Performance measured on standard FR4 backplane such as standards provided by TYCO for 10GE XAUI.
3. Measured with PCML receiver without input equalization, using PCML output driver at 1300 mVpp output swing at beginning of line.
4. Combined input equalization + output pre-emphasis performance will be better than individual performance, but less than the sum of the two lengths.
5. Output pre-emphasis has greatest effect for data-rates higher than 1 Gbps.
6. Test setup: pattern generator → DUT → test backplane → error detector.

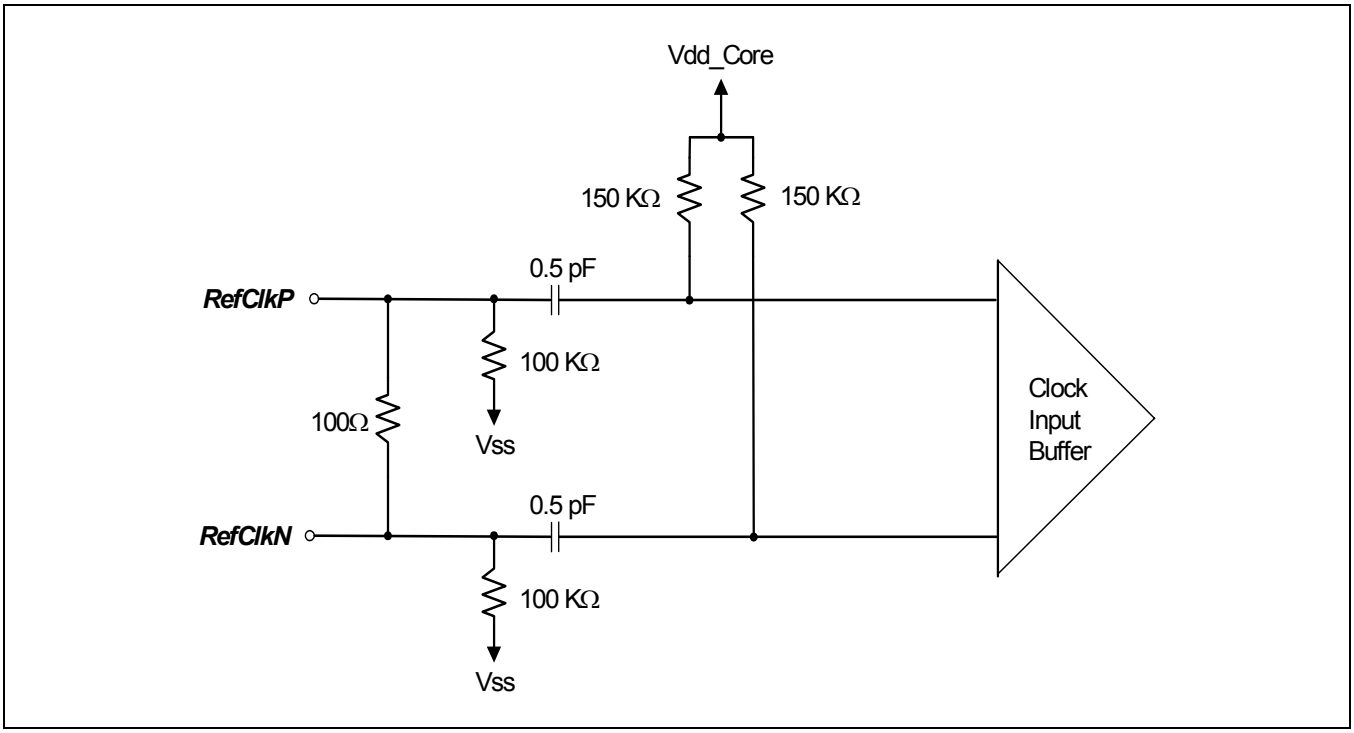
Table 2-10. Reference Clock Input

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
F_{ref}	Input frequency (*Refclk_ctrl* [3:1] = 000b)	2,3	10	19.44	25	MHz
F_{ref}	Input frequency (*Refclk_ctrl* [3:1] = 001b)	2,3	20	38.88	50	MHz
F_{ref}	Input frequency (*Refclk_ctrl* [3:1] = 010b)	2,3	40	77.76	100	MHz
F_{ref}	Input frequency (*Refclk_ctrl* [3:1] = 011b)	2,3	80	155.52	200	MHz
F_{ref}	Input frequency (*Refclk_ctrl* [3:1] = 100b)	2	120	250	300	MHz
F_{ref}	Input frequency (*Refclk_ctrl* [3:1] = 101b)	2,3	160	311.04	400	MHz
F_{ref}	Input frequency (*Refclk_ctrl* [3:1] = 110b)	2,3	320	622.08	800	MHz
V_{ID}	Input differential voltage (P-P)	4,5	100	—	1600	mV
V_{ICM}	Input common-mode voltage	2,5	250	—	***AVdd_I/O***	mV
—	Input duty cycle	—	40	50	60	%
—	Frequency stability	2	—	—	100	ppm
R_{IN}	Differential termination	5	—	100	—	Ω
—	Internal pull-down to ***Vss***	—	—	100	—	KΩ
—	Maximum DC input current	—	—	—	15	mA

NOTES:

1. Specified at recommended operation conditions – see Table 2-2.
2. Used for frequency reference CDR acquisition.
3. Typical values are exact integer ratios for SONET applications.
4. Example 1200 mV_{pp} differential = 600 mV_{pp} for each single-ended terminal.
5. Input can accept a CMOS single-ended clock on differential P terminal when differential N terminal is decoupled to ground with a large enough capacitor. CMOS input will then see an effective 100Ω load.
6. See Figure 2-2 for input termination circuit.

Figure 2-2. Reference Clock Input Internal Circuitry



2.5 CDR Performance Specifications

Table 2-11. CDR High-Speed Performance (1 of 3)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DR_{IN}	Input signal data-rate (NRZ data) divider ratio = 1	—	2	—	3.2	Gbps
DR_{IN}	Input signal data-rate (NRZ data) divider ratio = 2	—	1	—	1.6	Gbps
DR_{IN}	Input signal data-rate (NRZ data) divider ratio = 4	—	500	—	800	Mbps
DR_{IN}	Input signal data-rate (NRZ data) divider ratio = 8	—	250	—	400	Mbps
DR_{IN}	Input signal data-rate (NRZ data) divider ratio = 12	—	167	—	267	Mbps
DR_{IN}	Input signal data-rate (NRZ data) divider ratio = 16	—	125	—	200	Mbps
DR_{IN}	Input signal data-rate (NRZ data) divider ratio = 24	—	83	—	133	Mbps
DR_{IN}	Input signal data-rate (NRZ data) divider ratio = 32	—	62.5	—	100	Mbps
DR_{IN}	Input signal data-rate (NRZ data) divider ratio = 48	—	42	—	67	Mbps
J_{TOL}	Jitter tolerance (Figure 2-4)	2	—	0.625	—	UI
J_{TRF}	Jitter transfer (Figure 2-5)	2, 16	—	—	—	—
J_{GEN}	Jitter generation (rms) at STS-N (N = 1, 3, 12, 48)	2, 12	—	4.5	6.5	mUI
J_{GEN}	Jitter generation (pp) at STS-N (N = 1, 3, 12, 48)	2, 12	—	30	55	mUI

Table 2-11. CDR High-Speed Performance (2 of 3)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
F_{LBW}	Default loop bandwidth: divider ratio = 1	3,4,5	—	—	2	MHz
F_{LBW}	Default loop bandwidth: divider ratio = 2	3,4,5	—	—	1	MHz
F_{LBW}	Default loop bandwidth: divider ratio = 4	3,4,5	—	—	500	KHz
F_{LBW}	Default loop bandwidth: divider ratio = 8	3,4,5	—	—	250	KHz
F_{LBW}	Default loop bandwidth: divider ratio = 12	3,4,5	—	—	167	KHz
F_{LBW}	Default loop bandwidth: divider ratio = 16	3,4,5	—	—	125	KHz
F_{LBW}	Default loop bandwidth: divider ratio = 24	3,4,5	—	—	83	KHz
F_{LBW}	Default loop bandwidth: divider ratio = 32	3,4,5	—	—	62.5	KHz
F_{LBW}	Default loop bandwidth: divider ratio = 48	3,4,5	—	—	41.6	KHz
R_j	Output data random jitter (pp)	13	—	—	100	mUI
D_j	Output data deterministic jitter (pp)	13	—	—	110	mUI
T_j	Output data total jitter (pp)	13	—	—	210	mUI
J_{rms}	Output data broadband jitter (rms)	14, 15	—	13	40	mUI
J_{pp}	Output data broadband jitter (pp)	14, 15	—	75	230	mUI
T_{SK}	Delay from falling edge of positive clock output to data transition (Figure 2-3)	—	-50	—	50	ps
J_{rms}	Output clock broadband jitter (rms)	14, 15	—	13	40	mUI
J_{pp}	Output clock broadband jitter (pp)	14, 15	—	75	230	mUI
C_{DC}	Output clock duty cycle	—	45	50	55	%
D_{DC}	Output data duty cycle	—	45	50	55	%
T_{LAT}	Latency from input to output (utilizing CDR)	—	—	1.75	2	ns

Table 2-11. CDR High-Speed Performance (3 of 3)

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
CH_{SK}	Channel to channel output data skew (utilizing CDR)	—	—	10	65	ps
—	Initialization time	6,7,10		2	—	ms
T_{FRA}	Frequency acquisition time	6,8		0.4	—	ms
T_{PLL}	Phase lock time with 100 ppm delta F	9,11			100	ns
T_{PLL}	Phase lock time with 0 ppm delta F	9,11			50	ns

NOTES:

1. Specified at recommended operating conditions – see Table 2-2.
2. Jitter tolerance, jitter transfer, and jitter generation specified with input equalization and output pre-emphasis disabled, utilizing PRBS 2^{23}-1, per GR-253 test methodologies.
3. Nominal loop bandwidth for 2.48832 GHz/ DRD.
4. Bandwidth is proportional to frequency.
5. For SONET data-rates, default meets SONET specifications.
6. Assume that reference is within +/-100 ppm of desired data-rate.
7. Time after power up, reset, or data-rate change.
8. Time from application of valid data to lock within +/-20% of lock phase.
9. Defined as when phase settles to within 20% of lock phase.
10. After reset (master or soft), initialization takes place, then frequency acquisition.
11. Based on nominal SONET bandwidth (bandwidth can be increased for lower phase lock time).
12. Jitter generation specified per GR-253, utilizing bandpass filter with passband 12 KHz to 20 MHz for STS-48.
13. R_j, D_j, T_j represent jitter measured to BER of 10^{-12} per FC-PI-2 specifications.
14. Broadband jitter defined as jitter measured on sampling oscilloscope without the use of filters.
15. Maximum value specified incorporates asynchronous aggressors.
16. Jitter transfer of CDR meets the SONET STS-48 mask if loop bandwidth is set to 80% of nominal by writing *Phadj_ctrl*_N[5:4] = 00b. Jitter transfer at STS-12 (STS-3) exceeds mask by 0.1 dB in frequency range 10 - 25.1 KHz (1.5 - 10 KHz).

Figure 2-3. Clock to Data Output Skew Timing

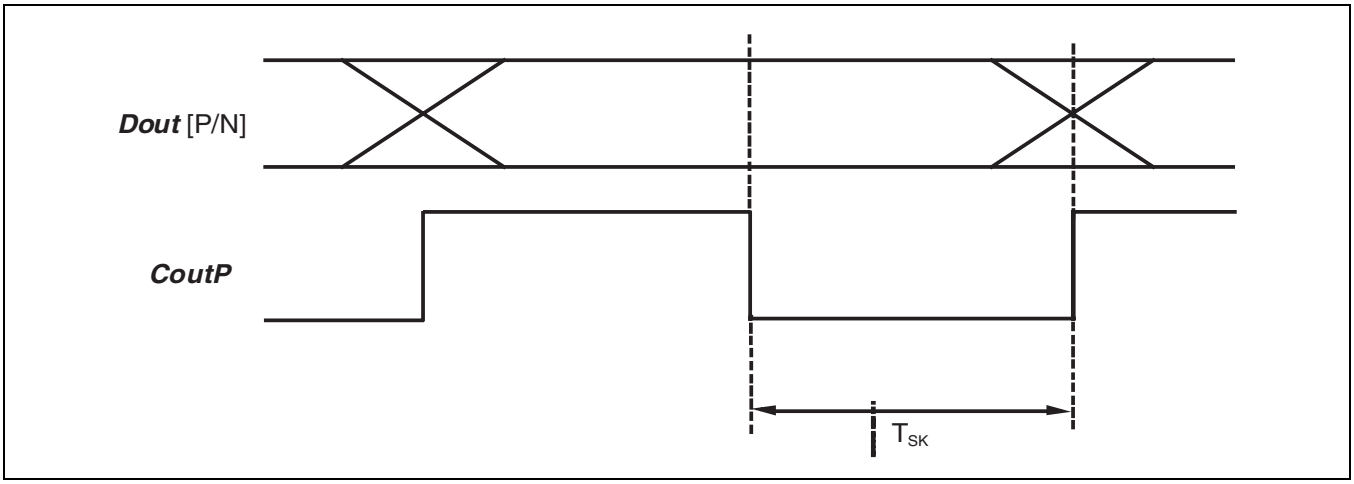


Figure 2-4. Jitter Tolerance Specification Mask

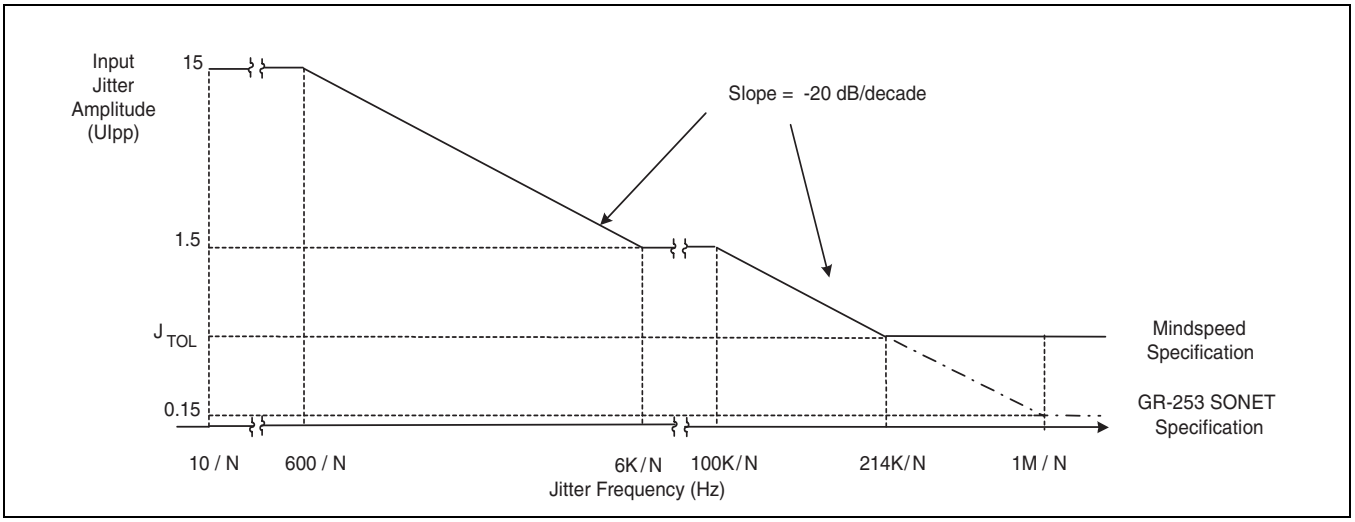


Figure 2-5. Jitter Transfer Specification Mask

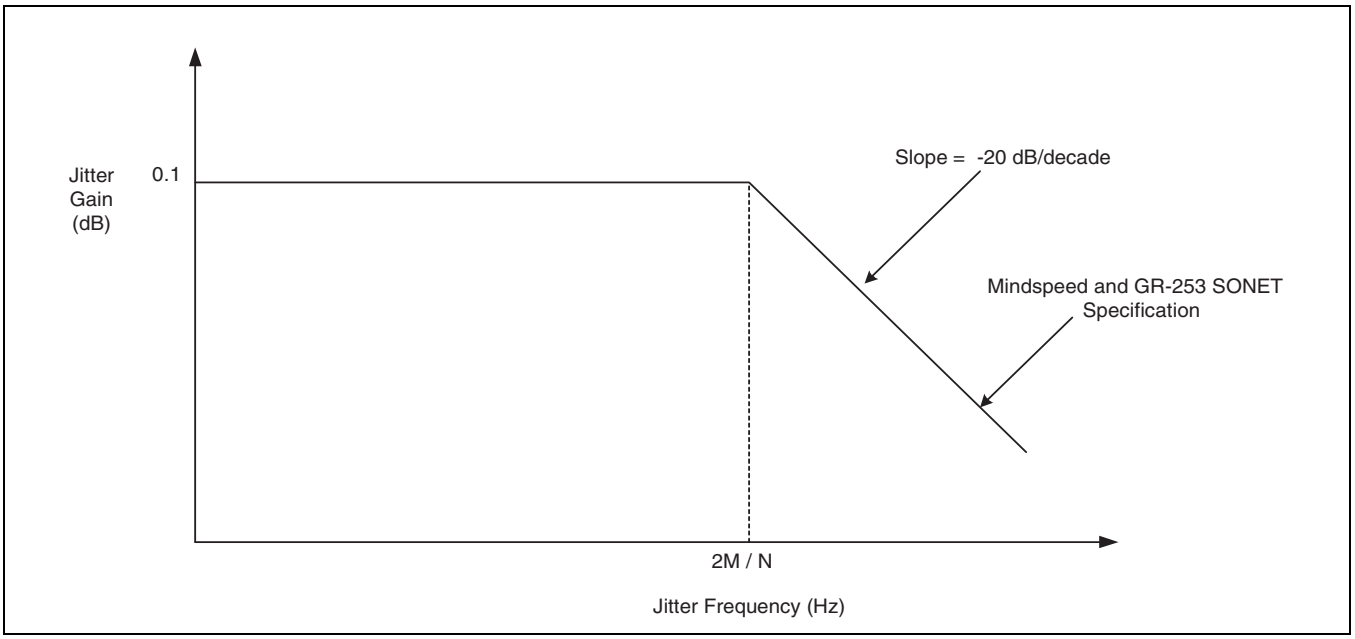


Table 2-12. CDR Alarm Performance

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
DT_{LOA}	***xLOA*** decision time	5	—	26	—	µs
—	***xLOA*** assertion transition density threshold (***xLOA*** = H to L)	5, 6	—	12.5	—	%
—	***xLOA*** de-assertion transition density threshold (***xLOA*** = L to H)	5, 6	—	12.5	—	%
DT_{LOL}	***xLOL*** decision time (measurement time)	2	10	420	3275	µs
WRW	***xLOL*** assertion frequency threshold (***xLOL*** = H to L)	2,3	±185	±2930	±250000	ppm
NRW	***xLOL*** de-assertion frequency threshold (***xLOL*** = L to H)	2,3	±120	±1955	±250000	ppm

NOTES:

1. Specified at recommended operating conditions – see Table 2-2.
2. Actual time is set with LOL window. Typical is the default value. Minimum and maximum indicate dynamic range.
3. Assume that reference is +/-100 ppm of operating frequency.
4. Computed for 2.48832 Gbps data-rate. Will scale with data-rate.
5. Fixed values.
6. Specification shown represents deviation from 50% transition density.

2.6 Package Drawings and Surface Mount Assembly Details

The M21012 is assembled in 72-pin 10 mm x 10 mm MicroLeadFrame (MLF) packages. This is a plastic encapsulated package with a copper leadframe. The MLF is a leadless package with lands on the bottom surface of the package.

The exposed die paddle serves as the IC ground (***Vss***), and the primary means of thermal dissipation. This die paddle should be soldered to the PCB. A cross-section of the MLF package can be found in Figure 2-6.

Figure 2-6. Cross-Section of MLF Package

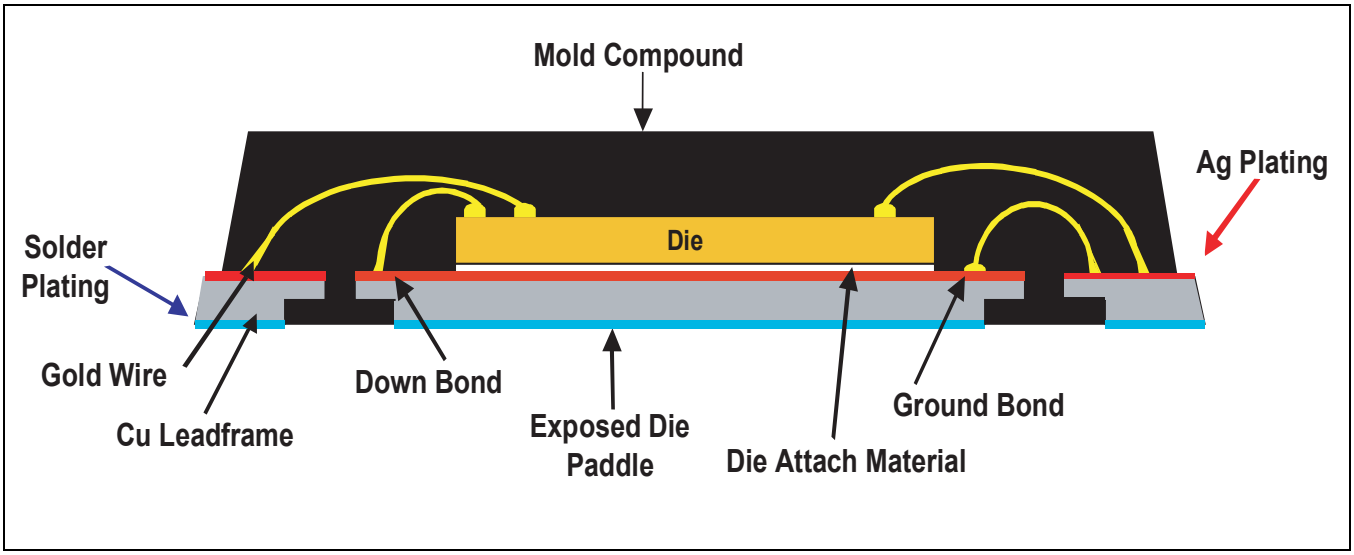
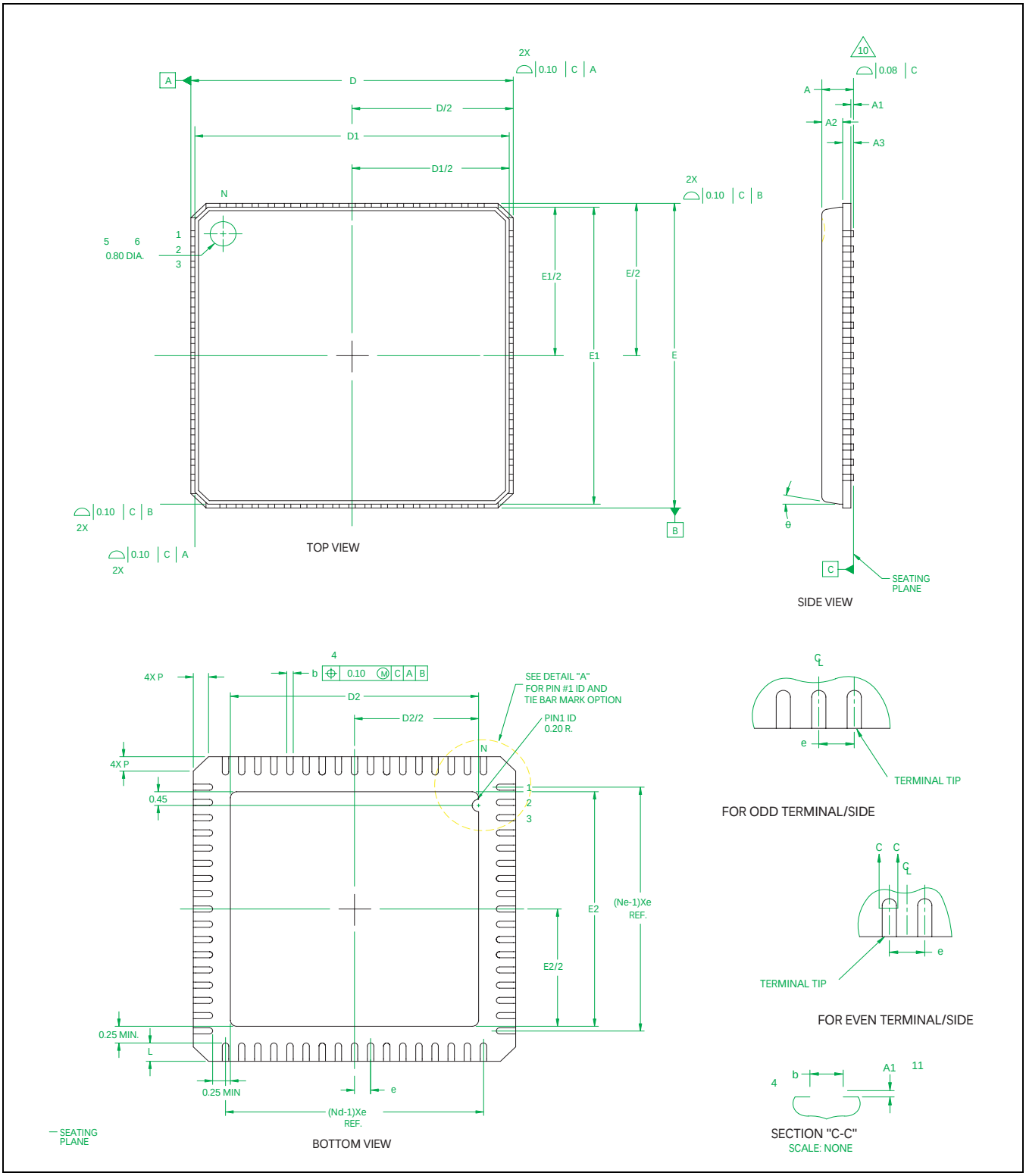


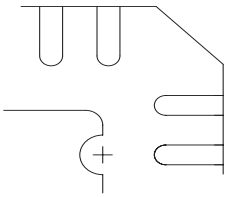
Figure 2-7 shows the package outline drawing for the 68-pin 10 mm x 10 mm MLF package (**Note:** See Figure 2-8 for dimensions of 72-pin package).

Figure 2-7. 68-Pin Package Drawing



The relevant dimensions for the 72-pin version of the package can be found in Figure 2-8.

Figure 2-8. 72-Pin Package Dimensions



STANDARD

DETAIL "A" - PIN #1 ID AND TIE BAR MARK OPTION

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e	0.50 BSC			
N	72			3
Nd	18			3
Ne	18			3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
Q	0.00	0.20	0.45	12
D2	SEE EXPOSED PAD VARIATION:C			
E2	SEE EXPOSED PAD VARIATION:C			

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	-	0.85	0.90	
A1	0.00	0.01	0.05	11
A2	-	0.65	0.70	
A3	0.20 REF.			
D	10.00 BSC			
D1	9.75 BSC			
E	10.00 BSC			
E1	9.75 BSC			
θ			12°	
P	0.24	0.42	0.60	
R	0.13	0.17	0.23	12

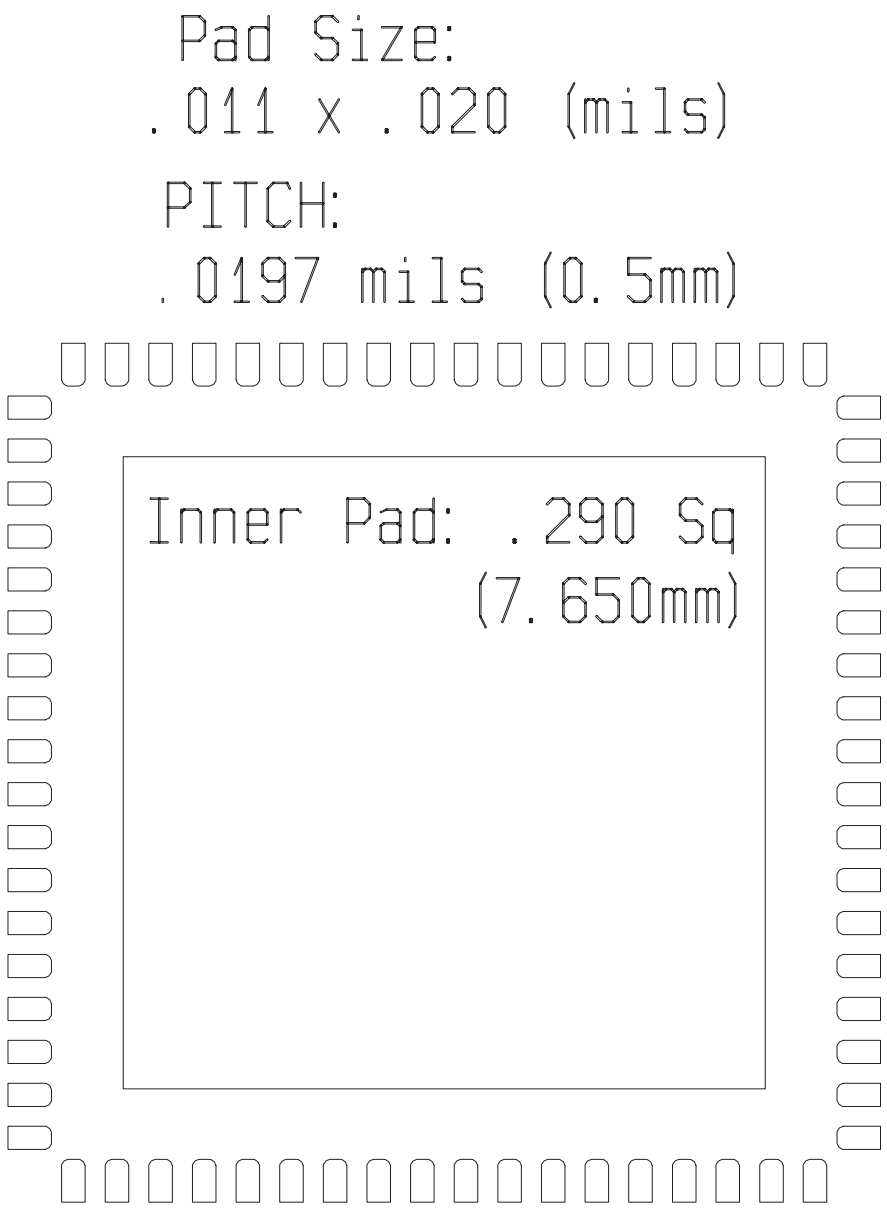
SYMBOLS		D2			E2			NOTE
		MIN	NOM	MAX	MIN	NOM	MAX	
EXPOSED PAD VARIATIONS	C	5.85	6.00	6.15	5.85	6.00	6.15	

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED
   BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE
   PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.08mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED
    PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.
12. Q AND R APPLIES ONLY FOR STRAGHT TIEBAR SHAPES.

The M21012 evaluation module (EVM) uses the PCB footprint shown in Figure 2-9.

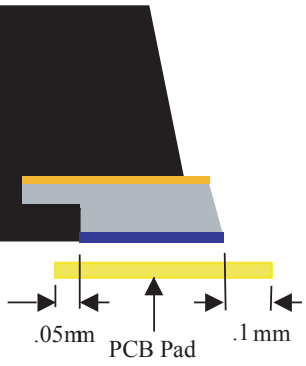
Figure 2-9. PCB Footprint for 72-Pin 10 mm MLF Package



Note: Pads placed on a .374 mils square (9.5 mm).
Add as many vias to ground in .290 square pad as possible.
Add .025 round clearances on soldermask in an even pattern to help solder ground pad.

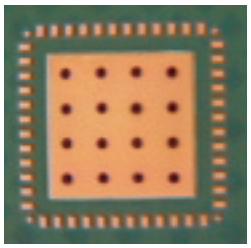
The pad length dimensions should account for component tolerances, PCB tolerances, and placement tolerances. At a minimum, the pad should extend at least 0.1 mm on the outside and 0.05 mm on the inside, as shown in Figure 2-10.

Figure 2-10. PCB Pad Extensions



To efficiently dissipate heat from the M21012, a thermal pad with thermal vias should be used on the PCB. An example of a thermal pad with a 4x4 via array is shown in Figure 2-11. The thermal vias provide a heat conduction path to inner and/or bottom layers of the PCB. The larger the via array, the lower the thermal resistance (θ_{ja}). It is recommended to use thermal vias with 1.0 to 1.2 mm pitch with 0.3 to 0.33 mm via diameter.

Figure 2-11. Recommended Via Array for Thermal Pad



For further details please refer to the relevant application note from package vendor Amkor (see list of references at the end of this document). Much of the material in this section has been adopted from the Amkor SMT application note.

2.7 PCB High-Speed Design and Layout Guidelines

A single power plane for the ***AVdd_IO*** and ***AVdd_Core*** power supplies with bulk capacitors (typically 10 µF) distributed throughout the board will mitigate most power-rail related voltage transients. A bulk capacitor should also be placed where the power enters the board. It is recommended that decoupling capacitors only be routed directly to the power pin if they can be placed within 1/8 of an inch of the pin. Decoupling capacitors should be dispersed around the outside of the device on the top side and underneath the IC on the bottom side of the board. It is recommended that 0.1 µF and 0.01 µF decoupling capacitors be used. All three capacitor values are not required on each pin, but should be dispersed uniformly to filter different frequencies of noise.

A continuous ground plane is the best way to minimize ground impedance. Return currents and power supply transients produce most ground noise during switching. Reducing ground plane impedance minimizes this effect. There is a high frequency decoupling effect from the capacitive effect of power/ground planes and this can be used to help minimize the amount of high frequency decoupling capacitors.

High-speed PCML signals should be routed with 50Ω equal length traces for P and N signals within each differential pair. Buried strip line is recommended for internal layers while microstrip line is used for signals routed on surface layers. There should be no discontinuity in the ground planes during the path of the signal traces.

Impedance discontinuities occur when a signal passes through vias and travels between layers. It is recommended to minimize the number of vias and layers that the transmit/receive signals travel through in the design. The system PCB should be designed so that high-speed signals pass through a minimal number of vias and remain on a single internal high-speed routing layer.

When vias need to be used, the via design should match the transmission line impedance by observing the following:

- Avoid through-hole vias; they cause stubs by extending the full cross-section of the PCB despite the fact that the layer change requires only a small length via (as in the case of adjacent layers). Use short blind vias.
- Avoid layer changes in general as the characteristic impedance of the transmission line changes as a result.

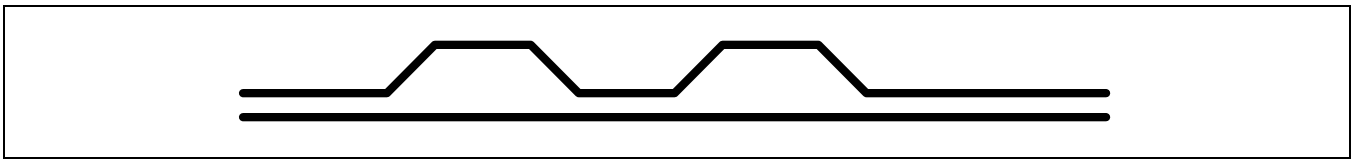
In general, some rules of thumb for PCB design for high data-rates are:

- PCB trace width for high-speed signals should closely match the SMT component width, so as to prevent stub effects from a sudden change in stripline width. A gradual increase in trace width is recommended as it meets the SMT pad.
- The PCB ground/power planes should be removed from under the I/O pins so as to reduce parasitic capacitance.
- High-speed traces should avoid sharp changes in direction. Using large radii will minimize impedance changes. Avoid bending traces by more than 45 degrees; otherwise, provide a circular bend so as to prevent the trace width from widening at the bend.
- Avoid trace stubs by minimizing components (resistors, capacitors) on the board. For instance, a termination resistor at the input of a receiver will inflict a stub effect at high frequency. Termination resistors integrated on chip will eliminate the stub. Components designed to DC couple to one another avoid the need for coupling capacitors and the inherent stubs created from them.

For high-speed differential signals, the trace lengths of each side of the differential pair should be matched to each other as much as possible. The skew between the P and N signals in a differential pair should be tightly controlled in order for the differential receiver to detect a valid data transition. When matching trace-lengths within a differential pair, care should be taken to avoid introducing large impedance discontinuities. The figures below show two methods of matching the trace-lengths for a differential pair.

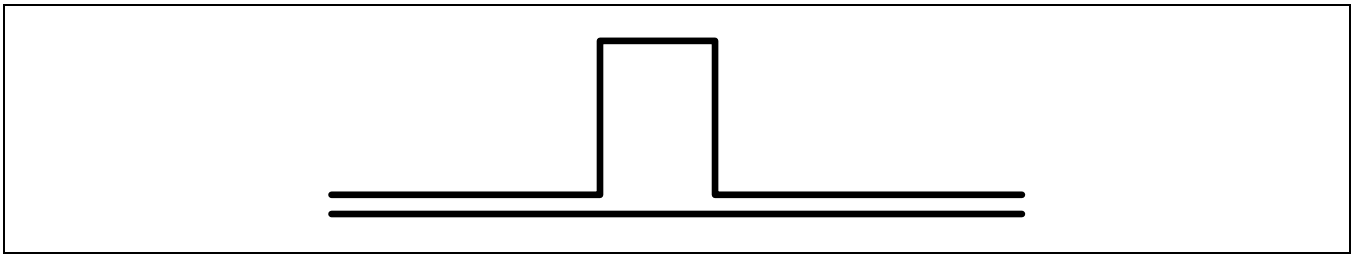
Typically, the preferred solution for trace-length matching in differential pairs is to use a serpentine pattern for the shorter signal as shown in Figure 2-12. Using a serpentine pattern for length matching will minimize the differential impedance discontinuity while making both trace-lengths equal.

Figure 2-12. Trace-Length Matching Using Serpentine Pattern



The loop length matching method shown in Figure 2-13 will match the trace lengths of a differential pair, but will create a large impedance discontinuity in the transmission line, which could result in higher jitter on the signal and/or a greater sensitivity to noise for the differential pair.

Figure 2-13. Loop Length Matching for Differential Traces



When using capacitors to AC-couple the input, care should be taken to minimize the pattern-dependant jitter (PD_J) associated with the low-frequency cutoff of the coupling network. When NRZ data containing long strings of 1s or 0s is applied to a high-pass filter, a voltage droop occurs. This voltage droop causes PD_J in much the same fashion as inter-symbol interference (ISI) is generated from dispersion effects of long trace-lengths in backplane material.

If needed, use 0.1 μF capacitors to AC-couple the high-speed output signals, and the reference clock inputs. The high-speed data input signals can be DC-coupled.

On the Evaluation Module (EVM), we have tied ***DVdd_I/O*** and ***AVdd_I/O*** together to minimize the number of power supply jacks. They are kept separate on-chip to give the flexibility to the system designers to supply a different voltage level for each. For instance, an FPGA can be used to supply power to ***DVdd_I/O***, while a lower voltage can be used to power ***AVdd_I/O*** to minimize power dissipation. On the EVM, we have also tied ***DVdd_Core*** and ***AVdd_Core*** together to minimize the number of power supply jacks. They are kept separate on-chip to provide more isolation, however, if the system board plane is properly decoupled, they can be tied together.

No inductive filtering on the system board is necessary between different power supplies of the IC. It is up to the system designer to determine if this needs to be considered for supplies that are coming from other parts of the system board (such as switching regulators or ASICs).

An inductor should not be used at the ***VddT*** pins. These pins were made available to create a low AC impedance, such that the 50Ω on-chip termination impedances see a common AC ground. This assures both common-mode and differential termination. If common-mode termination is not important (such as in LVDS applications), simply leave the ***VddT*** pins floating. Note that a low AC impedance can also be created by tying the ***VddT*** pins to the ***AVdd_I/O*** plane, thus saving on the number of external capacitors. This, however, implies a CML-like data interface (unless the data is AC-coupled). ***VddT*** is not really a supply plane on-chip, it is simply the point to which the 50Ω input impedances are tied.

Power planes should be decoupled to ground planes using thin dielectric layers, to increase capacitance (preferably 2-4 mils). Reference ground layers should be used on both sides of inner layer routing planes, with controlled impedance. The total board thickness should meet the standard drill holes to board thickness ratio of 1:12 or 1:14.

Use 1/2 ounce copper clad on all layers, which is approximately 0.7 mils. Avoid placing solder mask and silk-screen on top of transmission lines; solder mask will add 1 - 2Ω to the overall impedance of the transmission line. Dielectric core material should be used wherever possible, as it will maintain its thickness and geometry during processing, better than pliable prepreg.

The microwave ground should follow the transmission line from end to end, or from signal input to output. It is best to designate layers as dedicated microwave/circuit ground planes, and properly isolate them from other ground planes by providing adequate distance. All microwave ground planes should be tied together.

Uncoupled microstrip transmission lines should be placed at a distance from each other of at least three times the transmission line width. Coupled microstrip transmission lines, such as differential signal pairs, must be placed close to each other and maintain the same separation distance throughout the board (separation distance of at

most twice the trace-width). For buried stripline transmission lines, it is good design practice to maintain equal distance between the conductor and the ground plane on both sides.

During PCB manufacturing, over- and under-etching of traces used for transmission lines results in impedance discontinuities. Use of wide traces for transmission lines will reduce the impact of etching issues. Wide traces also help compensate for skin-effect losses in transmission lines. It should be noted, however, that the wider the traces in a differential pair, the thicker the underlying dielectric layer needs to be.

Surface mount connectors are preferred over through-mount connectors. Connectors should be selected that have controlled characteristic impedances that match the characteristic impedances of the transmission lines.

3.0 Registers

Table 3-1. Register Table Summary

Addr	Register Name	d7: MSB	d6	d5	d4	d3	d2	d1	d0: LSB
Common Registers									
00h	*Globctrl*	powerup	MSPD int	MSPD int	MSPD int	MSPD int	MSPD int	reserved	clear_alm
04h	*Refclk_ctrl*	reserved	reserved	reserved	reserved	ref_divr[2]	ref_divr[1]	ref_divr[0]	MSPD int
05h	*Mastreset*	rst	rst	rst	rst	rst	rst	rst	rst
06h	*Chipcode*	chipcode[7]	chipcode[6]	chipcode[5]	chipcode[4]	chipcode[3]	chipcode[2]	chipcode[1]	chipcode[0]
07h	*Revcode*	revcode[7]	revcode[6]	revcode[5]	revcode[4]	revcode[3]	revcode[2]	revcode[1]	revcode[0]
10h	*BISTrx_chsel*					reserved	chan[2]	chan[1]	chan[0]
11h	*BISTrx_ctrl*	MSPD int	rx_ctrclr	rx_patt[3]	rx_patt[2]	rx_patt[1]	rx_patt[0]	en_rx	rx_rst
12h	*BISTrx_error*	err[7]	err[6]	err[5]	err[4]	err[3]	err[2]	err[1]	err[0]
14h	*BISTtx_chsel*	reserved	reserved	reserved	reserved	MSPD int	MSPD int	tx_chan_1	tx_chan_0
15h	*BISTtx_ctrl*	err_insert	rx2txclk	tx_patt[3]	tx_patt[2]	tx_patt[1]	tx_patt[0]	en_tx	tx_rst
17h	*BISTtx_LOLctrl*	tacq_LOL[2]	tacq_LOL[1]	tacq_LOL[0]	narwin_LOL[3]	narwin_LOL[2]	narwin_LOL[1]	narwin_LOL[0]	widwin_LOL
18h	*BISTtx_PLL_ctrlA*	softreset	MSPD int	reserved	MSPD int	reserved	MSPD int	reserved	MSPD int
19h	*BISTtx_PLL_ctrlB*	PLLmode[1]	PLLmode[0]	MSPD int	MSPD int	data_rate[3]	data_rate[2]	data_rate[1]	data_rate[0]
1Ah	*BISTtx_PLL_ctrlC*	VCO_divr[7]	VCO_divr[6]	VCO_divr[5]	VCO_divr[4]	VCO_divr[3]	VCO_divr[2]	VCO_divr[1]	VCO_divr[0]
1Bh	*BIST_pattern0*					pattern[19]	pattern[18]	pattern[17]	pattern[16]
1Ch	*BIST_pattern1*	pattern[15]	pattern[14]	pattern[13]	pattern[12]	pattern[11]	pattern[10]	pattern[9]	pattern[8]
1Dh	*BIST_pattern2*	pattern[7]	pattern[6]	pattern[5]	pattern[4]	pattern[3]	pattern[2]	pattern[1]	pattern[0]
1Fh	*BISTtx_alarm*	tx_LOL	reserved	reserved	MSPD int	MSPD int	MSPD int	MSPD int	MSPD int
20h	*Temp_mon*					reserved	reserved	en_temp_mon	strobe_temp
21h	*Temp_value*					temp[3]	temp[2]	temp[1]	temp[0]
30h	*Alarm_LOL*	MSPD int	MSPD int	MSPD int	MSPD int	LOL_3	LOL_2	LOL_1	LOL_0
31h	*Alarm_LOA*	MSPD int	MSPD int	MSPD int	MSPD int	LOA_3	LOA_2	LOA_1	LOA_0
Per channel registers (N = channel/CDR#, M = N+4)									
M0h	*CDR_ctrlA*_N	softreset	MSPD int	inh_force	MSPD int	autoinh_en	MSPD int	LOA_en	MSPD int
M1h	*CDR_ctrlB*_N	CDRmode[1]	CDRmode[0]	MSPD int	reserved	data_rate[3]	data_rate[2]	data_rate[1]	data_rate[0]
M2h	*CDR_ctrlC*_N	VCO_divr[7]	VCO_divr[6]	VCO_divr[5]	VCO_divr[4]	VCO_divr[3]	VCO_divr[2]	VCO_divr[1]	VCO_divr[0]
M3h	*Out_ctrl*_N	outlvl[1]	outlvl[0]	reserved	reserved	data_pol_flip	dataout_en	clkout_en	clk_pol_flip
M4h	*Preemp_ctrl*_N	reserved	MSPD int	MSPD int	MSPD int	MSPD int	preemph[2]	preemph[1]	preemph[0]
M5h	*Ineq_ctrl*_N	reserved	MSPD int	MSPD int	en_DCservo	MSPD int	in_eq[2]	in_eq[1]	in_eq[0]
M6h	*Phadj_ctrl*_N	i_trim[1]	i_trim[0]	r_sel[1]	r_sel[0]	phase_adj[3]	phase_adj[2]	phase_adj[1]	phase_adj[0]
M9h	*LOL_ctrl*_N	tacq_LOL[2]	tacq_LOL[1]	tacq_LOL[0]	narwin_LOL[3]	narwin_LOL[2]	narwin_LOL[1]	narwin_LOL[0]	widwin_LOL
MAh	*Jitter_reduc*_N	MSPD int	MSPD int	lowjitter	MSPD int	MSPD int	MSPD int	MSPD int	MSPD int

NOTES:

1. N = 0 for channel/CDR 0, N = 1 for channel/CDR 1,.., N = 3 for channel/CDR 3.
2. M = 4 for channel/CDR 0, M = 5 for channel/CDR 1,..., M = 7 for channel/CDR 3. For example channel/CDR 0 starts at address 40h, channel/CDR 1 at 50h, channel/CDR 2 at 60h, channel/CDR 3 at 70h.

3.1 Global Control Registers

Nomenclature:

1. Reserved bits: bits that exist and reserved for future use by Mindspeed.
2. Bits not defined and not reserved do not exist.
3. Do not write to reserved or undefined bits – operation not guaranteed.
4. MSPD internal: defines an internal function. Must always write the default value to MSPD internal bits. When in doubt, read back default value after reset.

3.1.1 Global Control

Table 3-2. Global Control (*Globctrl*: Address 00h)

Bits	Type	Default	Label	Description
7	R/W	1b	powerup	Powers up the IC by enabling the current references 1b: Power up the IC (chip powerup) 0b: Power down the IC
6:2	R/W	00000b	MSPD internal	N/A
1	R/W	0b	Reserved	N/A
0	R/W	0b	clear_alm	Clears the *Alarm_LOA*, *Alarm_LOL* alarm registers 1b: Clear alarms 0b: Normal operation - latch alarm bits **Note**: Upon writing a 1b to this bit, it clears the registers, and user needs to write a 0b to enable the normal state.

3.1.2 External Reference Frequency Divider Control (RFD)

Table 3-3. External Reference Frequency Divider Control (RFD) (*Refclk_ctrl*: Address 04h)

Bits	Type	Default	Label	Description
7:4	R/W	0b	Reserved	N/A
3:1	R/W	000b	ref_divr	Sets the divider ratio to scale down ***RefClk*** to the internal rate for FRA/LOA 000b: RFD = 1 001b: RFD = 2 010b: RFD = 4 011b: RFD = 8 100b: RFD = 12 101b: RFD = 16 110b: RFD = 32
0	R/W	0b	MSPD internal	N/A

3.1.3 Master IC Reset

Table 3-4. Master IC Reset (Mastreset: Address 05h)

Bits	Type	Default	Label	Description
7:0	R/W	0b	rst	Same feature as hardware ***xRST***. Resets the entire IC AAh: Reset upon write to this register with AAh 00h: Normal operation [Default] **Note**: All other values are ignored.

3.1.4 IC Electronic Identification

Table 3-5. IC Electronic ID (Chipcode: Address 06h)

Bits	Type	Default	Label	Description
7:0	R	12h	chipcode	This register contains the identification of this IC. **Note**: For M21011 default is 11h, and for M21001 default is 10h.

3.1.5 IC Revision Code

Table 3-6. IC Revision Code (Revcode: Address 07h)

Bits	Type	Default	Label	Description
7:0	R	20h	revcode	This register contains the revision of the IC.

3.1.6 Built In Self-Test (BIST) Receiver Channel Select

Table 3-7. Built In Self-Test (BIST) Receiver Channel Select (BISTrx_chsel: Address 10h)

Bits	Type	Default	Label	Description
7:3	R/W	0b	Reserved	N/A
2:0	R/W	000b	chan	Selects which CDR to route into the BIST receiver (active when *BISTrx_ctrl* [1]=1) 000b: Output CDR 0 to BIST 001b: Output CDR 1 to BIST 010b: Output CDR 2 to BIST 011b: Output CDR 3 to BIST

3.1.7 Built In Self-Test (BIST) Receiver Main Control Register

Table 3-8. Built In Self-Test (BIST) Receiver Main Control Register (*BISTrx_ctrl*: Address 11h)

Bits	Type	Default	Label	Description
7	R/W	0b	MSPD internal	N/A
6	R/W	0b	rx_ctrclr	Clear the BIST Rx error count register, *BISTrx_error* (active when *BISTrx_ctrl* [1] = 1) 0b: Normal operation 1b: Clear register
5:2	R/W	0000b	rx_patt	Selects the BIST Rx test pattern (active when *BISTrx_ctrl* [1] = 1) 0000b: PRBS 2^7-1 0001b: PRBS 2^{15}-1 0010b: PRBS 2^{23}-1 0011b: PRBS 2^{31}-1 0100b: Fibre channel CJTPAT 0101b: Fibre channel CRPAT 0110b: 8b/10b countdown pattern 0111b: 16 bit user programmable pattern 1000b: 20 bit user programmable pattern
1	R/W	0b	en_rx	Powers up the BIST Rx 0b: Power down 1b: Power up and enable
0	R/W	1b	rx_rst	Resets the BIST Rx (recommended after powerup/enable, active when *BISTrx_ctrl* [1] = 1) 0b: Normal BIST Rx operation 1b: Reset of BIST Rx

3.1.8 Built In Self-Test (BIST) Receiver Bit Error Counter

Table 3-9. Built In Self-Test (BIST) Receiver Bit Error Counter (*BISTrx_error*: Address 12h)

Bits	Type	Default	Label	Description
7:0	R/W	00h	err	Bit error count (active when *BISTrx_ctrl* [1] = 1) This register is set to 00h upon reset, and is incremented for every bit error the BIST Rx receives, up to FFh. At FFh, the register will stay at this level until cleared.

3.1.9 Built In Self-Test (BIST) Transmitter Channel Select

Table 3-10. Built In Self-Test (BIST) Transmitter Channel Select (*BISTtx_chsel*: Address 14h)

Bits	Type	Default	Label	Description
7:4	R/W	0000b	Reserved	N/A
3:2	R/W	00b	MSPD internal	N/A
1:0	R/W	00b	tx_chan	Selects which output channel the BIST Tx outputs the test pattern on (active when *BISTtx_ctrl* [1] = 1) Bit map: 1b = BIST Tx on, 0b = BIST Tx off [1]: Output channel 1 [0]: Output channel 0 **Note**: Registers are set up to allow for multicasting BIST Tx output.

3.1.10 Built In Self-Test (BIST) Transmitter Main Control Register

Table 3-11. Built In Self-Test (BIST) Transmitter Main Control Register (*BISTtx_ctrl*: Address 15h)

Bits	Type	Default	Label	Description
7	R/W	0b	err_insert	Inserts a single bit error into the PRBS Tx 1b: Insert error 0b: Normal operation **Note:** Setting the register high allows one error to be inserted into the data stream. To insert another error, the user needs to clear, then set this register bit.
6	R/W	0b	rx2txclk	Selects the source of the clock for the BIST Tx PLL (active when *BISTtx_ctrl* [1] = 1) 0b: External reference frequency 1b: Recovered clock from BIST Rx **Note:** For the recovered clock option, the BIST Rx must be enabled with *BISTrx_ctrl* [1] = 1, and use the recovered clock from the same CDR selected by BIST Rx. This option only works for the full-rate case.
5:2	R/W	0000b	tx_patt	Selects the BIST Tx test pattern (active when *BISTtx_ctrl* [1] = 1) 0000b: PRBS 2^7-1 0001b: PRBS 2^{15}-1 0010b: PRBS 2^{23}-1 0011b: PRBS 2^{31}-1 0100b: Fibre channel CJTPAT 0101b: Fibre channel CRPAT 0110b: 8b/10b countdown pattern 0111b: 16 bit user programmable pattern 1000b: 20 bit user programmable pattern
1	R/W	0b	en_tx	Powers up the BIST Tx and PLL 0b: Power down 1b: Power up and enable
0	R/W	1b	tx_rst	Resets the BIST Tx (recommended after powerup/enable; active when *BISTtx_ctrl* [1] = 1) 0b: Normal BIST Tx operation 1b: Reset of BIST Tx

3.1.11 Built In Self-Test (BIST) Transmitter PLL Loss of Lock Register

Table 3-12. Built In Self-Test (BIST) Transmitter PLL Loss of Lock Register (BISTtx_LOLctrl: Address 17h) (1 of 2)

Bits	Type	Default	Label	Description
7:5	R/W	101b	tacq_LOL	Sets the value for the LOL reference window **Code** **Value** 000b 128 001b 256 010b 512 011b 1024 100b 2048 101b 4096 110b 8192 111b 16384
4:1	R/W	0011b	narwin_LOL	Sets the narrow LOL window for the LOL = H to LOL = L transition (transition to in lock threshold) **Code** **Value** 0000b 2 0001b 3 0010b 4 0011b 6 0100b 8 0101b 12 0110b 16 0111b 24 1000b 9 1001b 10 1010b 11 1011b 12 1100b 13 1101b 14 1110b 15 1111b 32

Table 3-12. Built In Self-Test (BIST) Transmitter PLL Loss of Lock Register (BISTtx_LOLctrl: Address 17h) (2 of 2)

Bits	Type	Default	Label	Description
0	R/W	0b	widwin_LOL	Sets the wide LOL window for the LOL = L to LOL = H transition (transition to out of lock threshold) **Narrow Code** / **Wide Code 0b** / **Wide Code 1b** 0000b 3 8 0001b 4 12 0010b 6 16 0011b 8 24 0100b 12 32 0101b 16 32 0110b 24 32 0111b 32 32 1000b 12 32 1001b 12 32 1010b 12 32 1011b 16 32 1100b 16 32 1101b 16 32 1110b 16 32 1111b 32 32

3.1.12 Built In Self-Test (BIST) Transmitter PLL Control Register A

Table 3-13. Built In Self-Test (BIST) Transmitter PLL Control Register A (BISTtx_PLL_ctrlA: Address 18h)

Bits	Type	Default	Label	Description
7	R/W	0b	softreset	Resets the BIST transmitter PLL (assuming *BISTtx_ctrl* [1] = 1b) 0b: Normal operation 1b: Reset PLL only
6	R/W	0b	MSPD internal	N/A
5	R/W	0b	Reserved	N/A
4	R/W	0b	MSPD internal	N/A
3	R/W	0b	Reserved	N/A
2	R/W	1b	MSPD internal	N/A
1	R/W	0b	Reserved	N/A
0	R/W	1b	MSPD internal	N/A

3.1.13 Built In Self-Test (BIST) Transmitter PLL Control Register B

Table 3-14. Built In Self-Test (BIST) Transmitter PLL Control Register B (*BISTtx_PLL_ctrlB*: Address 19h)

Bits	Type	Default	Label	Description
7:6	R/W	00b	PLLmode	Determines state of the PLL. Must be enabled in addition to the BIST Tx (*BISTtx_ctrl* [1] = 1b) 00b: Channel active, PLL powered up 11b: Channel active, PLL powered down
5:4	R/W	01b	MSPD internal	N/A
3:0	R/W	0000b	data_rate	Data-rate divider (DRD): this divides down the VCO frequency to the desired data-rate 0000b: DRD = 1 0001b: DRD = 2 0010b: DRD = 4 0011b: DRD = 8 0100b: DRD = 12 0101b: DRD = 16 0110b: DRD = 24 0111b: DRD = 32 1000b: DRD = 48 **Note**: Please consult $F_{vco,max}$ and $F_{vco,min}$ to determine the frequency range of each DRD ratio.

3.1.14 Built In Self-Test (BIST) Transmitter PLL Control Register C

Table 3-15. Built In Self-Test (BIST) Transmitter PLL Control Register C (*BISTtx_PLL_ctrlC*: Address 1Ah)

Bits	Type	Default	Label	Description
7:0	R/W	10000000b	VCO_divr	VCO comparison divider (VCD): this divider divides down the VCO to compare it with the divided down reference, for use in the FRA mode. Binary value reflects the divider ratio 01h: Minimum value (VCD = 1) . . . FFh: Maximum value (VCD = 255)

3.1.15 Built In Self-Test (BIST) Transmitter 20 bit User Programmable Pattern

Table 3-16. Built In Self-Test (BIST) Transmitter 20 bit User Programmable Pattern (*BIST_pattern0*: Address 1Bh)

Bits	Type	Default	Label	Description
3:0	R/W	1100b	pattern	Sets the 20 bit user programmable pattern used in the BIST [3] MSB : Pattern bit#19 [2] : Pattern bit#18 [1] : Pattern bit#17 [0] LSB : Pattern bit#16

3.1.16 Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern

Table 3-17. Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern (BIST_pattern1: Address 1Ch)

Bits	Type	Default	Label	Description
7:0	R/W	11001100b	pattern	Sets the 16/20 bit user programmable pattern used in the BIST [7] MSB : Pattern bit#15 [6] : Pattern bit#14 [5] : Pattern bit#13 [4] : Pattern bit#12 [3] : Pattern bit#11 [2] : Pattern bit#10 [1] : Pattern bit#9 [0] LSB : Pattern bit#8

3.1.17 Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern

Table 3-18. Built In Self-Test (BIST) Transmitter 16/20 bit User Programmable Pattern (BIST_pattern2: Address 1Dh)

Bits	Type	Default	Label	Description
7:0	R/W	11001100b	pattern	Sets the 16/20 bit user programmable pattern used in the BIST [7] MSB : Pattern bit#7 [6] : Pattern bit#6 [5] : Pattern bit#5 [4] : Pattern bit#4 [3] : Pattern bit#3 [2] : Pattern bit#2 [1] : Pattern bit#1 [0] LSB : Pattern bit#0

3.1.18 Built In Self-Test (BIST) Transmitter Alarm

Table 3-19. Built In Self-Test (BIST) Transmitter Alarm (BISTtx_alarm: Address 1Fh)

Bits	Type	Default	Label	Description
7	R	0b	tx_LOL	Loss of lock for the BIST Tx PLL (active when *BISTtx_ctrl* [1] = 1) 0b: Normal operation 1b: Loss of lock
6:5	R/W	00b	Reserved	N/A
4:0	R/W	00000b	MSPD internal	N/A

3.1.19 Internal Junction Temperature Monitor

Table 3-20. Internal Junction Temperature Monitor (*Temp_mon*: Address 20h)

Bits	Type	Default	Label	Description
3:2	R/W	00b	Reserved	N/A
1	R/W	0b	en_temp_mon	Power up and enable the temperature monitor 1b: Power up and enable temperature monitor 0b: Disable temperature monitor
0	R/W	0b	strobe_temp	Strobes ADC for temperature measurement 1b: Read temperature 0b: Ok to read temperature **Note**: To strobe ADC, a rising edge should be provided by writing 1b, then writing 0b to return to default state.

3.1.20 Internal Junction Temperature Value

Table 3-21. Internal Junction Temperature Value (*Temp_value*: Address 21h)

Bits	Type	Default	Label	Description
3:0	R	N/A	temp	A read of these bits returns the temperature from the last write cycle (to strobe_temp)

Junction Temperature	temp	Condition
$T_j \geq 130°C$	1100b	High-alarm
$130°C > T_j \geq 120°C$	1011b	High-alarm
$120°C > T_j \geq 110°C$	1010b	High-warning
$110°C > T_j \geq 100°C$	1001b	Normal
$100°C > T_j \geq 90°C$	1000b	Normal
$90°C > T_j \geq 80°C$	0111b	Normal
$80°C > T_j \geq 10°C$	0110b	Normal
$10°C > T_j \geq 0°C$	0101b	Normal
$0°C > T_j \geq -10°C$	0100b	Normal
$-10°C > T_j \geq -20°C$	0011b	Normal
$-20°C > T_j \geq -30°C$	0010b	Low-warning
$-30°C > T_j \geq -40°C$	0001b	Low-alarm
$-40°C > T_j$	0000b	Low-alarm

3.1.21 CDR Loss of Lock Register Alarm Status

Table 3-22. CDR Loss of Lock Register Alarm Status (*Alarm_LOL*: Address 30h)

Bits	Type	Default	Label	Description
7:4	R/W	0000b	MSPD internal	N/A
3:0	R	N/A	LOL	Latched loss of lock alarm status 1b = loss of CDR lock, 0b = normal operation [3]: CDR 3 [2]: CDR 2 [1]: CDR 1 [0]: CDR 0 **Note:** After a clear (*Globctrl* [0] = 1), this register is cleared and will latch any new alarms that make a L to H transition, and set any pre-existing alarm conditions to H.

3.1.22 Loss of Activity Register Alarm Status

Table 3-23. Loss of Activity Register Alarm Status (*Alarm_LOA*: Address 31h)

Bits	Type	Default	Label	Description
7:4	R/W	0000b	MSPD internal	N/A
3:0	R	N/A	LOA	Latched loss of activity alarm status 1b = loss of input signal, 0b = normal operation [3]: Channel 3 [2]: Channel 2 [1]: Channel 1 [0]: Channel 0 **Note:** After a clear (*Globctrl* [0] = 1), this register is cleared and will latch any new alarms that make a L to H transition, and set any pre-existing alarm conditions to H.

3.2 Individual Channel/CDR Control

Multiple Instance Nomenclature

1. N = 0 for channel/CDR 0, N = 1 for channel/CDR 1,.., N = 3 for channel/CDR 3.
2. M = 4 for channel/CDR 0, M = 5 for channel/CDR 1,.., M = 7 for channel/CDR 3. For example channel/CDR 0 starts at address 40h, channel/CDR 1 at 50h, channel/CDR 2 at 60h, channel/CDR 3 at 70h.

3.2.1 CDR N Control Register A

Table 3-24. CDR N Control Register A (*CDR_ctrlA_*N: Address M0h)

Bits	Type	Default	Label	Description
7	R/W	0b	softreset	Resets individual CDR N (setup registers remain unchanged; need to softreset after data-rate change) 0b: Normal operation 1b: Reset single CDR only
6	R/W	0b	MSPD internal	N/A
5	R/W	0b	inh_force	Manual control of the output inhibit if *CDR_ctrlA*_N [3] = 0 0b: Normal operation 1b: Forced inhibit
4	R/W	0b	MSPD internal	N/A
3	R/W	1b	autoinh_en	Auto inhibit of the output (***DoutP*** = H, ***DoutN*** = L) if CDR N has a LOL or LOA condition 0b: Auto inhibit disabled, *CDR_ctrlA*_N [5] determines inhibit force state 1b: Auto inhibit enabled
2	R/W	1b	MSPD internal	N/A
1	R/W	1b	LOA_en	Enables the transition density based loss of activity detector for channel N 0b: Disable and power down LOA circuit 1b: Enable LOA circuit
0	R/W	1b	MSPD internal	N/A

3.2.2 CDR N Control Register B

Table 3-25. CDR N Control Register B (CDR_ctrlB_N: Address M1h)

Bits	Type	Default	Label	Description
7:6	R/W	00b	CDRmode	Determines state of the PLL 00b: CDR powered up and active 01b: CDR powered up and bypassed 10b: CDR powered down (no signal through) 11b: CDR powered down and bypassed
5	R/W	0b	MSPD internal	N/A
4	R/W	0b	Reserved	N/A
3:0	R/W	0000b	data_rate	Data-rate divider (DRD): this divides down the VCO frequency to the desired data-rate to match input data-rate 0000b: DRD = 1 0001b: DRD = 2 0010b: DRD = 4 0011b: DRD = 8 0100b: DRD = 12 0101b: DRD = 16 0110b: DRD = 24 0111b: DRD = 32 1000b: DRD = 48 **Note:** Please consult $F_{vco,max}$ and $F_{vco,min}$ to determine frequency range of each DRD ratio.

3.2.3 CDR N Control Register C

Table 3-26. CDR N Control Register C (CDR_ctrlC_N: Address M2h)

Bits	Type	Default	Label	Description
7:0	R/W	10000000b	VCO_divr	VCO comparison divider (VCD): this divides down the VCO, to compare it with the scaled reference clock, for use in the FRA/LOA mode. Binary value reflects the divider ratio 1h: Minimum value (VCD = 1) . . . FFh: Maximum value (VCD = 255)

3.2.4 Output Buffer Control for CDR N

Table 3-27. Output Buffer Control for CDR N (*Out_ctrl*_N: Address M3h)

Bits	Type	Default	Label	Description
7:6	R/W	10b	outlvl	Determines the output swing of a data and/or clock buffer for CDR N In PCML mode: 00b: Power down 01b: 600 mV 10b: 1V 11b: 1.3V For LVDS, the output swing is reduced to: 00b: Power down 01b: RRL 450 mV 10b: GPL 650 mV 11b: 1V For PCML+, the output swing is increased to: 00b: Power down 01b: 1V 10b: 1.3V 11b: 1.6V
5:4	R/W	00b	Reserved	N/A
3	R/W	0b	data_pol_flip	Flips the polarity of the output data 0b: Normal 1b: Polarity flip
2	R/W	1b	dataout_en	Enables the data output driver N 1b: Data output enabled to level specified in *Out_ctrl*_N [7:6] 0b: Data output disabled and powered down
1	R/W	0b	clkout_en	Enables the clock output driver N 1b: Clock output enabled to level specified in *Out_ctrl*_N [7:6] 0b: Clock output disabled and powered down
0	R/W	0b	clk_pol_flip	Flips the polarity of the output clock 0b: Normal 1b: Polarity flip

3.2.5 Output Buffer Pre-Emphasis Control for Output N

Table 3-28. Output Buffer Pre-Emphasis Control for Output N (*Preemp_ctrl*_N: Address M4h)

Bits	Type	Default	Label	Description
7	R/W	0b	Reserved	N/A
6:3	R/W	1000b	MSPD internal	N/A
2:0	R/W	000b	preemph	Selects the digital pre-emphasis level 111b: 200% 110b: 150% 101b: 100% 100b: 75% 011b: 50% 010b: 37.5% 001b: 25% 000b: Pre-emphasis off

3.2.6 Input Equalization Control for Output N

Table 3-29. Input Equalization Control for Output N (*Ineq_ctrl_*N: Address M5h)

Bits	Type	Default	Label	Description
7	R/W	0b	Reserved	N/A
6:5	R/W	00b	MSPD internal	N/A
4	R/W	1b	en_DCservo	Enables DC servo in the input channel to remove offset based deterministic jitter 0b: DC servo D_j attenuator off 1b: DC servo D_j attenuator on
3	R/W	0b	MSPD internal	N/A
2:0	R/W	000b	in_eq	Selects the input equalization level 111b: Maximum input equalization level . . . 100b: Nominal input equalization level . . . 001b: Minimum input equalization level 000b: Input equalization disabled **Note:** The 100b setting is optimized for PCB trace lengths between 10 - 46 inches, although other settings may be optimal for some applications.

3.2.7 CDR N Loop Bandwidth and Data Sampling Point Adjust

Table 3-30. CDR N Loop Bandwidth and Data Sampling Point Adjust (*Phadj_ctrl_*N: Address M6h)

Bits	Type	Default	Label	Description
7:6	R/W	10b	i_trim	Adjusts the charge-pump current; the loop bandwidth (F_{LBW}) scales proportionately 00b: 0.65x 01b: 0.8x 10b: Nominal 11b: 1.15x
5:4	R/W	01b	r_sel	Adjusts the resistor of the CDR loop filter; the loop bandwidth (F_{LBW}) scales proportionately 00b: 80% of the nominal value 01b: Nominal 10b: 4x nominal value
3:0	R/W	0000b	phase_adj	Adjusts the static phase offset (sampling point) of the data 1111b: -122.5 mUI 1110b: -105 mUI 1101b: -87.5 mUI 1100b: -70 mUI 1011b: -52.5 mUI 1010b: -35.0 mUI 1001b: -17.5 mUI 1000b: 0 mUI 0000b: 0 mUI 0001b: 17.5 mUI 0010b: 35.0 mUI 0011b: 52.5 mUI 0100b: 70.0 mUI 0101b: 87.5 mUI 0110b: 105 mUI 0111b: 122.5 mUI

3.2.8 CDR N FRA LOL Window Control

Table 3-31. CDR N FRA LOL Window Control (*LOL_ctrl_*N: Address M9h) (1 of 2)

Bits	Type	Default	Label	Description
7:5	R/W	101b	tacq_LOL	Sets the value for the LOL reference window **Code** **Value** 000b 128 001b 256 010b 512 011b 1024 100b 2048 101b 4096 110b 8192 111b 16384

Table 3-31. CDR N FRA LOL Window Control (LOL_ctrl_N: Address M9h) (2 of 2)

Bits	Type	Default	Label	Description
4:1	R/W	0100b	narwin_LOL	Sets the narrow LOL window for the LOL = H to LOL = L transition (transition to in lock threshold) **Code** **Value** 0000b 2 0001b 3 0010b 4 0011b 6 0100b 8 0101b 12 0110b 16 0111b 24 1000b 9 1001b 10 1010b 11 1011b 12 1100b 13 1101b 14 1110b 15 1111b 32
0	R/W	0b	widwin_LOL	Sets the wide LOL window for the LOL = L to LOL = H transition (transition to out of lock threshold) **Narrow Code** **Wide Code 0b** **Wide Code 1b** 0000b 3 8 0001b 4 12 0010b 6 16 0011b 8 24 0100b 12 32 0101b 16 32 0110b 24 32 0111b 32 32 1000b 12 32 1001b 12 32 1010b 12 32 1011b 16 32 1100b 16 32 1101b 16 32 1110b 16 32 1111b 32 32

3.2.9 Jitter Reduction Control

Table 3-32. Jitter Reduction Control (*Jitter_reduc_*N: Address MAh)

Bits	Type	Default	Label	Description
7:6	R/W	01b	MSPD internal	N/A
5	R/W	0b	lowjitter	When data-rate is in the range (2.45 Gbps - 2.55 Gbps)/DRD, setting this bit to 1b will reduce output jitter (DRD is data-rate divider). 1b: Reduce output jitter 0b: Normal operation **Note:** This bit should be set to 1b for SONET STS-N, and Gigabit Ethernet applications.
4:0	R/W		MSPD internal	Any value may be written to this register with no effect on performance.

4.0 Appendices

4.1 Glossary of Terms/Acronyms

Table 4-1 contains a list of acronyms used in this data sheet.

Table 4-1. Acronyms

BER	Bit-Error Rate
BIST	Built-In Self Test
CDR	Clock and Data Recovery array
DRD	Data-Rate Divider
EVM	Evaluation Module
FLL	Frequency Lock Loop
FRA	Frequency Reference Acquisition
IE	Input Equalizer
ISI	Inter-Symbol Interference
LOA	Loss of Activity
LOL	Loss of Lock
LOLCir	Loss of Lock Circuitry
MLF	MicroLeadFrame
NRW	Narrow Reference Window
PCB	Printed Circuit Board
PLL	Phase Lock Loop
RFD	Reference Frequency Divider
SONET	Synchronous Optical Network
VCD	VCO Comparison Divider
WRW	Wide Reference Window
XPTS	Crosspoint Switch

4.2 Reference Documents

4.2.1 External

The following external documents were referenced in this data sheet.

- Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria GR-253-CORE
- The I^2C Bus Specification version 2.1
- Fibre Channel - Methodologies for Jitter and Signal Quality Specification - MJSQ & FC-PI-2
- Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages
- Amkor Technology Thermal Test Report TT-00-06

4.2.2 Mindspeed

The following Mindspeed documents were referenced in this data sheet.

- M21012/M21011/M21001 Evaluation Module User Guide
- Jitter tolerance and generation of Mindspeed Technologies crosspoint switches and clock & data recovery arrays

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