Multi-Output Power Supply with VCOM Amplifier for EPD

Features

- **Single Chip Power Management Solution for E-paper Displays**
- **Input Supply Voltage Range: 3.0~5.5V**
- **I²C Series Interface**
- **Boost Converter for Positive Rail Base (HVINP)**
- **Inverting Buck-Boost Converter for Negative Rail Base (HVINN)**
- **Accurate Voltage Tracking between HVINP and HVINN: ±50mV**
- **Integrated Two Power Switches with Soft-start Control for Source Driver Supply**
  -POS: +15V/120mA
  -NEG: -15V/120mA
- **Two Charge Pump for Gate Driver Supply**
  -DGVDD: +22V/20mA
  -DGVEE:-22V/20mA
- **Accurate and Adjustable VCOM Voltage for Panel Backplane Biasing**
  - -0.3 to -2.85V/100mA, 10mV per step
  -8-bit Control
- **Programmable Turn-on/Turn-off Timing in every Output Voltage**
- **Remote Temperature Sensing**
- **POK Output**
- **FAULT Output**
- **Enable Input**
- **Current Limit Protection**
- **Over Temperature Protection**
- **Fault Events Report in Every Output for Easy Debugging**
- **1MHz Fixed PWM Frequency**
- **Up to 85% efficiency for the Boost**
- **Internal Soft Start Control**
- **Available in TQFN5x5-32 Package**
- **Halogen and Lead Free Available (RoHS Compliant)**

General Description

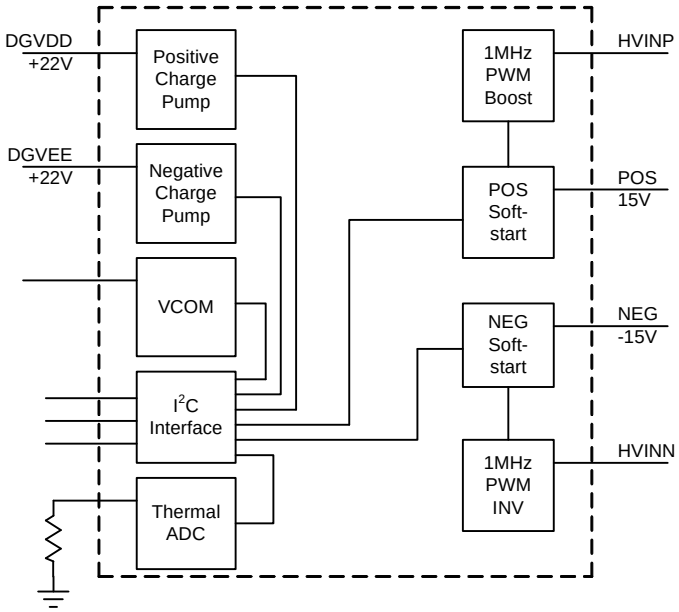
The APW7223 is a single chip, multi outputs PMIC for E-paper displays. Two PWM converters respectively generate positive and negative voltages which are boosted to higher voltage by two charge pumps for both source and gate drivers. Two integrated power switches are used to disconnect these PWM outputs from load in shutdown mode. All PWM and charge pump output voltages are adjustable by external resistors and their power on/off timings can be individually programmable via I²C interface. One accurate VCOM voltage, for backplane biasing, is adjustable via I²C interface from -0.3V to -2.85V with 10mV per step. The VCOM is capable of sourcing and sinking current, depending on panel condition, at lease 100mA. An external negative temperature coefficient(NTC) resistor is incorporated to sense remote temperature. This remote temperature sensing can be used to monitor the battery's surface temperature to avoid over heating. The temperature data is mapped from the voltage on TS pin according to a preset conversion table. Approximately every 250µs the APW7223 executes the voltage/temperature conversion and stores the temperature date in register in two's complement format.

The APW7223 is available in a space saving TQFN5x5 32-pin package and is specified over the -40°C to +85°C extended temperature range.

Applications

- **E-paper Displays**

Simplified Application Circuit



Ordering and Marking Information

APW7223 □□□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

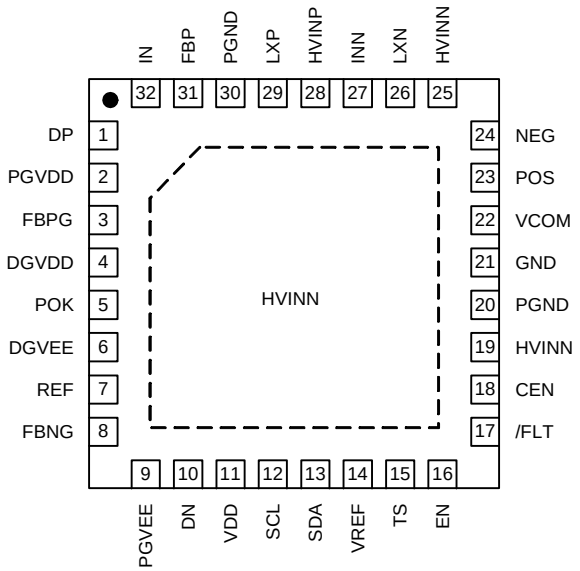
Package Code
QB : TQFN5x5-32
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APW7223QB: APW 7223 XXXXX

XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
	IN, INN, CEN, EN, POK, /FLT, FBP, FBPG, FBNG, REF, VDD, SCL, SDA, TS to GND Voltage	-0.3 ~ 6.5	V
	VREF to GND Voltage	-0.3 ~ 4	V
	LXP, HVINP, POS, PGVDD, DP to PGND	-0.3 ~ 24	V
	LXN, HVINN, NEG, PGVEE, DN, PBKG, VCOM to PGND	-24 ~ 0.3	V
	DGVDD to PGND	-0.3 ~ 40	V
	DGVEE to PGND	-40 ~ 0.3	V
	PGND to GND Voltage	-0.3 ~ 0.3	V
P_D	Power Dissipation	Internally Limited	W
	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	20	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
	IN, INN, VDD, SCL, SDA, TS to GND Voltage	-0.3 ~ 5.5	V
	CEN, EN, POK, /FLT, FBP, FBPG, FBNG, REF to GND Voltage	-0.3 ~ V_{IN}+0.3	V
	LXP, HVINP to PGND Voltage	12 ~ 18	V
	POS, PGVDD, DP to PGND Voltage	-0.3 ~ V_{HVINP}+0.3	V
	LXN, HVINN to PGND Voltage	-20 ~ V_{IN}+0.3	V
	NEG, PGVEE, DN, VCOM, PBKG to PGND Voltage	-V_{HVINN}-0.3 ~ 0.3	V
	DGVDD to PGND	-0.3 ~ 30	V
	DGVEE to PGND	-30 ~ 0.3	V
	PGND to GND Voltage	-0.3 ~ 0.3	V
	LXP, LXN, INN, PGND RMS Current	-0.3 ~1.6	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=3.6V and T_A= 25°C.

Symbol	Parameter	Test Conditions	APW7223			Unit
			Min	Typ	Max	
INPUT SUPPLY and REFERENCE VOLTAGE						
V_{IN}	Input Voltage Range		3	-	5.5	V
	IN UVLO Threshold		2.5	2.8	2.95	V
	IN UVLO Hysteresis		-	0.15	-	V
I_{DD1}	IN Quiescent Current	EN=GND and the Shutdown bit=0	-	40	60	µA
I_{DD2}		V_{EN}=3.6V, No Switching	-	2	3.5	mA
	VDD Input Voltage		1.6	-	5.5	V
	VDD UVLO Threshold	V_{VDD} rising	1.0	1.2	1.5	V
	VDD UVLO Hysteresis		-	50	-	mV
	VDD Quiescent Current	Normal Mode	-	20	50	µA
	REF Output Voltage	No Load	-	1.250	-	V
	REF UVLO Threshold	REF Rising	-	1.0	1.2	V
	REF UVLO Threshold		-	50	-	mV

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=3.6V and T_A= 25°C.

Symbol	Parameter	Test Conditions	APW7223			Unit
			Min	Typ	Max	
INPUT SUPPLY and REFERENCE VOLTAGE						
	VDD Quiescent Current	Normal Mode	-	20	50	μA
	REF Output Voltage	No Load	-	1.250	-	V
	REF UVLO Threshold	REF Rising	-	1.0	1.2	V
	REF UVLO Threshold		-	50	-	mV
	REFOK High Threshold	REF rising	-	1.5	-	V
	REFOK Low Threshold	REF falling	-	1.1	-	V
	REF Load Regulation	0 < I_{REF} < 100μA	-	10	20	mV
	REF Line Regulation	3V < V_{IN} < 5.5V	-	2	5	mV
	VREF Output Voltage	No Load (10mV/step)	2.51	2.56	2.61	V
	VREF Output Current		5	-	-	mA
STEP-UP REGULATOR						
V_{HVINP}	Output Voltage Range		V_{IN}	-	18	V
	Operating Frequency		850	1000	1150	kHz
	Oscillator Maximum Duty Cycle		91	95	98	%
	FBP Regulation Voltage		1.238	1.250	1.262	V
	FBP Load Regulation	1mA < I_{POS} < 200mA	-	-1	-	%
	FBP Line Regulation	V_{IN} = 3V to 5.5V	-0.3	-0.08	0.3	%/V
	FBP Input Bias Current	V_{FBP}=1.25V	-	-	100	nA
	LXP On Resistance	I_{LXP} = 0.2A	-	250	500	mΩ
	LXP Leakage Current	EN=GND, V_{LXP} = 18V	-	-	20	μA
	LXP Current Limit	Duty Cycle = 80%	1.5	1.8	-	A
	Soft-Start Period		-	680	-	μs
INVERTING REGULATOR						
	INN Input Voltage Range		3	-	5.5	V
	INN Quiescent Current	No Switching	-	80	-	μA
		Switching	-	0.5	-	mA
V_{HVINN}	Output Voltage Range		-18	-	-	V
	Operating Frequency		850	1000	1150	kHz
	Oscillator Maximum Duty Cycle		91	95	98	%
	LXN On-Resistance	INN to LXN, I_{LXN} = 0.2A	-	250	-	mΩ
	LXN Leakage Current	IN=3.6V, LXN= -18V	-	-	20	μA
	LXN Current Limit	Duty Cycle = 80%	1.8	2.1	-	A
	Soft-Start Current Limit		-	500	-	mA
	V_{POS}-V_{NEG} Regulation Voltage		-50	-	50	mV

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=3.6V and T_A= 25°C.

Symbol	Parameter	Test Conditions	APW7223			Unit
			Min	Typ	Max	
POSITIVE CHARGE PUMP REGULATOR						
	HVINP-DP Current Limit		200	300	-	mA
	Oscillator Frequency		400	500	600	kHz
	FBPG Regulation Voltage		1.238	1.250	1.262	V
	FBPG Line Regulation	V_{HVINP}=12V to 18V	-	0.05	0.2	%/V
	FBPG Input Bias Current	V_{FBPG} = 1.25V	-50	-	50	nA
	DP On-Resistance High	I_{DP} = 100mA	-	20	-	Ω
	DP On-Resistance Low	I_{DP} = -100mA	-	24	-	Ω
	Soft-Start Period		-	2.5	-	ms
NEGATIVE CHARGE PUMP REGULATOR						
	HVINN-DN Current Limit		200	300	-	mA
	Oscillator Frequency		400	500	600	kHz
	FBNG Regulation Voltage		-12	0	12	mV
	FBNG Line Regulation	V_{NEG} = -12V to -18V	-	0.05	0.2	%/V
	FBNG Input Bias Current	V_{FBNG} = 0V	-50	-	50	nA
	DN On-Resistance High	I_{DN} = 100mA	-	20	-	Ω
	DN On-Resistance Low	I_{DP} = -100mA	-	12	-	Ω
	Soft-Start Period		-	2	-	ms
VCOM						
	Input Supply Range		V_{HVINN}	-	-5	V
	HVINN Quiescent Current		-	0.6	5	mA
	VCOMP Voltage High	I_{VCOM} = 5mA	-	-	-0.3	V
	VCOMP Voltage Low	I_{VCOM} = -5mA	-2.85	-	-	V
	VCOM Output Current	Sourcing	100	-	-	mA
		Sinking	100	-	-	mA
	VCOM Tri-State Leakage	CEN=GND	-	-	1	µA
SEQUENCE SWITCHES						
V_{POS}	POS Output Range	Tracks HVINP	V_{IN}	-	18	V
	POS On-Resistance	(HVINP-POS), I_{POS} = 100mA	-	0.5	1	Ω
	POS Discharge Resistance		-	200	-	Ω
	POS Soft-Start Charge Time		-	2	-	ms
V_{NEG}	NEG Output Range	Tracks HVINN	-18	-	-	V
	NEG On-Resistance	(HVINN-NEG), I_{NEG} = 100mA	-	0.5	1	Ω
	NEG Discharge Resistance		-	150	-	Ω
	NEG Soft-Start Charge Time		-	2	-	ms
	PGVDD On-Resistance	(HVINP-PGVDD), I_{PGVDD} = 30mA	-	20	-	Ω
	PGVEE On-Resistance	(HVINN-PGVEE), I_{PGVEE} = 30mA	-	10	-	Ω

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=3.6V and T_A= 25°C.

Symbol	Parameter	Test Conditions	APW7223			Unit
			Min	Typ	Max	
SEQUENCE SWITCHES						
	DGVDD Input Voltage Range		-	-	30	V
	DGVDD Discharge Resistance		-	100	-	Ω
	DGVEE Input Voltage Range		-30	-	0	V
	DGVEE Discharge Resistance		-	150	-	Ω
	VCOM Discharge Resistance		-	1000	-	Ω
FAULT PROTECTION						
	FBP Fault Threshold	V_{FBP} Falling	0.94	1.00	1.05	V
	FBPG Fault Threshold	V_{FBPG} Falling	0.94	1.00	1.05	V
	HVINN Fault Threshold	V_{HVINN} Rising	$-V_{HVINP}$ *0.85	$-V_{HVINP}$ *0.80	$-V_{HVINP}$ *0.75	mV
	FBNG Fault Threshold	V_{FBNG} Falling	200	250	330	mV
	Fault Debounce		-	250	-	µs
	Thermal Shutdown	Hysteresis = 30°C	-	160	-	°C
TEMPERATURE SENSOR						
	Temperature Resolution	Monotonicity guaranteed	10	-	-	Bits
		LSB	-	0.5	-	°C
	Conversion Time		-	19	-	µs
	Conversion Rate	CONF: D7=D6=0	-	250	-	Conv /µs
PROGRAMMABLE VCOM CALIBRATOR						
	VCOM-DAC Voltage Resolution		8	-	-	Bits
	VCOM-DAC Differential Nonlinearity	Monotonic over temperature	-1	-	+1	LSB
	VCOM-DAC Zero-Scale Error		0	+1	+2	LSB
	VCOM-DAC Full-Scale Error		-4	-	+4	LSB
	Memory Factory Setting		-	80	-	Hex
	Memory Program Voltage	Supply to /FLT pin	7.00	7.15	7.3	V
	Memory Write Cycles		8	-	-	times
	Memory Write Time	Need to confirm	TBD	-	-	ms
CONTROL LOGIC						
	Input Low Voltage (IN)	EN, CEN	-	-	0.4	V
	Input High Voltage (IN)	EN, CEN	1.2	-	-	V
	POK Logic-Low Output Voltage	I_{POK} = -6mA	-	-	0.4	V
	/FLT Leakage Current	V_{FLT} = 5.5V	-	-	1	µA
	/FLT Output Low Voltage	I_{FLT} = 6mA	-	-	0.4	V

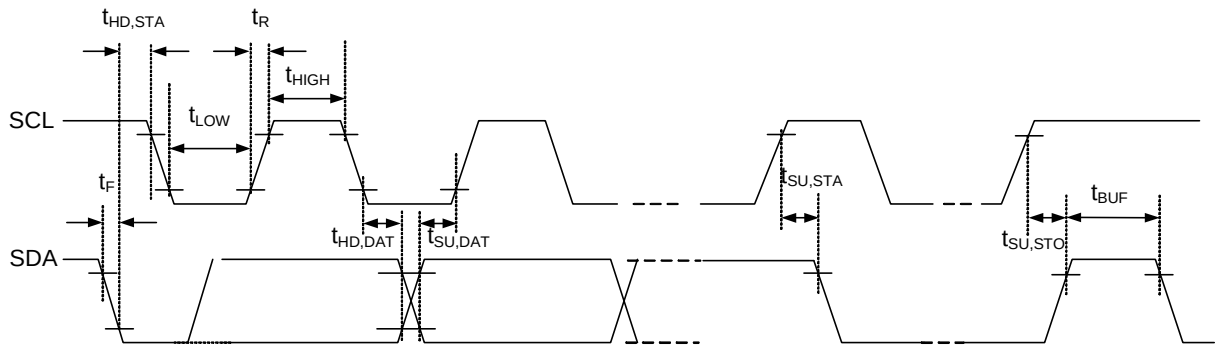
Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=3.6V and T_A= 25°C.

Symbol	Parameter	Test Conditions	APW7223			Unit
			Min	Typ	Max	
I²C INTERFACE						
	Input Capacitance	SDA, SCL	-	5	-	pF
V_{IL}	Input Low Voltage	SDA, SCL	-	-	0.3*V_{VDD}	V
V_{IH}	Input High Voltage	SDA, SCL	0.7*V_{VDD}	-	-	V
	SDA Sink Current	V_{SDA} = 0.4V	6	-	-	mA
F_{SCL}	SCL Frequency		DC	-	400	kHz
t_{HIGH}	SCL High Time		600	-	-	ns
t_{LOW}	SCL Low Time		1300	-	-	ns
t_R	SDA, SCL Rise Time	C_{BUS} = Total Bus Line Capacitance (pF)	20+ 10xC_{BUS}	-	300	ns
t_F	SDA, SCL Fall Time	C_{BUS} = Total Bus Line Capacitance (pF)	20+ 10xC_{BUS}	-	300	Ns
$t_{HD:STA}$	START Hold Time	10% of SDA to 90% of SCL	600	-	-	ns
$t_{SU:STA}$	START Setup Time		600	-	-	ns
$t_{HD:DAT}$	Data Input Hold Time		0	-	-	ns
$t_{SU:DAT}$	Data Input Setup Time		100	-	-	ns
$t_{SU:STO}$	STOP Setup Time		600	-	-	ns
t_{BUF}	Bus Free Time		1300	-	-	ns
	Input Spike Suppression	SDA, SCL	-	-	50	ns
$t_{TIMEOUT}$	SDA Reset Low Time (note 5)		-	-	50	ms

Note 4: Guaranteed by design, not production tested.

Note 5: Holding the SDA line low for a time greater than $t_{TIMEOUT}$ causes the device to reset SDA to the IDLE state of the serial bus communication (SDA set high).



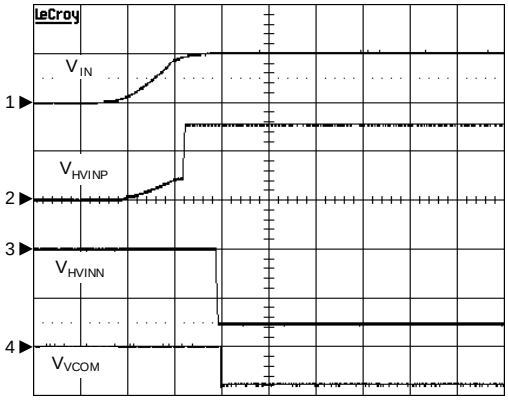
Pin Description

PIN		Function
NO.	NAME	
1	DP	Regulated charge pump driver for GVDD. Connect to flying cap.
2	PGVDD	Supplies the HVINP voltage for the positive charge pump. Connect as shown in Figure 1.
3	FBPG	Feedback input for GVDD. Threshold = 1.25V.
4	DGVDD	Connect the output of the positive charge pump to DGVDD as shown in Figure 1.
5	POK	Power OK. Open drain output that goes low when all outputs have reached regulation.
6	DGVEE	Connect the output of the negative charge pump to DGVEE as shown in Figure 1.
7	REF	IC voltage reference. 1.25V. Connect an 1μF cap to this pin.
8	FBNG	Feedback input for GVEE. Threshold = 0V.
9	PGVEE	Supplies the HVINN voltage to the negative charge pump for the GVEE output. Connect as shown in Figure 1.
10	DN	Regulated charge pump driver for GVEE. Connect to flying cap.
11	VDD	Logic supply input for the I^2C. Bypass to GND through a minimum 0.1μF capacitor.
12	SCL	I^2C Serial clock input.
13	SDA	I^2C Serial data input/output.
14	VREF	Filter pin for 2.5V Internal reference to ADC.
15	TS	Thermistor input pin. Connect a 10k NTC thermistor and a 7kΩ linearization resistor between this pin and GND.
16	EN	Enable pin. Logic high initiates power-up sequencing. Logic low initiates power down sequencing.
17	/FLT	Fault Indicator. Open drain output goes low during a fault condition.
18	CEN	VCOM Enable. Logic high enables VCOM output. Logic low causes the load on the VCOM output to be discharged
19	HVINN	Input power for the NEG voltage rail. Connect the output of the inverting converter to this pin.
20	PGND	Power Ground.
21	GND	Analog Ground. Connected this pin PGND.
22	VCOM	VCOM output.
23	POS	Positive Source Driver Output Voltage.
24	NEG	Negative Source Driver Output Voltage.
25	HVINN	Input power for the NEG voltage rail. Connect the output of the inverting converter to this pin.
26	LXN	DC-DC inverting converter inductor/diode connection.
27	INN	Inverting converter power input. 3V to 5.5V.
28	HVINP	Input power for the POS voltage rail. Connect the output of the Step-up converter to this pin.
29	LXP	Step-up converter inductor/diode connection.
30	PGND	Power Ground.
31	FBP	Feedback pin for HVINP output. Threshold = 1.25V
32	IN	IC power input.
Exposed Pad		Die substrate/thermal pad. Connected this pad to HVINN.

Operating Waveforms

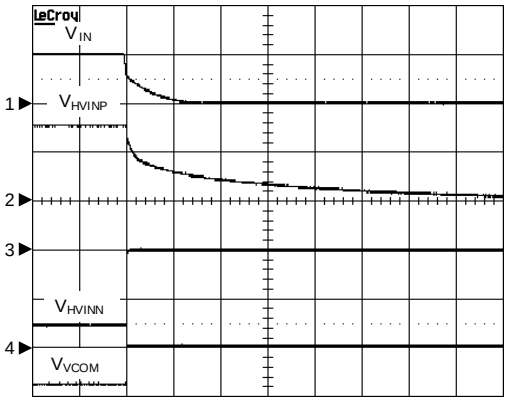
The test condition is V_{IN}=5V, T_A= 25°C unless otherwise specified.

Power On-1



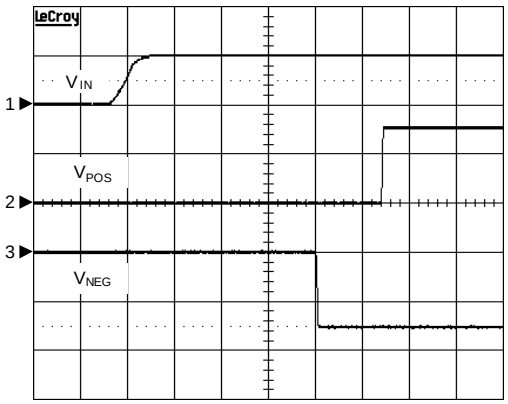
V_{IN} =5V, C1 =C5=22µF, L1=L2=4.7µH, R1=330kΩ, R2=30kΩ, C2=C6=4.7µF, C11=1µF
CH1: V_{IN}, 5V/Div, DC
CH2: V_{HVINP}, 10V/Div, DC
CH3: V_{HVINN}, 10V/Div, DC
CH4: V_{VCOM}, 2V/Div, DC
TIME: 10ms/Div

Power Off-1



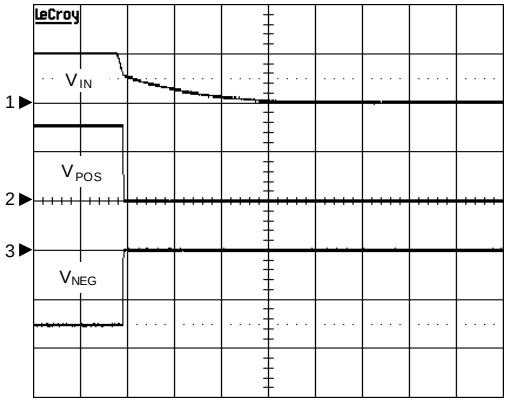
V_{IN} =5V, C1 =C5=22µF, L1=L2=4.7µH, R1=330kΩ, R2=30kΩ, C2=C6=4.7µF, C11=1µF
CH1: V_{IN}, 5V/Div, DC
CH2: V_{HVINP}, 10V/Div, DC
CH3: V_{HVINN}, 10V/Div, DC
CH4: V_{VCOM}, 2V/Div, DC
TIME: 500ms/Div

Power On-2



V_{IN} =5V, C1 =C5=22µF, L1=L2=4.7µH, R1=330kΩ, R2=30kΩ,C2=C6=4.7µF, C3=C4=1µF
CH1: V_{IN}, 5V/Div, DC
CH2: V_{POS}, 10V/Div, DC
CH3: V_{NEG}, 10V/Div, DC
TIME: 20ms/Div

Power Off-2

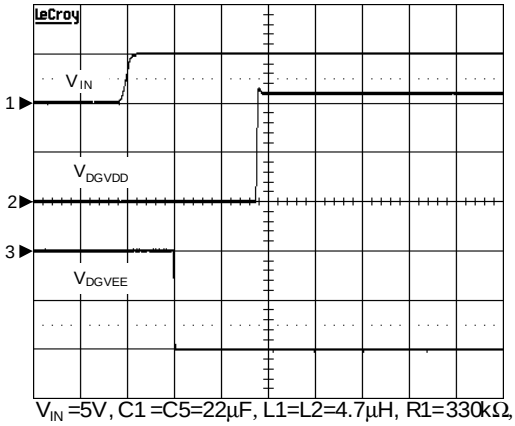


V_{IN} =5V, C1 =C5=22µF, L1=L2=4.7µH, R1=330kΩ, R2=30kΩ, C2=C6=4.7µF, C3=C4=1µF
CH1: V_{IN}, 5V/Div, DC
CH2: V_{POS}, 10V/Div, DC
CH3: V_{NEG}, 10V/Div, DC
TIME: 200ms/Div

Operating Waveforms

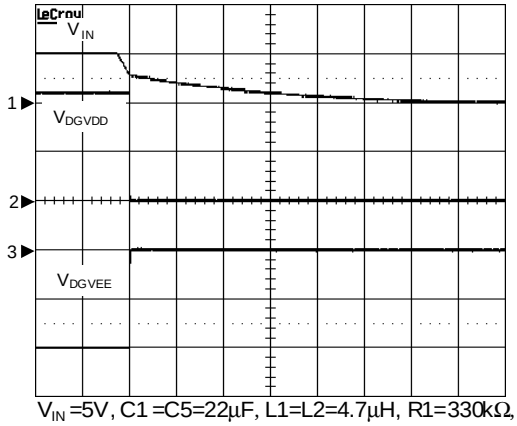
The test condition is V_{IN}=5V, T_A= 25°C unless otherwise specified.

Power On-3



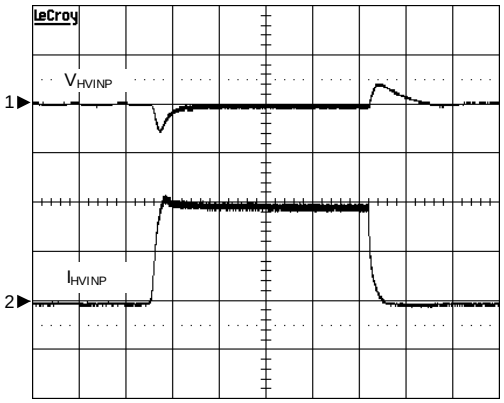
V_{IN} =5V, C1 =C5=22µF, L1=L2=4.7µH, R1=330kΩ, R2=30kΩ, C13=C14=C15=1µF, R11=330kΩ, R12=20kΩ
CH1: V_{IN}, 5V/Div, DC
CH2: V_{DGVDD}, 10V/Div, DC
CH3: V_{DGVEE}, 10V/Div, DC
TIME: 50ms/Div

Power Off-3



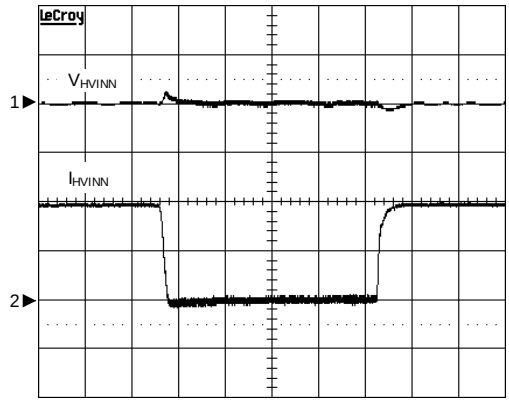
V_{IN} =5V, C1 =C5=22µF, L1=L2=4.7µH, R1=330kΩ, R2=30kΩ, C13=C14=C15=1µF, R11=330kΩ, R12=20kΩ
CH1: V_{IN}, 5V/Div, DC
CH2: V_{DGVDD}, 10V/Div, DC
CH3: V_{DGVEE}, 10V/Div, DC
TIME: 100ms/Div

Load Transient-1



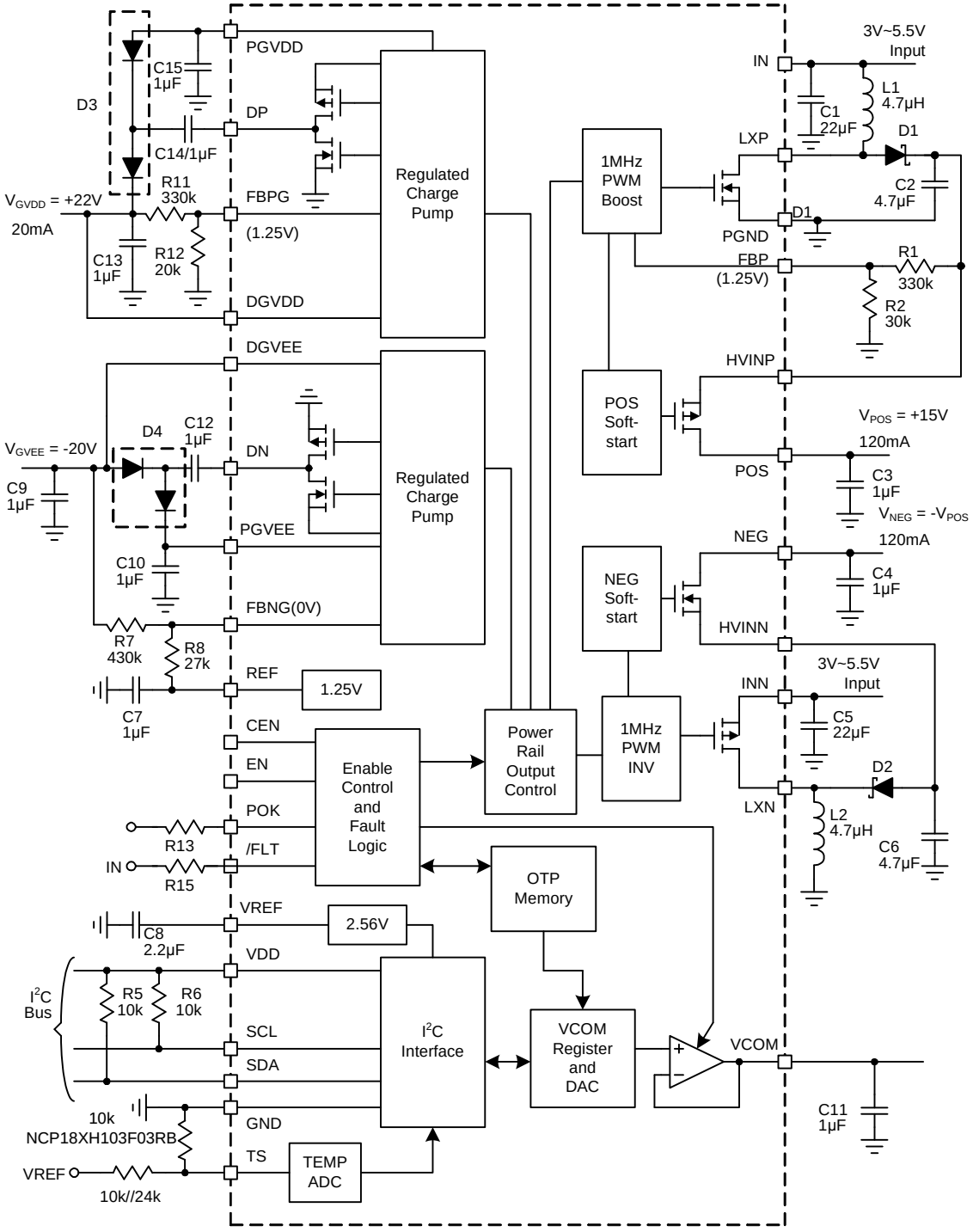
V_{IN} =5V, C1=22µF, C2=4.7µF, L1=4.7µH, R1=330kΩ, R2=30kΩ, I_{HVINP}=0mA-200mA-0mA
CH1: V_{HVINP}, 1V/Div, offset=15V
CH2: I_{HVINP}, 100mA/Div, DC
TIME: 200µs/Div

Load Transient-2



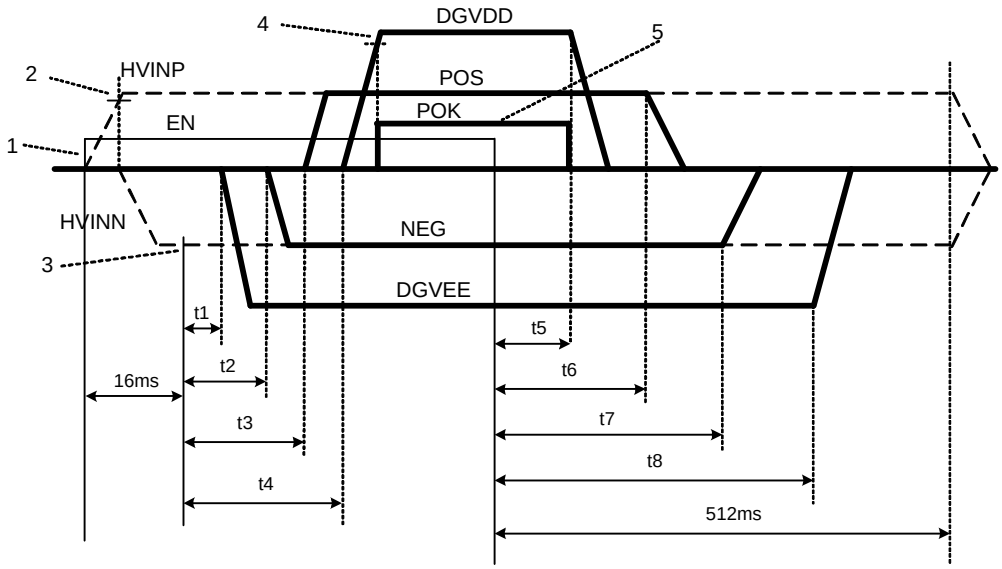
V_{IN} =5V, C5=22µF, C6=4.7µF, L2=4.7µH, I_{HVINN}=0mA-200mA-0mA
CH1: V_{HVINN}, 1V/Div, offset=-15V
CH2: I_{HVINP}, 100mA/Div, DC
TIME: 200µs/Div

Block Diagram and Typical Application Circuit



Note : Forced 3.3V to VREF pin for V_{COM} : -0.3V to -3.59V

Power Sequence



Pulling the EN pin high initiates an adjustable pre-set power-up sequence while pulling the EN pin low initiates an adjustable pre-set power-down sequence. The power-up/power-down sequence and timing between rails are determined by the user's values programmed into the Timing Registers via I^2C before the EN pin is pulled high/low. The desired sequence and timing between rails contained in the Timing Registers can also be stored in the MTP, such that desired timing information is loaded into the Timing Registers at power-up.

Figure 2 shows a sample power-up and power-down sequence. The sequence and timing between the power rails for both power-up and power-down are accomplished by programming the desired t1-t8 times into the Timing Registers and/or storing the desired t1-t8 times into the MTP.

1. The HVINP power rail begins its soft-start sequence once EN is driven high.
2. The HVINN power rails begin its soft-start sequence once HVINP soft-start period has expired.
3. Each power rail will begin to power-up at a time depending on the values stored in the timing registers(t1-t4).
4. POK is asserted high after FBNG, NEG, POS and FBPG have all exceeded 80% of their regulation voltages and all the corresponding power rails' soft-start periods have expired.
5. Once EN goes low, each power rail is actively discharged at a time depending on the values stored in the timing registers (t5-t8). Approximately 512 ms after EN is driven low, HVINP and HVINN are powered down but not actively discharged.

Function Description

Main Control Loop

The APW7223 is a single chip power supplies designed to for portable e-paper displays applications. Two high efficiency DC/DC boost converters generate +/-15V rails which are boosted to +/- 22V by two change pumps to provide the gate driver supply panel. Two tracking LDOs create the +/-15V source driver supplies which support up to 120mA of output current. All rails are adjustable through the I²C interface to accommodate specific panel requirements.

Under-Voltage Lockout

An under-voltage lockout function prevents the device from operating if the input voltage on V_{IN} is lower than approximately 2.8V. The device automatically enters the shutdown mode if the voltage on V_{IN} drops below approximately 2.65V. This under-voltage lockout function is implemented in order to prevent the malfunctioning of the converter.

VCOM

Accurate back-plane biasing is provided by a linear amplifier and can be adjusted either by the I²C interface. The VCOM driver can source or sink current depending on panel condition.

For automatic VCOM adjustment in production line, VCOM can be set from -0.3V to -2.85V with 8 bits control through the serial interface. The power switch is integrated to isolate VCOM driver.

Soft-start

The APW7223 has a built-in soft-start to control the output voltage rise during start-up. During soft-start, an internal ramp voltage, connected to the one of the positive inputs of the error amplifier, raises up to replace the reference voltage (1.25V typical) until the ramp voltage reaches the reference voltage. Then the voltage on FBx regulated at reference voltage.

Pulse Skipping Modulation Mode (PSM)

The APW7223 is a fixed frequency PWM peak current mode control step-down converter. At light loads, the APW7223 will automatically enter in pulse skipping mode operation to reduce the dominant switching losses. These controls get low quiescent current, help to maintain high efficiency over the complete load range.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7223. When the junction temperature exceeds 160°C, a thermal sensor turns off the both power MOSFETs, allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and regulate the output voltage again after the junction temperature cools by 30°C. The OTP designed with a 30°C hysteresis lowers the average Junction Temperature (T_J) during continuous thermal overload conditions, increasing the life time of the device.

Temperature Sensor

The APW7223 allows the user to take full control of the temperature sensing circuit at the expense of additional I²C read/writes and associated software over-head in the main processor. It is designed for use with host processors that can read and write to multiple registers using standard I²C protocol.

Fault Protection

The under-voltage protection circuit monitors the voltage on FBx (V_{FBx}) by Under-Voltage (UV) comparator to protect the PWM converter against short-circuit conditions. When the V_{FBx} falls below the falling UVP threshold (20% of REF), a fault signal is generated and the device turns off all MOSFETs. The converter shuts down and the output is latched to be floating. The APW7223 will initials a soft-start process until re-cycle EN or V_{IN}.

Function Description (Cont.)

Load Disconnected

The APW7223 completely disconnects the loads from the input when in shutdown mode. In most boost converters the external rectifying diode and inductor form a DC current path from the battery to the output. This can drain the battery even in shutdown if a load were connected at the boost converter output. The APW7223 integrated 4 isolated switch at POS/NEG/PGVDD/PGVEE. When these switches turn off during shutdown there is no DC path from the input to POS/NEG/PGVDD/PGVEE.

Application Information

Input Capacitor Selection

Because buck converters have a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes. Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 4.7μF input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the input and GND pin of the device for better performance.

Inductor Selection

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, ΔIL, is 40% of maximum output current. The recommended inductor value can be calculated as below:

$$L \geq \frac{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\cdot \Delta I_L}$$

$I_{L(MAX)} = I_{OUT(MAX)} + 1/2 \times \Delta IL$

To avoid saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

Output Voltage Setting

In the adjustable version, the output voltage is set by a resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing as shown in “Typical Application Circuits”. A suggestion of maximum value of R2 is 400kΩ to keep the minimum current that provides enough noise rejection ability through the resistor divider. The output voltage can be calculated as below:

$$V_{OUT} = V_{REF}\cdot\left(1+\frac{R1}{R2}\right) = 1.25\cdot\left(1+\frac{R1}{R2}\right)$$

Output Capacitor Selection

The current-mode control scheme of the APW7223 allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

I²C Programming

The APW7223's I²C Slave Address is a hard-coded 7 bit address 90h(1001000). The APW7223 supports the following write and read protocol and contains 17 registers.

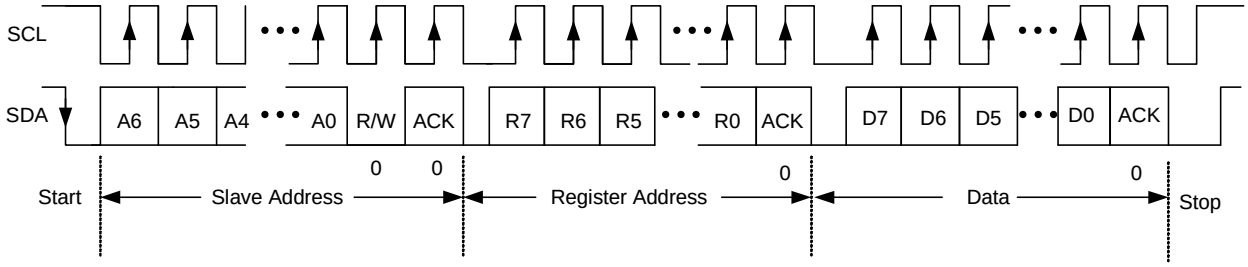


Figure 1. The Write Protocol of I²C interface writing to the APW7223

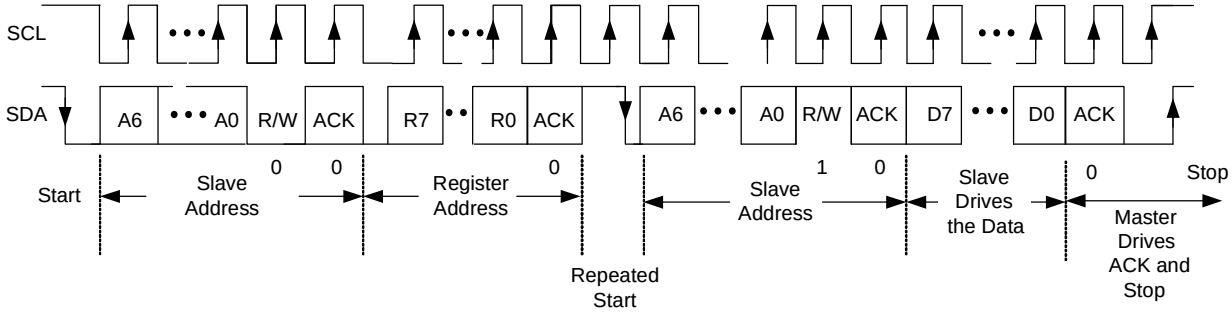


Figure 2. The Read Protocol of I²C interface reading from the APW7223

Register Address Map

Register	Address (Hex)	R/W	Name	Power On Default
1	00	Read only	External Temperature Register	N/A
2	01	R/W	Temperature Offset (for calibration)	00h
3	02	R/W	Configuration Register	N/A
4	03	R/W	Enable Register	00
5	04	R/W	VCOM_ADJUST	80h
6	05	Read only	Fault Register	N/A
7	06	R/W	Programming Control Register	00h
8	07	R/W	t1 Timing Register	1Eh
9	08	R/W	t2 Timing Register	3Ch
10	09	R/W	t3 Timing Register	5Ah
11	0A	R/W	t4 Timing Register	78h
12	0B	R/W	t5 Timing Register	1Eh
13	0C	R/W	t6 Timing Register	3Ch
14	0D	R/W	t7 Timing Register	5Ah
15	0E	R/W	t8 Timing Register	78h
16	0F	Read only	Product Revision ID	00h
17	10	Read only	Product ID	4Dh

Register Definition

Register Address: 00h

Field Name	External Temperature[7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Sign	Temperature Data						
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default								

Field Name	Bit Definition
ExternalTemperature[7:0]	Temperature readout: 1000 0001: -127°C … 1111 1110: -2°C 1111 1111: -1°C 0000 0000: 0°C 0000 0001: +1°C 0000 0010: +2°C … 0111 1111: +127°C When the Configuration register (02h) has been written “01h”, meaning the temperature conversion is shutdown, reading from this ExternalTemperature register will return a NACK.

Register Definition

Register Address: 01h

Field Name	TempOffset[7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Sign	Temperature Offset Code						
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	0	0	0	0	0	0	0	0

Field Name	Bit Definition
TempOffset[7:0]	For some reason the user may want to set a temperature offset from the temperature readout. Temperature Offset Selection 1111 0110: -10°C … 1111 1110: -2°C 1111 1111: -1°C **0000 0000: 0°C** 0000 0001: +1°C 0000 0010: +2°C … 0000 1010: +10°C

Register Address: 02h

Field Name	Configuration[7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved							ShutDown
Read/Write								R/W
Power On Default								0

Field Name	Bit Definition
Configuration[0:0]	**"0h"**: The APW7223 temperature immediately begins a temperature conversion and performs subsequent temperature conversion approximately every 250us. **"01h"**: The APW7223 temperature conversion is shut down. The internal NTC circuit and ADC bias is disabled.

Register Address: 03h

Field Name	Enable[7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved						VCOM_EN	EN
Read/Write							R/W	R/W
Power On Default							0	0

Field Name	Bit Definition
Enable[1:0]	00: V_{COM} and all outputs are disabled. 01: V_{COM} is disabled, the other outputs is enabled. 10: V_{COM} is enabled, the other outputs is disabled (Note) 11: V_{COM} and all outputs are enabled. Note: Because HVINN is disabled, there is no voltage to supply the V_{COM}, resulting V_{COM} no output voltage too.

Register Definition

Register Address: 04h

Field Name	VCOM_ADJUST[7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	VCOM Voltage Code							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	1	0	0	0	0	0	0	0

Field Name	Bit Definition	
	Vcom voltage adjustment	
VCOM_ADJUST[7:0]	VREF=open(VVREF=internal 2.56V) 0000 0000: -0.300V 0000 0001: -0.310V 0000 0010: -0.320V … 1000 0000: -1.58V … 1111 1111: -2.850V	VREF=forced 3.3V 0000 0000: -0.3000V 0000 0001: -0.3129V 0000 0010: -0.3258V … 1000 0000: -1.9514V … 1111 1111: -3.5900V

Register Address: 05h

Field Name	FAULT[7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	POK	OT	HVINN_ FAULT	HVINP_ FAULT	POS_ FAULT	NEG_ FAULT	GVDD_ FAULT	GVEE_ FAULT
Read/Write	R/W	R	R	R	R	R	R	R
Power On Default								

Field Name	Bit Definition
FAULT[7:0]	The POK bit=”1” indicates all outputs voltages have risen above their POK thresholds; otherwise, there is at least one fault occurrence. The OT bit=”1” indicates over temperature has occurred. The HVINN_FAULT bit=”1” indicates the HVINN voltage is not good, and UV or SC is likely happening on it. The HVINP_FAULT bit=”1” indicates the HVINP voltage is not good and UV or SC is likely happening on it. The POS_FAULT bit=”1” indicates the POS voltage is not good and UV or SC is likely happening on it. The NEG_FAULT bit=”1” indicates the NEG voltage is not good and UV or SC is likely happening on it. The GVDD_FAULT bit=”1” indicates the GVDD voltage is not good and UV or SC is likely happening on it. The GVEE_FAULT bit=”1” indicates the GVEE voltage is not good and UV or SC is likely happening on it.

Register Definition

Register Address: 06h

Field Name	ProgrammingControl[7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reversed						TIMING	DVR
Read/Write							R/W	R/W
Power On Default							0	0

Field Name	Bit Definition
ProgramControl[1:0]	This register is used to control a multiplexer which determines the timing t1~t8 and VCOM voltage are programmed by either the registers(eq. timing registers and/or VCOM_ADJUST) or by the OTP(one-time programmable memory) values. The Bit "TIMING" and "DVR" can be separately written and read. When writing "1" to the TIMING and/or DVR bit, the t1~t8 timing and/or VCOM voltage are programmed according to the current values stored in those timing registers(08h~0Fh registers) and/or VCOM_ADJUST register. When writing "0" to the TIMING and/or DVR bit, the t1~t8 timing and/or VCOM voltage are programmed according to the current values stored in the OTP memory. Furthermore, in the meantime writing(Note 1) to the t1~t8 timing registers and/or VCOM_ADJUT register will rewrite the OTP memory's values. The OTP memory can be rewritten for several times: **8 times rewriting for VCOM voltage .** **2 times rewriting for each t1~t8 timing.** When TIMING or DVR bit is "0" and you are writing 08h~0Fh or 04h registers, you will alter the timgings' or VCOM voltage's default values. When the OTP memory is run out, those default values will not be altered. Note 1: In the OTP memory rewriting process, The APW7223 needs a 7.15V voltage to be supplied to the /FLT pin, otherwise OTP values will not be altered.

Register Address: 07h~0Eh

Field Name	Timing[7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Timing code							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power On Default	Various values among 08h~0Fh register, see Bit Definition below							

Field Name	Bit Definition
Timing[7:0]	The t1~t8 timing is programmable by writing following value into corresponding register to meet your application. 0000 0000=0ms 0000 0001=1ms 0000 0010=2ms 0000 0011=3ms 0000 0100=4ms … 1111 1111=255ms The power on default value of t1 (07h register) and t5 (0Bh register) is "1Eh" The power on default value of t2 (08h register) and t6 (0Ch register) is "3Ch" The power on default value of t3 (09h register) and t7 (0Dh register) is "5Ah" The power on default value of t4 (0Ah register) and t8 (0Eh register) is "78h"

Register Definition

Register Address: 0Fh

Field Name	Product Revision ID[7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Reserved				ID code			
Read/Write					R	R	R	R
Power On Default					0	0	0	0

Field Name	Bit Definition
Product Revision ID[3:0]	**This register stores the version code:** First version: “00h” Second version: “01h” Third version: “02h” … … The eighth version:”07h”

Register Address: 10h

Field Name	Product ID[7:0]							
Data Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	Product ID code							
Read/Write	R	R	R	R	R	R	R	R
Power On Default	0	1	0	0	1	1	0	1

Field Name	Bit Definition
Product ID[7:0]	Read only, Product ID=”4Dh”

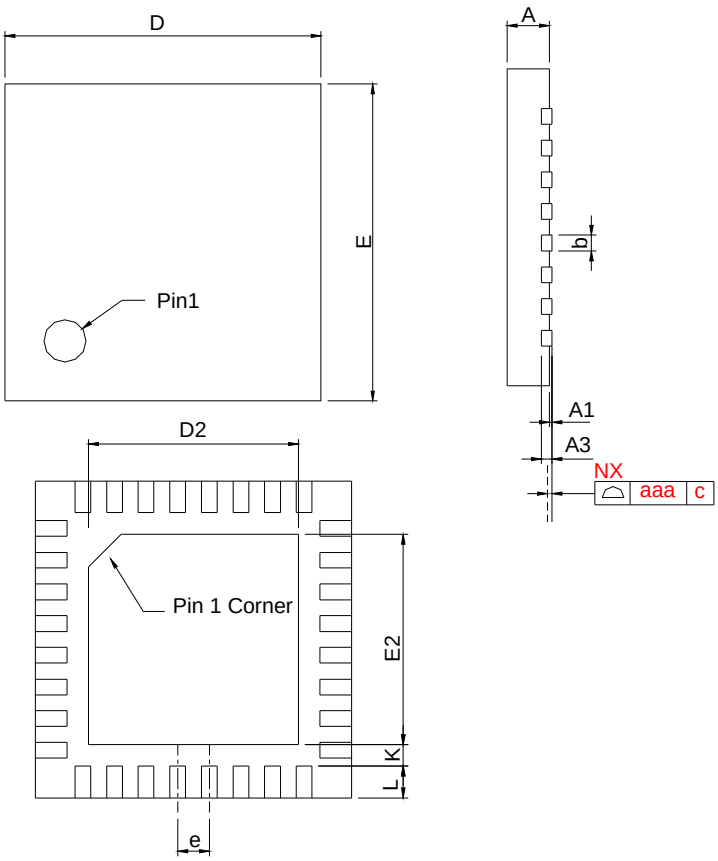
Layout Considerations

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor C1 and C2 should be placed close to the IN/INN and GND. Connecting the capacitor and IN/INN-GND with short and wide trace without any via holes for good input voltage filtering. The distance between IN/GND to capacitor less than 2mm respectively is recommended.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the SW pin to minimize the noise coupling into other circuits.
3. The output capacitor should be place closed to VOUT and GND.
4. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
5. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

Package Information

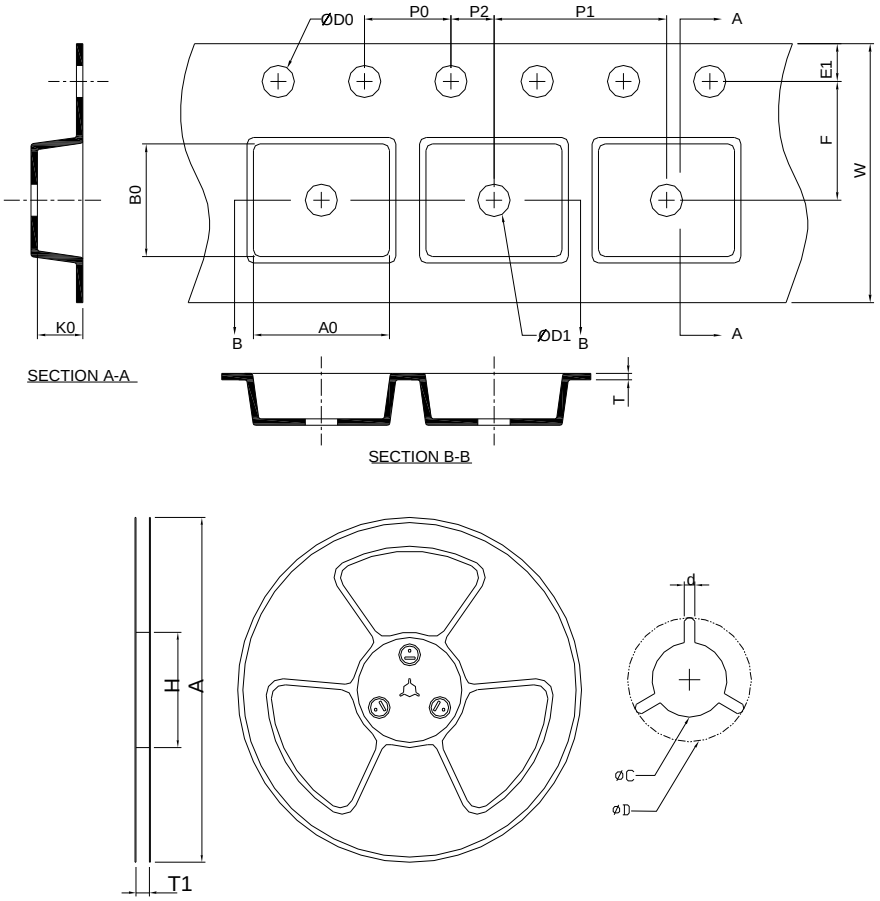
TQFN5x5-32



SYMBOL	TQFN5x5-32			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	4.90	5.10	0.193	0.201
D2	3.50	3.80	0.138	0.150
E	4.90	5.10	0.193	0.201
E2	3.50	3.80	0.138	0.150
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-220 WHHD-4.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN 5x5	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.35±0.20	5.35±0.20	1.00±0.20

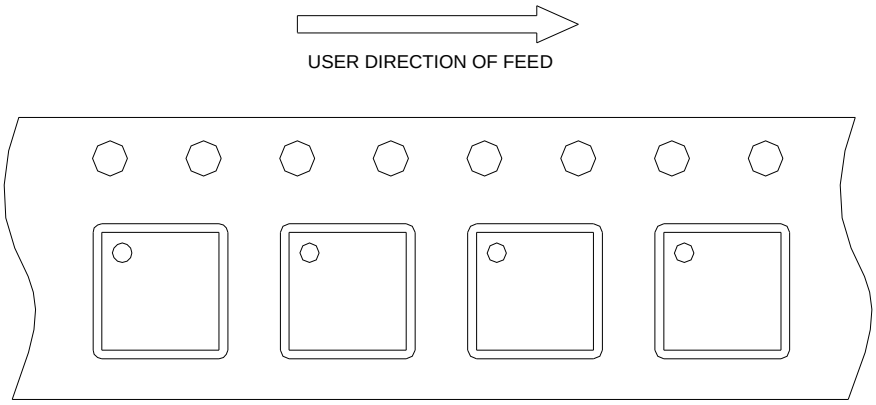
(mm)

Devices Per Unit

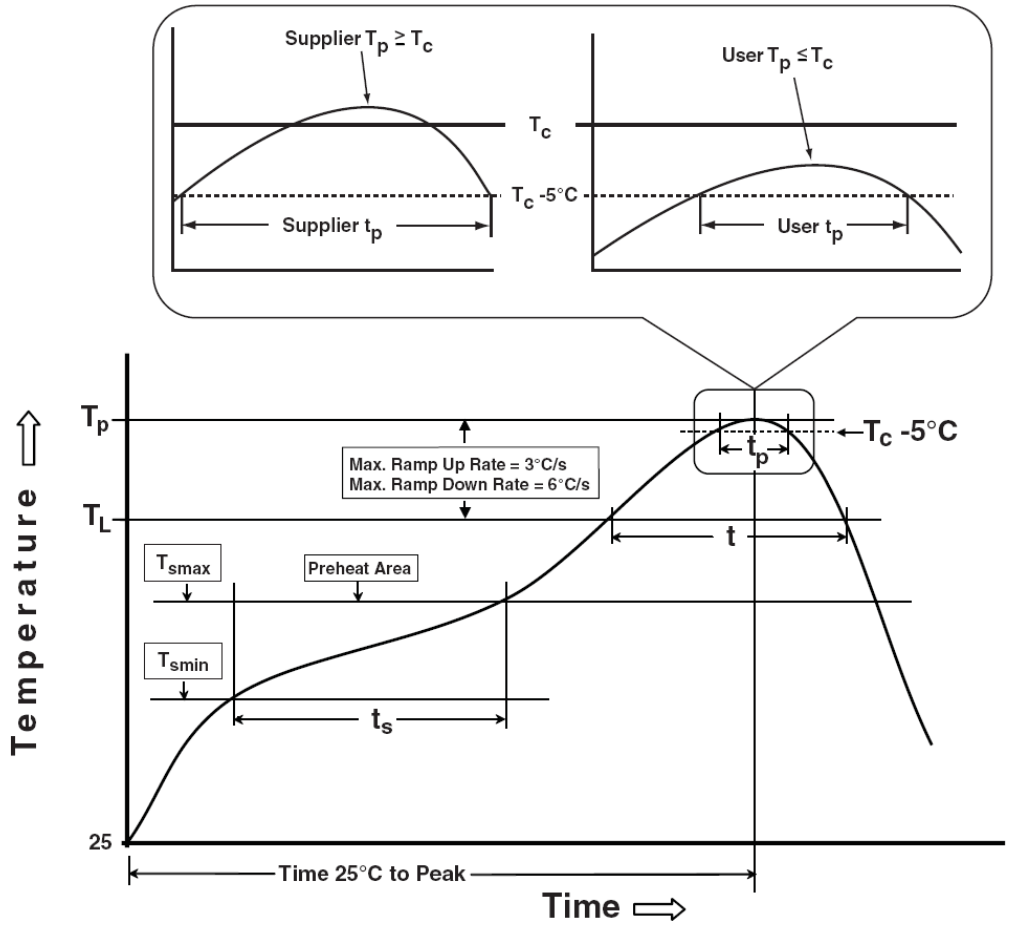
Package Type	Unit	Quantity
TQFN5x5-32	Tape & Reel	2500

Taping Direction Information

TQFN5x5-32



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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