ADVANCE DATA SHEET

■ AC207

2.5V 10/100-TX 8-Port Repeater with Integrated Bridge

GENERAL DESCRIPTION

The AC207 is an unmanaged 8-port 10/100-Mbps repeater with an integrated bridge. The AC207 provides a low-cost and integrated solution for unmanaged repeater applications.

The AC207 is a Class II Repeater. The device provides eight 10/100-Mbps copper media ports. The AC207 also provides one selectable MII/7-wire interface. The MII/7-wire interface can be connected to a MAC. The AC207 provides 10/100-Mbps auto-negotiation and parallel detection for all ports. However, the option to configure each transceiver port via EEPROM interface is available. The AC207 provides two internal repeater state machines, one operating at 10 Mbps and the other at 100 Mbps. Once the technology is set, the device automatically connects each port to the appropriate repeater segment.

The AC207 integrates repeater and bridge technologies with store-and-forward forwarding mechanisms.

FEATURES

- Low power (<1A total current consumption when used with 1.25;1 transformer) eight port 10/100-Mbps repeater with built-in bridge function.
- MDC/MDIO for control/status of transceiver components.
- Eight integrated 10/100-Mbps IEEE 802.3u compliant transceivers.
- Fully integrated adaptive equalizer provides phase/amplitude compensation for various cable lengths up to 30dB @ 100 MHz.
- Patent-pending DC restoration technique reduces offset/baseline wander.
- IEEE 802.3u-compliant auto-negotiation.
- Unique scrambler seed for all port for better EMI.
- Supports in the 9th ports for media independent interface (MII) or 7-wire interface to connect to MAC.
- Non-blocking 10/100M bridge with MAC. One segment of a bridge is fixed to 100 Mbps while the other segment can be configured for 10 or 100 Mbps.
- Bridge functions include:
  - Embedded 32K bytes memory for address table and packet buffer.
  - Local MAC address filtering.
  - XOR hashing scheme.
  - Short routing decision time.
  - Forwarding schemes: store-and-forward.
  - Address table up to 1K entries.
- Programmable LED display for activity, link, speed, partition, utilization, and collision rate.
- Advanced power management includes:
  - Each transceiver port can be turned off independently.
  - Standby mode, which reduces power when the port is not connected.
- Low power 2.5V 0.25µm CMOS implementation with 128-pin QFP package.
- Input tolerance to 3.3V

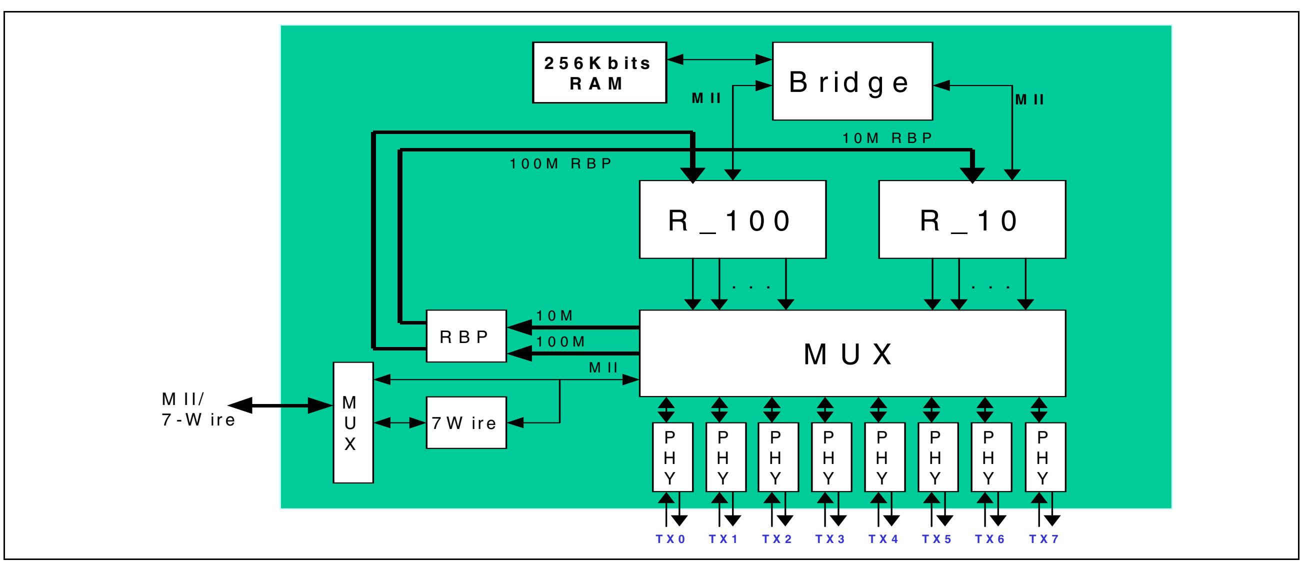

Figure 1: Functional Block Diagram

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Revision History

Revision	*Date*	*Change Description*
AC207-DS04-405-R	07/08/02	Minor text updates.
AC207-DS03-R	06/07/02	Minor technical update.
AC207-DS02-R	06/20/01	Updated tables.
AC207-DS01-R	02/08/01	Updated text in ”Scrambler” subsection of ”Functional Description” to read that “When the BT Control register 23.11 is set to 1 the data scrambling function is disabled, the 5-bit data stream is clocked directly to the device’s PMA sublayer.” Added pin #114 to “DGND” of Table 12, ”Power and Ground,” on page 16. Added pins # 1, 2, 3, 4, 6, 7, 8, 9, 11, 12, 13, 14, 16, 18, 19, 20, 21, 22, 24, 25, 26, 27 to Table 13, ”No Connects,” on page 16. Updated Section 4 ”Electrical Characteristics” and Section 5 ”Digital Timing Characteristics”. Various text changes. Added Section 6 ”Mechanical Information”, outlining packaging specifications. Updated Digital Input Voltage from “–0.5V to Vcc” to “–0.5V to 3.3V” in Section 4 ”Electrical Characteristics”. Updated LED Timing.
AC207-DS00-R	10/9/00	Initial release.

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Section 1: Functional Description

Functional Description

The AC207 is an unmanaged integrated 10/100 Mbps repeater with integrated bridge functions. The device provides eight 10/100BASE-TX twisted pair interface ports. The AC207 includes a built-in 2-segment bridge for 10/100-Mbps connection. The AC207 provides the highest integration chip solution for dual speed hub system. The result is ultra low power consumption that consumes less than 1A maximum when all ports are running 100BASE-TX full-speed. The built-in power management function powers down the individual transceiver ports when not used (no cable detected) which further drives down the power consumption and improves long-term reliability.

Clocks, Reset and Power Management Functions

The AC207 requires a single 25-MHz clock signal at the CLK input pin. An internal PLL generates all of the clock frequencies needed by the device from the single clock input.

The AC207 can be reset in two ways:

1. During initial power-on.
2. Hardware reset: A logic low signal of 10 μs pulse width applies to RST pin.

During reset, all mode pins latch in, the internal address table is initialized, and the internal state machine is reset to known states. At the completion of the reset sequence, all ports are enabled for frame reception and transmission.

The AC207 offers the following power management:

- Power-down mode: Refer to the Power-down register. For example, port 1 has a base address of Hex 00. During power-down, the device is able to respond through the MDC/MDIO interface.
- Energy detects mode: The device powers down all of the unused circuitry when the cable is not installed. The Energy Detect (ED) circuit stays on to monitor incoming signals from the media. The MDC/MDIO interface is turned on in response to any access transaction. The transmit circuit sends out a link pulse with minimum power consumption. If a valid signal is received from the media, the device is powered up and resumes normal transmit/receive operation.

Transceiver and Transmit Function

In 100BASE-TX mode, the Transceiver transmits MLT-3 signal to the cable via isolation transformer. MLT-3 data is a three level signal data. This data is scrambled when transmitted to the media. The MLT-3 data is synchronous to the 25-MHz clock.

In 10BASE-T mode, Manchester code is generated by the 10BASE-T core logic, which synthesizes through the output waveshaping driver. This helps reduce any EMI emission, which eliminates the need for an external filter.

MII

The MII interface is for direct connection of an external device to the repeater. The transmit data on the MII interface is 4-bit nibbles at 25/2.5-MHz rate. This MII interface is connected to the repeater via the MII TXD lines. The external device asserts TX_EN during transmission, or forces an error in the encoded data using TX_ER.

Scrambler

In 100BASE-TX mode, the internal 5-bit transmit data stream is scrambled as defined by the TP-PMD Stream Cipher function in order to reduce radiated emissions on the twisted pair cable. The scrambler encodes a plain text NRZ bit stream using a key stream periodic sequence of 2047 bits generated by the recursive linear function:

```
X [n] = X [n-11] + X [n-9] (modulo 2)
```

The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range, thus eliminating peaks at a single frequency. EMI emission can be further reduced by assigning a unique scrambled seed to each port. When the BT Control register 23.11 is set to 1 the data scrambling function is disabled, the 5-bit data stream is clocked directly to the device’s PMA sublayer.

Parallel to Serial and NRZ – NRZI to MLT-3 Conversion

The internal 5-bit NRZ data is clocked into Transceiver’s shift register with a 25-MHz clock, and clocked out with a 125-MHz clock to convert it into a serial bit stream. Both clocks are generated by an on-chip clock synthesizer, and they are in sync to each other. The serialized data is further converted from NRZ to NRZI format, which produces a transition on every logic 1 and no transition on logic 0. To further reduce EMI emission, the NRZI data is converted to MLT-3 signal. The effect offers a 3 dB to 6 dB reduction in EMI emissions over an un-converted NRZI signals, thus increases the output signals’ margin of operating within the FCC Class B limit.

When there is a transition occurring in NRZI data, there is a corresponding transition for MLT-3 data. For NRZI data, it changes the count up/down direction after every single transition. For MLT-3 data, it changes the count up/down direction after every two transitions. The NRZI to MLT-3 data conversion is implemented without reference to the bit timing or clock information. The conversion requires detecting transition of the incoming NRZI data and set up the count up/down direction for the MLT-3 data. Asserting FX_SEL high bypasses this encoding.

Multimode Transmit Driver

The multimode driver transmits MLT-3 coded signal in 100BASE-TX mode and Manchester coded signal in 10BASE-T mode.

The slew rate of the transmitted MLT-3 signal can be controlled to eliminate high frequency EMI component. The MLT-3 signal after the magnetic has a typical rise/fall time of approximately 4 ns, which is within the target range specified in the ANSI TP- PMD standard.

In 10BASE-T mode, high frequency pre-emphasis is performed which extends the cable-driving distance without the need of an external filter. FLP/NLP also drive out through the 10BASE-T driver. The 10BASE-T and 100BASE-TX transmit signals are multiplexed to the transmit output driver. This arrangement results in using the same external transformer for both the 10BASE-T and the 100BASE-TX. The driver output level is set by a built-in bandgap reference and an external resistor connected to the RIBB output pin. The resistor sets the output current for all modes of operation. Each of the TXOP/N outputs is an open drain device which has a source resistance of 10 Ω maximum and a current rating of 40 mA for the 2 V_{p-p} MLT-3 signal, 100 mA for 5V_{p-p} Manchester signal when used 1:1 transformer.

PLL Clock Synthesizer

The Transceiver also includes on-chip PLL clock synthesizer that generates a 125-MHz and a 25-MHz clock for the 100BASE-TX or a 100-MHz and 20-MHz clock for the 10BASE-T and auto-negotiation operations. The PLL clock generator uses a fully differential VCO cell that induces a very low jitter. The Zero Dead Zone Phase Detection method implemented in this design provides excellent phase tracking. A charge pump with charge sharing compensation is also included to further reduce jitter at different loop filter voltages. On-chip loop filter eliminates the need for external components and avoids external noise pickup. Only one external 25-MHz crystal or a signal source is required as a reference clock.

Receive Function

In 100BASE-TX mode, the receive function implements the reverse order function in the transmit path. It includes a receiver with adaptive equalization and DC restoration, MLT-3 to NRZI conversion, data and clock recovery at 125 MHz, NRZI to NRZ conversion, Serial-to-Parallel conversion, de-scrambling, and 5B to 4B decoding. The receiver circuit starts with a DC bias for the differential RX± inputs, follows with a low-pass filter to filter out high frequency noise from the transmission channel media. An energy detect circuit is also added to determine whether there is any signal energy on the media. This is useful in the power-saving mode. The amplification ratio and slicer threshold is set by the on-chip bandgap reference.

In 10BASE-T mode, signal first passes through a 3^{rd} order lowpass filter, which filters all the noise from the cable, board, and transformer. This eliminates the need for a 10BASE-T external filter. A Manchester decoder and a Serial-to Parallel follows to generate the 4-bit data in MII mode.

Adaptive Equalizer

Each of the eight transceivers is designed to accommodate for maximum cable length of 150 meters UTP CAT5 cable. A 150 meters of UTP CAT-5 cable, such as AT&T 1061, has an attenuation of 31 dB at 100 MHz. A typical attenuation of a 100-meter cable is 20 dB. The worst case attenuation is around 24-26 dB defined by TP-PMD.

The amplitude and phase distortion from the cable causes inter-symbol interference (ISI) which makes clock and data recovery impossible. Adaptive equalizer is done by matching the inverse transfer function of the twist-pair cable. This is a variable equalizer that changes its equalizer frequency response in accordance to cable length. The cable length is estimated based on comparisons of incoming signal strength against some the known cable characteristics. The equalizer has a monotonically frequency response, and tunes itself automatically for any cable length to compensate for the amplitude and phase distortion incurred from the cable.

Link Monitor

Signal levels are detected through a squelch detection circuitry. A signal detect (SD) circuit follows the equalizer and is asserted high when the peak detector detects a post-equalized signal with peak to ground voltage level larger than 400 mV. This is approximately 40% of a normal signal voltage level. In addition, the energy level must be sustained longer than 2~3 µs in order for the signal detects be asserted. It gets de-asserted approximately 1~2 µs after the energy level is consistently less than 300 mV from peak to ground.

In 100BASE-TX mode, when no signal or invalid signal is detected on the receive pair, the link monitor enters in the link fail state where only scrambled idle code is transmitted. When a valid signal is detected for a minimum period of time, the link monitor enters a link pass state and transmit and receive functions are entered.

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the RXIP/RXIN pins for the presence of valid link pulses.

Baseline Wander Compensation

The 100BASE-TX data stream is not always DC balanced. The transformer blocks the DC component of the incoming signal, thus the DC offset of the differential receives inputs can wander. The shift in the signal levels, coupled with non-zero rise and fall times of the serial stream can cause pulse-width distortion, creating jitter and possible increases in error rates. Therefore, a DC restoration circuit is needed to compensate for the attenuation of DC component. The Transceiver implemented is a patent-pending DC restoration circuit, unlike the traditional implementation; it does not need the feedback information from the slicer and clock recovery. This not only simplifies the system/circuit design but also eliminates any random/systematic offset on the receive path. In 10BASE-T mode, the baseline wander correction circuit is not required and is bypassed.

Clock/Data Recovery

The equalized MLT-3 signal passes through a slicer circuit that converts to NRZI format. The transceiver uses a mixed-signal phase locked loop (PLL) to extract clock information of the incoming NRZI data. The extracted clock is used to re-time the data stream and set the data boundaries. The transmit clock is locked to the 25-MHz clock input while the receive clock is locked to the incoming data streams. When initial lock is achieved, the PLL switches to lock to the data stream, extracts a 125-MHz clock and uses that for bit framing to recover data. The recovered 125-MHz clock is also used to generate an internal 25-MHz RX_CLK. The PLL requires no external components for its operation and has high noise immunity and low jitter. It provides fast phase align (lock) to data in one transition and its data/clock acquisition time after power-on is less than 60 transitions. The PLL can maintain lock on run-lengths of up to 60 data bits in the absence of signal transitions. When no valid data is present, i.e. when the SD is de-asserted, the PLL switches back to lock with TX_CLK, and provides a continuously running RX_CLK.

Decoder/Descrambler

The descrambler detects the state of the transmit Linear Feedback Shift Register (LFSR) by looking for a sequence representing consecutive idle codes. The descrambler acquires lock with the data stream by recognizing IDLE bursts of 30 or more bits and locking to its de-ciphering Linear Feedback Shift Register (LFSR).

Once lock is acquired, the device operates with the inter-packet-gap (IPG) as low as 40 ns. Before lock occurs, the de-scrambler requires a minimum of 720 nS of idle in between packet in order to acquire lock.

The deciphering logic also tracks the number of consecutive receive errors detected while RX_DV is asserted. Once the error counter exceeds its limit (currently set to 64 consecutive errors), the logic assumes that lock has been lost, and the de-cipher circuit resets itself. The process of regaining lock begins again.

Stream cipher de-scrambler is not used in 10BASE-T mode.

Auto-Negotiation and Miscellaneous Functions

Each of the Transceiver contains the ability to negotiate its mode of operation over the twisted pair using the auto-negotiation mechanism defined in the clause 28 IEEE 802.3u specification. Auto-negotiation may be disabled by software via EEPROM. The Transceiver automatically chooses its mode of operation by detecting the incoming signal.

During auto-negotiation, the auto-negotiation advertisement register is sent to its link partner through a series of fast link pulse (FLP). When auto-negotiation enabled, transceiver sends FLP during the following conditions: a) power-on, b) link loss, and c) restart command. At the same time, the device monitors incoming data to determine its mode of operation. Parallel detection circuit is enabled as soon as 10BASE-T idle or 100BASE-TX idle is detected. The mode of operation is configured based on the technology of the incoming signal. When the device receives a burst of FLP from its link partner with 3 identical link code words (ignoring acknowledge bit), it stores these code words in the auto-negotiation link partner ability register and waits for the next 3 identical code word. Once the device detects the second code word, it configures itself to the highest technology that is common to both ends. The technology priorities are 1) 100BASE-TX, half-duplex, 2) 10BASE-T half-duplex. Once auto-negotiation is complete, the status register reflects the actual speed that was chosen.

Parallel Detection

The Transceiver also checks for 10BASE-T NLP or 100BASE-TX idle symbols. If either is detected, the device automatically configures to match the detected operating speed in half-duplex mode. This ability allows the device to communicate with legacy 10BASE-T and 100BASE-TX systems.

Carrier Sense/RXDV for MII Port Only

Carrier sense is asserted asynchronously on the CRS pins as soon as activity is detected on the receive data stream. RX_DV is asserted as soon as a valid SSD (Start-of-Stream Delimiter) is detected. Carrier sense and RX_DV are de-asserted synchronously upon detection of a valid end of stream delimiter or two consecutive idle code groups in the receive data stream. If carrier sense is asserted and a valid SSD is not detected immediately, RX_ER is asserted instead of RX_DV.

In 10BASE-T mode, carrier sense is asserted asynchronously on the CRS pin when valid preamble activity is detected on the RXIP/RXIN pins. In half-duplex mode, the CRS is activated during transmit and receive of data.

Cable Length Monitor

The AC207 can also detect the length of the cable and display the result in the interrupt control/status register, i.e., 0000 stands for < 10m cable used, 0001 stands for ~ 10 meter of cable, 1111 stands for 150 meter cable. It detects the proper connectivity of the cable and helps to manage the cable distribution.

Bridge Function

MII Interface

The bridge supports MII for 10/100 Mbps. Port 0 of the bridge can support either 10 or 100, while port 1 supports only at 100 Mbps. Refer to the mode pin table to configure port 0.

Forwarding Scheme

The bridge supports the store-and-forward scheme only. It does not support cut-through-forward. With store-and-forward, the incoming packet should be completely received to the buffer without error before it can be sent out.

Address Recognition

The self-learning bridge function is based on source address field of packets. The bridge uses the XOR hashing algorithm to address look-up table. Programmable aging time and fast aging control is supported.

Reset and Restart

At the power-on, the bridge initially goes to SRAM self-test mode. It generates 8 patterns to evaluate SRAM status.

Media Access Control

The Bridge MAC compiles with certain IEEE 802.3 MAC protocols such as frame formatting and collision handling but does generate CRC codes. It generates a 56-bit preamble and start of frame delimiter while a packet is sending. In half-duplex mode, the device listens before transmitting, to prevent traffic jam. During collision, a packet is retransmitted at a random time.

Initialization and Setup

Hardware Configuration

Several different states of operation can be chosen through hardware configuration. External pins may be pulled high or low at reset time. The combination of high and low values determines the power-on state of the device.

Many of these pins are multi-function pins which change their meaning when reset ends.

Software Configuration

Several different states of transceiver operation may be chosen through the MDC/MDIO interface. Refer to Section 3: "Register Descriptions" on page 17.

LEDs

Using an LED display matrix with a refresh technique, only 14 pins are required to drive up to 48 LEDs with unique information. On, Off, and Flash states are used to indicate different information. With a reduced number of signals, the LED display is easier to route on the board, and less costly. The active-low LED data is driven out of LED_D[0:7] pins for each port and the corresponding LED functions are LED_LN[5:0] pin. Refer to "LED Display/Configuration/PROM Interface" on page 15 and "LED Display Matrix" on page 34 for the details.

The AC207 supports 2 LEDs per port. The following table describes how each of the LED is connected.

Signals LED_D[2:6] are indicators of port 1 through 8. Signals LED_LN[0:5] are events driven of port 1 through 8.

Table 1: LED Connections

<table>
<tr><th>Signals</th><th>Events</th><th colspan="9">Descriptions</th></tr>
<tr><td>LED_LN[0]</td><td>Link status/activity</td><td colspan="9">Active low indicates 100M link is good. Blinking indicates 100M activity.</td></tr>
<tr><td>LED_LN[1]</td><td>Speed/partition</td><td colspan="9">Active low indicates 10M link is good. Blinking indicates 10M activity.</td></tr>
<tr><td rowspan="3">LED_LN[2]</td><td rowspan="3">Display utilization on bridge segment A (100 Mbps)</td><td colspan="9">LED_LN[2] is active low, indicating 100M utilization. Utilization indicator is not per port basis, but rather per segment basis. The LED_D[0:7] indicates percentage of utilization.</td></tr>
<tr><td>LED_D[0:7]</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Percent Util.</td><td>non</td><td>non</td><td>85%</td><td>65%</td><td>45%</td><td>25%</td><td>12%</td><td>1%</td></tr>
<tr><td rowspan="3">LED_LN[3]</td><td rowspan="3">Display utilization on bridge segment B
(10 Mbps)</td><td colspan="9">LED_LN[3] is active low, indicating 10M utilization. Utilization indicator is not per port basis, but rather per segment basis. The LED_D[0:7] indicates percentage of utilization.</td></tr>
<tr><td>LED_D[0:7]</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Percent Util.</td><td>non</td><td>non</td><td>non</td><td>65%</td><td>45%</td><td>25%</td><td>12%</td><td>1%</td></tr>
<tr><td rowspan="3">LED_LN[4]</td><td rowspan="3">Display collision on bridge segment A (100 Mbps)</td><td colspan="9">LED_LN[4] is active low, indicating collision. Collision indicator is not per port basis, but rather per segment basis. The LED_D[1:7] indicates percentage of collision. However, LED_D0 only indicates collision occurrence.</td></tr>
<tr><td>LED_D[0:7]</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Percent Col.</td><td>66%</td><td>32%</td><td>16%</td><td>8%</td><td>4%</td><td>2%</td><td>1%</td><td>Col.</td></tr>
<tr><td rowspan="3">LED_LN[5]</td><td rowspan="3">Display collision on bridge segment B (10 Mbps)</td><td colspan="9">LED_LN[5] is active low, indicating collision. Collision indicator is not per port basis, but rather per segment basis. The LED_D[1:7] indicates percentage of collision. However, LED_D0 only indicates collision occurrence.</td></tr>
<tr><td>LED_D[0:7]</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Percent Col.</td><td>66%</td><td>32%</td><td>16%</td><td>8%</td><td>4%</td><td>2%</td><td>1%</td><td>Col.</td></tr>
</table>

ADDRESSING ALGORITHM, ROUTING, LEARNING AND AGING

ADDRESS TABLE

The address table can store up to 1K entries and each entry consists of 48-bit MAC address, 8-bit port identifier, 1-bit indication flag and 6-bit aging timer.

Table 2: Content of Address Lookup Table

3130				**0**
V	Timer	Port#	MAC#1	MAC#2
MAC#3		MAC#4	MAC#5	MAC#6

Bit 30: Entry valid / empty indication, 1: valid entry, 0: empty entry.

Bit 29-24: Aging timer.

Bit 23-16: Port number

Address Recognition

The exclusive or addressing algorithm is used for address lookup table addressing. Refer to Figure 2.

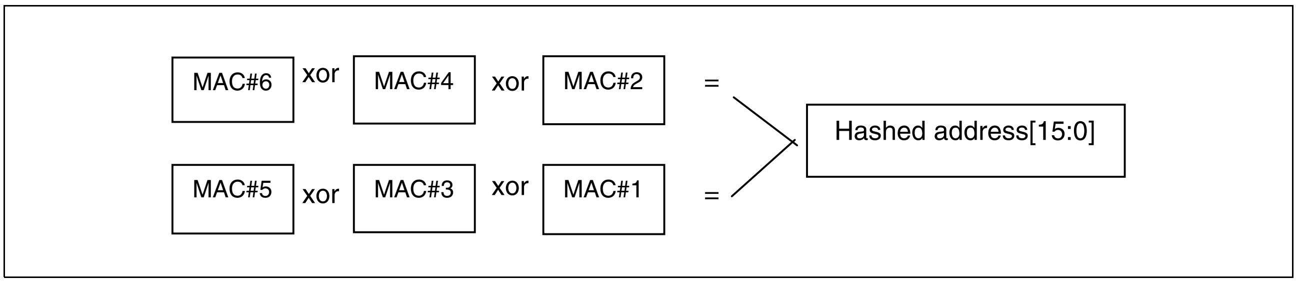

Figure 2: Exclusive or Hashing Algorithm

The final address of address lookup table is the hashed address[9:0].

Routing Decision

If a record is empty, the packet is broadcast and treated as an unknown frame. Otherwise, the record is read, and compared with the current DA. If two addresses are the same, the port number is decided, and the packet is forwarded to the assigned port. If address collision occurred, different MAC address, the incoming packet is considered an unknown packet.

Learning Process

The address learning process is composed of the SA packets and the addressing algorithm described above. The bridge checks each incoming packets integrity and buffers availability. If a packet is error-free and the buffer is available, the SA/ port number pair of the packet is written into the address lookup table. Figure 3 describes the general operations of address learning and recognition.

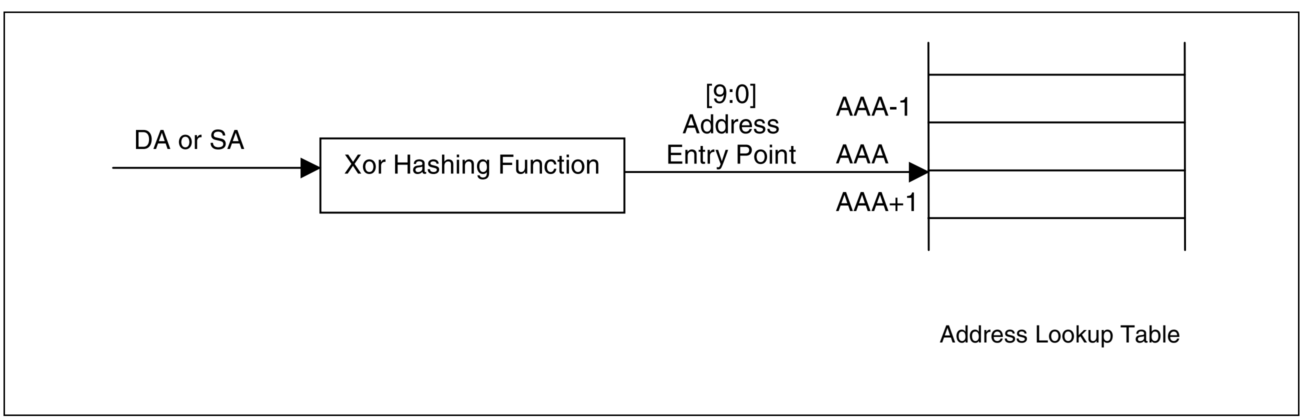

Figure 3: Address Learning and Recognition

Aging Time

The bridge automatically examines the status of address lookup table. The round robin speed and checking timer are dependent on the aging time. The bridge aging time is set at 300 seconds. When the aging timer is started after power-on, the bridge guaranties that free spaces can be released from occupied address entries.

Forwarding Scheme

The store-and-forward algorithm is used. The incoming packet has to be completely stored in the buffer and verified error-free before forwarding operations take place.

Buffer Management and Queues

The bridge buffering management continues to store received packets into memory. The buffer size for 100M port is 16K bytes, and 8K bytes for 10M port.

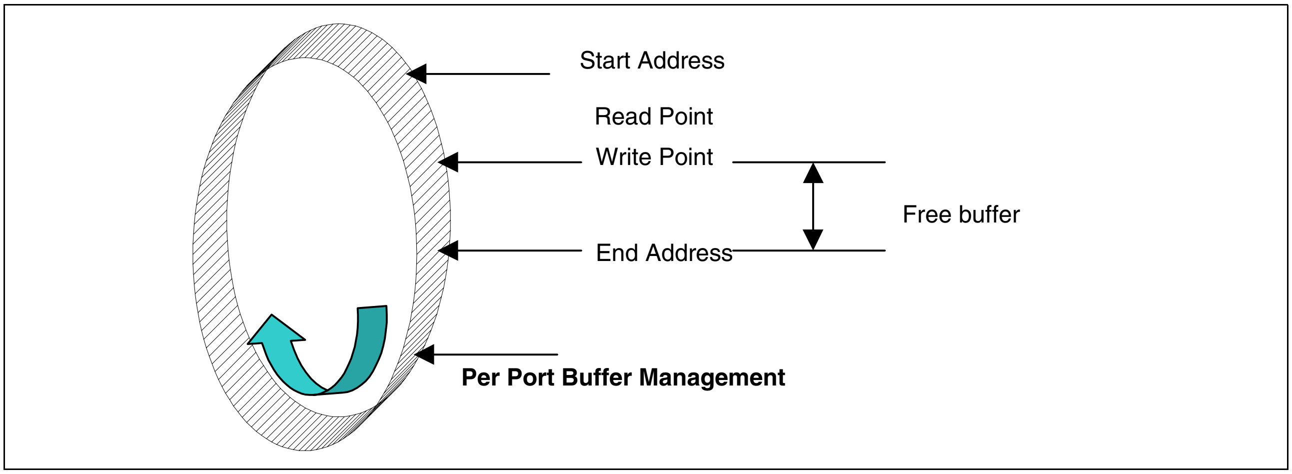

Figure 4: Basic Memory Management Concept

The bridge uses the six pointers to control per port buffer status. Start Address point is the beginning of memory address for each port and the End Address point is the last address of memory for each port. The Read/Write and shadow Read/Write pointers are dynamically changed depending on the current outgoing and incoming packets in the storage. If the Write pointer reaches the Read pointer and the size between write and read pointers is smaller than 2K bytes, buffer is full. On the other hand, when read/write pointers are equal, the buffer is empty.

Table 3: Embedded Memory Structure

	31	0
0x0000	2k x 32 for address lookup table	
0x07FF		
0x0800	4k x 32 for 100M Bridge Port	
0x17FF		
0x1800	2k x 32 for 10M Bridge Port	
0x1FFF		

Section 2: Pins

PIN DESCRIPTIONS

Many of these device pins have multiple functions. The separate descriptions of each pin are listed in the proper sections. Designers must assure that they have identified all modes of operation prior to final design.

The pin assignment shown below and in the pin description table are subjected to change without notice. The user is advised to contact Altima Communications Inc. before implementing any design based on the information provided in this data sheet.

Signals types:

I = Input

O = Output

Z = High impedance

U = Pull up with 10k ohm

D = Pull down with 10k ohm

S = Schimitt Trigger

A = Analog signal

P = Power

G = Ground

* = Active Low Signal

Table 4: MDI (Media Dependent Interface) Pins (TX)

Pin Name	Pin #	Type	Description
RXP_7	107	AI	Receiver input positive for both 10BASE-T and 100BASE-TX.
RXP_6	96	AI	
RXP_5	95	AI	
RXIP_4	84	AI	
RXIP_3	83	AI	
RXIP_2	72	AI	
RXIP_1	71	AI	
RXIP_0	60	AI	
RXIN_7	106	AI	Receiver input negative for both 10BASE-T and 100BASE-TX.
RXIN_6	97	AI	
RXIN_5	94	AI	
RXIN_4	85	AI	
RXIN_3	82	AI	
RXIN_2	73	AI	
RXIN_1	70	AI	
RXIN_0	61	AI	
TXOP_7	104	AO	Transmitter output positive for both 10BASE-T and 100BASE-TX.
TXOP_6	99	AO	
TXOP_5	92	AO	
TXOP_4	87	AO	
TXOP_3	80	AO	
TXOP_2	75	AO	
TXOP_1	68	AO	
TXOP_0	63	AO	
TXON_7	103	AO	Transmitter output negative for both 10BASE-T and 100BASE-TX.
TXON_6	100	AO	
TXON_5	91	AO	
TXON_4	88	AO	
TXON_3	79	AO	
TXON_2	76	AO	
TXON_1	67	AO	
TXON_0	64	AO	

Table 5: MII (Media Independent) Pins

Pin Name	Pin #	Type	Description
MII_TXD3 MII_TXD2 MII_TXD1 MII_TXD0	44 43 42 41	I,D	MII transmit data. The MAC sources MII_TXD[3:0] synchronous with MII_TXCLK when MII_TXEN is asserted.
MII_TXCLK	33	O,D,S	MII transmit clock. Continuous (25 MHz/2.5 MHz) clock output used by MAC to synchronize MII_TXEN, MII_TXD[3:0], and MII_TXER.
MII_TXEN	40	I,D	MII transmit enable. Indicates MAC has presented valid data on the MII_TXD[3:0].
MII_RXD3/MII_SPDSEL MII_RXD2/MODE3 MII_RXD1/TP125 MII_RXD0	38 37 36 35	I/O,U I/O,D I/O,U O,U	MII receive data. The Phy will source MII_RXD[3:0] synchronous with MII_RXCLK when MII_RXDV is asserted. After power-on, the MII_SPDSEL is latched for port speed selection. 1=100Mb, 0=10Mb
MII_RXCLK	31	O,D,S	MII transmit clock. continuous (25 MHz/2.5 MHz) clock output used by MAC to synchronize MII_RXDV, MII_RXD[3:0], and MII_RXER.
MII_RXDV	28	O,D	MII Receive data-valid. Phy has presented valid recovered on the MII_RXD[3:0].
MII_CRS	29	O,D	MII carrier sense. Active when carrier has been sensed.
MII_RXER	34	O,D	MII receive error. Indicates Phy has received invalid symbol data.
MII_COL	30	O,D	MII collision detection. Active when collision is detected.

Table 6: 7-wire (Serial Network Interface) Pins

Pin Name	Pin #	Type	Description
SNI_TXD (MII_TXD0)	41	I,D	Serial transmit data. The MAC sources SNI_TXD synchronous with SNI_TXCLK when SNI_TXEN is asserted.
SNI_TXCLK (MII_TXCLK)	33	O	Serial transmit clock. continuous (10 MHz) clock output used by MAC to synchronize SNI_TXEN and SNI_TXD.
SNI_TXEN (MII_TXEN)	40	I,D	Serial transmit enable. Indicates MAC has presented valid data on the SNI_TXD.
SNI_RXD (MII_RXD0)	35	O	Serial receive data. The Phy sources SNI_RXD synchronous with SNI_RXCLK when SNI_CRS is asserted.
SNI_RXCLK (MII_RXCLK)	31	O	Serial receive clock. Continuous (10 MHz) clock output used by MAC to synchronize SNI_CRS and SNI_RXD.
SNI_CRS (MII_CRS)	29	O	Serial carrier sense. Active when carrier has been sensed.
SNI_COL (MII_COL)	30	O	Serial collision detection. Active when collision is detected.

Table 7: EEPROM Interface

Pin Name	Pin #	Type	Description
PROM_CS	127	O	PROM chip select. Connected to Chip Select pin of 93C46 serial EEPROM.
PROM_CLK (LED_D[6])	124	O	PROM clock. Connected to CLK pin of 93C46 serial EEPROM.
PROM_OUT (LED_D[5])	123	O	PROM data out. Connected to Data_In pin of 93C46 serial EE-PROM.
PROM_IN (LED_D[7])	125	I,D	PROM data in. Connected to Data_Out pin of 93C46 serial EE-PROM.

Table 8: MDC/MDIO Interface

Pin Name	Pin #	Type	Description
MDC (PROM_CS)	127	I,U	Clock signal between the external device and PHY registers for communication synchronization.
MDIO	128	I/O,D	Data input/output. It is a bi-directional data interface used by the external manager to access internal PHY registers within AC207. This pin has internal pull-down register.

LED Display/Configuration/PROM Interface

The LED pins are shared with reset-read configuration pins, test pins and EEPROM interface. The value applied on the reset-read pins is only valid at the end of the reset cycle. The EEPROM interface is active after the reset cycle. Once the data in the EEPROM is read, the same pins are used for LED display. 48 LED outputs are available through an 6x8 matrix.

Table 9: LED Pins

Pin Name	Pin #	Type	Description
LED_LN[5] LED_LN[4] LED_LN[3] LED_LN[2] LED_LN[1] LED_LN[0]	50 51 52 53 54 55	O 48 mA	Enable corresponding LED display line in the display matrix, active low output. The detail of how to program and connect the LEDs is in the LED Setup section. LED_LN*[5]: Display 10BT collision rate and segment collision status. LED_LN*[4]: Display 100-Mbps Collision rate and segment collision status LED_LN*[3]: Display 10M segment utilization rate LED_LN*[2]: Display 100M segment utilization rate LED_LN*[1]: Programmable LED display. The default is to display 10M Link/Activity information of each port. LED_LN*[0]: Programmable LED display. The default is to display 100M Link/Activity information of each port.
LED_D[7] LED_D[6] LED_D[5] LED_D[4] LED_D[3] LED_D[2] LED_D[1] LED_D[0]	125 124 123 122 121 120 119 118	I/O, D	Output for LED display information of each column in the display matrix. Active high output.

Table 10: Configuration and Set-up

Pin Name	Pin #	Type	Description
Mode[3] (MII_RXD2) Mode[2] (LED_D[4]) Mode[1] (LED_D[1]) Mode[0] (LED_D[0])	37 122 119 118	I,D	Mode[3:2] MII 00 MII 01 7-wire 10 not used 11 not used
TP125 (MII_RXD1)	36	I	1:select 1:1.25 xformer
ChipID[1] (LED_D[2]) ChipID[0] (LED_D[3])	120 121	I,D	The device must be assigned with ChipID=0
IBREF	112	I	Reference bias resistor. Connected to analog ground through a 10k (1%) resistor.

Table 11: Clock and Reset

Pin Name	Pin #	Type	Description
RESET*	47	I,U	Reset to initial and defaulted state.
CLK	48	I	25-MHz-system-clock reference input. This pin shall be connected to an external 25-MHz-clock source. Multiple devices should be synchronous to the same external clock source.

Table 12: Power and Ground

Pin Name	Pin #	Type	Description
DVCC	115, 126, 10, 23, 39, 46	P	2.5V power for digital circuit, total of 9 pins.
DGND	114, 116, 117, 5, 15, 32, 45, 49	G	Ground for digital circuit, total 10 pins.
AVCC	108, 109, 110, 57, 58, 59	P	2.5V power for analog circuit, total 16 pins.
AGND	105, 62, 65, 66, 69, 74, 77, 78, 81, 86, 89, 90, 93, 98, 101, 102	G	Ground for analog circuit, total 16 pins
GAVDD	113	P	2.5V power supply for common analog circuit
GAGND	111, 56	G	Ground for common analog circuit

Table 13: No Connects

Pin Name	Pin #	Type	Description
N/C	1, 2, 3, 4, 6, 7, 8, 9, 11, 12, 13, 14, 16, 17, 18, 19, 20, 21, 22, 24, 25, 26, 27	N/C	No Connects

Section 3: Register Descriptions

The following standard registers are supported. (Register numbers are in Decimal format, the values are in Hex format).

NOTE: When writing to registers, it is recommended that a read/modify/write operation be performed, as unintended bits may get set to unwanted states. This applies to all registers, including those with reserved bits.

Register Description

AC207 register sets are listed below. Each register contains 16-bit data. The addresses shown below are hexadecimal.

Table 14: Register Set

PHY Addr	*Offset Addr*	*Definition*	*Type*	*Default*
8	0 – 4	PHY Port Status registers	–	–
8	0	PHY port link status	RO	–
8	1	PHY port polarity status	RO	–
8	2	PHY port partition status for 100 Mb	RO	–
8	3	Port partition status for 10 Mb	RO	–
8	4	PHY port speed status	RO	–
8	5	PHY port isolation status	RO	–
8	6	Initial Device Configuration register	R/W	–
8	7	Bridge Configuration register	R/W	–
8	8	Device revision number	RO	–
0	0 – 31	PHY 1 registers	–	–
0	0	PHY Control register	R/W	3000
0	1	PHY Status register	RO	2849
0	2	PHY Identifier 1 register	RO	0022
0	3	PHY Identifier 2 register	RO	5541
0	4	Auto-Negotiation Advertisement register	RO	00A1
0	5	Auto-Negotiation Link Partner Ability register	RO	0001
0	6	Auto-Negotiation Expansion register	RO	0004
0	7	Auto Negotiation Next Page Transmit register	RO	2001
0	8 – 15	Reserved	–	0000
0	16	PHY 10BASE-T Control register	R/W	–

Table 14: Register Set (Cont.)

PHY Addr	Offset Addr	Definition	Type	Default
0	17	PHY Interrupt Control/Status register	–	–
0	18	Diagnostic register	–	–
0	19	Test register	RO	–
0	20	Cable Length register	RO	–
0	21	Receive error count	–	–
0	22	Power Management register	–	–
0	23	Transceiver Mode register	–	–
0	24 – 31	Reserved	–	–
1	0 – 31	PHY 2 registers	–	–
2	0 – 31	PHY 3 registers	–	–
3	0 – 31	PHY 4 registers	–	–
4	0 – 31	PHY 5 registers	–	–
5	0 – 31	PHY 6 registers	–	–
6	0 – 31	PHY 7 registers	–	–
7	0 – 31	PHY 8 registers	–	–
8	0 – 31	LED Effect registers	–	–
8	16	Reserved	–	–
8	17	Reserved	RO	0000
8	18	LED effect with partition/isolation event	R/W	–
8	19	LED effect with link event	R/W	–
8	20	LED effect with activity (CRS) event	R/W	–
8	21	LED effect with auto-neg event	R/W	–
8	22	LED effect with speed100 event	R/W	–
8	23	LED register control mode	R/W	–

PHY PORT STATUS REGISTER

Table 15: PHY Port Status Register

Name	Type	Address	Description
PHY Port Link Status	R	00	1: Link good, default = 0.
PHY Port Polarity Status	R	01	1: the polarity has been crossed, default = 0.
PHY Port Partition Status for 100Mb	R	02	1: the port has been partitioned, default = 0.
PHY Port Partition Status for 10Mb	R	03	1: the port has been partitioned, default = 0.
PHY Port Speed Status	R	04	1: 100M, 0:10M, default = 0.
PHY Port Isolation Status (Fast Ethernet only)	R	05	1: the port has been isolated, default = 0.

Table 16: PHY Port Status

15:9	8	7	6	5	4	3	2	1	0
RSV	MII	Port 8	Port 7	Port 6	Port 5	Port 4	Port 3	Port 2	Port 1

Initial Device Configuration Register

Table 17: Initial Device Configuration Register

Name	Type	Address	Description
MII Configuration	R/W	06	Used to give the status of MII port. Default is set by pin.

Bit	Name	Type	Description		Default
15:12	Mode	RO	Mode[3:0]	Digital Interface	MODE pins
			0000	MII	
			0100	7-wire	
			Others	Reserved	
11	Reserved (write clear enable)	RO			
10	Reserved (MIB enable)	RO	Reserved		0
9	Disable partition	R/W	1:disable partition function of MII interface		0
8	External transform selection	R/W	1:external transform 1:1.25, 0:external transform 1:1		Ext pin
7	MIIB speed select	R/W	1:100M interface, 0:10M interface		Ext Pin
6:2	Switch debug	R/W	Selection control for debugging signals		00000
1	100M repeater partition alternative	R/W	0: normal, un-partition a port only when data can be transmitted out from the port for 560 bit-time without a collision. 1: alternate, un-partition a port when data can be either transmitted from the port or received from the port for 560 bit-time without a collision.		0
0	10M repeater partition alternative	R/W	0: normal, un-partition a port when data can be either transmitted from the port or received from the port for 560 bit-time without a collision. 1: alternate, un-partition a port only when data can be received from the port for 560 bit-time without a collision		0

BRIDGE CONFIGURATION REGISTER

Table 18: Bridge Configuration Register

Name	Type	Address	Description
Bridge Configuration register	R/W	07	Used to configure Bridge.

Bit	Name	Type	Description	Default
15	Watchdog reset	R/W	1:reset when WDOG even occur. 0:dosen't reset when WDOG even occur.	1
14	Loose length	R/W	1:receives frame with length from 1519 to 1548. 0:rejects frame with length over 1518.	1
13	Dribble error	R/W	1:enable, 0:disable receive dribble error packets.	0
12	Address table initialization disable	R/W	1:disable, 0:enable address table init. While this bit is 1, the address table only contains few entries for speed up function verification.	0
11	Aging speed up	R/W	1:enable, 0:disable aging speed up.	0
10	10M back pressure	R/W	1:enable, 0:disable 10M back pressure function.	0
9	100M back pressure	R/W	1:enable, 0:dieable 100M back pressure function.	0
8	Collision test	R/W	1:enable, 0:disable collision test.	0
7:0	Reserved	R		00

PHY REGISTERS

The following registers are defined for each PHY port. The base addresses of PHY 1 to PHY 8 are 0, 1, 2, 3, 4, 5, 6, and 7 respectively.

PHY CONFIGURATION REGISTER

Table 19: PHY Configuration Register 0

Bit	Name	Definition	Mode	Default
0.15	Reset	1 = PHY reset This bit is self-clearing.	RW/SC	0
0.14	Loopback	1 = Loopback mode, which internally loop the transmit of AC207 to its receive, thus it will ignore all the activity on the cable media. 0 = Normal operation.	RW	0
0.13	Speed select	1 = 100 Mbps 0 = 10 Mbps. This bit will be ignored if auto-negotiation is enabled. It will no longer reflect auto-negotiation result.	RW	1
0.12	Auto-neg enable	1 = Enable auto-negotiate process (overrides 0.13 and 0.8) 0 = Disable auto-negotiate process. In force mode, speed is selected via bit 0.13.	RW	1
0.11	Power-down	1 = Power-down mode, which puts AC207 in low-power stand-by mode, which only reacts to access transaction. 0 = Normal operation.	RW	0
0.10	Isolate	1 = Electrical isolation of PHY from MII and cable media. 0 = Normal operation.	RW	0
0.9	Restart auto-negotiation	1 = Restart auto-negotiation process. 0 = Normal operation.	RW/ SC	0
0.8	Duplex mode	1 = Full-duplex. 0 = Half-duplex. Full-duplex is not supported on this chip. It will no longer reflect auto-negotiation result.	RO	0
0.7	Collision test	1 = Enable collision test, which issues the COL signal in response to the assertion of TX_EN signal. 0 = Disable COL test.	RW	0
0.6:0	Reserved		RO	000000

PHY Status Register

Table 20: PHY Status Register 1

Bit	Name	Definition	Mode	Default
1.15	100BASE-T4	Tied to zero indicates no 100BASE-T4 capability.	RO	0
1.14	100BASE-TX full-duplex	Tied to zero indicates no 100BASE-TX full-duplex support.	RO	0
1.13	100BASE-TX half-duplex	1 = 100BASE-TX with half-duplex. 0 = No TX half-duplex ability.	RO	1
1.12	10BASE-T full-duplex	Tied to zero indicates no 10BASE-T full-duplex support.	RO	0
1.11	10BASE-T half-duplex	1 = 10BASE-T with half-duplex. 0 = No 10BASE-T half-duplex ability.	RO	1
1.10:6	Reserved		RO	00001
1.5	Auto-negotiate complete	1 = Auto-negotiate process completed, indicates Reg. 4, 5, 6 are valid. 0 = Auto-negotiate process not completed.	RO	N/A
1.4	Remote fault	1 = Remote fault condition detected. 0 = No remote fault. After this bit is set, it will remain set until it is clear by reading register 1 via MDC/MDIO interface.	SC/LH	N/A
1.3	Auto-negotiate ability	1 = Able to perform auto-negotiation function, its value is determined by ANEGA pin. 0 = Unable to perform auto-negotiation function.	RO	1
1.2	Link status	1 = Link is established, however, if AC207 link fails, this bit will become cleared and remain cleared until register is read via MDC/MDIO interface. 0 = Link is down, or have been dropped.	SC/LL	0
1.1	Jabber detect	1 = Jabber condition detect. 0 = No Jabber condition detected.	SC/LH	0
1.0	Extended capability	1 = Extended register capable. This bit is tied permanently to one.	RO	1

PHY Identifier 1 Register

Table 21: PHY Identifier 1 Register

Register Bit	Name	Description	Mode	Default
2.15:0	OUI*	Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	0022 (HEX)

PHY Identifier 2 Register

Table 22: PHY Identifier 2 Register

Register Bit	Name	Description	Mode	Default
3.15:10	OUI	Assigned to the 19th through 24th bits of the OUI.	RO	010101
3.9:4	Model number	Six bit manufacturer's model number; 101 is encoded as 010001.	RO	010100
3.3:0	Revision number	Four bits manufacturer's revision number. 0001 stands for Rev. A, etc.	RO	0001

Auto-Negotiation Advertisement Register

Table 23: Auto-Negotiation Advertisement Register

Bit	Name	Definition	Mode	Default
4.15	Next page	1 = Desire Next Page. 0 = Next Page is not desired.	RW	0
4.14	Acknowledge	This bit will be set internally after receiving 3 consecutive and consistent FLP bursts.	RO	0
4.13	Remote fault	1 = Remote fault detected. 0 = No remote fault.	RW	0
4.12:10	Reserved	For future technology.	RW	000
4.9	100BASE-T4	Tied to zero indicates no 100BASE-T4 support.	RO	0
4.8	100BASE-TX full-duplex	1 = 100BASE-TX with full-duplex. 0 = No 100BASE-TX full-duplex ability.	RO	0
4.7	100BASE-TX	1 = 100BASE-TX capable. 0 = No 100BASE-TX capability.	RW	1
4.6	10BASE-T full-duplex	1 = 10 Mbps with full-duplex. 0 = No 10 Mbps with full-duplex capability.	RO	0
4.5	10BASE-T	1 = 10 Mbps capable. 0 = No 10 Mbps capability.	RW	1
4.4:0	Selector field	[00001] = IEEE 802.3.	RO	00001

AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER

Table 24: Auto-Negotiation Link Partner Ability Register

Register Bit	Name	Description	Mode	Default
5.15:0	Technology	Technology capability field, which indicates the technology capability of link partner. The bit definition is the same as Reg. 4.15:0.	RO	0001(H)

AUTO-NEGOTIATION EXPANSION REGISTER

Table 25: Register 6: Auto-Negotiation Expansion Register

Register Bit	Name	Description	Mode	Default
6.15:5	Reserved		RO	0000 0000 000
6.4	Parallel detection fault	1 = Fault detected by parallel detection logic. This is caused by unstable link, or concurrent link up condition. 0 = No fault detected by parallel detection logic.	SC/LH	0
6.3	Link partner next page able	1 = Link partner supports next page function. 0 = Link partner does not support next page function.	RO	0
6.2	Next page able		RO	1
6.1	Page received	1 = A new link code word has been received. The contains of the received link code word is located in register 5.	SC/LH	0
6.0	Link partner auto-negotiation able	1 = Link partner is auto-negotiation able. 1 = Link partner is not auto-negotiation able.	RO	0

AUTO-NEGOTIATION NEXT PAGE TRANSMIT REGISTER

Table 26: Auto-Negotiation Next Page Transmit Register

Register Bit	Name	Description	Mode	Default
7.15	NP	1 = Another next page is desired.	RW	0
7.14	Reserved		RO	0
7.13	Message page	1 = Message page. 0 = Un-formatted Page.	RW	1
7.12	ACK2	Acknowledge2. 1 = Will comply with message. 0 = Can not comply with message.	RW	0
7.11	Toggle	1 = Previous value of transmitted link code word equal to 0. 0 = Previous value of transmitted link code word equal to 1.	RO	N/A
7:10:0	Code	Message/un-formatted code field.	RW	0001

PHY 10BASE-T Configuration Register

Table 27: PHY 10BASE-T Configuration Register

Register Bit	Name	Description	Mode	Default
16.14	Reserved		RO	0
16.13	TXJAM	1=Force CIM to send jam pattern. 0=Normal operation mode	RO	0
16.12	CIM disable	1 = Disable carrier integrity monitor function. 0 = Enable carrier integrity monitor function. Default is 0.	RW	1
16.11	SEQ test inhibit	1 = Disable 10BASE-T SEQ testing. 0 = Enable 10BASE-T SEQ testing, which will generate a COL pulse following the completion of a packet transmission.	RW	0
16.10	BT normal loop back	1 = Enable 10BASE-T normal loop back. 0 = Disable 10BASE-T normal loop back.	RW	0
16.[9:6]	Reserved		RO	0
16:5	Auto polarity disable	1 = Disable auto-polarity detection/correction. 0 = Enable auto-polarity detection/correction.	RW	0
16.4	Reverse polarity	When Reg16.5 is set to 0, this bit will set to 1 if Reverse Polarity is detected on the media, otherwise it will be zero. When Reg16.5 is set to 1, writing a one to the bit will reverse the polarity of the transmitter. Note: the reverse polarity is detected either through 8 inverted NLP or through a burst of inverted FLP.	RW	0
16:[3:0]	Reserved		RO	0

PHY Interrupt Control/Status Register

Table 28: PHY Interrupt Control/Status Register

Register Bit	Name	Description	Mode	Default
17.15	Jabber_IE	Jabber Interrupt Enable.	RW	0
17.14	Rx_Er_IE	Receive Error Interrupt Enable.	RW	0
17.13	Page_Rx_IE	Page Received Interrupt Enable.	RW	0
17.12	PD_Fault_IE	Parallel Detection Fault Interrupt Enable.	RW	0
17.11	LP_Ack_IE	Link Partner Acknowledge Interrupt Enable.	RW	0
17.10	Link_Schange_ IE	Link Status Changed Interrupt Enable.	RW	0
17.9	R_Fault_IE	Remote Fault Interrupt Enable.	RW	0
17.8	Aneg_Comp_IE	Auto-Neg Complete Interrupt Enable.	RW	0
17.7	Jabber_Int	This bit is set when a jabber event is detected.	RC	0
17.6	Rx_Er_Int	This bit is set when RX_ER transitions high.	RC	0
17.5	Page_Rx_Int	This bit is set when a new page is received from link partner during Auto-Negotiation.	RC	0
17.4	PD_Fault_Int	This bit is set when parallel detect fault is detected.	RC	0
17.3	LP_Ack_Int	This bit is set when the FLP with acknowledge bit set is received.	RC	0
17.2	Link_Schanged Int	This bit is set when link status is changed.	RC	0
17.1	R_Fault_Int	This bit is set when remote fault is detected.	RC	0
17.0	A_Neg_Comp Int	This bit is set when Auto-Neg is completed.	RC	0

Diagnostic Register

Table 29: Diagnostic Register

Register Bit	Name	Description	Mode	Default
18.15	Lp_lpbk	Link pulse loopback. 1 = loopback the link pulse for auto-negotiation testing	RW	0
18.14	Send_nlp	1 = force link pulse generator to send nlp event in auto-negotiation mode.	RW	0
18.13	Force link pass bt	1 = force 10BASE-T link pass	RW	0
18.12	Force link pass tx	1 = force 100 TX link pass	RW	0
18.11	DPLX	This bit indicates the result of the Auto-Neg for duplex arbitration.	RO	0
18.10	Speed	This bit indicates the result of the Auto-Neg for data speed arbitration.	RO	X
18.9	RX_PASS	In 10BT mode, this bit indicates that Manchester data has been detected. In 100BT mode, it indicates valid signal has been received but not necessarily locked on to.	RC	X
18.8	RX_LOCK	Indicates the receive PLL has locked onto the received signal for the selected speed of operation (10BASE-T or 100BASE-TX). This bit is set whenever a cycle-slip occurs, and will remain set until it is read.	RC	X
18.[7:4]	ARB_STATE HIGHEST	Highest state of auto-negotiation state machine since reset on last read operation.	RC	TBD
18.[3:0]	ARB_STATE LOWEST	Lowest state of auto-negotiation state machine since reset on last read operation.	RC	TBD

Cable Length Register

Table 30: Cable Length Register

Register Bit	Name	Description	Mode	Default
20.[15:9]	Reserved		RO	0000000
20.8	Adaptation disable	1 = Disable adaptation	RW	0
20.[7:4]	Cable length indication	These bits are to indicate cable length from 0 to 150 meters. Each bit represents 10 meters. For example, if the cable length is 100 meters then bits [7:4] = 1010. These bits are only applicable to 100TX mode.	RW	XXXX
20.[3:0]	Adaptation low limit	Adaptation setting, when SD signal is first detected.	RO	XXXX

Receive Error Count

Table 31: Receive Error Count

Register Bit	Name	Description	Mode	Default
21.[15:0]	Receive error count	Count number of receiving packets with error. This register can only be cleared by reset (software or hardware).	RO	0000

Power Management Register

Table 32: Power Management Register

Register Bit	Name	Description	Mode	Default
22.[15:14]	Reserved		RO	00
22.13	PD_PLL	1=Power-down PLL circuit	RO	X
22.12	PD_EQUAL	1=Power-down equalizer circuit	RO	X
22.11	PD_BT_RCVR	1=Power-down 10BASE-T receiver	RO	X
22.10	PD_LP	1=Power-down link pulse receiver	RO	X
22.9	PD_EN_DET	1=Power-down energy detect circuit	RO	X
22.8	PD_FX	1=Power-down FX circuit	RO	X
22.[7:6]	Reserved		RW	00
22.5	MSK_PLL	0=Force power-up PLL circuit	RW	X
22.4	MSK_EQUAL	0=Force power-up equalizer circuit	RW	X
22.3	MSK_BT_RCVR	0=Force power-up 10BASE-T receiver	RW	X
22.2	MSK_LP	0=Force power-up link pulse receiver	RW	X
22.1	MSK_EN_DET	0=Force power-up energy detect circuit	RW	X
22.0	MSK_FX	0=Force power-up FX circuit	RW	X

Transceiver Mode Register

Table 33: Transceiver Mode Register

Register Bit	Name	Description	Mode	Default
23.15	Reserved		RO	0
23.14	Reserved		RO	0
23.13	Clk_rclk_save	1 = set rclk save mode. Rclk will be shut off after 64 cycles of each packet	RW	0
23.12	Reserved		RO	0
23.11	Scramble disable	1 = disable scrambler	RW	0
23.10	Serial bt enable	1 = enable serial bt mode	RW	0
23.9	Pcsbp	1 = enable PCS bypass mode	RW	0
23:8	Age timer en	1 = enable age timer in adaptation 0 = disable age timer in adaptation.	RW	0
23.7	Reserved		RO	0
23:6	Reserved		RO	0
23.5	Force re-adapt	1 = force adaptation to re-adapt Write 1 to this bit will force adaptation to re-adapt. This bit will always be read as 0.	RO	0
23.[4:0]	Dlock drop counter	D lock drop counter	RO	XXXXX

Test and LED Effect Register

This set of the registers is defined for the whole chip. The base address is hex 08.

LED Effect with Partition/Isolation Event

Table 34: LED Effect with Partition/Isolation Event

Register Bit	Name	Description	Mode	Default
15:12	Blink rate [7:4]	Set the blink rate bits [7:0] with LED Effect with Partition/Isolation Event Register (PHY Addr = 8; Reg Addr = 18), abbreviated as REG_LED_EFFECT in the following equation. Blink Rate = 1 / (16ms x {REG_LED_EFFECT[15:12], 4‘b0000} x 2)	RW	0001
11:10	Reserved		RO	00
9:8	LED on with part/ ISO event	When partition/isolation, turn on corresponding LED 1:0.	RW	00
7:6	Reserved		RO	00
5:4	LED blink with part/ ISO event	When partition/isolation, blink corresponding LED 1:0.	RW	00
3:2	Reserved		RO	00
1:0	LED off with part/ ISO event	When partition/isolation, turn off corresponding LED 1:0.	RW	00

LED Effect with Link Event

Table 35: LED Effect with Link Event

Register Bit	Name	Description	Mode	Default
15:10	Reserved		RO	00000
9:8	LED on with link event	When link up, turn on corresponding LED 1:0.	RW	11
7:6	Reserved		RO	00
5:4	LED blink with link event	When link up, blink corresponding LED 1:0.	RW	11
3:2	Reserved		RO	00
1:0	LED off with link event	When link up, turn off corresponding LED 1:0.	RW	00

LED Effect with Activity (CRS) Event

Table 36: LED Effect with Activity (CRS) Event

Register Bit	Name	Description	Mode	Default
15:10	Reserved		RO	00000
9:8	LED on with activity event	When activity, turn on corresponding LED 1:0.	RW	00
7:6	Reserved		RO	00
5:4	LED blink with activity event	When activity, blink corresponding LED 1:0.	RW	11
3:2	Reserved		RO	00
1:0	LED off with activity event	When activity, turn off corresponding LED 1:0.	RW	00

LED Effect with Auto-Negotiating Event

Table 37: LED Effect with Auto-Negotiating Event

Register Bit	Name	Description	Mode	Default
15:10	Reserved		RO	00000
9:8	LED on with auto-negotiating event	When auto-negotiating, turn on corresponding LED 1:0.	RW	00
7:6	Reserved		RO	00
5:4	LED blink with auto-negotiating event	When auto-negotiating, blink corresponding LED 1:0.	RW	00
3:2	Reserved		RO	00
1:0	LED off with auto-negotiating event	When auto-negotiating, turn off corresponding LED 1:0.	RW	00

LED EFFECT WITH SPEED100 EVENT

Table 38: LED Effect with Speed100 Event

Register Bit	Name	Description	Mode	Default
15:10	Reserved		RO	00000
9:8	LED on with Speed100 event	When Speed100, turn on corresponding LED 1:0.	RW	01
7:6	Reserved		RO	00
5:4	LED blink with Speed100 event	When Speed100, blink corresponding LED 1:0.	RW	01
3:2	Reserved		RO	00
1:0	LED off with Speed100 event	When Speed100, turn off corresponding LED 1:0.	RW	10

LED REGISTER CONTROL MODE

Table 39: LED Register Control Mode

Register Bit	Name	Description	Mode	Default
15:8	LED data	Set value shown on the LED_D[7:0].	RW	000000
7:6	Reserved		RO	00
5:0	LED column	Control which lane of the LED_D should be turned on.	RW	000000

EEPROM TABLE

EEPROM is used to configure the initial setting of the bridge, repeater, and transceiver.

Table 40: EEPROM

Address	Description	Default	Assign To
0	First word	5A3C	
1	Test Configuration register0	0080	PHY=8, Reg=28
2	Initial Repeater Configuration register	0180	PHY=8, Reg=6
3	Bridge Configuration register	D000	PHY=8, Reg=7
4	Initialize Port 0 Configuration register	3000	PHY=0, Reg=0
5	Initialize Port 1 Configuration register	3000	PHY=1 Reg=0
6	Initialize Port 2 Confutation register	3000	PHY=2, Reg=0
7	Initialize Port 3 Configuration register	3000	PHY=3, Reg=0
8	Initialize Port 4 Configuration register	3000	PHY=4, Reg=0
9	Initialize Port 5 Configuration register	3000	PHY=5, Reg=0
10	Initialize Port 6 Configuration register	3000	PHY=6, Reg=0
11	Initialize Port 7 Configuration register	3000	PHY=7, Reg=0
12	LED Effect with partition/isolation event	1000	PHY=8, Reg=18
13	LED effect with link event	0330	PHY=8, Reg=19
14	LED effect with activity (CRS) event	0030	PHY=8, Reg=20
15	LED effect with auto-neg event	0000	PHY=8, Reg=21
16	LED effect with Speed100 event	0200	PHY=8, Reg=22

4B/5B Code-Group Table

Table 41: 4B/5B Code-Group Table

PCS Code Group[4:0]	SYMBOL Name	MII (TXD/RXD [3:0])	Description
11110	0	0000	Data 0
01001	1	0001	Data 1
10100	2	0010	Data 2
10101	3	0011	Data 3
01010	4	0100	Data 4
01011	5	0101	Data 5
01110	6	0110	Data 6
01111	7	0111	Data 7
10010	8	1000	Data 8
10011	9	1001	Data 9
10110	A	1010	Data A
10111	B	1011	Data B
11010	C	1100	Data C
11011	D	1101	Data D
11100	E	1110	Data E
11101	F	1111	Data F
Idle and Control Code			
11111	I	0000	Inter-Packet Idle; used as inter-stream fill code.
11000	J	0101	Start of stream delimiter, part 1 of 2; always use in pair with K symbol.
10001	K	0101	Start of stream delimiter, part 2 of 2; always use in pair with J symbol.
01101	T	Undefined	End of stream delimiter, part 1 of 2; always use in pair with R symbol.
00111	R	Undefined	End of stream delimiter, part 2 of 2; always use in pair with T symbol.
Invalid Code			
00100	H	Undefined	Transmit Error; used to send HALT code-group
00000	V	Undefined	Invalid code
00001	V	Undefined	Invalid code
00010	V	Undefined	Invalid code
00011	V	Undefined	Invalid code
00101	V	Undefined	Invalid code
00110	V	Undefined	Invalid code
01000	V	Undefined	Invalid code
01100	V	Undefined	Invalid code
10000	V	Undefined	Invalid code
11001	V	Undefined	Invalid code

LED Display Matrix

The LED Display uses refresh technique. By using the LED display matrix, the number of ports to drive the LED can be significantly reduced. 2 LED's are assigned for each port. On, Off, and Flash states are used to indicate different information. With reduced LED counts, and reduced number of signals, the LED display will be easier to route on the board, and less costly.

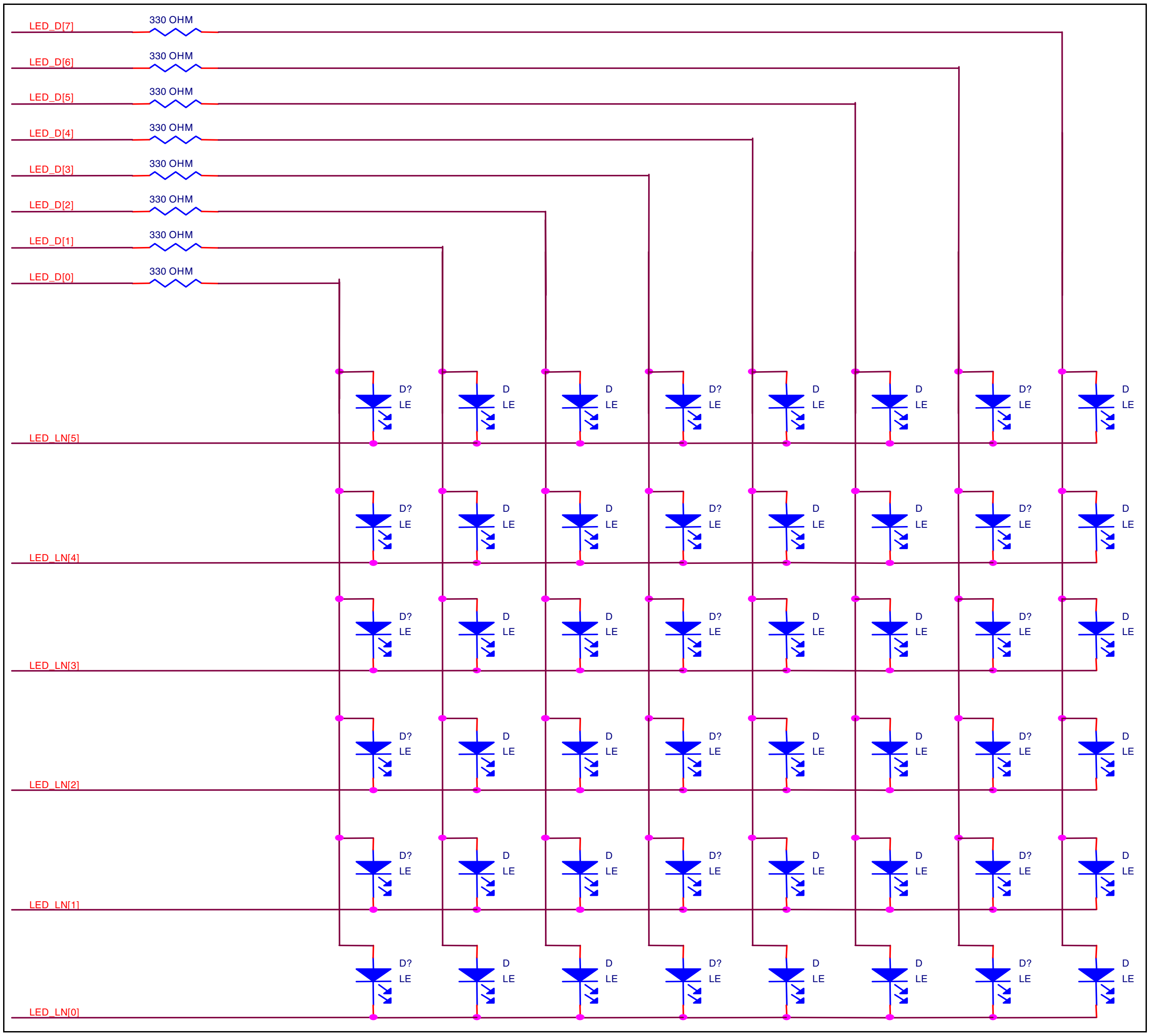

Figure 5: LED Display Matrix

Section 4: Electrical Characteristics

The following electrical characteristics are design goals rather than characterized numbers.

Absolute Maximum Ratings

Storage temperature.............................. -55^{o}C to +150^{o}C

Vcc supply referenced to GND............ -0.5V to 2.5V

Digital input voltage................................ -0.5V to 3.3V

DC output voltage................................... -0.5V to Vcc

Operating Range

Operating temperature (Ta) .... 0^{o}C to 70^{o}C

Vcc supply voltage range (Vcc) .... 2.375V to 2.625V

Table 42: Total Power Consumption

Parameter	***Symbol***	***Conditions***		***Min***	***Typ***	***Max***	***Units***
Supply current (per port)	Icc	10BASE-T, Idle				53	mA
		10BASE-T, Normal activity		53		153	mA
		100BASE-TX				103	mA
		10/100BASE-TX, low power without cable				44	mA
		Power-down				44	mA
Supply current (dual speed hub)	Icc	Mode 00	Master	680			mA

Table 43: TTL I/O Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input voltage high	Vih		2.0			V
Input voltage low	Vil				0.8	V
Input current	Ii		-10		10	mA
Output voltage high	Voh		2.0			V
Output voltage low	Vol				0.4	V
Output current high	Ioh		8			mA
Output current low	Iol		-8			mA
Input capacitance	Ci			10		pF
Output transition time		3.15V < VCC < 3.45V		5		ns
Tristate leakage current	|Ioz|				10	uA

REFCLK Pins

Table 44: REFCLK Pins

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input voltage low	Vil				0.8	V
Input voltage high	Vih		2.0			V
Input clock frequency tolerance	F			100		ppm
Input clock duty cycle	Tdc		40		60	%
Input capacitance	Cin			3.0		pF

I/O Characteristics – LED Pins

Table 45: I/O Characteristics – LED Pins

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output low voltage	Vol				0.4	V
Output high voltage	Voh					V
Input current	Ii		27			mA
Output current	Io					mA

100BASE-TX Transceiver Characteristics

Table 46: 100BASE-TX Transceiver Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Peak-to-peak differential output voltage	Vp	Note 1	1.9	2.0	2.1	V
Output voltage symmetry	Vss	Note 1	0.98		1.02	mV
Signal rise/fall time	Trf	Note 1	3.0		5.0	ns
Rise/fall time symmetry	Trfs	Note 1	0		0.5	ns
Duty cycle distortion	Dcd		0		0.5	ps
Overshoot/undershoot	Vos				5	%
Output jitter		Scrambled Idle			1.4	ns
Receive jitter tolerance					4	ns
Output current high	Ioh	1:1 Transformer			40	mA
Output current high	Ioh	1.25:1 Transformer			32	mA
Common mode input voltage				1.25		V
Differential input resistance				4		KΩ
Note 1: 50Ω (± 1%) resistor to VCC on each output						

10BASE-T Transceiver Characteristics

Table 47: 10BASE-T Transceiver Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Peak-to-peak differential output voltage	Vop	Note 1	4.4	5	5.6	V
Start of idle pulse width			300		350	ns
Output jitter					1.4	ns
Receive jitter tolerance					32	ns
Differential squelch threshold	Vds		300	400	500	mV
Common mode rejection				25		V
Note 1: 50Ω (± 1%) resistor to VCC on each output						

Section 5: Digital Timing Characteristics

POWER-ON RESET

Table 48: Power-on Reset

Parameter	*SYM*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
RST* low period	tRST		150	-	-	µs
Configuration	tCONF		100	-	-	ns

Figure 6: Power-on Reset

PHY MDC/MDIO INTERFACE

Table 49: PHY MDC/MDIO Interface

Parameter	*SYM*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
MDC low period	tMDCL		–	300	–	ns
MDC high period	tMDCH		–	300	–	ns
Receive data setup time	tRDS	Setup on read cycle	10	–	–	ns
Receive data hold time	tRDH	Hold on read cycle	10	–	–	ns
Transmit data delay time	tTDD	Delay on write cycle	3	–	–	ns

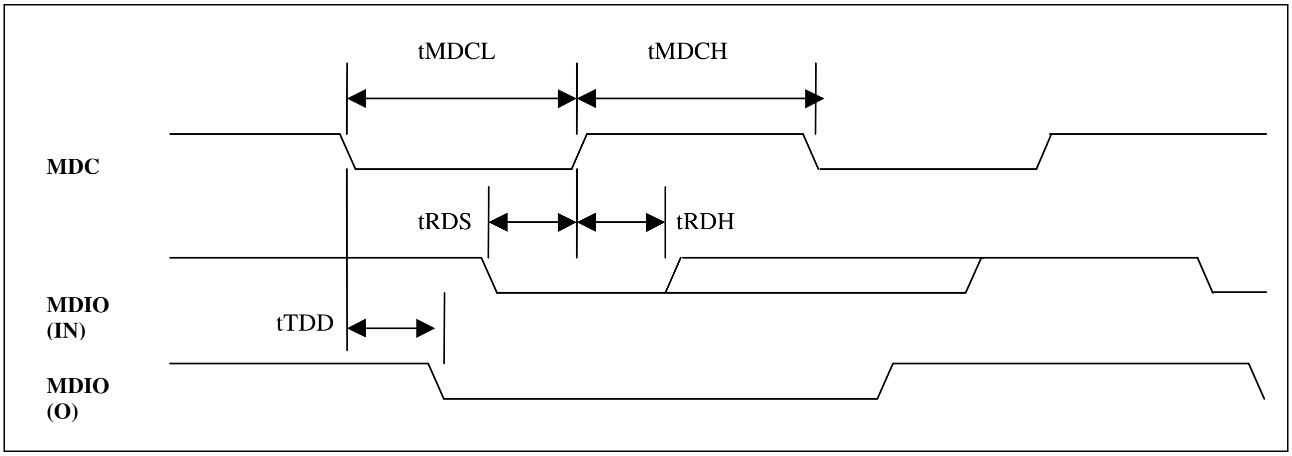

Figure 7: PHY MDC/MDIO Interface Timing

7-Wire Input Timing

Table 50: 7-Wire Input Timing

Parameter	*SYM*	*Min*	*Typ*	*Max*	*Units*
SNI_TXCLK period	tCK	–	100	–	ns
SNI_TXCLK high period	tCKH	40	–	60	ns
SNI_TXCLK low period	tCKL	40	–	60	ns
SNI_TXD/SNI_TXEN to SNI_TXCLK rising setup time	tDS	10	–	–	ns
SNI_TXD/SNI_TXEN to SNI_TXCLK rising hold time	tDH	10	–	–	ns

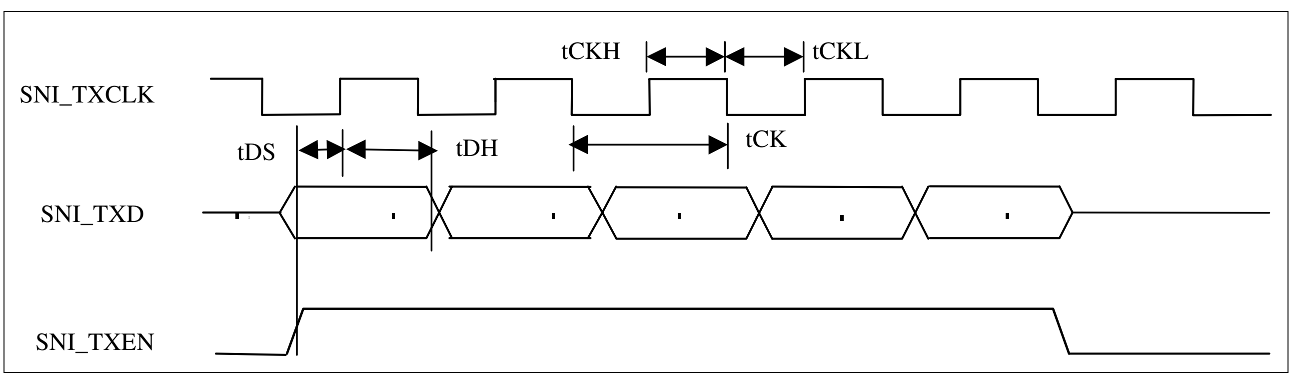

Figure 8: 7-Wire Input Timing

7-WIRE OUTPUT TIMING

Table 51: 7-Wire Output Timing

Parameter	SYM	Min	Typ	Max	Units
SNI_RXCLK period	tCK	–	100	–	ns
SNI_RXCLK high period	tCKH	40	–	60	ns
SNI_RXCLK low period	tCKL	40	–	60	ns
SNI_RXCLK rising to SNI_RXD/ SNI_CRS/SNI_COL output delay	tOD	–	–	70	ns

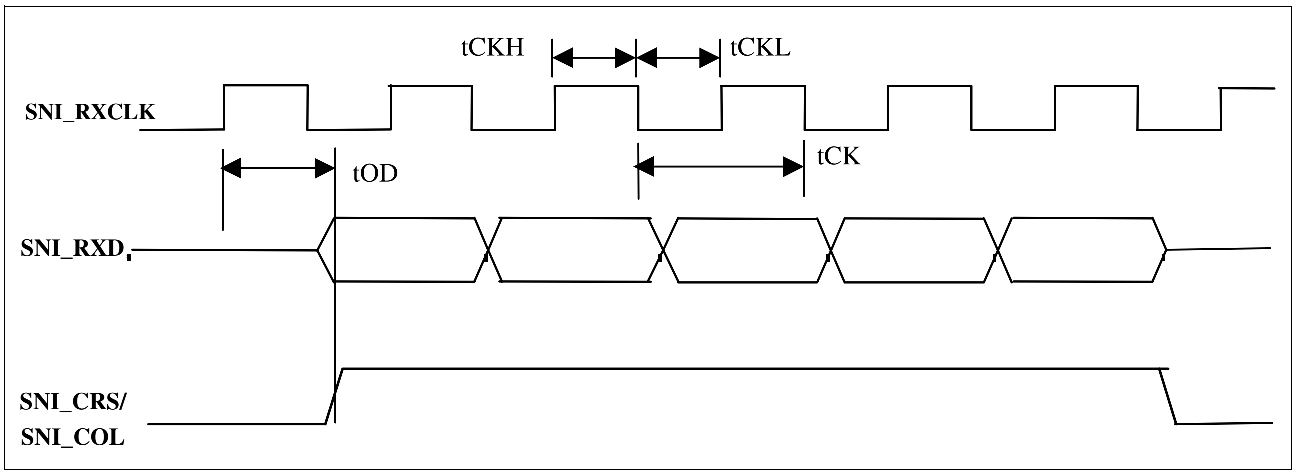

Figure 9: 7-Wire Output Timing

100BASE-TX MII Input Timing

Table 52: 100BASE-TX MII Input Timing

Parameter	SYM	Min	Typ	Max	Units
MII_TXCLK period	tCK	–	40	–	ns
MII_RXCLK high period	tCKH	18	–	22	ns
MII_RXCLK low period	tCKL	18	–	22	ns
MII_TXD, MII_TXEN to MII_TXCLK rising setup time	tTXS	10	–	–	ns
MII_TXD, MII_TX_EN to MII_TXCLK rising hold time	tTXH	10	–	–	ns

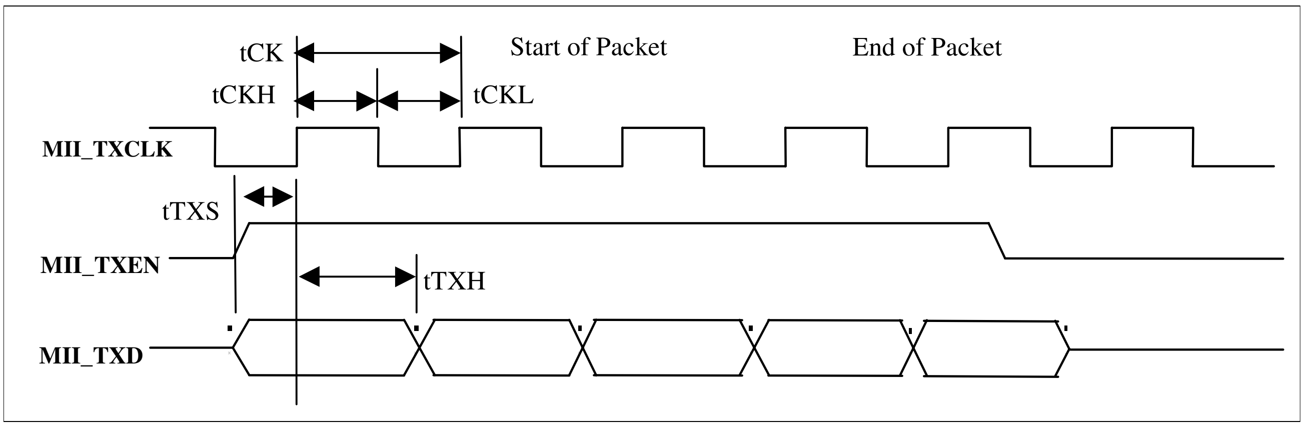

Figure 10: 100BASE-TX MII Input Timing

100BASE-TX MII OUTPUT TIMING

Table 53: 100BASE-TX MII Output Timing

Parameter	SYM	Min	Typ	Max	Units
MII_RXCLK period	tCK	–	40	–	ns
MII_RXCLK high period	tCKH	18	–	22	ns
MII_RXCLK low period	tCKL	18	–	22	ns
MII_CRS rising to MII_RXDV rising	tCSVA	0	–	10	ns
MII_RXCLK rising to MII_RXD, MII_RXDV, MII_CRS output delay	tRXOD	20	–	30	ns

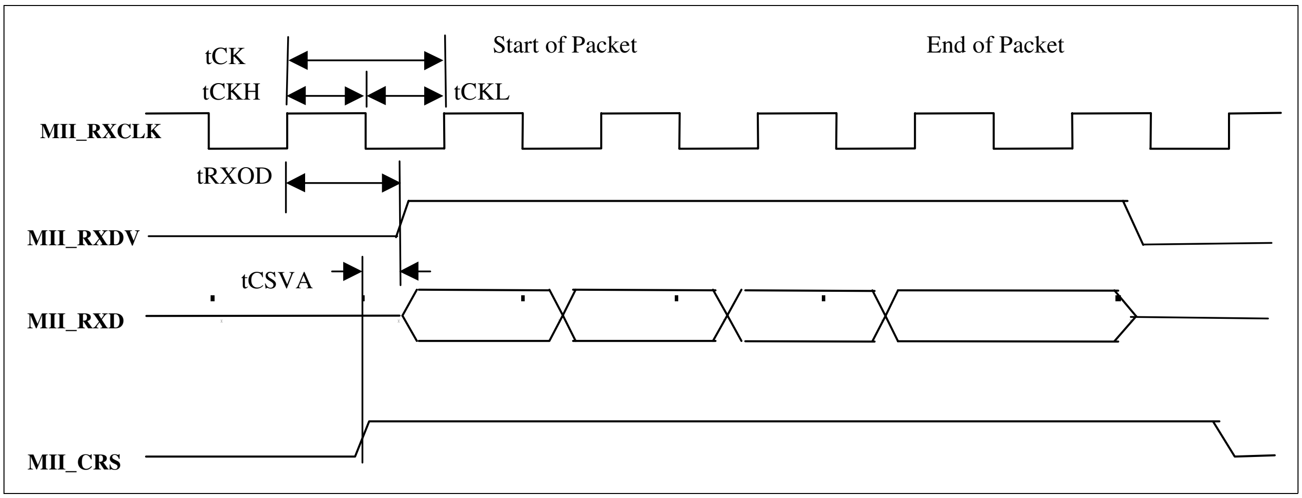

Figure 11: 100BASE-TX MII Output Timing

10BASE-TX MII INPUT TIMING

Table 54: 10BASE-TX MII Input Timing

Parameter	***SYM***	***Min***	***Typ***	***Max***	***Units***
MII_TXCLK period	tCK	-	400	-	ns
MII_RXCLK high period	tCKH	180	-	220	ns
MII_RXCLK low period	tCKL	180	-	220	ns
mii_txd, MII_TXEN to MII_TXCLK rising setup Time	tTXS	10	-	-	ns
MII_TXD, MII_TX_EN to MII_TXCLK rising hold time	tTXH	10	-	-	ns

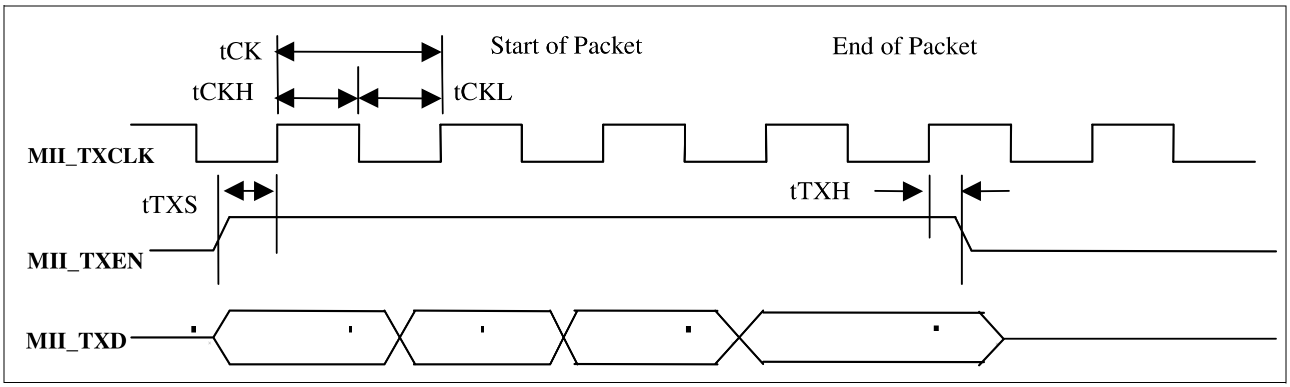

Figure 12: 10BASE-TX MII Input Timing

10BASE-TX MII OUTPUT TIMING

Table 55: 10BASE-TX MII Output Timing

Parameter	SYM	Min	Typ	Max	Units
MII_RXCLK period	tCK	-	400	-	ns
MII_RXCLK high period	tCKH	180	-	220	ns
MII_RXCLK low period	tCKL	180	-	220	ns
MII_CRS rising to MII_RXDV rising	tCSVA	0	-	10	ns
MII_RXCLK rising to MII_RXD, MII_RXDV, MII_CRS output delay	tRXOD	200	-	220	ns

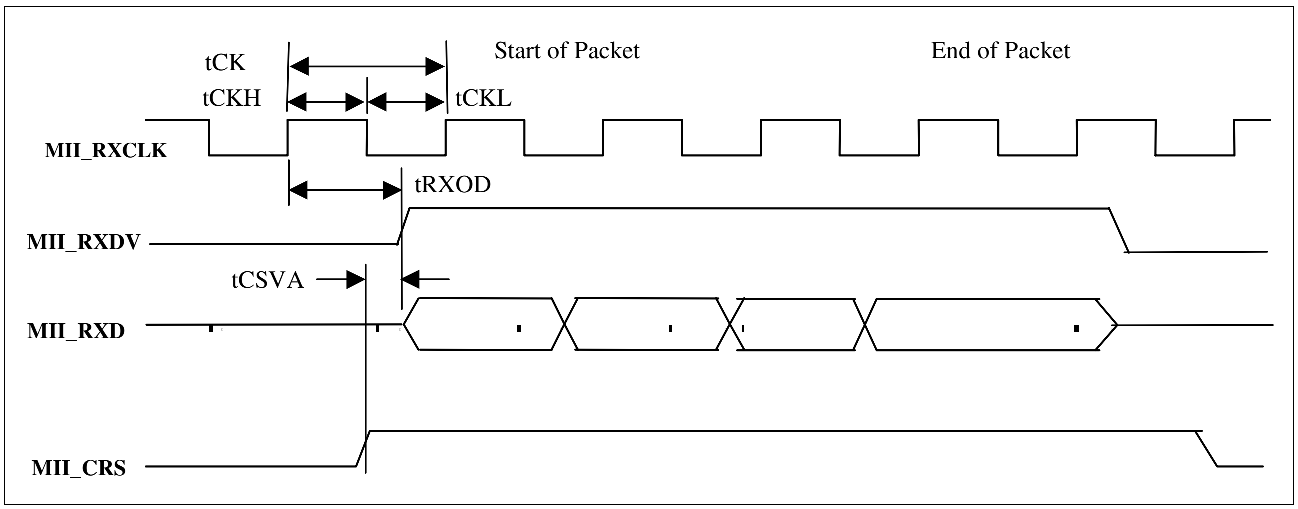

Figure 13: 10BASE-TX MII Output Timing

EEPROM INTERFACE TIMING

Table 56: EEPROM Interface Timing

Parameter	SYM	Min	Typ	Max	Units
PROM_CLK period	tECK	-	5120	-	ns
PROM_CLK low period	tECKL	2550	-	2570	ns
PROM_CLK high period	tECKH	2550	-	2570	ns
PROM_IN to PROM_CLK rising hold time	tERDS	10	-	-	ns
PROM_IN to PROM_CLK rising hold time	tERDH	10	-	-	ns
PROM_CLK falling to PROM_OUT output delay time	tEWDD	-	-	20	

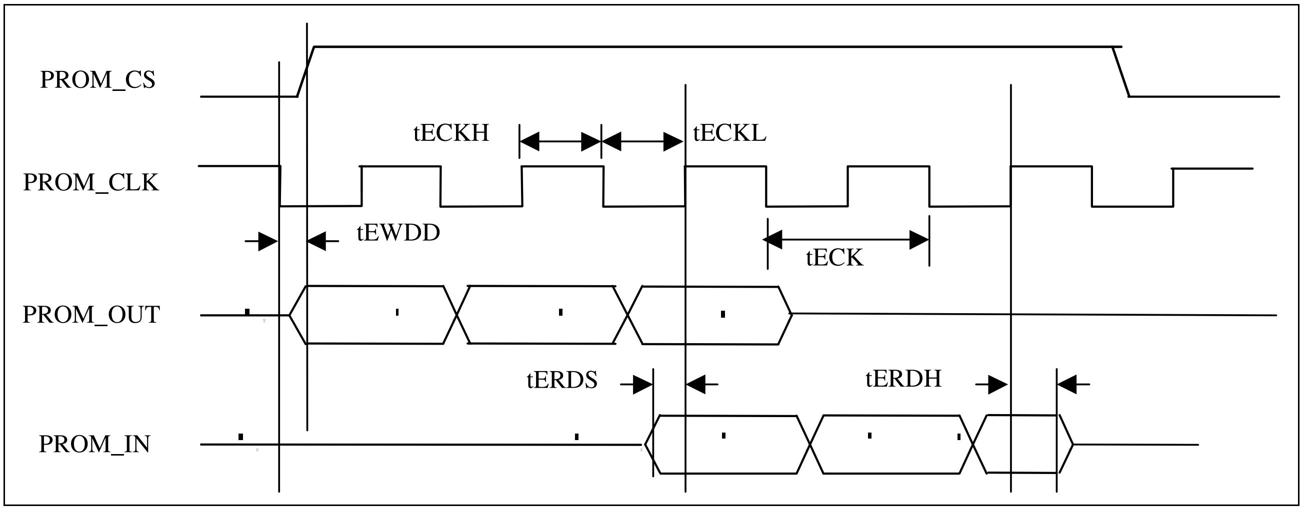

Figure 14: EEPROM Interface Timing

LED TIMING

Table 57: LED Timing

Parameter	*SYM*	*Conditions*	*Min*	*Typ*	*Max*	*Units*
Pulse width	tPW			2		ms
LED_D[n] falling to LED_D[n+1] falling	tPP			2		ms
LED_D[n] falling to LED_D[n] falling	tPD			16		ms

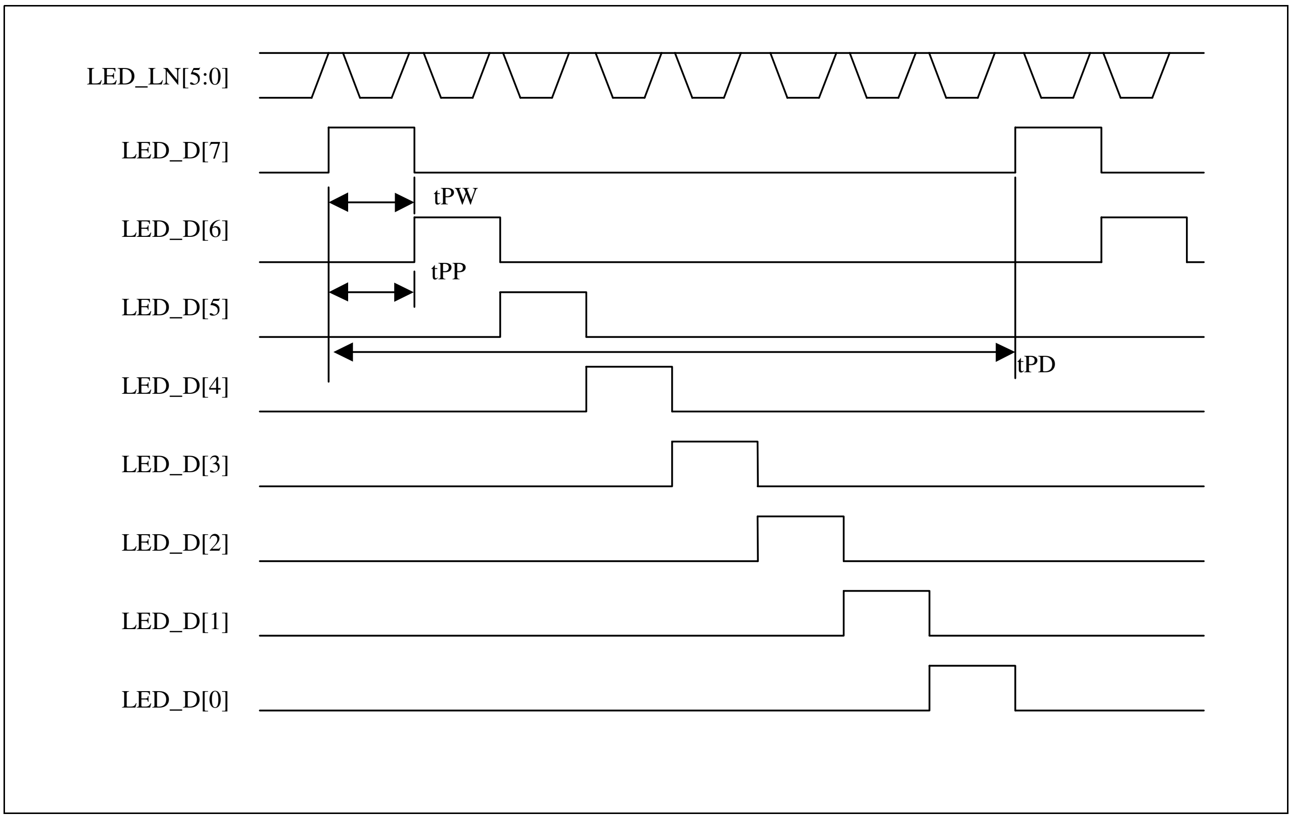

Figure 15: LED Timing

TX Application Termination

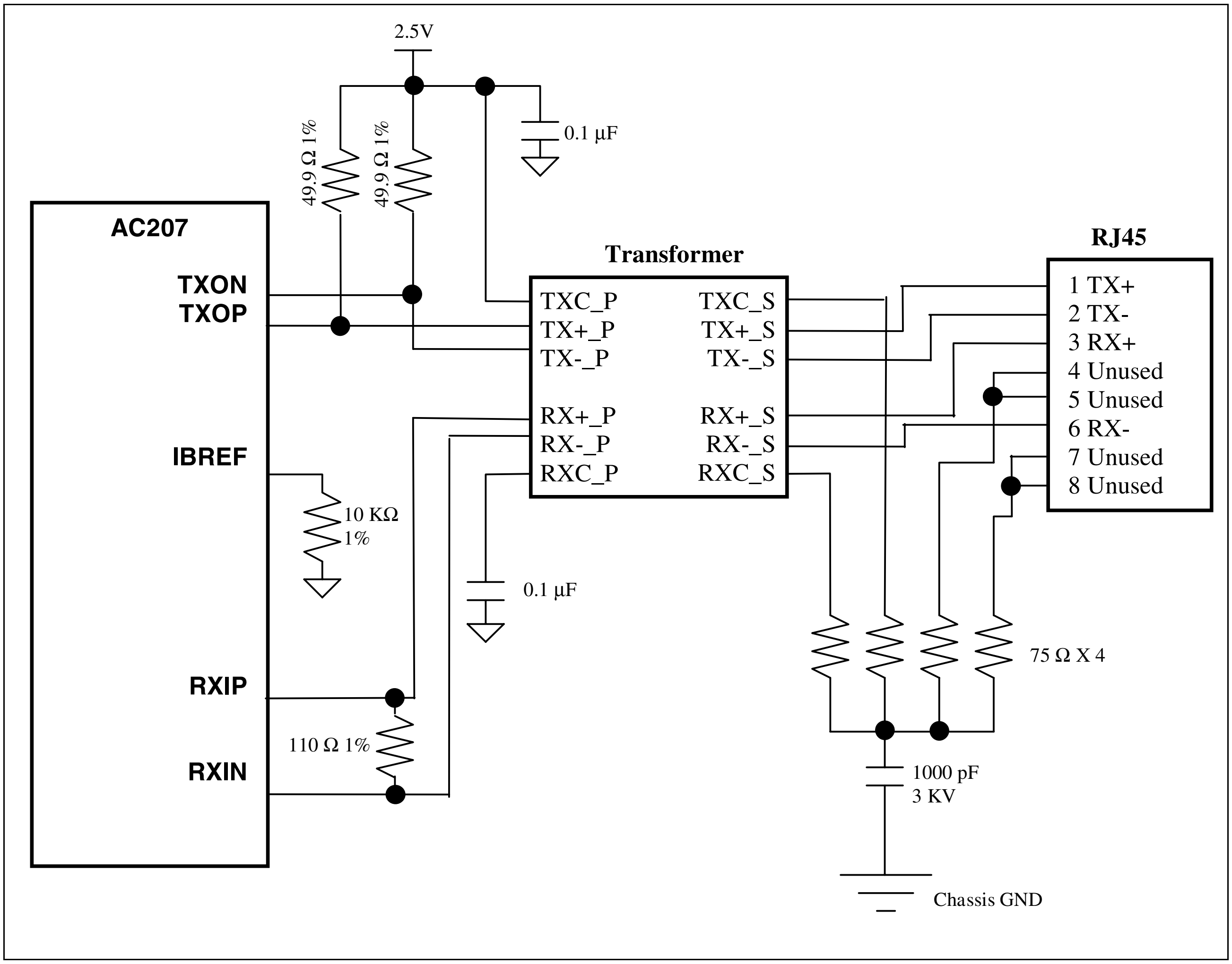

Figure 16: Application Termination

Section 6: Mechanical Information

Table 58: Package Dimensions for the AC207

N	A	A1	A2	B	D	D1	D2	E	E1	E2	e	L	L1
128	3.40 Max	0.25 Min	2.70 ± 0.2	0.200 ± 0.1	23.20 ± 0.25	20.00 ± 0.10	18.5 ± 0.10	17.20 ± 0.25	14.00 ± 0.10	12.50 ± 0.10	0.50	0.88 ± 0.2	1.60 ± 0.12

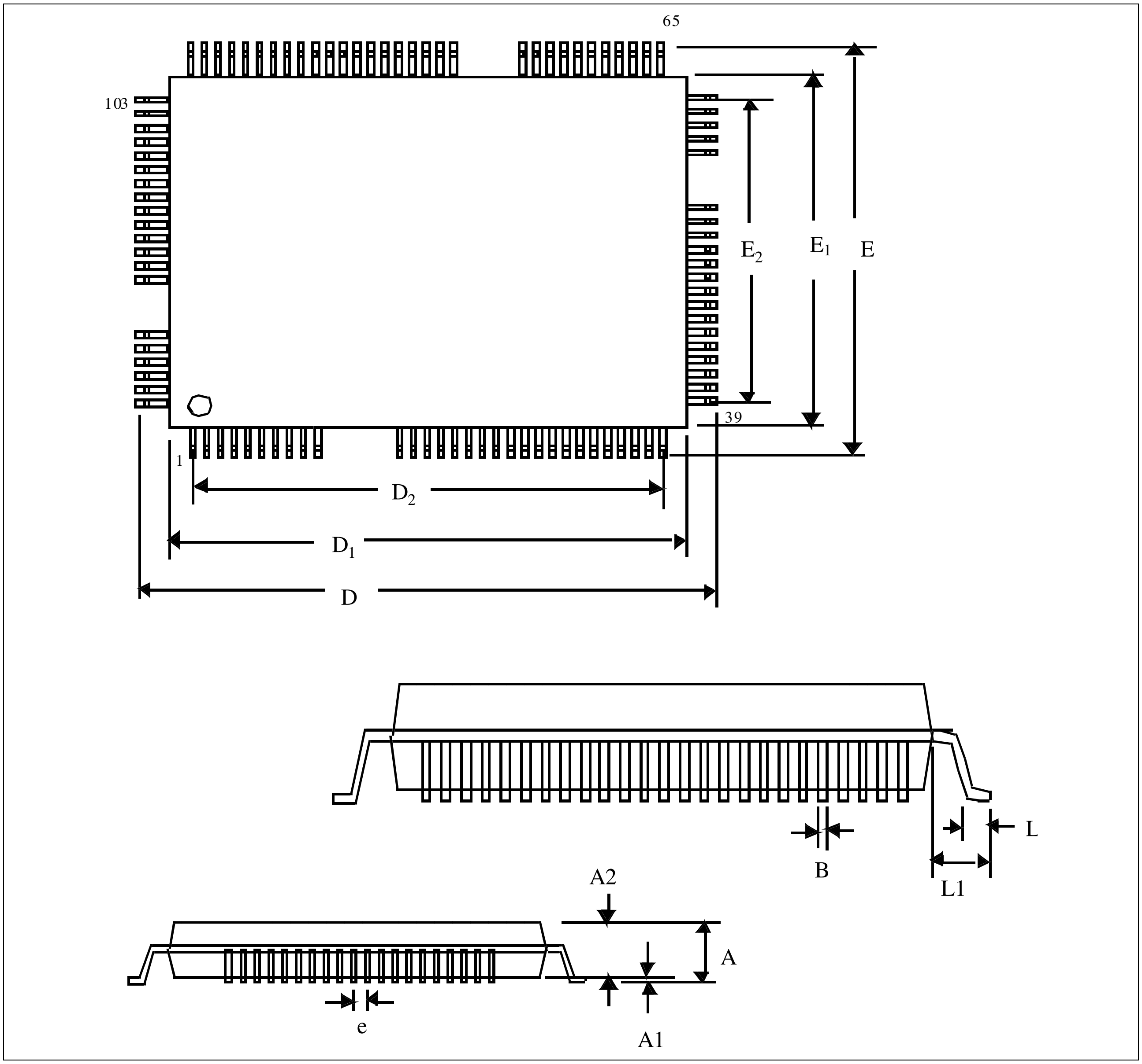

Figure 17: 128-pin PQFP

Section 7: Ordering Information

Part Number	Package	Ambient Temperature
AC207KQM	128-pin PQFP	0° to 70° C

Broadcom

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