



PJL9434A

60V N-Channel Enhancement Mode MOSFET

Voltage

60 V

Current

10 A

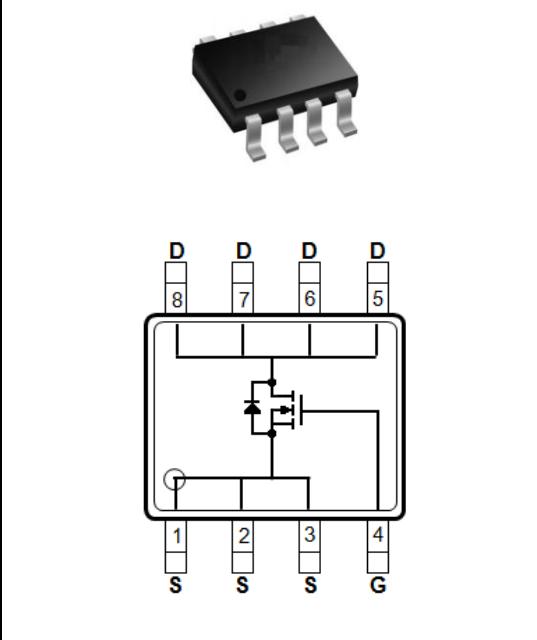
Features

- RDS(ON) , V_{GS}@10V, I_D@10A<12mΩ
- RDS(ON) , V_{GS}@4.5V, I_D@5.0A<15mΩ
- Advanced Trench Process Technology
- High density cell design for ultra low on-resistance
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std.
(Halogen Free)

Mechanical Data

- Case: SOP-8 package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0029 ounces, 0.083 grams
- Marking: L9434A

SOP-8



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
Drain-Source Voltage	V _{DS}	60	V
Gate-Source Voltage	V _{GS}	+20	V
Continuous Drain Current	$T_A=25^\circ\text{C}$	10	A
		8	
Pulsed Drain Current ^(Note 1)	I _{DM}	40	A
Power Dissipation	$T_A=25^\circ\text{C}$	2.5	W
		1.6	
Single Pulse Avalanche Energy ^(Note 5)	E _{AS}	5.0	mJ
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55~150	°C
Typical Thermal resistance - Junction to Ambient, t≤10s ^(Note 6)	R _{θJA}	50	°C/W



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Electrical Characteristics ($T_A=25^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.7	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$	-	10.5	12	$m\Omega$
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=5A$	-	12	15	$m\Omega$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Dynamic (Note 7)						
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=10A,$ $V_{GS}=10V$ (Note 1,2)	-	39	-	nC
Gate-Source Charge	Q_{gs}		-	6.1	-	
Gate-Drain Charge	Q_{gd}		-	6.7	-	
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0MHz$	-	2256	-	pF
Output Capacitance	C_{oss}		-	145	-	
Reverse Transfer Capacitance	C_{rss}		-	93	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=15V, I_D=10A,$ $V_{GS}=10V, R_G=6\Omega$ (Note 1,2)	-	7.5	-	ns
Turn-On Rise Time	t_r		-	36	-	
Turn-Off Delay Time	$t_{d(off)}$		-	49	-	
Turn-Off Fall Time	t_f		-	12	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_s	---	-	-	10	A
Diode Forward Voltage	V_{SD}	$I_s=1.0A, V_{GS}=0V$	-	0.67	1.0	V

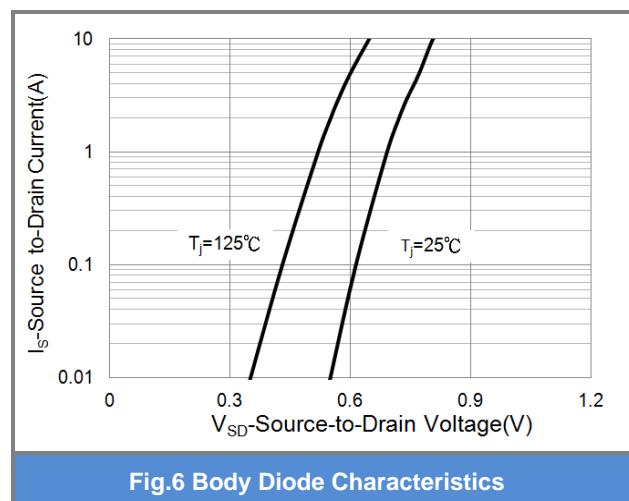
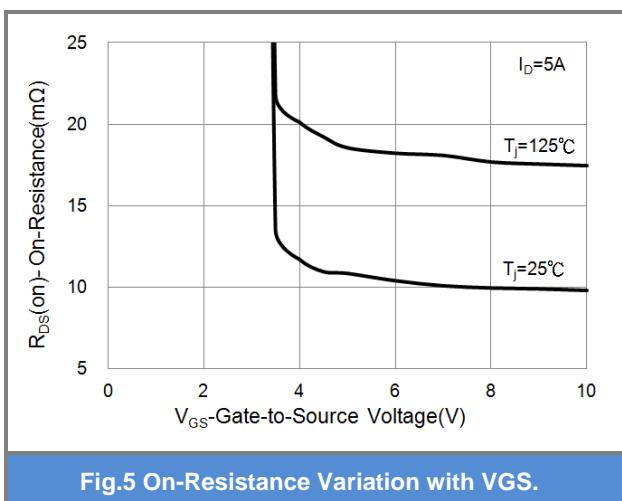
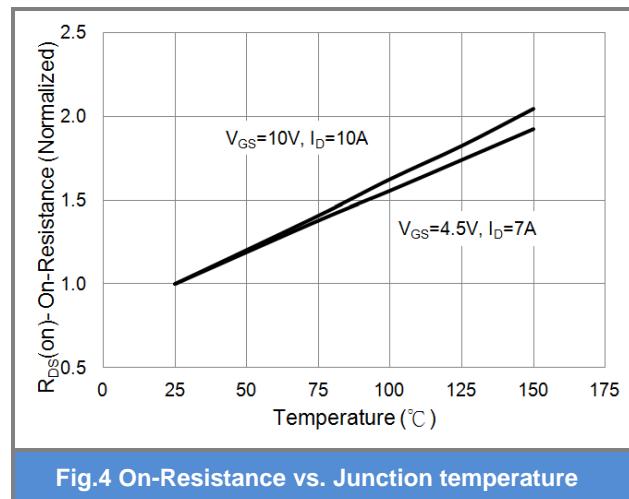
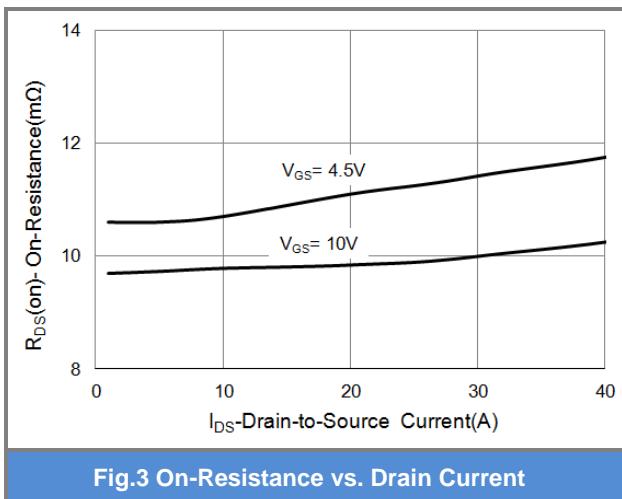
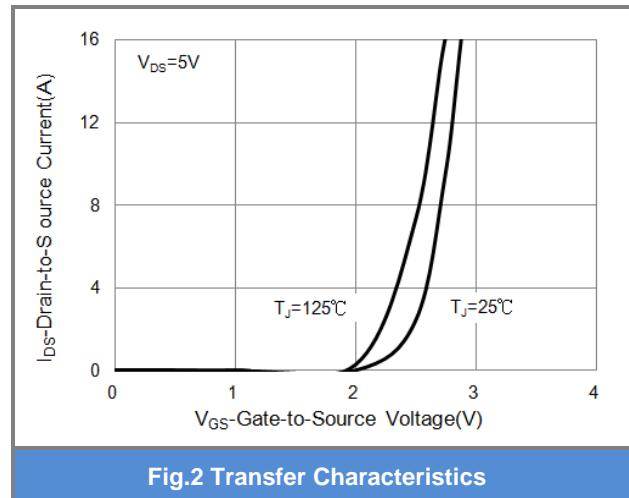
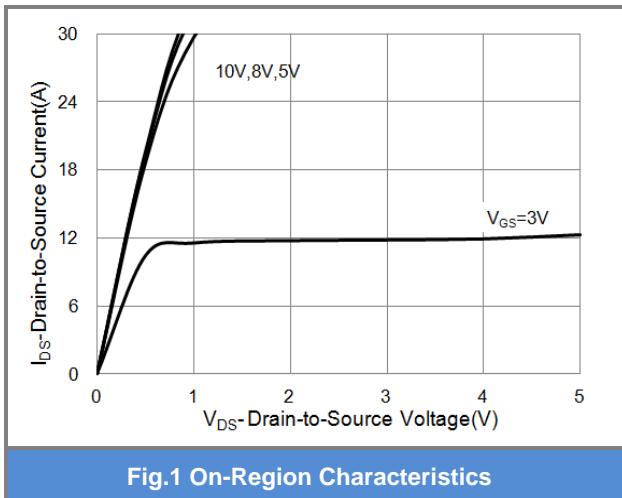
NOTES :

1. Pulse width<300us, Duty cycle<2%
2. Essentially independent of operating temperature typical characteristics.
3. The maximum current rating is package limited.
4. Repetitive rating, pulse width limited by junction temperature $T_J(MAX)=150^\circ C$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ C$.
5. The test condition is $L=0.1mH, I_{AS}=10A, V_{DD}=50V, V_{GS}=10V$
6. $R_{Theta A}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
7. Guaranteed by design, not subject to production testing.



PJL9434A

TYPICAL CHARACTERISTIC CURVES





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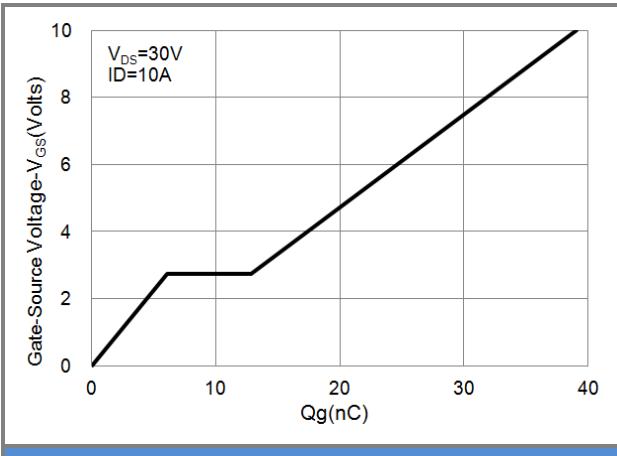


Fig.7 Gate-Charge Characteristics

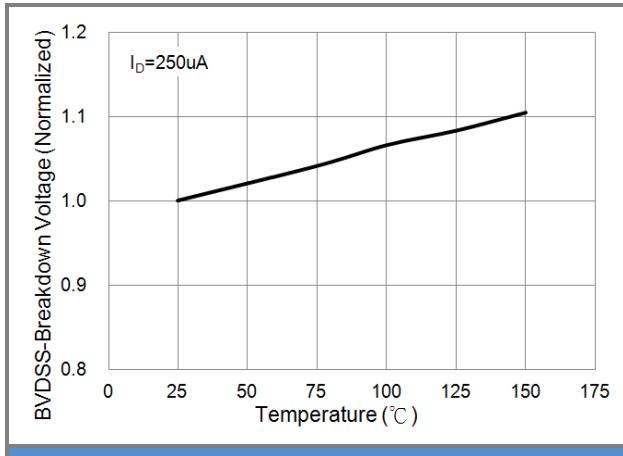


Fig.8 Breakdown Voltage Variation vs. Temperature

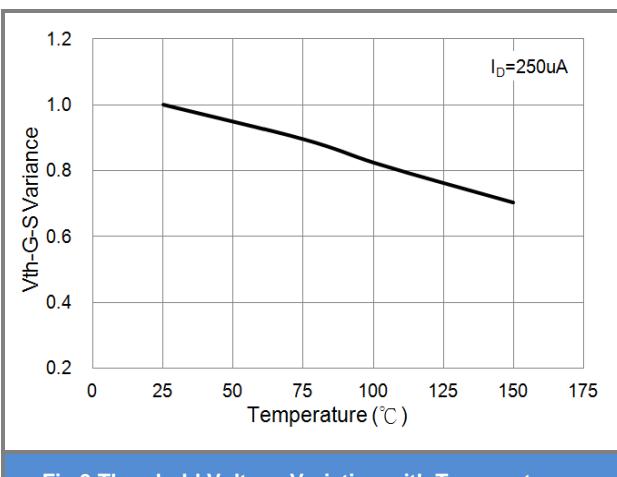


Fig.9 Threshold Voltage Variation with Temperature.

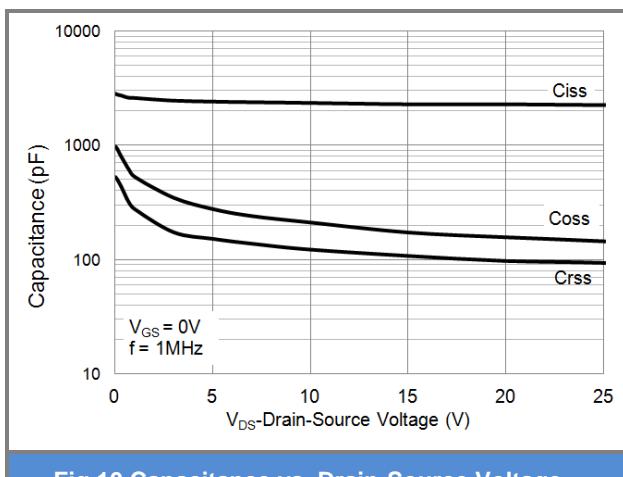


Fig.10 Capacitance vs. Drain-Source Voltage.

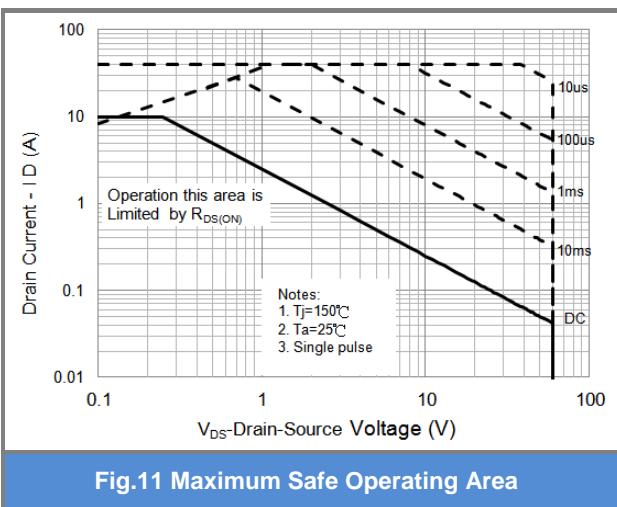


Fig.11 Maximum Safe Operating Area



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TYPICAL CHARACTERISTIC CURVES

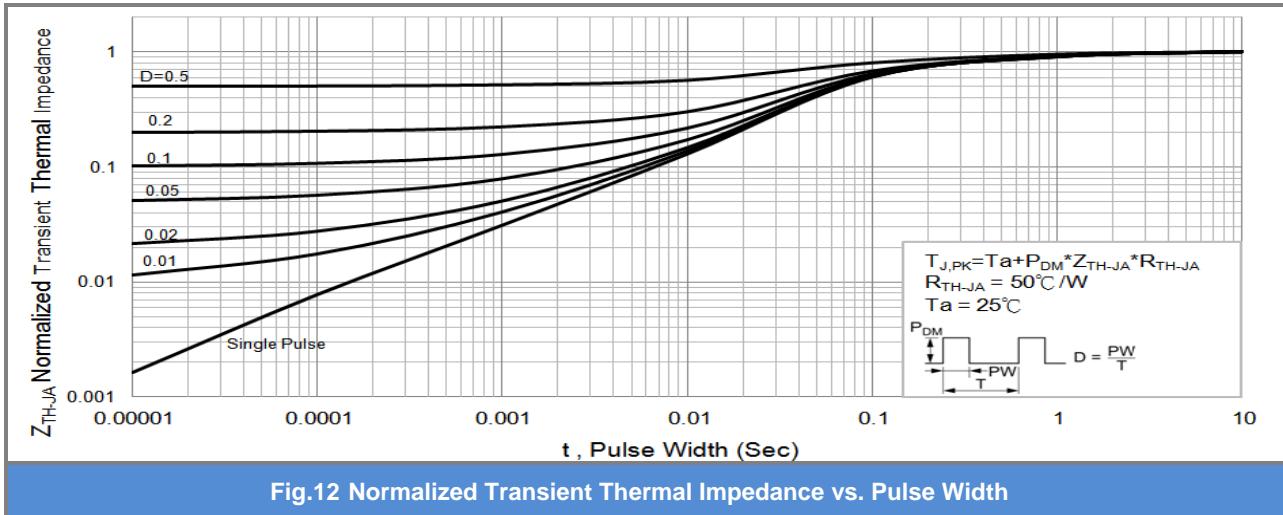


Fig.12 Normalized Transient Thermal Impedance vs. Pulse Width

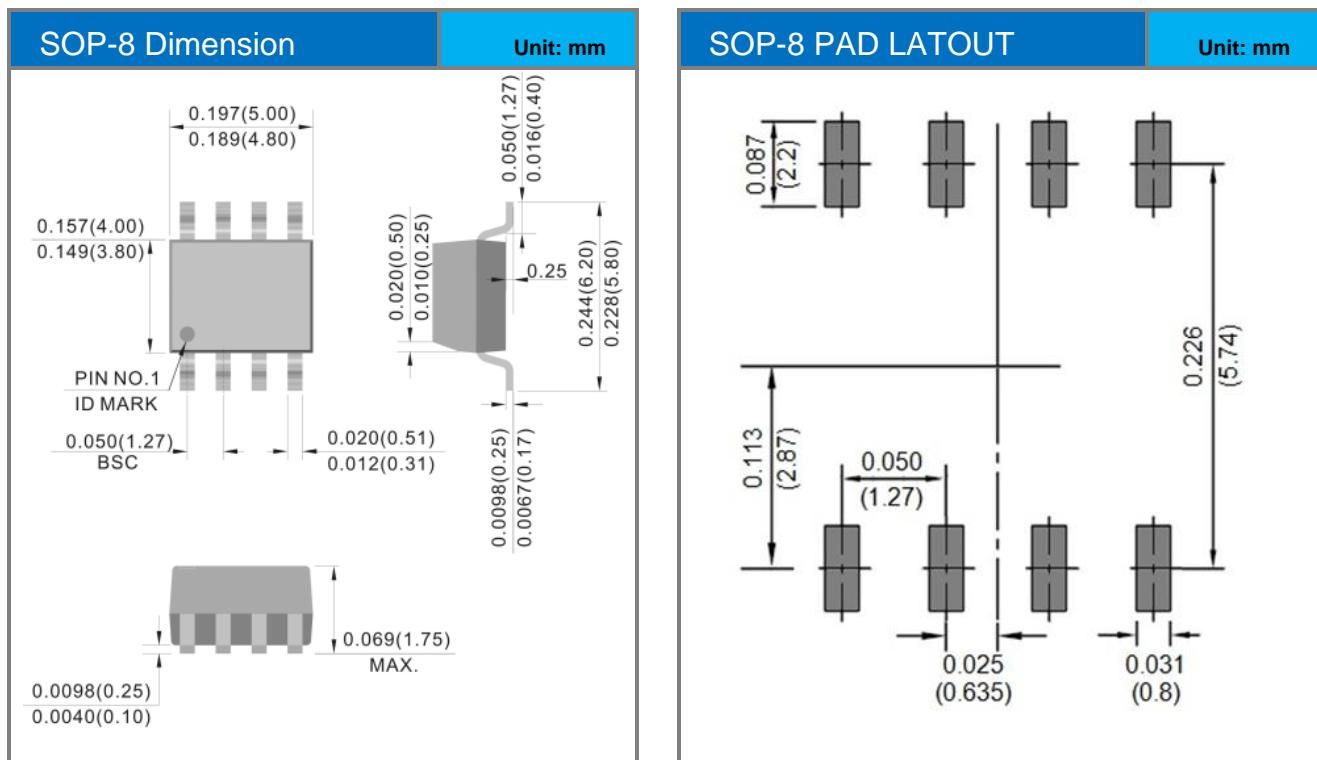


PJL9434A

PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJL9434A_R2_00001	SOP-8	2.5K pcs / 13" reel	L9434A	Halogen free

Packaging Information & Mounting Pad Layout





PJL9434A

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