

Features



The following is a list of the main components and interfaces on the AT32UC3C-EK:

- Main MCU: 32-bit AVR UC3 AT32UC3C0512 (TQFP144)
 - 512KBytes internal flash, 256KBytes internal RAM
 - Up to 66MHz operation
 - Controller Area Network Interfaces
 - Peripheral event system
 - FlashVault™ allows pre-programmed, secure library support for end user applications
 - DSP Floating point instructions
- One serial data flash, 64Mbits
- One serial EEPROM 128-bits
- Four LEDs
- Two push buttons

- One reset pushbutton
- Powered through USB connector or through external power supply (header J1 or J2)
- 16MHz oscillator for the main clock, one RTC 32kHz crystal and one free footprint for additional oscillator
- JTAG and NEXUS Connectors for programming and debugging on the Atmel AT32UC3C0512C MCU
- One QTouch[®] (Atmel AT42QT1060) with six buttons connected through the TWI
- One QVGA LCD display with resistive touch screen
- One jack connector to output audio samples
- One microphone input to record audio signal
- Two CAN Interfaces and two LIN Interfaces
- One SD/MMC slot connector
- One SDRAM 256Mbits
- Wireless Header (WLESS) for the wireless expansion header or for any SPI-based or TWI-based or USART-based external communication
- Atmel AVRMC300 expansion headers to be able to manage motor control applications
- J27: USB (2.0 mini A-B receptacle) connected to the 32-bit Atmel AVR UC3 AT32UC3B1256
 - AT32UC3C0512 and AT32UC3B1256 are connected through two pins
 - The pre-loaded firmware on the AT32UC3B1256 acts as a UART-USB CDC virtual com port gateway
 - The J28 jumper can be used to set the AT32UC3B1256 in boot loader mode at power up
 - JTAG connector for programming and debugging the AT32UC3B1256 (J13)

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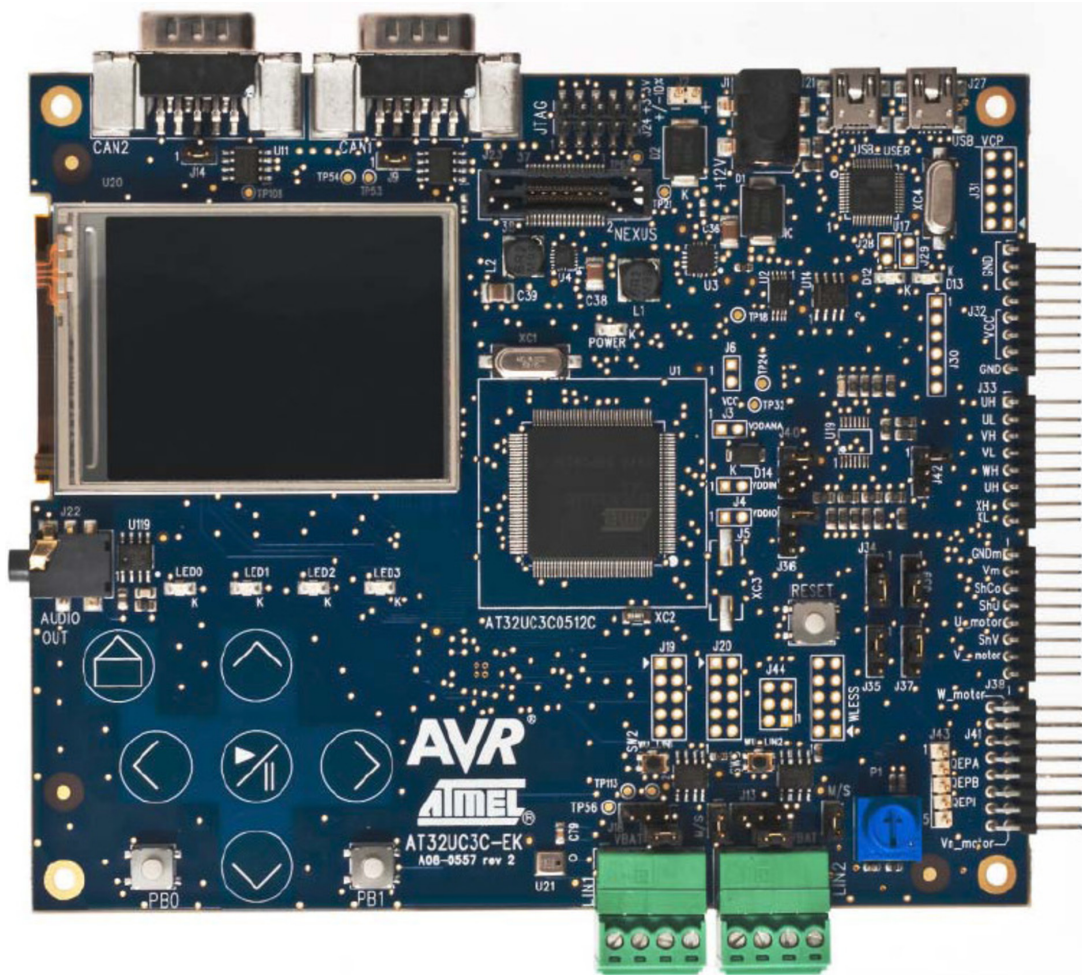
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1. Introduction

The Atmel® AT32UC3C-EK is an evaluation kit and development system for the Atmel AVR® UC3 AT32UC3C0512C microcontroller.

As a development system, the board notably provides on-board memory, a USB communication interface, CAN and LIN network interfaces, and the JTAG programming and debugging interface. The AT32UC3C-EK also features expansion headers; one of these is the wireless expansion header (named WLESS header on the PCB).

Figure 1-1 The AT32UC3C-EK Evaluation Kit



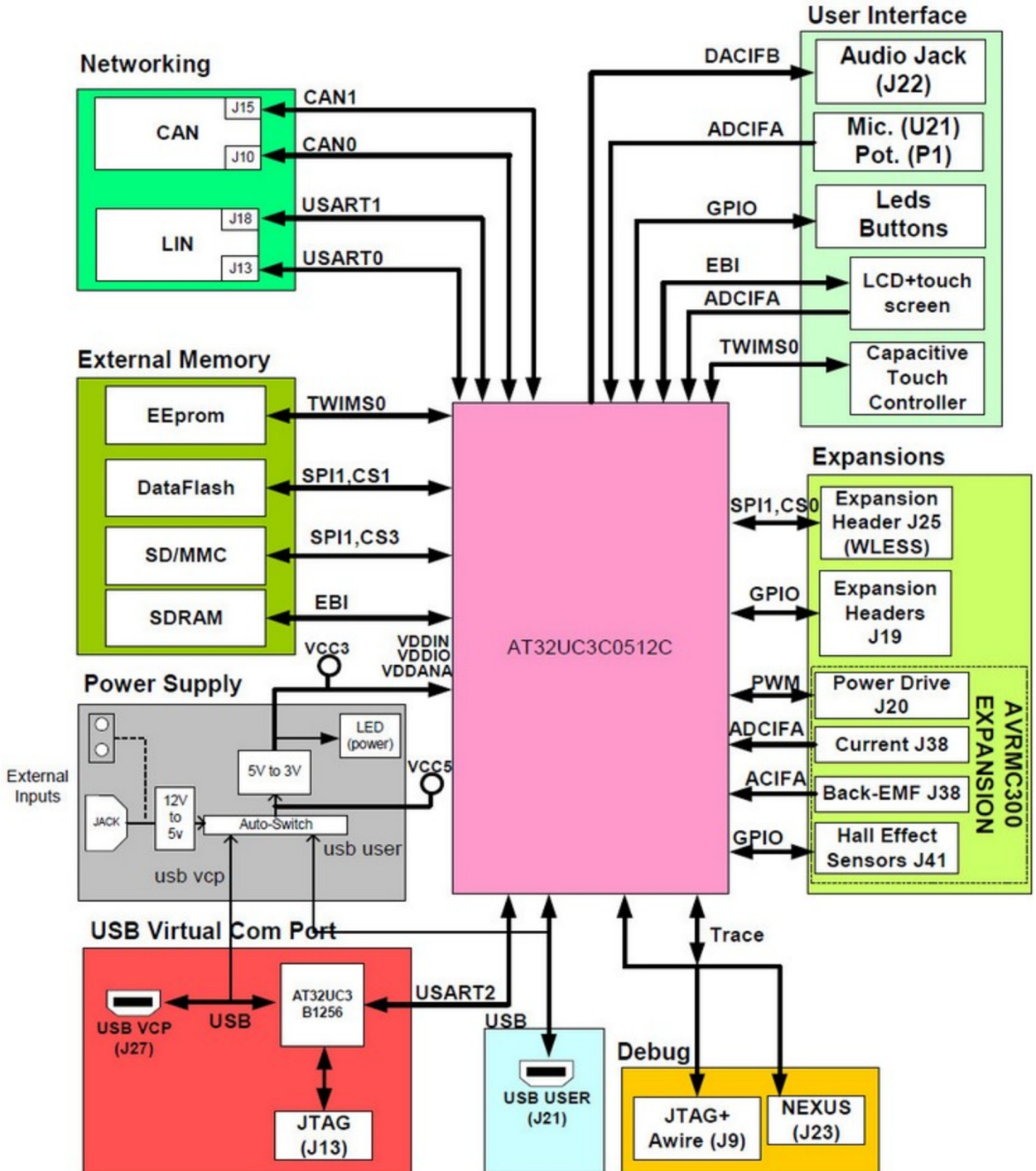
1.1. Acronyms

ASF	AVR Software Framework
CAN	Controlled Area Network
LIN	Local Interconnect Network
HMI	Human Machine Interface

2. Kit Overview

This chapter lists the features provided by the AT32UC3C-EK evaluation kit and describes the content of the box the kit is packaged in.

Figure 2-1 AT32UC3C-EK Block Diagram



2.1. Kit Contents

The AT32UC3C-EK toolbox contains the following items:

- One AVR Technical Library DVD
- One AT32UC3C-EK customer letter
- One AT32UC3C-EK Getting Started Guide
- One AT32UC3C-EK evaluation kit
- Two mini-B plug to std-A plug ~1.5m USB cable
- Five 2-pin cables
- One 10-pin flat cable

Figure 2-2 Unpacked AT32UC3C-EK Toolbox



2.2. Power-Up and Getting Started

Refer to the [AVR32777: AT32UC3L-EK Getting Started Guide](#).

2.3. Reference Materials

1. [The AVR UC3 C0 series datasheet](#)
2. [The AT32UC3C-EK Schematics and Assembly bottom/top views](#)
3. [The AT32UC3C-EK Getting Started document](#)
4. [The AVRMC300 Getting Started](#)
5. [The 32-bit AVR UC3 C series Schematic Checklist](#)
6. [The AVR Software Framework](#)

All pre-loaded firmware source code is available in the AVR Software Framework version 2.0 or higher.

7. [Debuggers](#)

3. Hardware Description

This chapter presents the hardware blocks of the AT32UC3C-EK hardware design. Each hardware block is described with:

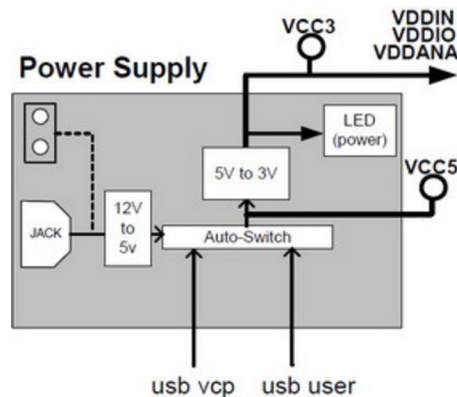
- An overview of the hardware block
- A location in the schematics document
- AT32UC3C-specific information (when relevant)
- All possible hardware configurations of the block and available test points

In each block description, the components reference and schematic can be found in the [AT32UC3C-EK Schematics and Assembly bottom/top views](#).

3.1. Power Supply

The power supply block of the AT32UC3C-EK is in charge of distributing power to all components of the board.

Figure 3-1 AT32UC3C-EK Power Supply Logical View



3.1.1. Overview

The AT32UC3C-EK can be powered from four different sources: 2x USB mini AB plug (5V input): labeled "USB USER" (J21) and "USB VCP" (J27) and 2x external power supply J1 jack connector or the J2 2-pins headers (DC 12V \pm 10%).

The AT32UC3C-EK will automatically switch to the more accurate power source if it senses voltage on it (external power supply is defined as the more accurate power source, then VBUS from "USB VCP" and the less accurate power source is VBUS from "USB USER").

These inputs go through an external 3.3V switch mode regulator which delivers supplies to the rest of the board with a 3.3V voltage.

The power indicator LED green D3, labeled "POWER", indicates if the 3.3V from the external regulator is present.

Refer to [Configurations and Test Points](#) on page 10 for a description of the possible hardware configurations of the power supply block.

Figure 3-2 AT32UC3C-EK Top View Power Supply Location

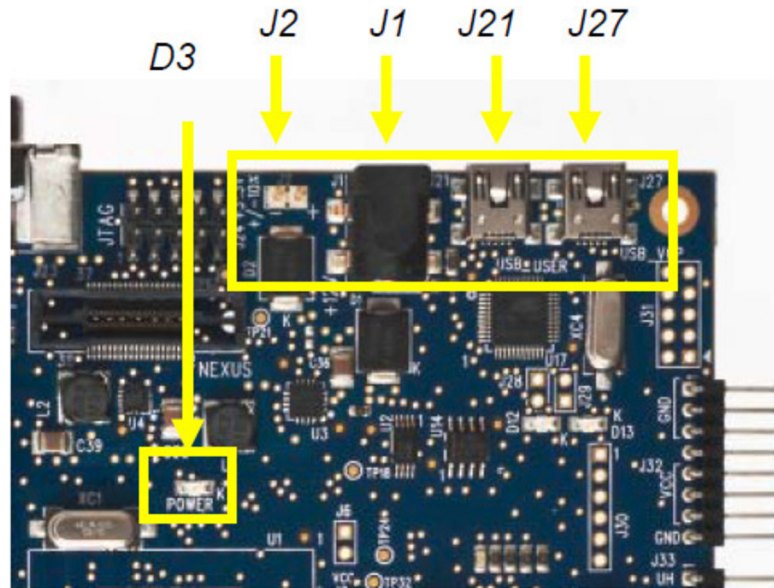
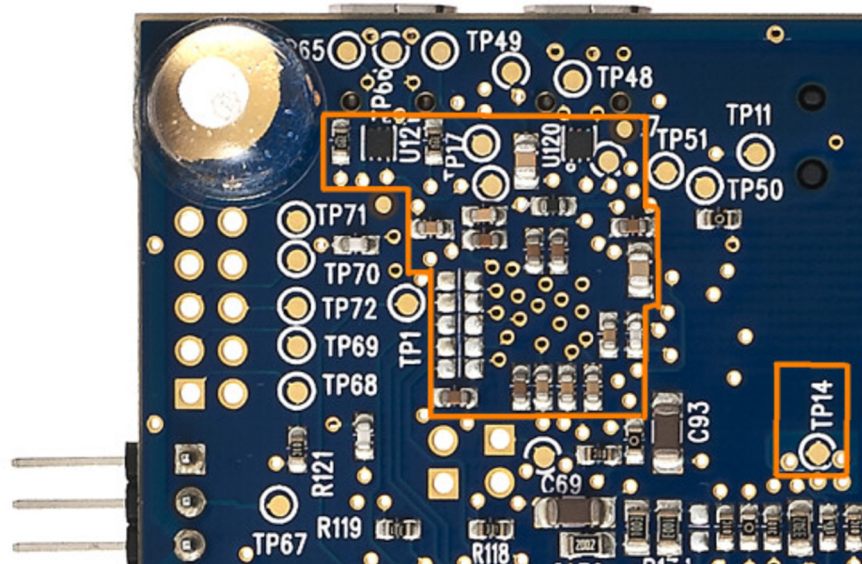


Figure 3-3 AT32UC3C-EK Bottom View Power Supply Location



3.1.2. UC3C-Specific Information

AT32UC3C0512C Power Supply Mode

Among the two power supply configurations supported by the Atmel AT32UC3C0512C, this board implements the 3.3V single supply mode configuration. Refer to the Supply Considerations section in the [AVR UC3 C0 Series datasheet](#) for schematic diagram of this mode.

AT32UC3C0512C pinout for the Power Supply Block

Table 3-1 UC3C Pinout for the Power Supply Block

QFP144 pin	GPIO	GPIO Alternate Functions	Feature
53	N.A.	N.A.	VDDIN5
54	N.A.	N.A.	VDDIN33

QFP144 pin	GPIO	GPIO Alternate Functions	Feature
52	N.A.	N.A.	GNDPLL
55	N.A.	N.A.	VDDCORE
56	N.A.	N.AG	NDCORE
37	N.A.	N.A.	GNDANA
34,35	N.A.	N.A.	ADCREFP/N
38	N.A.	N.A.	VDDANA
5,76,104,119	N.A.	N.A.	GNDVDDIO
5,75,103,118	N.A.	N.A.	VDDIO

3.1.3. Configurations and Test Points

3.1.3.1. Hardware Configurations

The default hardware configuration of the power supply block implies that:

- The power supply source is one of the 2x USB plugs, "USB USER" or "USB VCP", or the jack header
 - [Figure 3-1 AT32UC3C-EK Power Supply Logical View](#) on page 8
 - [Figure 2-1 AT32UC3C-EK Block Diagram](#) on page 6
- The 2-pins header (J2) can also be used as a power supply source (not available by default)

Mount the 0Ω R73 resistor (solder strap) and remove the 0Ω R71 resistor, to enable the 2-pins header external entry (J2).

3.1.3.2. Test Points

A few test points covering the power supply block have been placed on the AT32UC3C-EK for the verification of important signals.

Table 3-2 Power Supply Block Test Points

Designation	Feature
TP12-14	Input voltage level after D1 when the J1 external Power Supply is used
TP20-21	Input voltage level after D2 when the J2 external Power Supply is used
TP22-23	Input voltage for 3.3V regulator. 5V nominal
TP24-25	Input voltage for all board components. 3.3V nominal
TP28-31	Input voltage for all board components except Atmel AT32UC3C0512C and Atmel AT42QT1080. Should be 3.3V nominal
TP27-30	Input voltage for the AT32UC3C0512C VDDIO pin. Should be 3.3V nominal
TP26-29	Input voltage for the AT32UC3C0512C VDDIN pin. Should be 3.3V nominal
TP32-33	Input voltage for the AT32UC3C0512C VDDANA pin. Should be 3.3V nominal
TP13	GND

3.1.4. Power Consumption Measurement

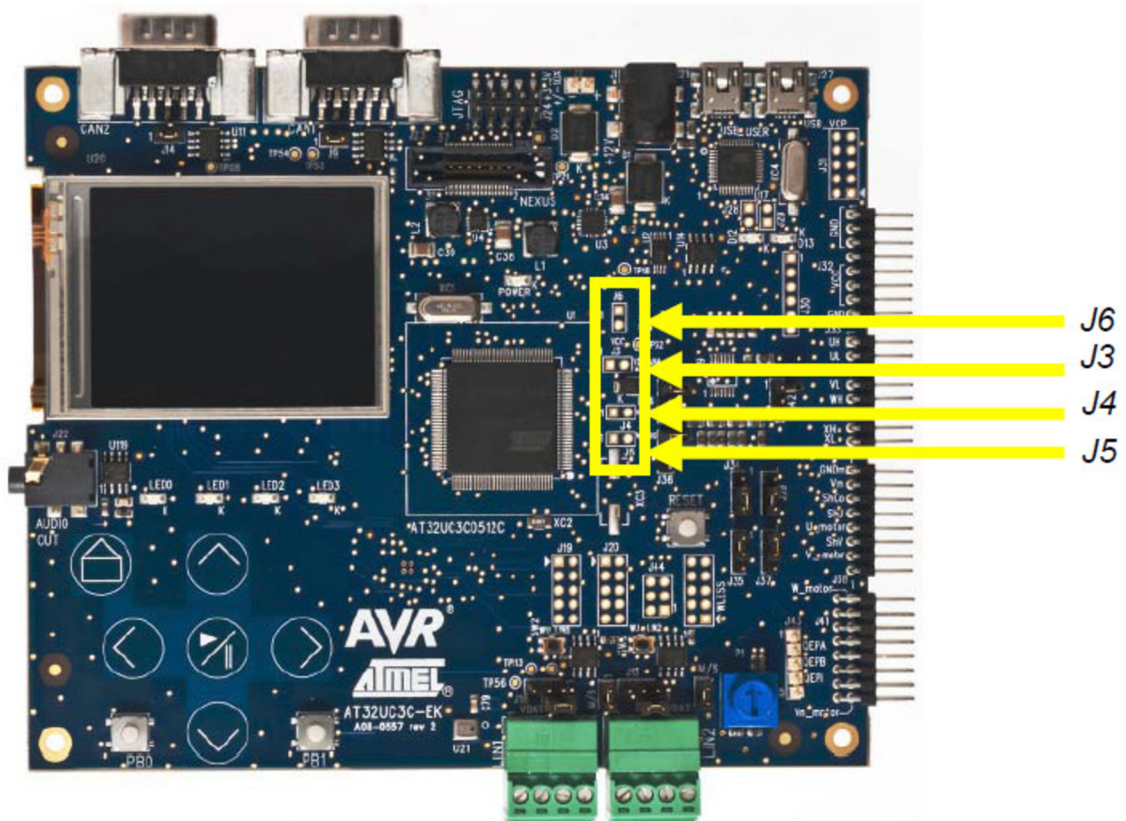
To measure the power consumption of the overall board not including the AT32UC3C0512C, remove the 0Ω R24, 25, 26, 27 resistors and insert the amp meter in the 2-pins header J6 (not mounted by default).

To measure the power consumption on the AT32UC3C0512C VDDIO, remove the 0Ω R26 resistor and insert the amp meter in the 2-pins header J5 (not mounted by default).

To measure the power consumption on the AT32UC3C0512C VDDIN, remove the 0Ω R25 resistor and insert the amp meter in the 2-pins header J4 (not mounted by default).

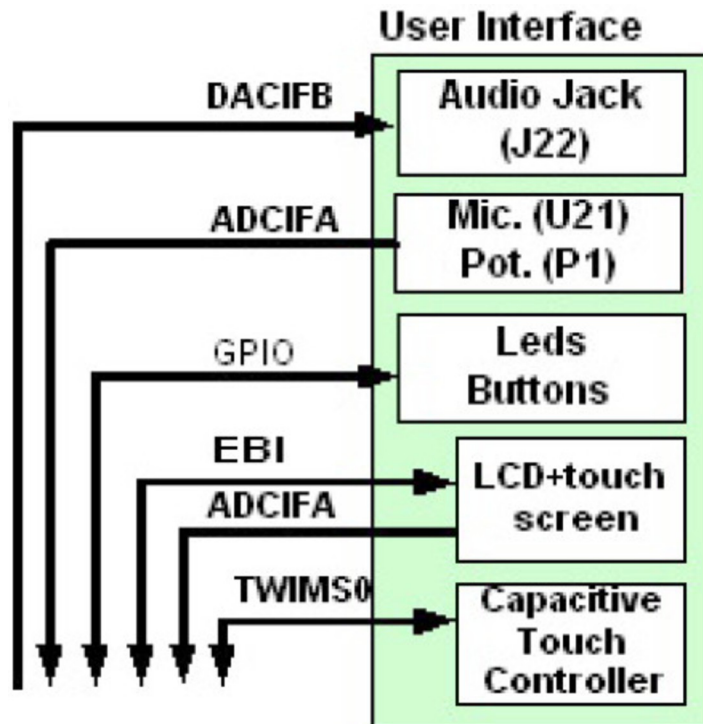
To measure the power consumption on the AT32UC3C0512C VDDANA, remove the 0Ω R24 resistor and insert the amp meter in the 2-pins header J3 (not mounted by default).

Figure 3-4 AT32UC3C-EK Power Consumption Measurement Headers Location



3.2. User Interface

Figure 3-5 AT32UC3C-EK User Interface Logical View



3.2.1. Overview

The main user interface offered by the kit is the touch user interface consisting of the:

- 6x button sensors interfaced through the TWI interface of the Atmel AT32UC3C0512C and a QVGA LCD display interfaced through the EBI interface of the AT32UC3C0512C with touch screen interfaced through the ADCIFA interface of the AT32UC3C0512C
- 4x general purpose LEDs (labeled LED0, LED1, LED2, and LED3) connected to the AT32UC3C0512C
- The 2x push-button labeled PB0 and PB1 used as general purpose push-button
- The push-buttons labeled RST used to generate an external reset to the AT32UC3C0512C
- An audio jack header is connected to one channel of the DACIFB IP of the AT32UC3C0512C
- A microphone and a potentiometer each connected to one channel of the ADCIFA interface of the AT32UC3C0512C

Note that there are other user interface components in the kit, these are related to:

- The USB Interface is presented in [USB Interface](#) on page 31
- The Virtual Com Port Interface is presented in [USB Interface](#) on page 31

Figure 3-6 AT32UC3C-EK Top View User Interface Location

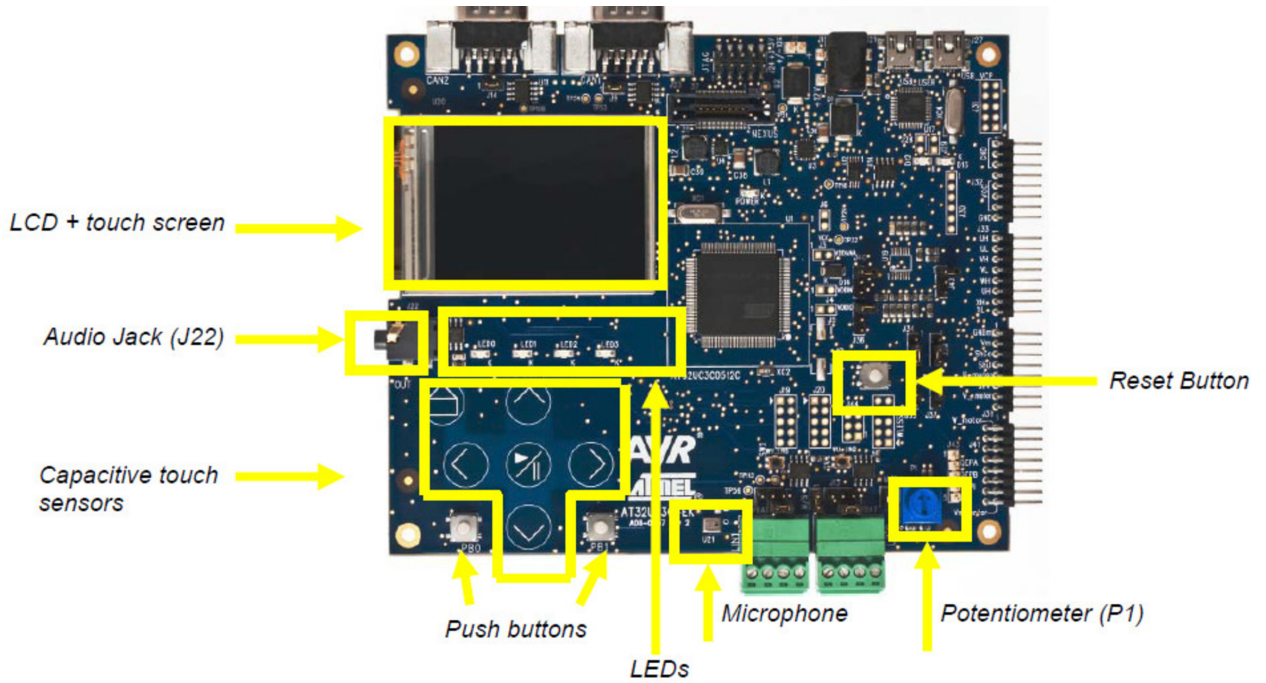
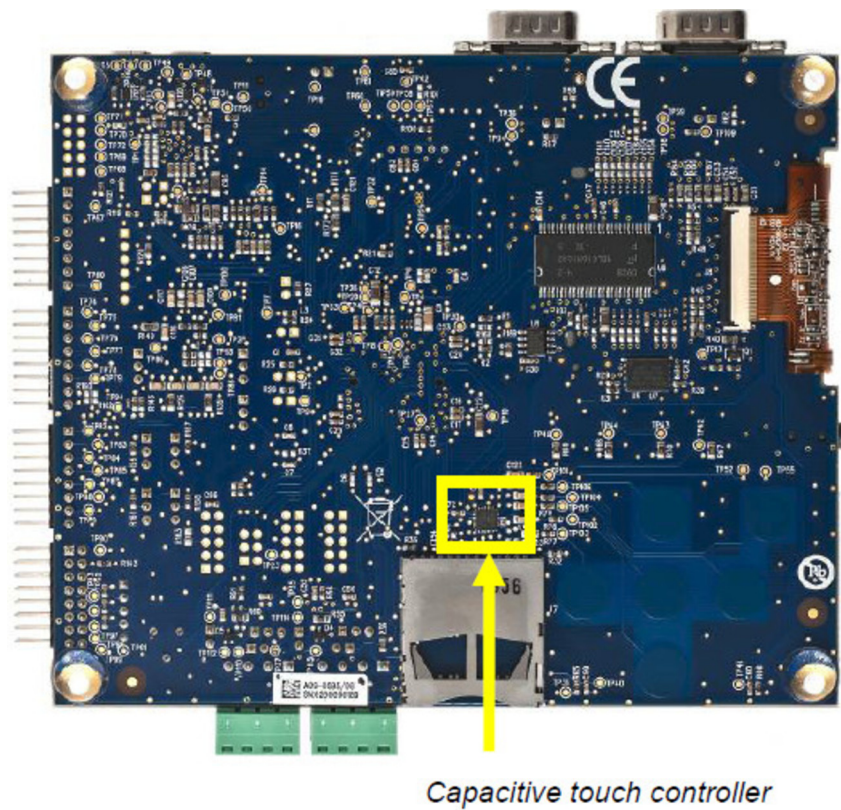


Figure 3-7 AT32UC3C-EK Bottom View User Interface Location



3.2.2. UC3C-Specific Information
AT32UC3C0512C pinout for the User Interface block

Table 3-3 UC3C Pinout for the Touch Sensors Interface

QFP144 pin	GPIO	GPIO Alternate Functions	Feature
73	PC02	TWIMS0_TWD	TWI Data
74	PC03	TWIMS0_TWCK	TWI Clock

Table 3-4 UC3C Pinout for the LEDs and Push-Buttons Interfaces

QFP144 pin	GPIO	GPIO Alternate functions	Feature
25	PA8	GPIO[8]	LED0
132	PD23	GPIO[119]	LED1
86	PC13	GPIO[77] or PWMH[2]	LED2
131	PD22	GPIO[118] or TC0-A2	LED3
31	PA14	GPIO[14]	PB0 push-button
48	PA29	GPIO[29] or EXTINT[0]	PB1 push-button
	N.A.	N.A.	RST push-button, connected to the RESET_N pin

Table 3-5 UC3C Pinout for the Audio Jack, Microphone, and Potentiometer

QFP144 pin	GPIO	GPIO Alternate functions	Feature
44	PA25	ADCIFA-ADCIN14	Microphone Input
32	PA15	DACIFB-DAC1B	Jack Audio
26	PA9	ADCIFA-ADCIN5	Potentiometer

Table 3-6 UC3C Pinout for the QVGA LCD Display

QFP144 pin	GPIO	GPIO Alternate functions	Feature
22	PA5	ADCIFA-ADCIN1	TFT YU Line Measurement
30	PA13	ADCIFA-ADCIN15	TFT YD Line Measurement
43	PA24	ADCIFA-ADCIN13	TFT XR Line Measurement
21	PA4	ADCIFA-ADCIN0	TFT XL Line Measurement
58	PB19	SPI1-MOSI	TFT Interface through the SPI is not implemented by default. See Configurations and Test Points on page 10
59	PB20	SPI1-MISO	TFT Interface through the SPI is not implemented by default. See Configurations and Test Points on page 10
60	PB21	SPI1-SCKI	TFT Interface through the SPI is not implemented by default. See Configurations and Test Points on page 10

QFP144 pin	GPIO	GPIO Alternate functions	Feature
92-106 107-109	PC19-31 PD0-2	EBI D0 - EBI D12 EBI D13 - EBI D15	TFT Data Bus
128	PD19	EBI A15	TFT TE Signal
134	PD25	EBI NWE0	TFT Write Signal
135	PD26	EBI NRD	TFT Read Signal
125	PD16	EBI 16	TFT Reset Signal
137	PD28	GPIO[124] or TC0-B0	TFT Backlight Signal

3.2.3. Hardware Configuration and Test Points

Hardware Configuration

The default hardware configuration of the user interface block connects the QVGA LCD Display is connected through parallel interface (with EBI). To switch to the serial interface (with SPI):

- Remove the 0Ω R44 and R52 resistors
- Mount the 0Ω R48 and R54 resistors

Test points

A few test points covering the user interface block have been placed on the Atmel AT32UC3C-EK for the verification of important signals.

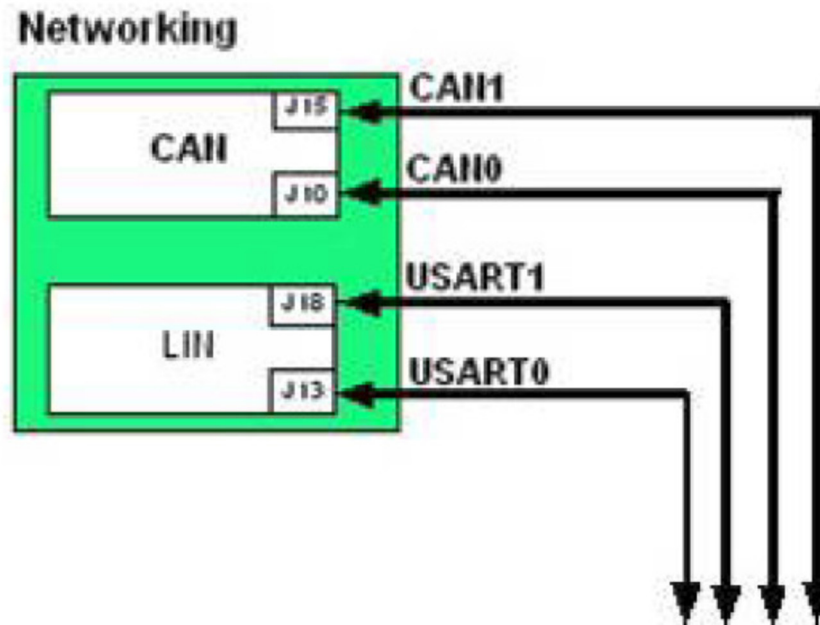
Table 3-7 Power Supply Block Test Points

Designation	Feature
TP1	Input voltage on the AT32UC3C0512C RESET_N pin depending on the state of the RST push-button
TP101-106	Input Capacitive Touch Buttons CS1-CS6
TP41	Input voltage on the AT32UC3C0512C PB0 pin depending on the state of the PB0 push-button
TP40	Input voltage on the AT32UC3C0512C PB1 pin depending on the state of the PB1 push-button
TP42	Voltage level on LED0
TP43	Voltage level on LED1
TP44	Voltage level on LED2
TP45	Voltage level on LED3

3.3. Networking

The networking block of the AT32UC3C-EK covers all components providing CAN and LIN bus interfaces through DB9 connectors and 3-pins headers.

Figure 3-8 Atmel AT32UC3C-EK Networking Logical View

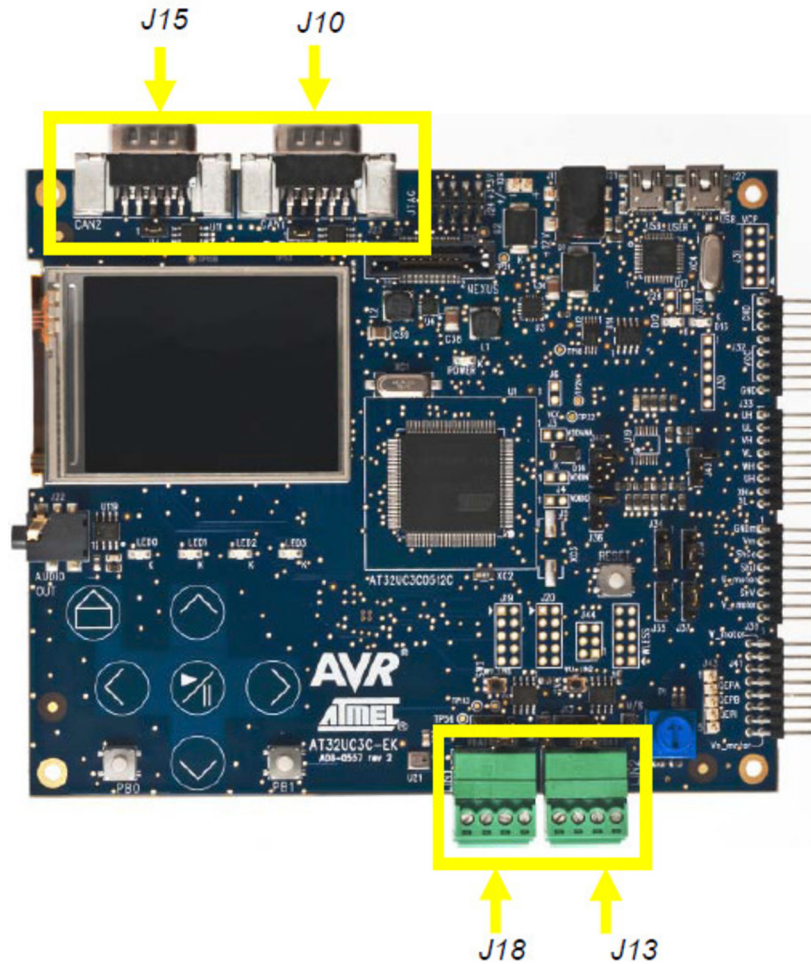


3.3.1. Overview

The networking block supports both CAN and LIN interface:

- The CAN transceivers are embedded on the UC3C-EK (U9 and U11) and termination resistors can be used as bus configuration through 2-pin headers (J9 and J14). See [Configurations and Test Points](#) on page 10. The physical connections of CAN bus are accessible through DB9 connectors (J10 and J15).
- The LIN transceivers are embedded on the UC3C-EK (U10 and U12). The master/slave configurations are accessible through 2-pin headers (J12 and J17). The board supports also the capability to be powered-up by LIN bus through 2 pin headers (J11 and J16). See [Configurations and Test Points](#) on page 10. The physical connections of LIN bus are accessible through 3-pins headers (J13 and J18).

Figure 3-9 AT32UC3C-EK Top View Networking Location



3.3.2. UC3C-Specific Information

AT32UC3C0512C pinout for the User Interface block

Table 3-8 UC3C Pinout for the CAN Interface

QFP144 pin	GPIO	GPIO Alternate functions	Feature
36	PB04	RX CAN0	RX CAN
37	PB05	TX CAN0	TX CAN
84	PC11	RX CAN1	RX CAN
85	PC12	TX CAN1	TX CAN

Table 3-9 UC3C Pinout for the LIN Interface

QFP144 pin	GPIO	GPIO Alternate functions	Feature
19	PB16	RX LIN0	RX LIN
20	PB17	TX LIN0	TX LIN

QFP144 pin	GPIO	GPIO Alternate functions	Feature
88	PC15	RX LIN1	RX LIN
89	PC16	TX LIN1	TX LIN

3.3.3. Configuration and Test Points

Hardware Configuration

The terminal resistors are mounted by default. Remove jumpers on the 2-pins headers (J9 or J14) to suppress this termination.

The default hardware configuration of the LIN block implies that two nodes are in master configuration. Only remove jumpers on the 2-pins headers (J12 or J17) to switch the node in slave configuration. Moreover, the board is by default powered by the LIN bus.

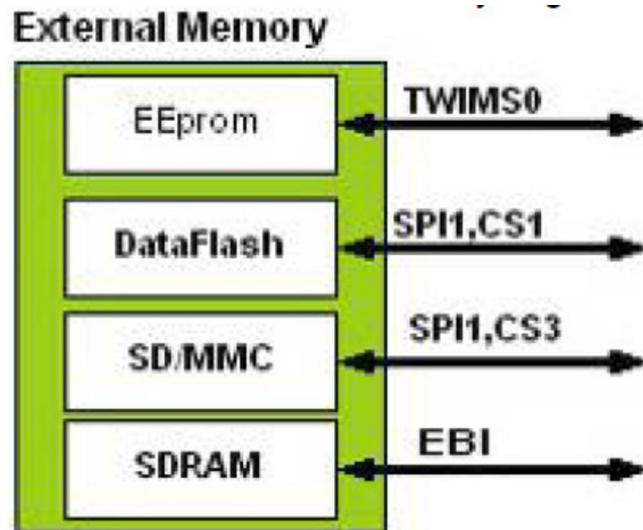
To suppress this feature, remove jumpers on the 2-pins headers (J11 or J16).

3.4. External Memory

The External Memory on the Atmel AT32UC3C-EK provides extra memory to the Atmel AT32UC3C0512C.

3.4.1. Overview

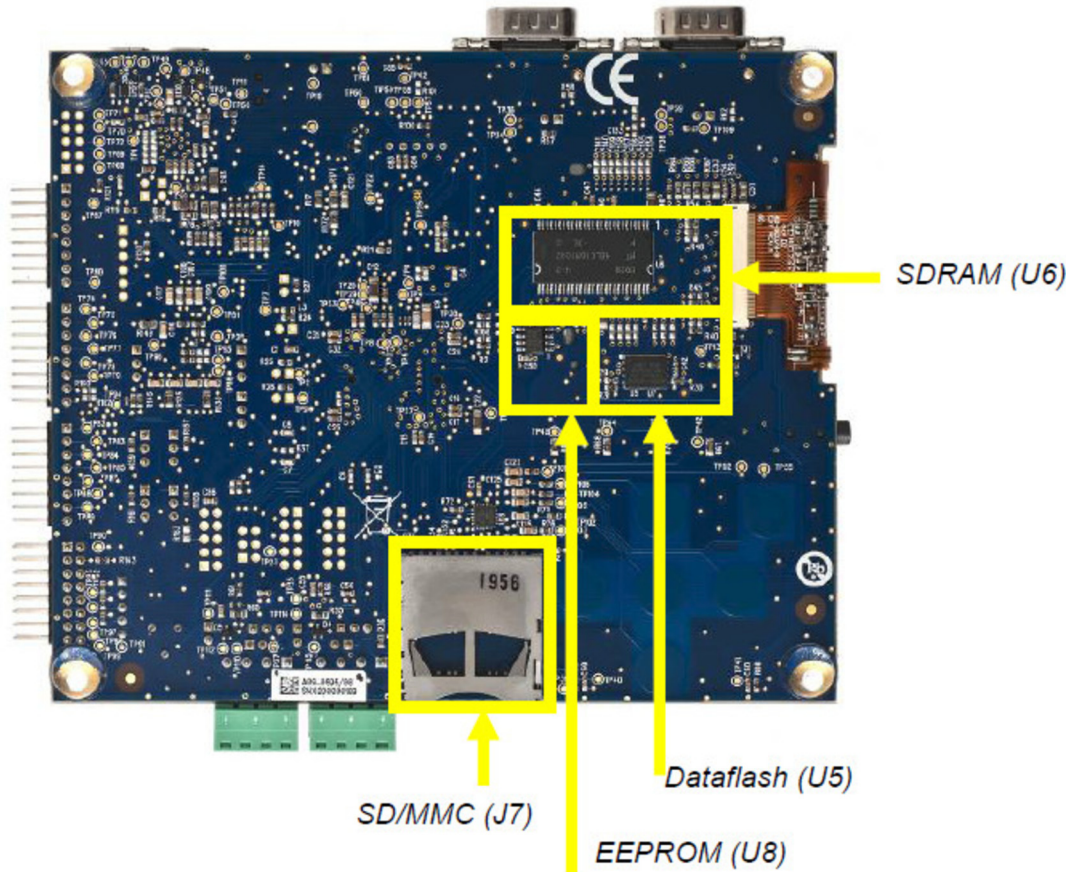
Figure 3-10 AT32UC3C-EK External Memory Logical View



The AT32UC3C-EK implements:

- A 128-bits Atmel EEPROM device (AT24C128) connected to the TWIMS0 interface of the Atmel AT32UC3C0512C and referenced as U8
- A 64Mbit Atmel Dataflash device (AT45DB642D-CNU) connected to the SPI1 interface (chip select 1) of the AT32UC3C0512C and referenced as U7
- A SD/MMC slot connected to the SPI1 interface (chip select 3) of the AT32UC3C0512C and referenced as J7
- A 256Mbit SDRAM (MT48LC16M16A2) connected to the EBI interface of the AT32UC3C0512C and referenced as U6

Figure 3-11 AT32UC3C-EK Bottom View External Memory Location



3.4.2. UC3C-Specific Information

Table 3-10 UC3C Pinout for the EEPROM

QFP144 pin	GPIO	GPIO Alternate functions	Feature
73	PC02	TWIM0_TWD	TWI Data
74	PC03	TWIM0_TWCK	TWI Clock

Table 3-11 UC3C Pinout for the Atmel DataFlash

QFP144 pin	GPIO	GPIO Alternate functions	Feature
58	PB19	SPI1.MISO	Dataflash SO
59	PB20	SPI1.MOSI	Dataflash SI
60	PB21	SPI1.SCK	Dataflash SCK
63	PB24	SPI1.NPCS1	Dataflash #CS
142	N.A.	N.A. RESET_N pin	Dataflash #RESET

Table 3-12 UC3C Pinout for the SD/MMC Slot

QFP144 pin	GPIO	GPIO Alternate functions	Feature
58	PB19	SPI1.MISO	SD SO
59	PB20	SPI1.MOSI	SD SI
60	PB21	SPI1.SCK	SD SCK
61	PB22	SPI1.NPCS3	SD #CS
139	PD30	GPIO[28]	SD Write Protect
47	PA28	GPIO[126]	SD Card Protect

Table 3-13 UC3C Pinout for the SDRAM

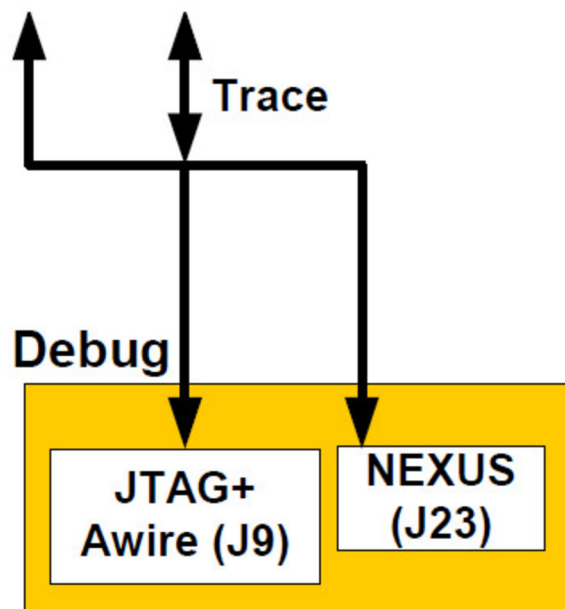
QFP144 pin	GPIO	GPIO Alternate functions	Feature
92-106	PC19-31	EBI D0 - EBI D12	SDRAM Data Bus
107-109	PD0-2	EBI D13- EBI D15	
112-124	PD5-15	EBI A2-A11	SDRAM Address Bus
126-127	PD17-18	EBI A13-A14	
129-130	PD20-21	EBI A16-A17	
122	PD13	EBI SDCK	SDRAM Clock
87	PC14	EBI SDCKE	SDRAM SDCKE
88	PC15	EBI SDWEN	SDRAM SDWEN
89	PC16	EBI CASn	SDRAM CASn
90	PC17	EBI RASn	SDRAM RASn
91	PC18	EBI SDA10	SDRAM SDA10
97	PD24	EBI DQM1	SDRAM DQM1
110	PD3	EBI DQM0	SDRAM DQM0
136	PD27	EBI CS	SDRAM CS

3.5. Programming and Debugging Interface

The Programming and Debugging Interface block of the Atmel AT32UC3C-EK provides the developer a mean to debug an application running on the Atmel AT32UC3C0512C.

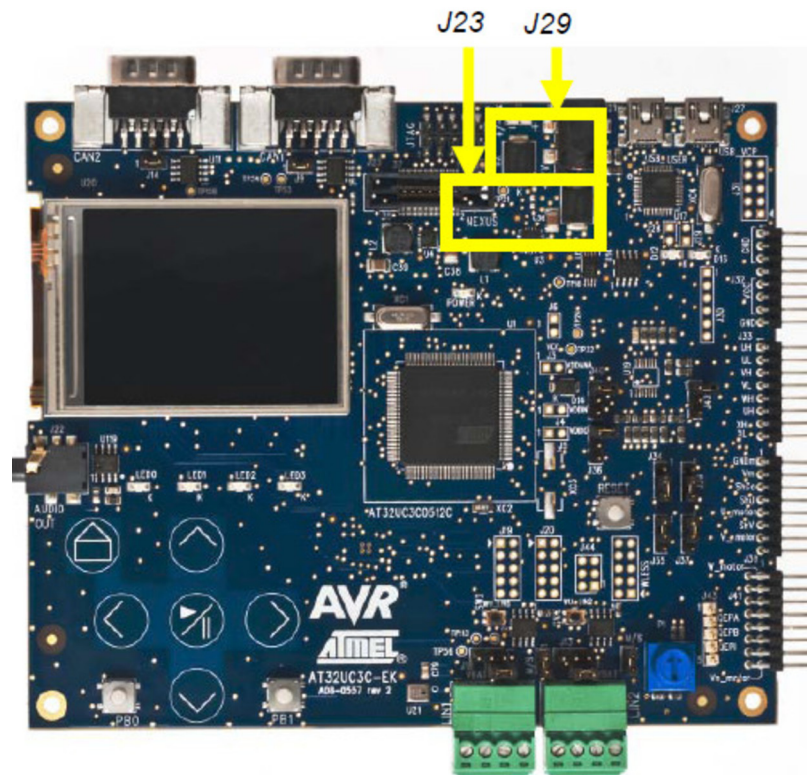
3.5.1. Overview

Figure 3-12 AT32UC3C-EK Programming and Debugging Interface Logical View



The main Programming and Debugging Interface of the AT32UC3C-EK is meant to program and debug the Atmel AT32UC3C0512C. There are two debug interfaces implemented in the AT32UC3C0512C: the JTAG interface accessible through the J24 connector and the NEXUS interface accessible through the J23 connector.

Figure 3-13 AT32UC3C-EK Programming and Debugging Interface Location



3.5.2. UC3C-Specific Information

Table 3-14 UC3C Pinout for the JTAG Interface

QFP144 pin	GPIO	GPIO Alternate functions	Feature
1	PA00	None	JTAG.TCK
2	PA01	None	JTAG.TDI
3	PA02	None	JTAG.TDO
4	PA03	None	JTAG.TMS
142	N.A.	N.A.	RESET_N pin. Used when enabling/disabling the JTAG or the aWire interface. Also, the aWire data is multiplexed on this pin.

Table 3-15 UC3C Pinout for the JTAG Interface

QFP144 pin	GPIO	GPIO Alternate functions	Feature
1	PA00	None	JTAG.TCK
2	PA01	None	JTAG.TDI
3	PA02	None	JTAG.TDO
4	PA03	None	JTAG.TMS
142	N.A.	N.A.	RESET_N pin. Used when enabling/disabling the JTAG or the aWire interface. Also, the aWire data is multiplexed on this pin.
27	PA10	N.A.	EVTI_N
9	PB06	N.A.	MDO[5]
18	PB15	N.A.	MDO[4]
17	PB14	N.A.	MDO[3]
46	PA27	N.A.	MDO[2]
45	PA26	N.A.	MDO[1]
36	PA19	N.A.	MDO[0]
138	PD29	N.A.	EVTO_N
65	PB26	N.A.	MCKO
64	PB25	N.A.	MSEO[1]
57	PB18	N.A.	MSEO[0]

3.5.3. Configuration and Test Points

Special Considerations for the NEXUS pins

On the Atmel AVR UC3 C series, the NEXUS pins are multiplexed with I/O lines. While using these multiplexed NEXUS lines all normal peripheral activity on these lines are disabled. The user must make sure that no external peripheral is blocking the NEXUS lines while debugging.

Table 3-16 Conflicts Conditions over the NEXUS Debugging Pins on page 23 highlights the components of the Atmel AT32UC3C-EK that might interfere with the multiplexed NEXUS pins. These components must not be used while debugging with the NEXUS interface.

Table 3-16 Conflicts Conditions over the NEXUS Debugging Pins

QFP144 pin	GPIO	Conflict conditions
18	PB15	Nexus pin in conflict with Wireless (WLESS) CTS Signal
17	PB14	Nexus pin in conflict with Wireless (WLESS) RTS Signal
64	PB25	Nexus pin in conflict with Wireless (WLESS) CS Signal

To summarize, debugging on NEXUS will not work if:

- The WLESS connector is used

Test Points

A few test points covering the Programming and Debugging Interface block have been placed on the AT32UC3C-EK for the verification of important signals.

Table 3-17 Programming and Debugging Interface Block Test Points

Designation	Feature
TP57	JTAG.TCK
TP58	JTAG.TDO
TP59	JTAG.TMS
TP60	JTAG.TDI
TP61	GND
TP62	VCC3
TP63	RESET_N

Using the aWire

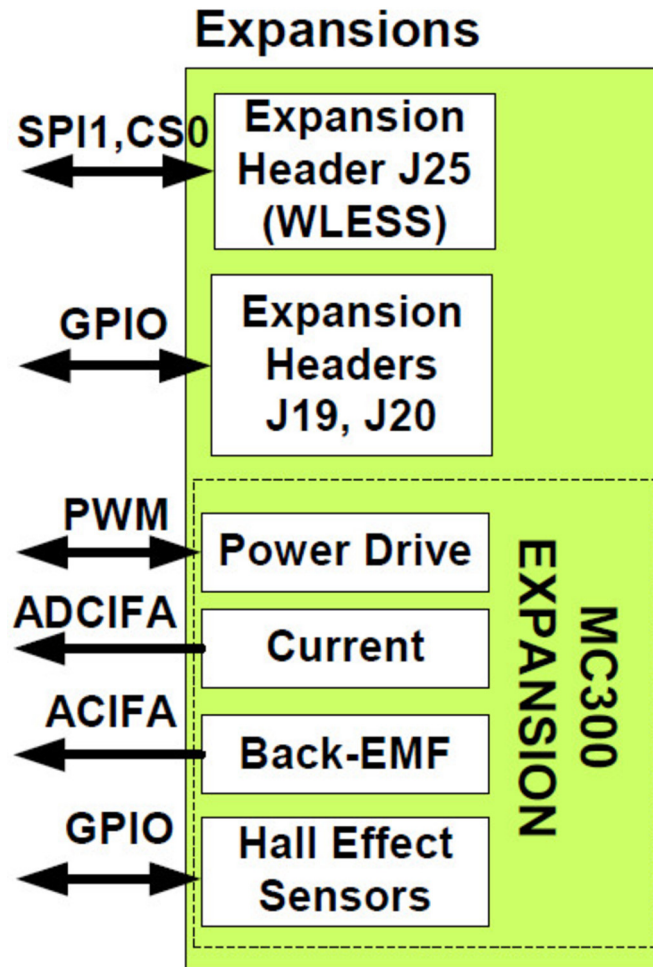
The Atmel AVR ONE! and JTAGICE mkII tools can interface with the Atmel AVR UC3 C series using the single-wire aWire interface available on J24. Check the documentation of these tools to find out the recommended pinout to connect to an aWire target.

3.6. Expansion Interface

The expansion interface on the AT32UC3C-EK offers the possibility to connect various external devices to the AT32UC3C0512.

3.6.1. Overview

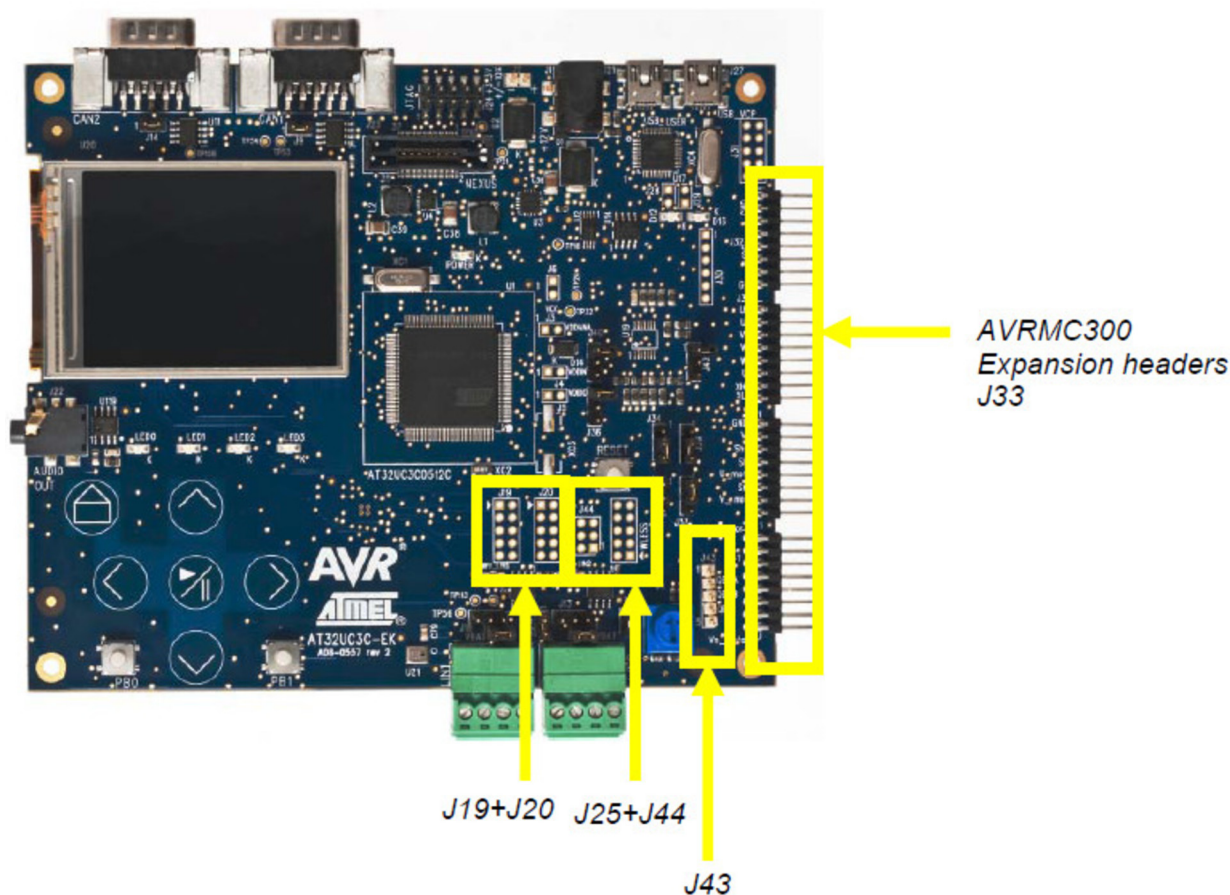
Figure 3-14 AT32UC3C-EK Expansion Interface Logical View



There are three expansion headers on the Atmel AT32UC3C-EK:

- The J25 header (labeled WLESS) to connect the wireless extension board to provide wireless communication capabilities to the kit. Signals on J25.1 and J25.2 are configurable with the J44 header. The Atmel AT32UC3C0512C modules available on J25 are USART1 and SPI1; depending on the J44 configuration, TWIMS0 is available too.
- The J19 and J20 headers provide access to several GPIOs of the AT32UC3C0512C and ground and VCC3.
- The Atmel AVRMC300 expansion offers the possibility to connect an AVRMC300 expansion motor control board:
 - The J33 header provides access to the power driver control signals (PWM signals)
 - The J38 header provides access to the current and back-EMF measurement (ADC and AC signals)
 - The J41 header provides access to Hall-Effect sensors (GPIO signals)
 - The J43 header provides access to quadrature decoder sensors (QDEC signals)
- Refer to [Reference Materials](#) on page 7 for more detailed information.

Figure 3-15 AT32UC3C-EK Top View Expansion Headers Location



3.6.2. UC3C-Specific Information

AT32UC3C0512C pinout for the Expansion Interfaces

Table 3-18 UC3C Pinout for the J25 and J44 Headers

QFP144 pin	GPIO	GPIO Alternate functions	Feature
17	PB14	USART1.RTS	Provides access to the USART1.RTS signal. Available on J25.1 if J44 is configured with a jumper connecting J44.3 to J44.5
18	PB15	USART1.CTS	Provides access to the USART1.CTS signal. Available on J25.2 if J44 is configured with a jumper connecting J44.4 to J44.6
19	PB25	SPI1.NPCS[0]	WLESS SPI Chip select. Available on J25.5
64	PB20	SPI0.MISO	WLESS.MISO signal. Available on J25.7
74	PC03	TWIMS0.TWCK	Provides access to the TWI0 TWCK signal. Available on J25.2 if J44 is configured with a jumper connecting J44.2 to J44.4
58	PB19	SPI1.MOSI	WLESS.MOSI signal. Available on J25.6

QFP144 pin	GPIO	GPIO Alternate functions	Feature
73	PC02	TWIMS0.TWD	Provides access to the TWIMS0 TWD signal. Available on J25.1 if J44 is configured with a jumper connecting J44.1 to J44.3
60	PB21	SPI1.SCK	WLESS SPI clock. Available on J25.8
19	PB16	USART1.TX	Provides access to the USART1.TX signal. Available on J25.4
20	PB17	USART1.RX	Provides access to the USART1.RX signal. Available on J25.3
N.A.	N.A.	N.A.	GND. Available on J25.9
N.A.	N.A.	N.A.	VCC3. Available on J25.10

Table 3-19 UC3C Pinout for the J19 Header

QFP144 pin	GPIO	GPIO Alternate functions	Feature
81	PC8	Software-dependant	J19.3
82	PC9	Software-dependant	J19.4
84	PC10	Software-dependant	J19.5
101	PC28	Software-dependant	J19.6
102	PC29	Software-dependant	J19.7
100	PC27	Software-dependant	J19.9
			GND on J19.10
			VCC3 on J19.2
			VCC5 on J19.8
			VCC12 on J19.1

Table 3-20 UC3C Pinout for the J20 Header

QFP144 pin	GPIO	GPIO Alternate functions	Feature
111	PD4	Software-dependant	J20.3
112	PD5	Software-dependant	J20.4
113	PD6	Software-dependant	J20.5
124	PD15	Software-dependant	J20.6
125	PD16	Software-dependant	J20.7
126	PD7	Software-dependant	J20.9
			GND on J20.10
			VCC3 on J20.2

QFP144 pin	GPIO	GPIO Alternate functions	Feature
			VCC5 on J20.8
			VCC12 on J20.1

Table 3-21 UC3C Pinout for the Power Drives Control Signal - J33

QFP144 pin	GPIO	GPIO Alternate functions	Feature
12	PB9	PWM-PWMH[0]	Provides access to the PWM UH signal available on J33.1
11	PB8	PWM-PWML[0]	Provides access to the PWM UL signal available on J33.2
14	PB11	PWM-PWMH[1]	Provides access to the PWM VH signal available on J33.3
13	PB10	PWM-PWML[1]	Provides access to the PWM VL signal available on J33.4
16	PB13	PWM-PWMH[2]	Provides access to the PWM WH signal available on J33.5
15	PB12	PWM-PWML[2]	Provides access to the PWM WL signal available on J33.6
18	PB15	PWM-PWMH[3]	Provides access to the PWM XH signal available on J33.5. See configuration section to activate this feature
17	PB14	PWM-PWML[3]	Provides access to the PWM XL signal available on J33.6. See configuration section to activate this feature

Table 3-22 UC3C Pinout for the Current and Back EMF Measurement - J38

QFP144 pin	GPIO	GPIO Alternate functions	Feature
23	PA6	ADCIFA-ADCIN2 or ACIFA-AC1AP1	ADC Input 0 positive channel or Analog Comparator 0 Input positive. See section AVRMC300 Configuration on page 28 to select one of the two features
23	PA7	ADCIFA-ADCIN3 or ACIFA-AC1AN1	ADC Input 1 positive channel or Analog Comparator 0 Input negative. See section AVRMC300 Configuration on page 28 to select one of the two features
39	PA20	ADCIFA-ADCIN9 or ACIFA-AC0AP0	ADC Input 0 negative channel or Analog Comparator 1 Input positive. See section AVRMC300 Configuration on page 28 to select one of the two features
41	PA22	ACIFA-AC0AN0	Analog Comparator 1 Input negative
42	PA23	ACIFA-AC0BP0	Analog Comparator 2 Input positive
40	PA21	ADCIFA-ADCIN0 or ACIFA-AC0BN0	ADC Input 1 negative channel or Analog Comparator 2 Input negative. See section AVRMC300 Configuration on page 28 to select one of the two features
29	PA12	DACIFB-DAC1A	DAC Output

Table 3-23 UC3C Pinout for the Hall Effect Sensors - J41

QFP144 pin	GPIO	GPIO Alternate functions	Feature
66	PB27	GPIO[59]	
67	PB28	GPIO[60]	
68	PB29	GPIO[61]	

Table 3-24 UC3C Pinout for the Hall Effect Sensors - J41

QFP144 pin	GPIO	GPIO Alternate functions	Feature
66	PB27	QDEC - QEPA	Quadrature Decoder Line A
67	PB28	QDEC - QEPB	Quadrature Decoder Line B
68	PB29	QDEC - QEPI	Quadrature Decoder Line I
			GND on J43.5
			VCC3 on J43.1

3.6.3. Configuration and Test Points

The J25.1 and J25.2 pins are configurable through the J44 header. Refer to [Table 3-18 UC3C Pinout for the J25 and J44 Headers](#) on page 25 for a description of the possible configurations.

AVRMC300 Configuration

The XL and XH signals are multiplexed with NEXUS signals. Due to that, 0Ω resistors (R160 and R162) are inserted between these signals and I/O signals. There are not mounted by default. It means NEXUS signals are functional. Just mount these resistors to activate XL and XH signals.

The differential measures and comparator detections are multiplexed. Due to that, 0Ω resistors (R157, R158, R159, and R161) are inserted. As there are mounted by default, differential measures and comparator detections are accessible.

Test points

None.

Weaknesses

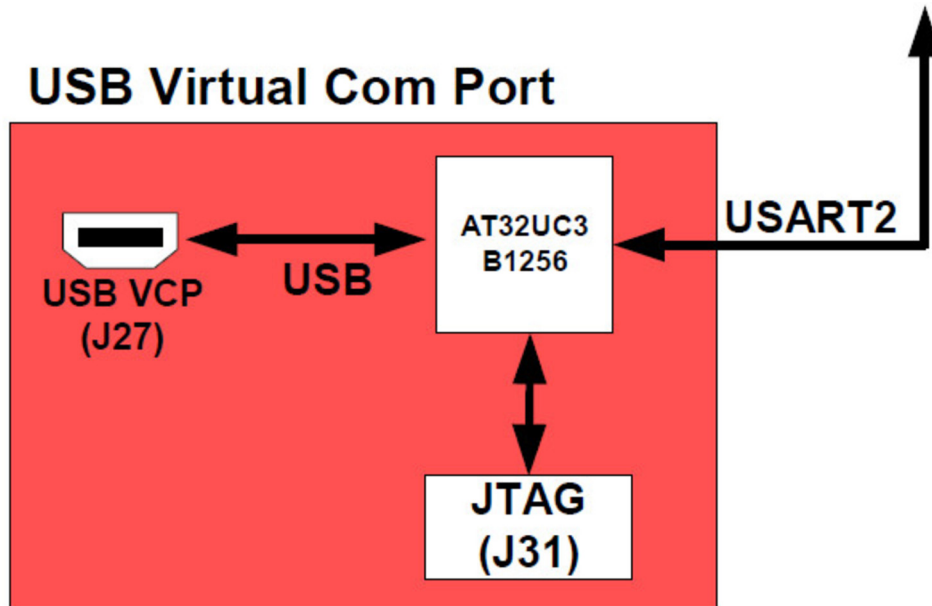
None known.

3.7. USB Virtual Com Port Interface

The USB Virtual Com Port interface on the Atmel AT32UC3C-EK offers USB CDC Serial Com Port communication capabilities to the Atmel AT32UC3C0512C through the on-board Atmel AT32UC3B1256 device.

3.7.1. Overview

Figure 3-16 AT32UC3C-EK Virtual Com Port Interface Logical View



The USB Virtual Com Port interface provides two features to the Atmel AT32UC3CEK kit:

- USB communication
- Power supply (see [Power Supply](#) on page 8 for a description of that feature)

The USB controller is the Atmel AT32UC3B1256. The AT32UC3B1256 comes pre-loaded with several firmwares:

- A USB DFU Bootloader to re-program the AT32UC3B1256
- A USB CDC-USART bridge where every data character received from USB is sent to the Atmel AT32UC3C0512C's USART2 and every character received from the AT32UC3C0512C's USART2 is sent to USB



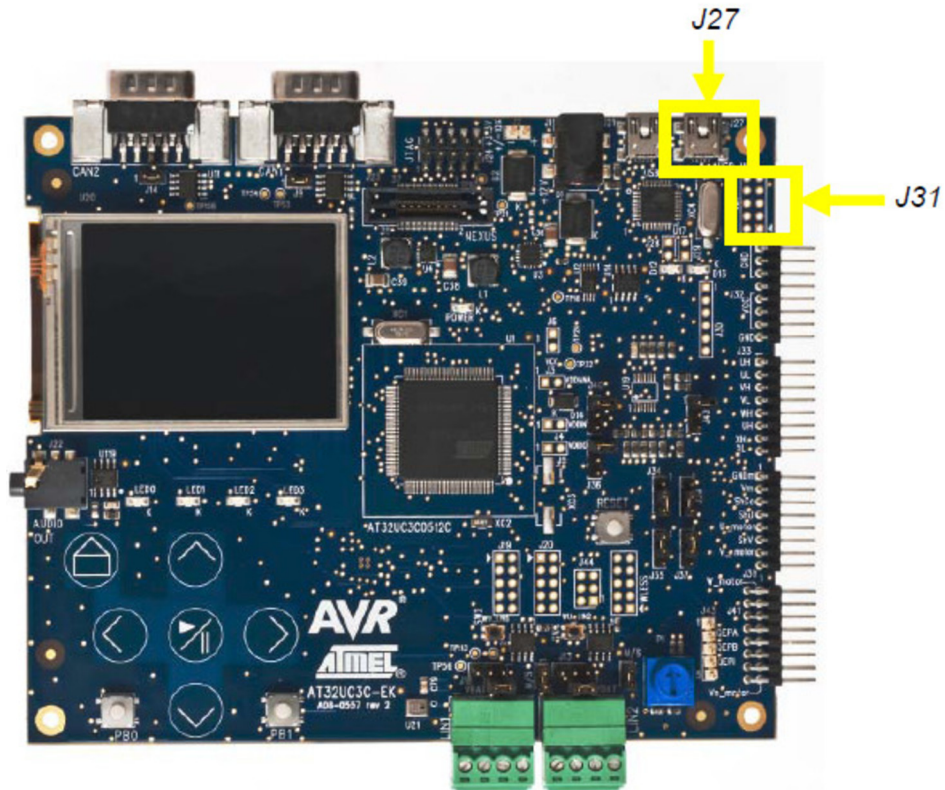
Attention:

Programming the AT32UC3B1256 will overwrite the default firmware.

The AT32UC3B1256 can be debugged through the JTAG interface J31 header.

The AT32UC3B1256 is connected to the AT32UC3C0512C's USART2 TX and RX pins.

Figure 3-17 AT32UC3C-EK Top View Virtual Com Port Interface Position



3.7.2. UC3C-Specific Information

Table 3-25 UC3C Pinout for the USB Virtual Com Port Interface Block

QFP144 pin	GPIO	GPIO Alternate functions	Feature
78	PC05	USART2.RXD	USART2 RX line
77	PC04	USART2.TXD	USART2 TX line

3.7.3. Configuration and Test Points

AT32UC3CB1256 Default Firmware Configuration

The default firmware pre-loaded on the Atmel AT32UC3B1256 is dynamically configurable upon power-up:

- The USB DFU Bootloader can be enabled by closing the J28 jumper
- Use FLIP/batchisp to read/write resources on the AT32UC3B1256 through the bootloader



Attention:

Programming the AT32UC3B1256 will overwrite the default firmware.

Test points

A few test points covering the USB Interface block have been placed on the Atmel AT32UC3C-EK for the verification of important signals.

Table 3-26 USB Interface Block Test Points

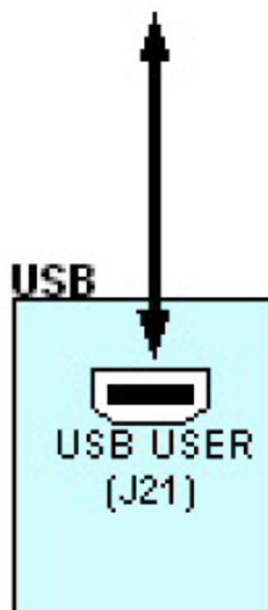
Designation	Feature
TP64	VBUS
TP65	D-
TP66	D+
TP67	GND
TP68	JTAG.TCK.UC3B
TP69	JTAG.TDO.UC3B
TP70	JTAG.TMS.UC3B
TP71	JTAG.TDI.UC3B
TP72	RESET_N.UC3B

3.8. USB Interface

The USB interface on the AT32UC3C-EK demonstrates the USB device and embedded host communication capabilities of the Atmel AT32UC3C0512C.

3.8.1. Overview

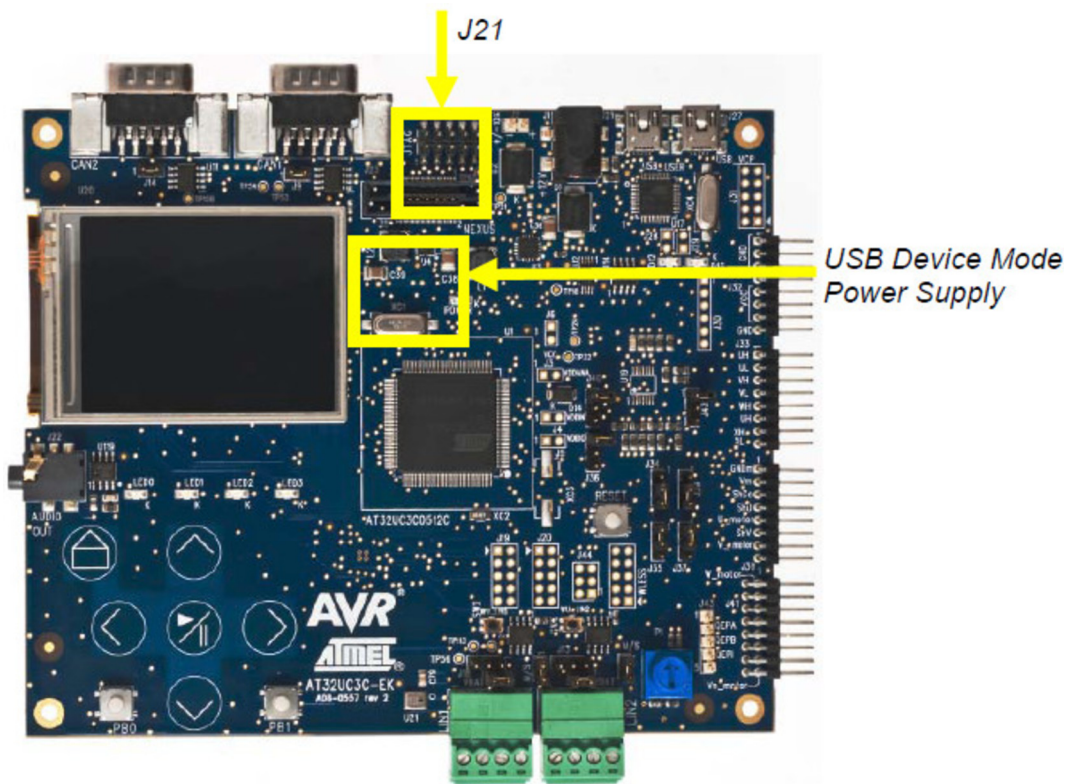
Figure 3-18 AT32UC3C-EK USB Interface Logical View



The USB interface provides two features to the AT32UC3C-EK kit:

- USB communication
- Power supply (see [Power Supply](#) on page 8 for a description of that feature) in USB device mode

Figure 3-19 AT32UC3C-EK Top View USB Interface Location



3.8.2. UC3C-Specific Information

Table 3-27 UC3C Pinout for the USB Interface Block

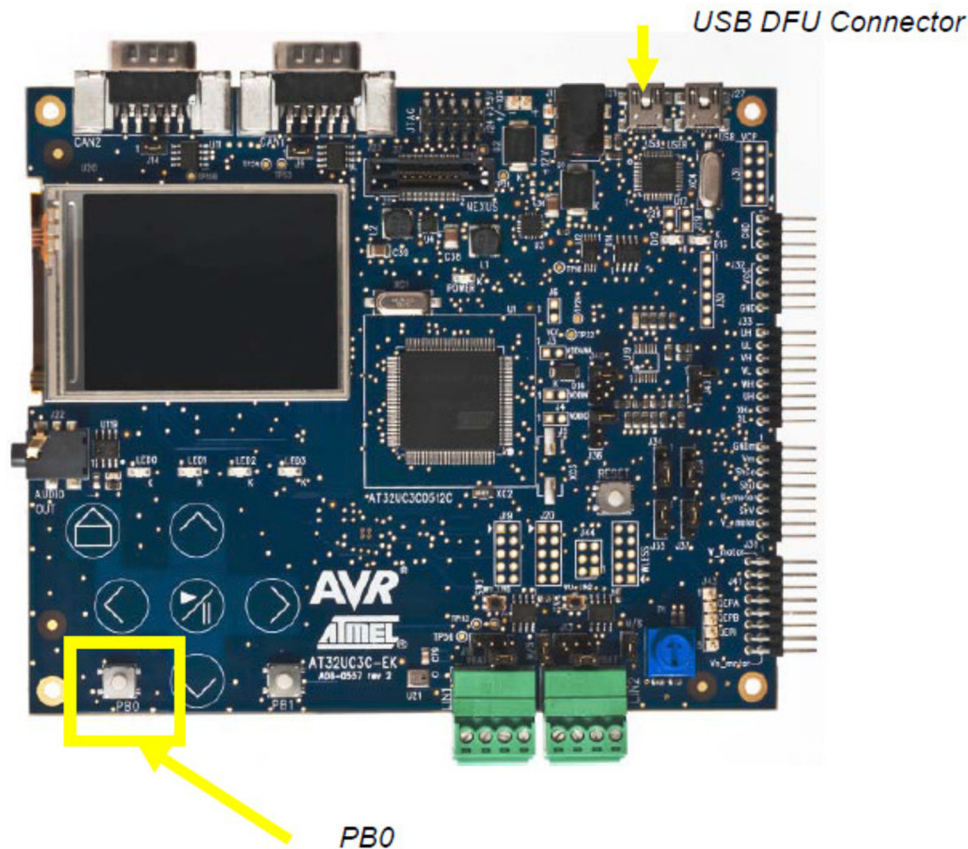
QFP144 pin	GPIO	GPIO Alternate functions	Feature
50	DM	USB	D-
51	DP	USB	D+
72	PC01	GPIO[65]	USB VBOF
71	PC00	GPIO[64]	USB ID
10	PB07	GPIO[39]	USB Over Current

3.8.3. Configuration

Bootloader

A USB DFU Bootloader is pre-loaded on the Atmel AT32UC3C0512C. To enter this bootloader mode, the PB0 push-button must be pressed upon reset, then released. It is then possible to program the AT32UC3C0512C through the USB DFU Bootloader.

Figure 3-20 Atmel AT32UC3C-EK Top View USB Bootloader Interface Location



USB over current detection

By default the overcurrent detection is not enabled. To enable this feature:

- Mount R85 resistor

3.9. AT32UC3C0512C

The Atmel AT32UC3C0512C is the central point of the Atmel AT32UC3C-EK.

3.9.1. Overview

See [Figure 2-1 AT32UC3C-EK Block Diagram](#) on page 6 for a logical view representing a logical view of the AT32UC3C0512C in the kit. The AT32UC3C0512C is powered from the Power Supply block. For a detailed presentation of the Power Supply block, see [Power Supply](#) on page 8.

The AT32UC3C0512C is in charge of the main User Interface block:

- The touch sensors
- The LEDs LED0-4
- The 2x push-button
- The RST push-button
- The QVGA LCD Display
- The microphone and audio jack

For a detailed presentation of the User Interface block, see [User Interface](#) on page 12 The AT32UC3C0512C can be programmed and debugged through the Programming and Debugging Interface

block that provides JTAG or aWire access. For a detailed presentation of the Programming and Debugging Interface block, see [Programming and Debugging Interface](#) on page 20.

The AT32UC3C0512C has access to:

- One external on-board Atmel DataFlash 64Mbit memory
- One external on-board Atmel EEPROM 128-bits memory
- One external on-board SDRAM 256Mbit memory
- One external on-board SD/MMC slot

For a detailed presentation of the External Memory block, see [External Memory](#) on page 18.

Four networking interfaces available on AT32UC3C0512C are accessible:

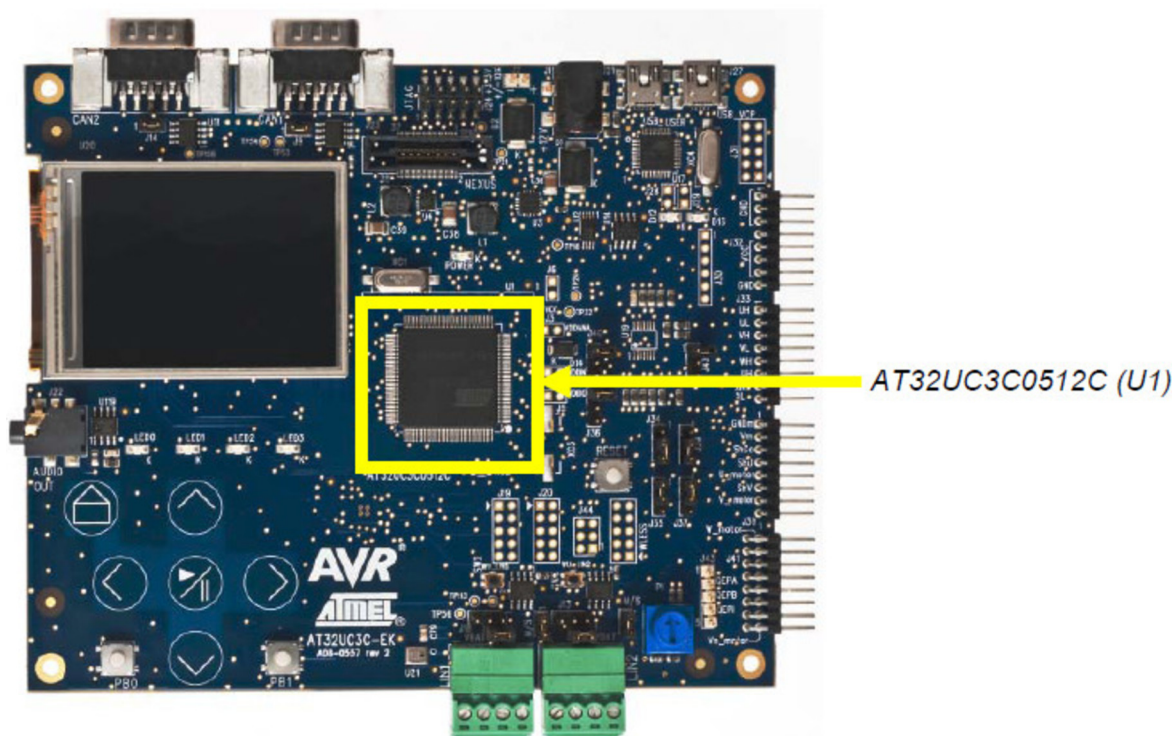
- Two CAN Interfaces
- Two LIN Interfaces

For a detailed presentation of the networking block, see [Networking](#) on page 15. The expansion interface offers the possibility to connect various external devices to the AT32UC3C0512C. The J25 connector (labeled WLESS) is dedicated to interface to wireless extension board (obviously dedicated firmware must be running on the AT32UC3C0512C to support that feature). For a detailed presentation of the expansion Interface block, see [Expansion Interface](#) on page 23.

The AVRMC300 expansion headers offer the possibility to connect AVRMC300 additional board to the AT32UC3C0512C. For a detailed presentation of the AVRMC300 expansion Interface block, see [Configuration and Test Points](#) on page 28.

The USB communication capabilities of the Atmel AT32UC3C0512C interface is also demonstrated and accessible through a mini-B connector. For a detailed presentation of the USB Interface block, see [USB Virtual Com Port Interface](#) on page 28

Figure 3-21 Atmel AT32UC3C-EK Top View AT32UC3C0512C Location



3.9.2. AT32UC3C0512C Pinout

Table 3-28 UC3C Pinout Power Supply Pins and JTAG Pins

QFP144 pin	GPIO	GPIO Alternate functions	Feature
53			VDDIN5
54			VDDIN33
52			GNDPLL
55			VDDCORE
56			GNDCORE
37			GNDANA
34-35			ADCREFP/N
38			VDDANA
5-76-104-119			GNDVDDIO
5-75-103-118			VDDIO
			RST push-button, connected to the RESET_N pin
1	PA00		JTAG.TCK
2	PA01		JTAG.TDI
3	PA02		JTAG.TDO
4	PA03		JTAG.TMS

Table 3-29 UC3C Pinout Port A

QFP144 pin	GPIO	GPIO Alternate functions	Feature
21	PA4	ADCIFA-ADCIN0	TFT XL Line Measurement
22	PA5	ADCIFA-ADCIN1	TFT YU Line Measurement
23	PA6	ADCIFA-ADCIN2 or ACIFA-AC1AP1	ADC Input 0 positive channel or Analog Comparator 0 Input positive.
23	PA7	ADCIFA-ADCIN3 or ACIFA-AC1AN1	ADC Input 1 positive channel or Analog Comparator 0 Input negative
25	PA8	GPIO[8]	LED0
26	PA9	ADCIFA-ADCIN5	Potentiometer
27	PA10		EVTI_N
28	PA11	ADCREFO	Analog Reference 0
29	PA12	DACIFB-DAC1A	DAC Output.
30	PA13	ADCIFA-ADCIN15	TFT YD Line Measurement
31	PA14	GPIO[14]	PB0 push-button
32	PA15	DACIFB-DAC1B	Jack Audio.

QFP144 pin	GPIO	GPIO Alternate functions	Feature
33	PA16	ADCREF1	Analog Reference1
36	PA19		MDO[0]
39	PA20	ADCIFA-ADCIN9 or ACIFA-AC0AP0	ADC Input 0 negative channel or Analog Comparator 1 Input positive.
40	PA21	ADCIFA-ADCIN10 or ACIFA-AC0BN0	ADC Input 1 negative channel or Analog Comparator 2 Input negative.
41	PA22	ACIFA-AC0AN0	Analog Comparator 1 Input negative.
42	PA23	ACIFA-AC0BP0	Analog Comparator 2 Input positive.
43	PA24	ADCIFA-ADCIN13	TFT XR Line Measurement
44	PA25	ADCIFA-ADCIN14	Microphone Input
45	PA26		MDO[1]
46	PA27		MDO[2]
47	PA28	GPIO[126]	SD Card Protect
48	PA29	GPIO[29] or EXTINT[0]	PB1 push-button

Table 3-30 UC3C Pinout Port A

QFP144 pin	GPIO	GPIO Alternate functions	Feature
140	PB00	Xin0	
141	PB01	Xout0	
142	PB02	Xin1	
143	PB03	Xout1	
36	PB04	RX	CAN0 RX CAN
37	PB05	TX	CAN0 TX CAN
9	PB06		MDO[5]
10	PB07	GPIO[39]	USB Over Current
11	PB8	PWM-PWML[0]	Provides access to the PWM UL signal available on J33.2.
12	PB9	PWM-PWMH[0]	Provides access to the PWM UH signal available on J33.1.
13	PB10	PWM-PWML[1]	Provides access to the PWM VL signal available on J33.4.
14	PB11	PWM-PWMH[1]	Provides access to the PWM VH signal available on J33.3.
15	PB12	PWM-PWML[2]	Provides access to the PWM WL signal available on J33.6.

QFP144 pin	GPIO	GPIO Alternate functions	Feature
16	PB13	PWM-PWMH[2]	Provides access to the PWM WH signal available on J33.5.
17	PB14	PWM-PWML[3]	Provides access to the PWM XL signal available on J33.6. See configuration section to activate this feature.
18	PB15		/ USART1.CTS / PWM-PWMH[3] MDO[4]
19	PB16	Rx LIN0 / USART1.RX	RX LIN / WLESS Rx Line
20	PB17	Tx LIN0 / USART1.TX	TX LIN / WLESS Tx Line
57	PB18		MSEO[0]
58	PB19	SPI1.MISO	Dataflash SO / SD SO / WLESS.MOSI / TFT Interface through the SPI
59	PB20	SPI1.MOSI	Dataflash SI / SD SI / WLESS.MISO / TFT Interface through the SPI
60	PB21	SPI1.SCK	Dataflash SCK / SD SCK / WLESS SPI clock / TFT Interface through the SPI
61	PB22	SPI1.NPCS3	SD #CS
62	PB23	SPI1.NPCS2	TFT SPI #CS
63	PB24	SPI1.NPCS1	Dataflash #CS
64	PB25	N.A/ SPI1.NPCS[]	MSEO[1]
65	PB26		MCKO
66	PB27	GPIO[59]/ QDEC - QEPA	
67	PB28	GPIO[60]/ QDEC - QEPB	

Table 3-31 UC3C Pinout Port C

QFP144 pin	GPIO	GPIO Alternate functions	Feature
71	PC00	GPIO[64]	USB ID
72	PC01	GPIO[65]	USB VBOF
73	PC02	TWIMS0_TWD	Touch TWI Data / EEPROM TWI Data / WLESS Data
74	PC03	TWIMS0_TWCK	Touch TWI Clock / EEPROM TWI Clock / WLESS Clock
77	PC04	USART2.TXD	USART3 TX line
78	PC05	USART2.RXD	USART3 RX line
79	PC06	GPIO[70]	UC3B_INT
80	PC07	GPIO[71]	Detect Interrupt of QTouch
81	PC08	Software-dependant	J19.3

QFP144 pin	GPIO	GPIO Alternate functions	Feature
82	PC09	Software-dependant	J19.4
84	PC10	Software-dependant	J19.5
84	PC11	RX	CAN1 RX CAN
85	PC12	TX	CAN1 TX CAN
86	PC13	GPIO[77]	or PWMH[2] LED2
87	PC14	EBI SDCKE	SDRAM SDCKE
88	PC15	RX LIN1 / EBI SDWEN	RX LIN / SDRAM SDWEN
89	PC16	TX LIN1 / EBI CASn	TX LIN / SDRAM CASn
90	PC17	EBI	RASn SDRAM RASn
91	PC18	EBI	SDA10 SDRAM SDA10
92	PC19	EBI-D0	TFT Data Bus
93	PC20	EBI-D1	TFT Data Bus
94	PC21	EBI-D2	TFT Data Bus
95	PC22	EBI-D3	TFT Data Bus
96	PC23	EBI-D4	TFT Data Bus
97	PC24	EBI-D5	TFT Data Bus
98	PC25	EBI-D6	TFT Data Bus
99	PC26	EBI-D7	TFT Data Bus
100	PC27	EBI-D8/Software-dependant	TFT Data Bus / J19.9
101	PC28	EBI-D9/Software-dependant	TFT Data Bus / J19.6
102	PC29	EBI-D10/Softwar-edependant	TFT Data Bus / J19.7
103	PC30	EBI-D11	TFT Data Bus
104	PC31	EBI-D12	TFT Data Bus

Table 3-32 UC3C Pinout Port C

QFP144 pin	GPIO	GPIO Alternate functions	Feature
107-109	PD0-2	EBI D13	SDRAM Data Bus.
108	PD1	EBI D14	SDRAM Data Bus.
109	PD2	EBI D15	SDRAM Data Bus.
110	PD3	EBI DQM0	SDRAM DQM0
111	PD4	Software-dependant	J20.3
112	PD5	EBI A2/	Software-dependant SDRAM Address Bus / J20.4
113	PD6	EBI A3/	Software-dependant SDRAM Address Bus / J20.5

QFP144 pin	GPIO	GPIO Alternate functions	Feature
114	PD7	EBI A3/	Software-dependant SDRAM Address Bus / J20.9
115	PD8	EBI A4	SDRAM Address Bus
116	PD9	EBI A5	SDRAM Address Bus
117	PD10	EBI A6	SDRAM Address Bus
120	PD11	EBI A7	SDRAM Address Bus
121	PD12	EBI A8	SDRAM Address Bus
122	PD13	EBI SDCK	SDRAM Clock
123	PD14	EBI A10	SDRAM Address Bus
124	PD15	EBI A11/Software-dependant	SDRAM Address Bus / J20.6
125	PD16	EBI A12/Software-dependant	TFT Reset Signal / J20.7
126	PD17	EBI A13	SDRAM Address Bus
127	PD18	EBI A14	SDRAM Address Bus
128	PD19	EBI A15	TFT TE Signal
129	PD20	EBI A16	SDRAM Address Bus
130	PD21	EBI A17	SDRAM Address Bus
131	PD22	GPIO[118] or TC0-A2	LED3
132	PD23	GPIO[119]	LED1
97	PD24	EBI DQM1	SDRAM DQM1
134	PD25	EBI NWE0	TFT Write Signal
135	PD26	EBI NRD	TFT Read Signal
136	PD27	EBI CS	SDRAM CS
137	PD28	GPIO[124] or TC0-B0	TFT Backlight Signal.
138	PD29		EVTO_N
139	PD30	GPIO[28]	SD Write Protect

3.9.3. Configuration

A USB DFU Bootloader is pre-loaded on the Atmel AT32UC3C0512C. To enter this bootloader mode, the PB0 push-button must be pressed upon reset then released. It is then possible to program the AT32UC3C0512C through the USB DFU Bootloader.

4. Evaluation Board/kit Important Notice

This evaluation board/kit is intended for use for **FURTHER ENGINEERING, DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY**. It is not a finished product and may not (yet) comply with some or any technical or legal requirements that are applicable to finished products, including, without limitation, directives regarding electromagnetic compatibility, recycling (WEEE), FCC, CE or UL (except as may be otherwise noted on the board/kit). Atmel supplied this board/kit "AS IS," without any warranties, with all faults, at the buyer's and further users' sole risk. The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies Atmel from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge and any other technical or legal concerns.

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