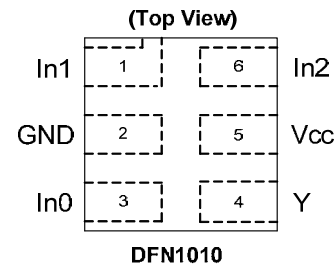
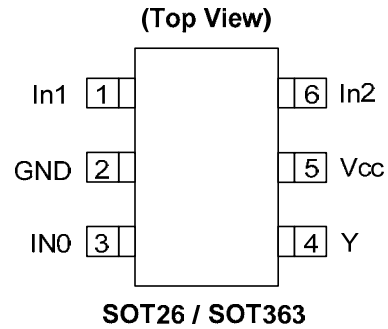


Description

The 74LVC1G58 is a single 3-input positive configurable multiple function gate with a standard totem pole output. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, OR, NAND, NOR, XOR, inverter or non-inverting buffer. All inputs can be connected to ground or Vcc as required. The device is designed for operation with a power supply range of 1.65V to 5.5V. The inputs are tolerant to 5.5V allowing this device to be used in a mixed voltage environment. The device is fully specified for partial power down applications using IOFF. The IOFF circuitry disables the output preventing damaging current backflow when the device is powered down. The user is reminded that the device can simulate several types of logic gates, but may respond differently due to the Schmitt action at the inputs.

Pin Assignments



Features

- Wide Supply Voltage Range from 1.65V to 5.5V
- ± 24mA Output Drive at 3.3V
- CMOS low power consumption
- IOFF Supports Partial-Power-Down Mode Operation
- Inputs accept up to 5.5V
- ESD Protection Exceeds JESD 22
 - 200-V Machine Model (A115-A)
 - 2000-V Human Body Model (A114-A)
- Latch-Up Exceeds 100mA per JESD 78, Class II
- Range of Package Options
- SOT26, SOT363, and DFN1010: Available in “Green” Molding Compound (no Br, Sb)
- Lead Free Finish/ RoHS Compliant (Note 1)

Applications

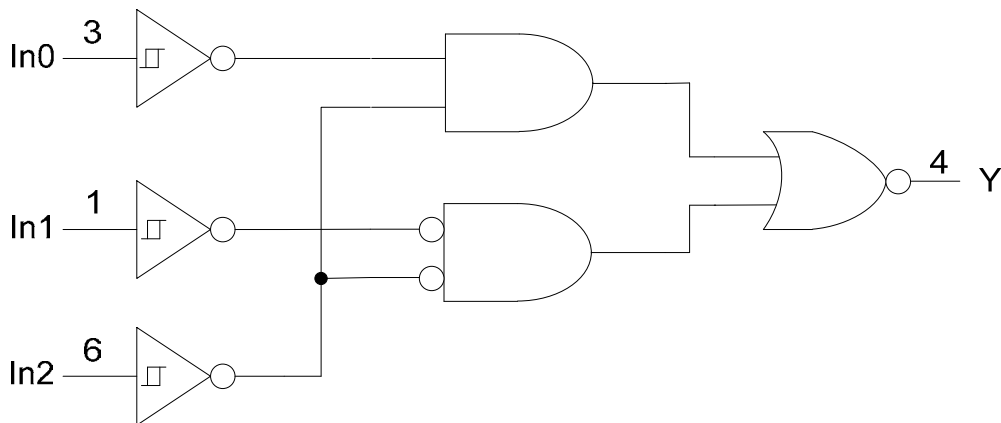
- Voltage Level Shifting
- General Purpose Logic
- Power Down Signal Isolation
- Wide array of products such as:
 - PCs, networking, notebooks, netbooks, PDAs
 - Computer peripherals, hard drives, CD/DVD ROM
 - TV, DVD, DVR, set top box
 - Cell Phones, Personal Navigation / GPS
 - MP3 players, Cameras, Video Recorders

Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead_free.html.

Pin Descriptions

Pin Name	Description
In1	Data Input
GND	Ground
In0	Data Input
Y	Data Output
Vcc	Supply Voltage
In2	Data Input

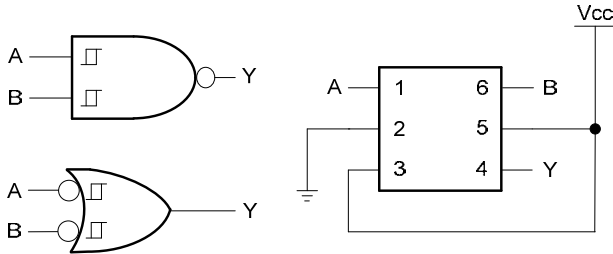
Logic Diagram



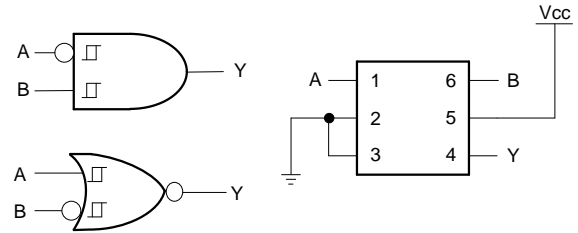
Function Table

Inputs			Output
In2	In1	In0	Y
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	L
H	H	H	L

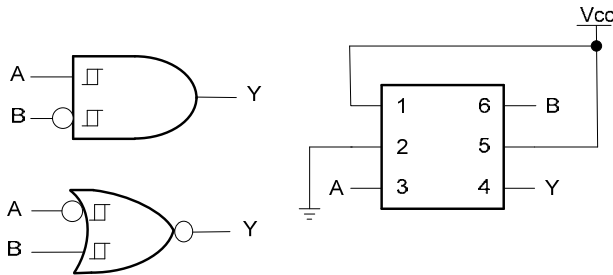
Logic Configurations



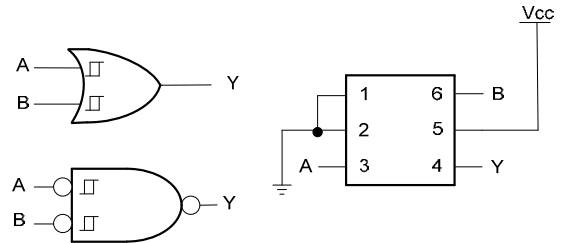
Configuration 1
2-Input NAND Gate
2-Input OR Gate with Both Inputs Inverted



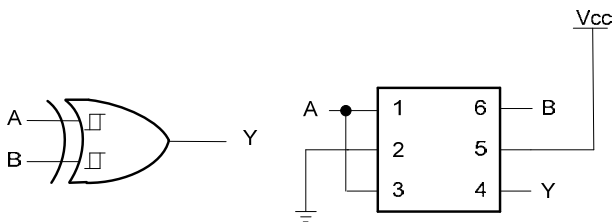
Configuration 2
2-Input AND Gate with A Input Inverted
2-Input NOR Gate with B Input Inverted



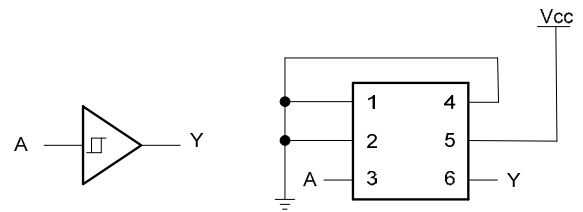
Configuration 3
2-Input AND Gate with B Input Inverted
2-Input NOR Gate with A Input Inverted



Configuration 4
2-Input OR Gate
2-Input NAND Gate with Both Inputs Inverted



Configuration 5
2-Input XOR Gate



Configuration 6
Buffer

Function Selection Table	
Logic Function	Configuration
2-input NAND	1
2-input NAND with both inputs inverted	4
2-input AND with inverted input	2,3
2-input NOR with inverted input	2,3
2-input OR	4
2-input OR with both inputs inverted	1
2-input XOR	5
1-input Buffer	6

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Absolute Maximum Ratings (Note 2)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	KV
ESD MM	Machine Model ESD Protection	200	V
V _{CC}	Supply Voltage Range	-0.5 to 6.5	V
V _I	Input Voltage Range	-0.5 to 6.5	V
V _o	Voltage applied to output in high impedance or I _{OFF} state	-0.5 to 6.5	V
V _o	Voltage applied to output in high or low state	-0.3 to V _{CC} +0.5	V
I _{IK}	Input Clamp Current V _I <0	-50	mA
I _{OK}	Output Clamp Current	-50	mA
I _o	Continuous output current	±50	mA
	Continuous current through V _{DD} or GND	±100	mA
T _J	Operating Junction Temperature	-40 to 150	°C
T _{STG}	Storage Temperature	-65 to 150	°C

Notes: 2. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Min	Max	Unit	
V _{CC}	Operating Voltage	Operating	1.65	5.5	V
		Data retention only	1.5		V
V _I	Input Voltage	0	5.5	V	
V _O	Output Voltage	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 1.65 V		-4	mA
		V _{CC} = 2.3 V		-8	
		V _{CC} = 3 V		-16	
		V _{CC} = 4.5 V		-32	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		8	
		V _{CC} = 3 V		16	
		V _{CC} = 4.5 V		32	
Δt/ΔV	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15V, 2.5 V ± 0.2 V		20	ns/V
		V _{CC} = 3.3 V ± 0.3 V		10	
		V _{CC} = 5 V ± 0.5 V		5	
T _A	Operating free-air temperature	-40	125	°C	

Notes: 3. Unused inputs should be held at V_{CC} or Ground.

Electrical Characteristics $T_A = -40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$ (All typical values are at $V_{CC} = 3.3\text{V}$, $T_A = 25\text{ }^\circ\text{C}$)

Symbol	Parameter	Test Conditions	Vcc	Min	Typ.	Max	Unit
V_{T+}	Positive-going input threshold voltage		1.65 V	0.70		1.20	
			2.3V	1.11		1.60	
			3 V	1.50		2.00	
			4.5 V	2.16		2.74	
			5.5 V	2.61		3.33	
V_{T-}	Negative-going input threshold voltage		1.65 V	0.30		0.72	
			2.3V	0.58		1.00	
			3 V	0.80		1.30	
			4.5 V	1.21		1.95	
			5.5 V	1.45		2.35	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)		1.65 V	0.30		0.62	
			2.3V	0.40		0.80	
			3 V	0.35		1.00	
			4.5 V	0.55		1.10	
			5.5 V	0.60		1.20	
V_{OH}	High Level Output Voltage	$I_{OH} = -100\mu\text{A}$	1.65 V to 5.5V	$V_{CC} - 0.1$			V
		$I_{OH} = -4\text{mA}$	1.65 V	1.2			
		$I_{OH} = -8\text{mA}$	2.3V	1.9			
		$I_{OH} = -16\text{mA}$	3 V	2.4			
		$I_{OH} = -24\text{mA}$		2.3			
		$I_{OH} = -32\text{mA}$	4.5 V	3.8			
V_{OL}	High-level Input Voltage	$I_{OL} = 100\mu\text{A}$	1.65 V to 5.5V			0.1	V
		$I_{OL} = 4\text{mA}$	1.65 V			0.45	
		$I_{OL} = 8\text{mA}$	2.3V			0.3	
		$I_{OL} = 16\text{mA}$	3 V			0.4	
		$I_{OL} = 24\text{mA}$				0.55	
		$I_{OL} = 32\text{mA}$	4.5			0.55	
I_I	Input Current	$V_I = 5.5\text{ V}$ or GND	0 to 5.5 V			± 5	μA
I_{OFF}	Power Down Leakage Current	V_I or $V_O = 5.5\text{V}$	0			± 10	μA
I_{CC}	Supply Current	$V_I = 5.5\text{V}$ of GND $I_O = 0$	1.65 V to 5.5V			10	μA
ΔI_{CC}	Additional Supply Current	One input at $V_{CC} - 0.6\text{ V}$ Other inputs at V_{CC} or GND	3 V to 5.5V			500	μA

Electrical Characteristics $T_A = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$ (All typical values are at $V_{CC} = 3.3\text{V}$, $T_A = 25\text{ }^\circ\text{C}$)

Symbol	Parameter	Test Conditions	Vcc	Min	Typ.	Max	Unit
V_{T+}	Positive-going input threshold voltage		1.65 V	0.70		1.20	
			2.3V	1.11		1.60	
			3 V	1.50		2.00	
			4.5 V	2.16		2.74	
			5.5 V	2.61		3.33	
V_{T-}	Negative-going input threshold voltage		1.65 V	0.30		0.75	
			2.3V	0.58		1.03	
			3 V	0.80		1.33	
			4.5 V	1.21		1.95	
			5.5 V	1.45		2.35	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)		1.65 V	0.30		0.62	
			2.3V	0.37		0.80	
			3 V	0.32		1.00	
			4.5 V	0.50		1.20	
			5.5 V	0.55		1.40	
V_{OH}	High Level Output Voltage	$I_{OH} = -100\mu\text{A}$	1.65 V to 5.5V	$V_{CC} - 0.1$			V
		$I_{OH} = -4\text{mA}$	1.65 V	0.95			
		$I_{OH} = -8\text{mA}$	2.3V	1.7			
		$I_{OH} = -16\text{mA}$	3 V	1.9			
		$I_{OH} = -24\text{mA}$		2.0			
		$I_{OH} = -32\text{mA}$	4.5 V	3.4			
V_{OL}	High-level Input Voltage	$I_{OL} = 100\mu\text{A}$	1.65 V to 5.5V			0.1	V
		$I_{OL} = 4\text{mA}$	1.65 V			0.7	
		$I_{OL} = 8\text{mA}$	2.3V			0.45	
		$I_{OL} = 16\text{mA}$	3 V			0.6	
		$I_{OL} = 24\text{mA}$				0.8	
		$I_{OL} = 32\text{mA}$	4.5			0.8	
I_I	Input Current	$V_I = 5.5\text{ V}$ or GND	0 to 5.5 V			± 100	μA
I_{OFF}	Power Down Leakage Current	V_I or $V_O = 5.5\text{V}$	0			± 200	μA
I_{CC}	Supply Current	$V_I = 5.5\text{V}$ of GND $I_O = 0$	1.65 V to 5.5V			200	μA
ΔI_{CC}	Additional Supply Current	One input at $V_{CC} - 0.6\text{V}$ Other inputs at V_{CC} or GND	3 V to 5.5V			5000	μA

Electrical Characteristics (All typical values are at $V_{CC} = 3.3V$, $T_A = 25^\circ C$)

Symbol	Parameter	Test Conditions	Vcc	Min	Typ.	Max	Unit
C_i	Input Capacitance	$V_i = V_{CC} - \text{or GND}$	3.3		3.5		pF
θ_{JA}	Thermal Resistance Junction-to-Ambient	SOT26	(Note 4)		166		$^\circ C/W$
		SOT363	(Note 4)		333		
		DFN1010	(Note 4)		231		
θ_{JC}	Thermal Resistance Junction-to-Case	SOT26	(Note 4)		46		$^\circ C/W$
		SOT363	(Note 4)		102		
		DFN1010	(Note 4)		TBD		

Notes: 4. Test condition for SOT26, SOT363 and DFN1010: Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

Switching Characteristics

$T_A = -40^\circ C$ to $85^\circ C$, $C_L = 30$ or $50pF$ as noted (see Figure 1)

Parameter	From (Input)	TO (OUTPUT)	$V_{CC} = 1.8 V \pm 0.15V$		$V_{CC} = 2.5 V \pm 0.2V$		$V_{CC} = 3.3 V \pm 0.3V$		$V_{CC} = 5 V \pm 0.5V$		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{pd}	Any	Y	1.0	14.4	0.7	8.3	0.7	6.3	0.7	5.1	ns

$T_A = -40^\circ C$ to $125^\circ C$, $C_L = 30$ or $50pF$ as noted (see Figure 1)

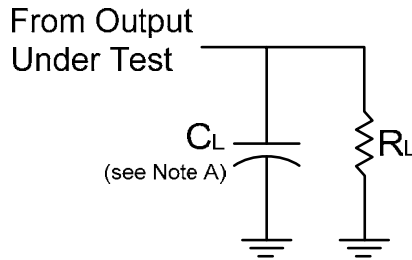
Parameter	From (Input)	TO (OUTPUT)	$V_{CC} = 1.8 V \pm 0.15V$		$V_{CC} = 2.5 V \pm 0.2V$		$V_{CC} = 3.3 V \pm 0.3V$		$V_{CC} = 5 V \pm 0.5V$		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{pd}	Any	Y	1.0	18.0	0.7	10.4	0.7	7.9	0.7	6.4	ns

Operating Characteristics

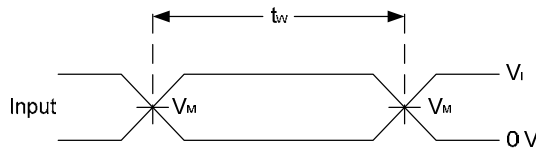
$T_A = 25^\circ C$

Parameter	Test Conditions	$V_{CC} = 1.8 V$	$V_{CC} = 2.5 V$	$V_{CC} = 3.3 V$	$V_{CC} = 5 V$	Unit	
		TYP	TYP	TYP	TYP		
C_{pd}	Power dissipation capacitance	$f = 10 \text{ MHz}$	22	22	23	24	pF

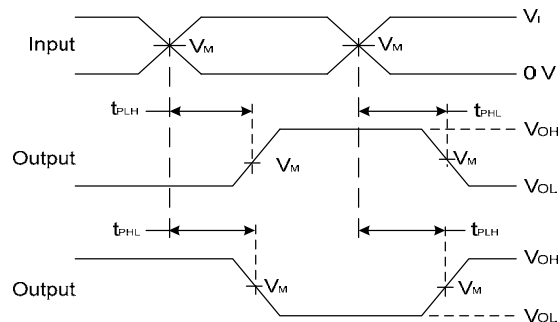
Parameter Measurement Information



V _{CC}	Inputs		V _M	C _L	R _L
	V _I	t _r /t _f			
1.8V±0.15V	V _{CC}	≤2ns	V _{CC} /2	30pF	1KΩ
2.5V±0.2V	V _{CC}	≤2ns	V _{CC} /2	30pF	500Ω
3.3V±0.3V	3V	≤2.5ns	1.5V	50pF	500Ω
5V±0.5V	V _{CC}	≤2.5ns	V _{CC} /2	50pF	500Ω



**Voltage Waveform
Pulse Duration**

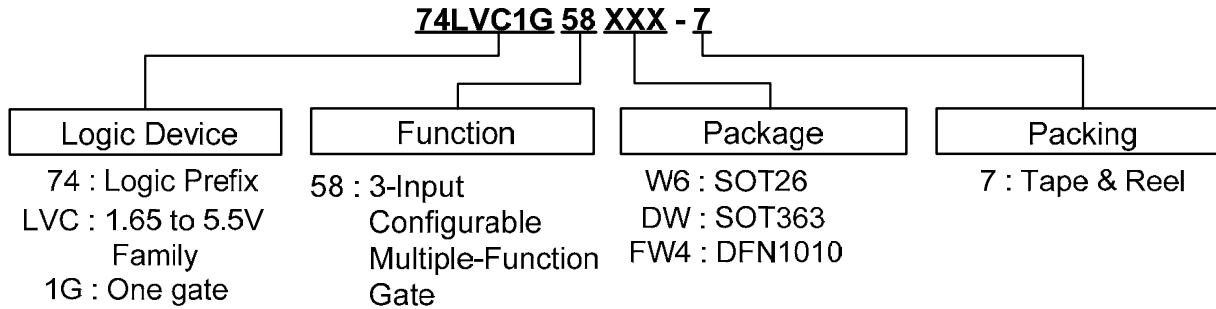


**Voltage Waveform
Propagation Delay Times
Inverting and Non Inverting Outputs**

- Notes:
- A. Includes test lead and test apparatus capacitance.
 - B. All pulses are supplied at pulse repetition rate ≤ 10 MHz
 - C. Inputs are measured separately one transition per measurement
 - D. t_{PLH} and t_{PHL} are the same as t_{PD}

Figure 1. Load Circuit and Voltage Waveforms

Ordering Information

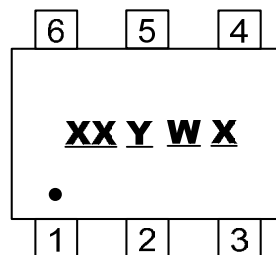


Device	Package Code	Packaging (Note 7)	7" Tape and Reel	
			Quantity	Part Number Suffix
74LVC1G58W6-7	W6	SOT26	3000/Tape & Reel	-7
74LVC1G58DW-7	DW	SOT363	3000/Tape & Reel	-7
74LVC1G58FW4-7	FW4	DFN1010	5000/Tape & Reel	-7

Notes: 7. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

Marking Information

(1) SOT26, SOT363



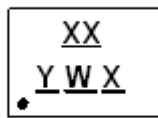
XX : Identification code
Y : Year 0~9
W : Week : A~Z : 1~26 week;
 a~z : 27~52 week; z represents
 52 and 53 week
X : A~Z : Internal Code

Part Number	Package	Identification Code
74LVC1G58W6	SOT26	TX
74LVC1G58DW	SOT363	TX

Marking Information (Continued)

(2) DFN1010

(Top View)

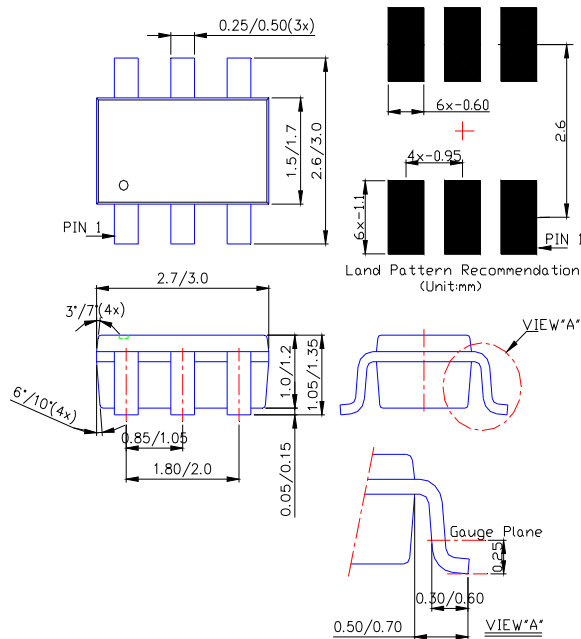


XX : Identification Code
Y : Year : 0~9
W : Week : A~Z : 1~26 week;
 a~z : 27~52 week; z represents
 52 and 53 week
X : A~Z : Internal code

Part Number	Package	Identification Code
74LVC1G58FW4	DFN1010	TX

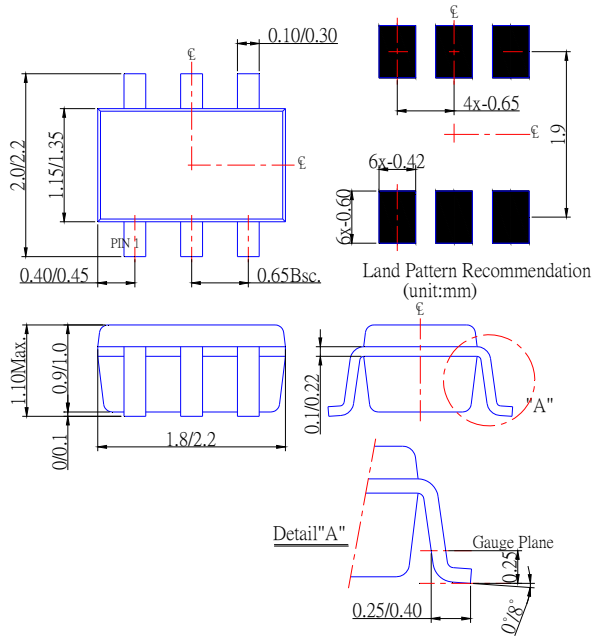
Package Outline Dimensions (All Dimensions in mm)

(1) Package Type: SOT26

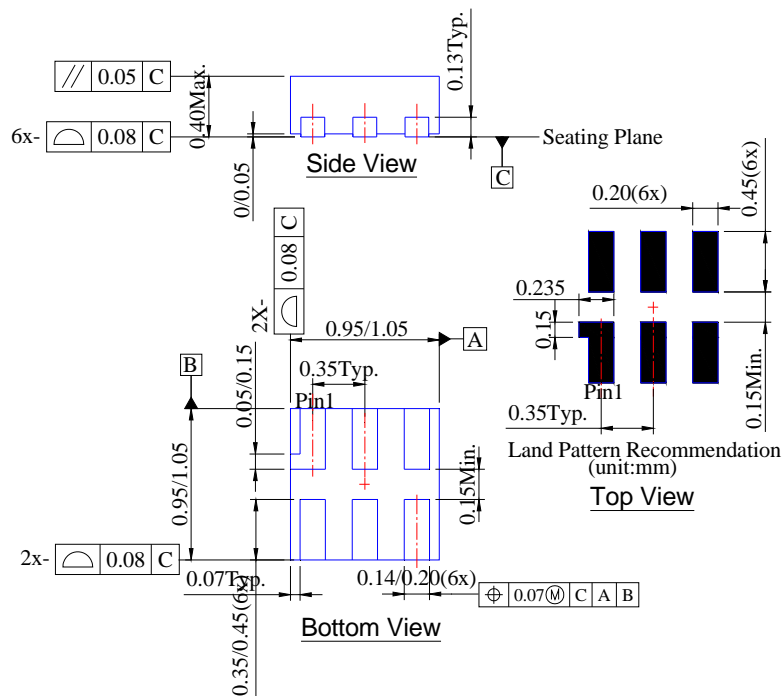


Package Outline Dimensions (All Dimensions in mm)

(2) Package Type: SOT363



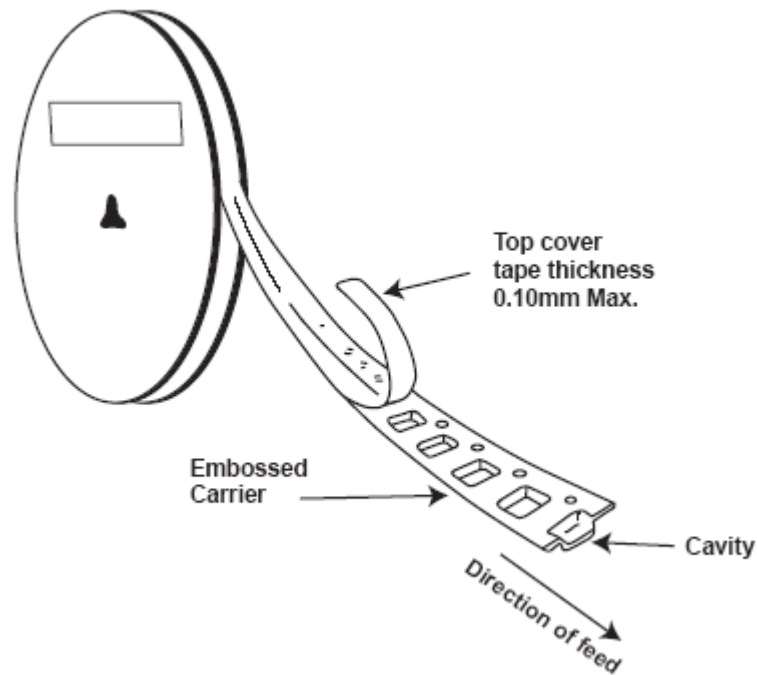
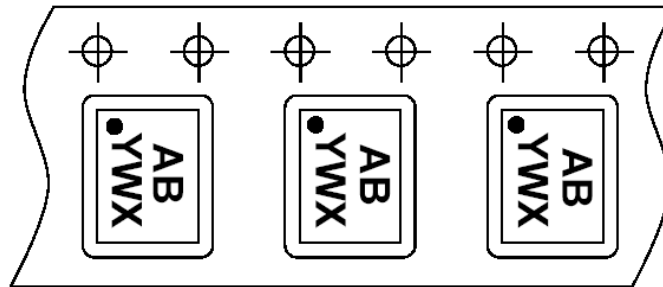
(3) Package Type: DFN1010



NEW PRODUCT

Taping Orientation (Note 8)

For DFN1010



Notes: 8. The taping orientation of the other package type can be found on our website at <http://www.diodes.com/datasheets/ap02007.pdf>

NEW PRODUCT

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