Si838x Data Sheet

Bipolar Digital Field Inputs for PLCs and Industrial I/O Modules

The Si838x provides eight channels for 24 V digital field interface to either sinking or sourcing inputs with integrated safety rated isolation. In combination with a few external components, this provides compliance to IEC 61131-2 switch types 1, 2, or 3. The input interface is based on Silicon Labs' ground-breaking CMOS based LED emulator technology which enables the bipolar capability (sinking or sourcing inputs) with no VDD required on the field side. The output interface to the controller allows for low power operation with 2.25 V operation capability. These products utilize Silicon Laboratories' proprietary silicon isolation technology, supporting up to 2.5 kV$_{RMS}$ withstand voltage. This technology enables high CMTI (50 kV/μs), lower prop delays and skew, reduced variation with temperature and age, and tighter part-to-part matching.

Product options include parallel or serialized outputs. Cascading capability for a total of 128 channels (16x Si838x) is possible with serial output option. The Si838x offers longer service life and dramatically higher reliability compared to opto-coupled input solutions.

Applications:

- Programmable logic controllers
- Industrial data acquisition
- Distributed control systems
- CNC machines
- I/O modules
- Motion control systems

Safety Regulatory Approvals:

- UL 1577 recognized
  - Up to 2500 V$_{RMS}$ for one minute
- CSA component notice 5A approval
  - IEC 60950-1
- VDE certification conformity
  - VDE 0884-10
- CQC certification approval
  - GB4943.1

KEY FEATURES

- Bipolar digital interface with 24 V sinking or sourcing inputs
- Eight total inputs in one package
- High data rates of up to 2 Mbps
- Safety rated integrated isolation of 2.5 kVrms
- Low input current of 1 mA typ
- No VDD required on field side
- Status LEDs on parallel outputs
- High electromagnetic immunity
- Programmable debounce times of up to 100 ms
- Transient immunity of 50 kV/μs
- Flow-through output configuration with eight outputs
- Option for SPI interface serialized outputs with daisy-chain capability
- Wide 2.25 to 5.5 V VDD operation
- Wide operating temperature range
  - –40 to +125 °C
- Compliant to IEC 61131-2
  - Type 1, 2, 3
- RoHS-compliant packages
  - QSOP-20

1. Ordering Guide

Table 1.1. Si838x Ordering Guide

Ordering Part Number	Serial or Parallel Output	Number of High-Speed Channels	Low Pass Filter Delay	Package Type	Isolation Rating
Si8380P-IU	P	0	0 ms	20-QSOP	2.5 kVrms
Si8382P-IU	P	2	0 ms	20-QSOP	2.5 kVrms
Si8384P-IU	P	4	0 ms	20-QSOP	2.5 kVrms
Si8388P-IU	P	8	0 ms	20-QSOP	2.5 kVrms
Si8380S-IU	S	0	0 ms	20-QSOP	2.5 kVrms
Si8380PF-IU	P	0	10 ms	20-QSOP	2.5 kVrms
Si8382PF-IU	P	2	10 ms	20-QSOP	2.5 kVrms
Si8384PF-IU	P	4	10 ms	20-QSOP	2.5 kVrms
Si8380PM-IU	P	0	30 ms	20-QSOP	2.5 kVrms
Si8382PM-IU	P	2	30 ms	20-QSOP	2.5 kVrms
Si8384PM-IU	P	4	30 ms	20-QSOP	2.5 kVrms
Si8380PS-IU	P	0	100 ms	20-QSOP	2.5 kVrms
Si8382PS-IU	P	2	100 ms	20-QSOP	2.5 kVrms
Si8384PS-IU	P	4	100 ms	20-QSOP	2.5 kVrms

2. Functional Description

2.1 Theory of Operation

The operation of a Si838x channel is analogous to that of a bipolar opto-coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si838x channel is shown in the figure below.

This product enables 24 V bipolar digital inputs to be connected to its input through a resistor network which acts as a voltage divider. The inputs can be sourcing or sinking type. To enable this functionality, there is a zero drop bridge and an LED emulator at the front end that drives an OOK (On-Off Key) modulator/demodulator across the capacitive isolation barrier.

On the output side, the debounce block controls the amount of debounce desired. There are four debounce delay time options available: no delay, or delays of 10, 30, or 100 ms. In addition, the user can use the SPI control to program user-specific debounce modes as explained in Section 2.3.2 Debounce Filtering Modes. The user-specific debounce programming is only available on the product option with SPI interface.
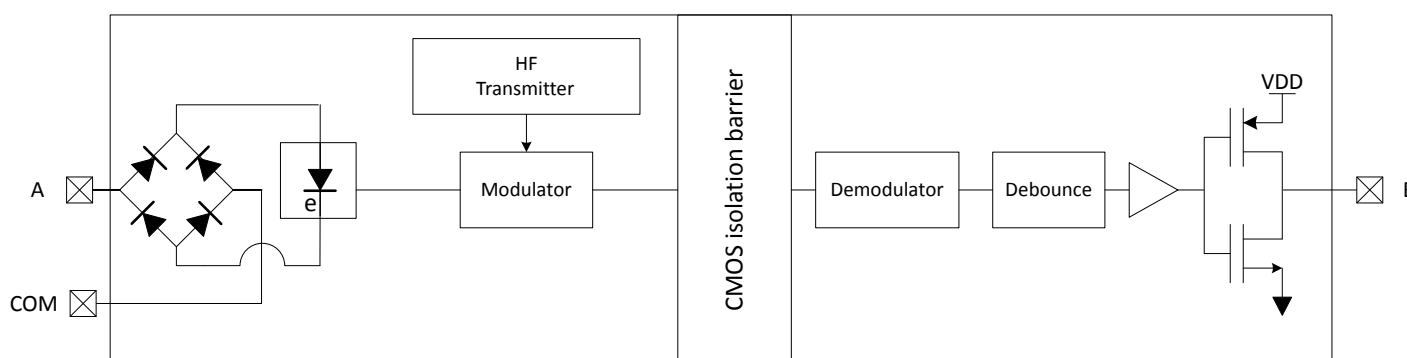

Figure 2.1. Simplified Channel Diagram

2.2 Serial Peripheral Interface

The Si8380S includes a Serial Peripheral Interface (SPI) that provides control and monitoring capability of the isolated channels using a commonly available microcontroller protocol. The direct-mapped registers allow an external master SPI controller to monitor the status of the eight PLC channels, as well as to control the delay and filtering modes for the debounce of each channel. Additionally, support is provided to easily daisy-chain up to sixteen PLC devices. Each of these daisy-chained devices may be uniquely addressed by one master SPI controller.

2.2.1 SPI Register Map

The addressable SPI registers include one eight-bit register to reflect the status of each of the eight channels, which is read-only. Also, four additional registers provide two bits to specify the debounce delay, and two bits to specify the debounce filtering mode for each of the eight channels. These user accessible SPI registers are illustrated in the following table.

Table 2.1. Si838x SPI Register Map

Name	Address	Access	Description
CHAN_STATUS	0x0	R	Current value of each of the eight PLC channels {PLC[7:0]}
DBNC_MODE0	0x1	R/W	Mode control bits for the first four channel debounce filters organized as: {md_ch3[1:0],md_ch2[1:0],md_ch1[1:0],md_ch0[1:0]}
DBNC_MODE1	0x2	R/W	Mode control bits for the second four channel debounce filters organized as: {md_ch7[1:0],md_ch6[1:0],md_ch5[1:0],md_ch4[1:0]}
DBNC_DLY0	0x3	R/W	Delay control bits for the first four channel debounce filters organized as: {dly_ch3[1:0],dly_ch2[1:0],dly_ch1[1:0],dly_ch0[1:0]}
DBNC_DLY1	0x4	R/W	Delay control bits for the second four channel debounce filters organized as: {dly_ch7[1:0],dly_ch6[1:0],dly_ch5[1:0],dly_ch4[1:0]}

2.2.2 SPI Communication Transactions

SPI communication is performed using a four wire control interface. The four Si838x device pins utilized for SPI include:
- SCLK (input) the SPI clock
- NSS (input) active low device select
- MOSI (input) master-out-slave-in
- MISO (output) master-in-slave-out

Additionally, a fifth wire SDI_THRU (output) is provided as an Si838x device pin to facilitate daisy chaining.

An Si838x SPI communication packet is composed of three serial bytes. In this sequence, byte0 is the control byte, and specifies the operation to be performed as well as the device to be selected in a daisy chain organization. The CID[3:0] field should be set to all zeros by the SPI master in non-daisy-chained operation. Next, byte1 specifies the address of the internal Si838x SPI register to be accessed. The final byte in the packet consists of either the data to be written to the addressed Si838x SPI register (using MOSI), or the data read from the addressed Si838x SPI register (using MISO). Details of the SPI communication packet are presented in the following figure for an Si838x SPI write transaction.
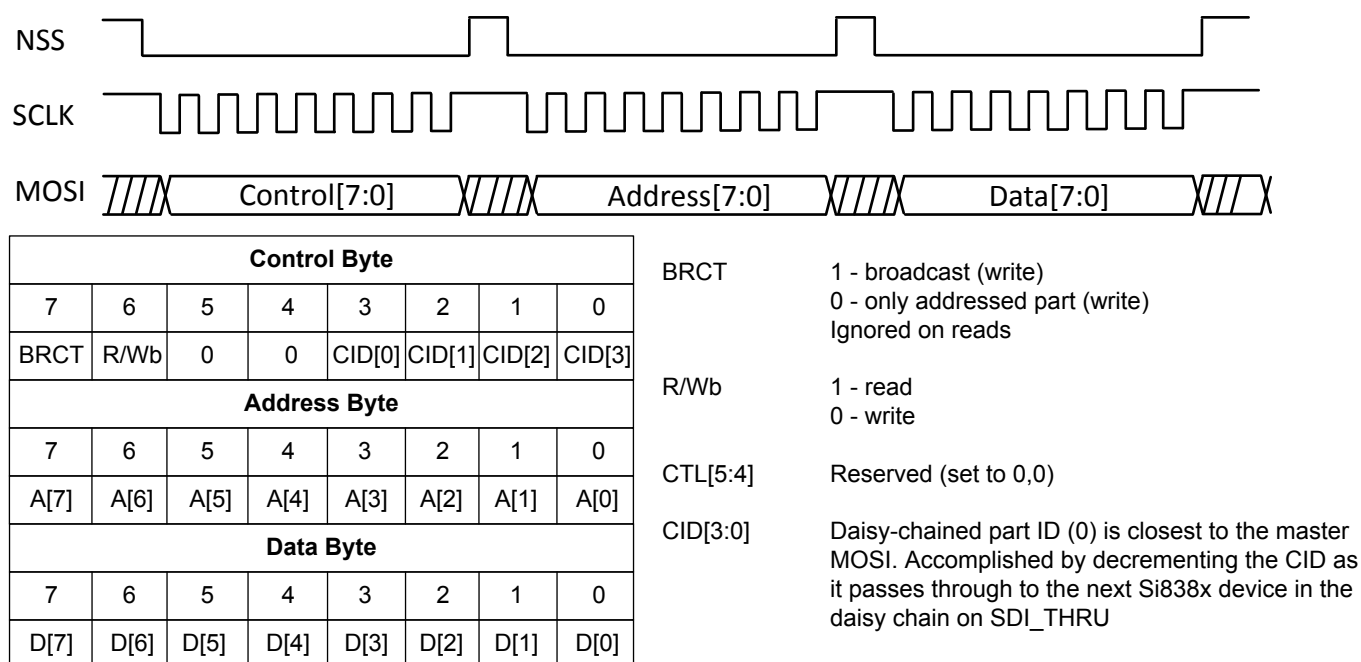

Control Byte							
7	6	5	4	3	2	1	0
BRCT	R/Wb	0	0	CID[0]	CID[1]	CID[2]	CID[3]

Address Byte							
7	6	5	4	3	2	1	0
A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]

Data Byte							
7	6	5	4	3	2	1	0
D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

BRCT — 1 - broadcast (write)
0 - only addressed part (write)
Ignored on reads

R/Wb — 1 - read
0 - write

CTL[5:4] — Reserved (set to 0,0)

CID[3:0] — Daisy-chained part ID (0) is closest to the master MOSI. Accomplished by decrementing the CID as it passes through to the next Si838x device in the daisy chain on SDI_THRU

Figure 2.2. SPI Communication Packet Structure, Write Operation and Control Byte Structure

The SPI master will provide the timing of the signals and framing of the communication packets for all Si838x SPI inputs: NSS, SCLK, and MOSI. Data is communicated from the SPI master to the Si838x using the MOSI signal. The NSS and SCLK signals provide the necessary control and timing reference allowing the Si838x to discern valid data on the MOSI signal. Data is returned to the SPI master by the Si838x utilizing the MISO signal only during the final byte of a three byte SPI read communication packet. At all other times, the MISO signal is tri-stated by the Si838x. Each of the eight bits for these three packets is captured by the Si838x on eight adjacent rising edges of SCLK. Each frame of eight bits is composed within bounding periods where the device select, NSS, is deasserted. Upon the reception of the eight bits within a byte transaction, the deassertion of NSS advances the byte counter within the internal Si838x SPI state machine. Should the transmission of an eight bit packet be corrupted, either with the deassertion of NSS before the eighth rising edge of SCLK, or with the absence of the deassertion of NSS after the eighth rising edge of SCLK, the internal SPI state machine may become unsynchronized with the master SPI controller.

To re-establish SPI synchronization with the Si838x, the SPI master may, at any time, deassert the SPI device select signal NSS, and force a clock cycle on SCLK. When unsynchronized, the rising edge of SCLK when NSS is deasserted (high) re-initializes the internal SPI state machine. The Si838x will then treat the immediately following eight bit SPI transaction after NSS is once again asserted as the first byte in a three byte SPI communication packet.

Any preceding communication packet will be abandoned by the Si838x at the point synchronization is lost, and the NSS signal is deasserted. This could occur at any point in the three byte sequence of a SPI communication packet. One should note that abandoning a SPI write operation early, even during the last byte of the three byte SPI communication packet, will leave the destination register unchanged. However, if the number of SCLK cycles exceeds eight during the last byte of the three byte SPI write packet, the destination Si838x register may be corrupted. To remedy both of these situations, it is recommended that such a corrupted write operation be repeated immediately following resynchronization of the SPI interface.

2.2.3 SPI Read Operation

Referring to Figure 2.2 SPI Communication Packet Structure, Write Operation and Control Byte Structure on page 3, in a SPI read operation the control byte will only have bit6 set to a 1 in a single Si838x device organization (no daisy-chaining). For the Si838x, bit7 (the broadcast bit) is ignored during a read operation since only one device may be read at a time in either a single or daisy chained organization.

The second byte in the three byte read packet is provided by the SPI master to designate the address of the Si838x internal register to be queried. If the read address provided does not correspond to a physically available Si838x internal register, all zeroes will be returned as the read value by the Si838x.

The read data is provided during the final byte of the three byte read communication packet to the querying master SPI device utilizing the Si838x's MISO output, which remains tristated at all other times.

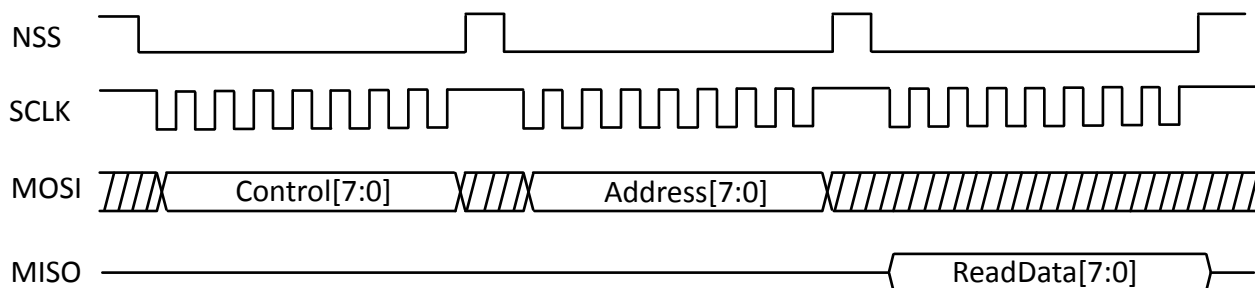The SPI read operation timing diagram is illustrated in the figure below.

Figure 2.3. SPI Read Operation

2.2.4 SPI Write Operation

Again referring to Figure 2.2 SPI Communication Packet Structure, Write Operation and Control Byte Structure on page 3, in a SPI write operation the control byte may optionally have bit7 (the broadcast bit) set to a 1. During a SPI write operation, the broadcast bit forces all daisy-chained Si838x devices to update the designated internal SPI register with the supplied write data, regardless of the Si838x device being addressed using the CID[3:0] field of the control word.

The second byte in the three byte write packet is provided by the SPI master to designate the address of the Si838x internal register to be updated. If the write address provided does not correspond to a physically available Si838x internal register, no internal Si838x SPI register update will occur.

The write data is provided by the SPI master during the final byte of the three byte write communication packet. The Si838x MISO output remains tri-stated during the entire SPI write operation.

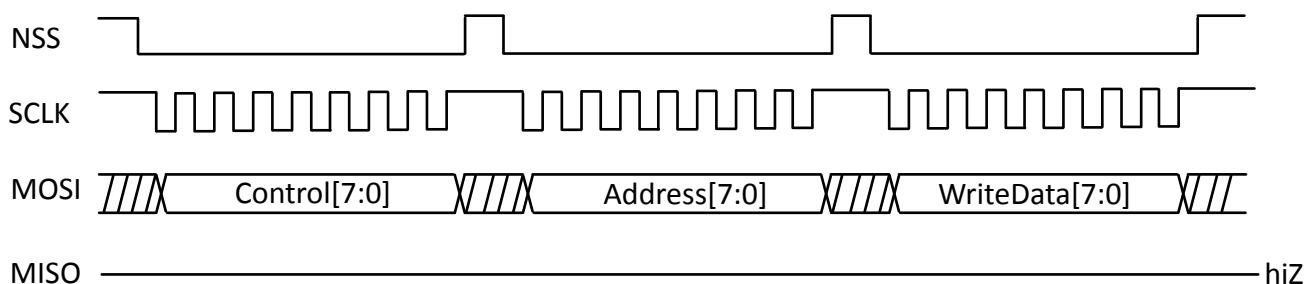The SPI write operation timing diagram is illustrated in the figure below.

Figure 2.4. SPI Write Operation

2.2.5 SPI Daisy Chain Organization

The Si838x provides the capability to easily interconnect multiple Si838x devices on a common SPI interface administered by a single SPI master requiring no additional control signals. To accomplish this, the Si838x includes the additional SPI device output pin SDI_THRU. Connecting together multiple Si838x devices in this manner utilizes the SDI_THRU pin of one Si838x device to feed the MOSI pin of the next Si838x device in the daisy-chain. All bits composing a SPI communication packet are passed directly through by the Si838x from the MOSI input to the SDI_THRU output unchanged, except for the CID[3:0] field of the control byte.

The least significant four bits of the control byte in a SPI communication packet, CID[3:0], are dedicated to addressing one of up to sixteen Si838x devices thus connected, with 0000 indicating the device whose MOSI pin is fed directly by the SPI master, 0001 the following Si838x device, etc. As this bit field is passed through the Si838x, it is decremented by one. This four bit field is placed in the control word by the SPI master in reverse order, allowing the carry of the decrement to ripple into the next bit in the CID field as the bits of the control word proceed: CID[0] is placed at bit 3 and CID[3] placed at bit 0 of the control word. When a given Si838x device in the daisy chain is presented with the CID[3:0] code of 0000, it is activated as the one to be addressed. All remaining operations between the SPI master and the Si838x activated in this manner proceed as previously discussed for the case of the single Si838x slave. The organization of an Si838x system daisy-chained in this manner is depicted in the figure below.
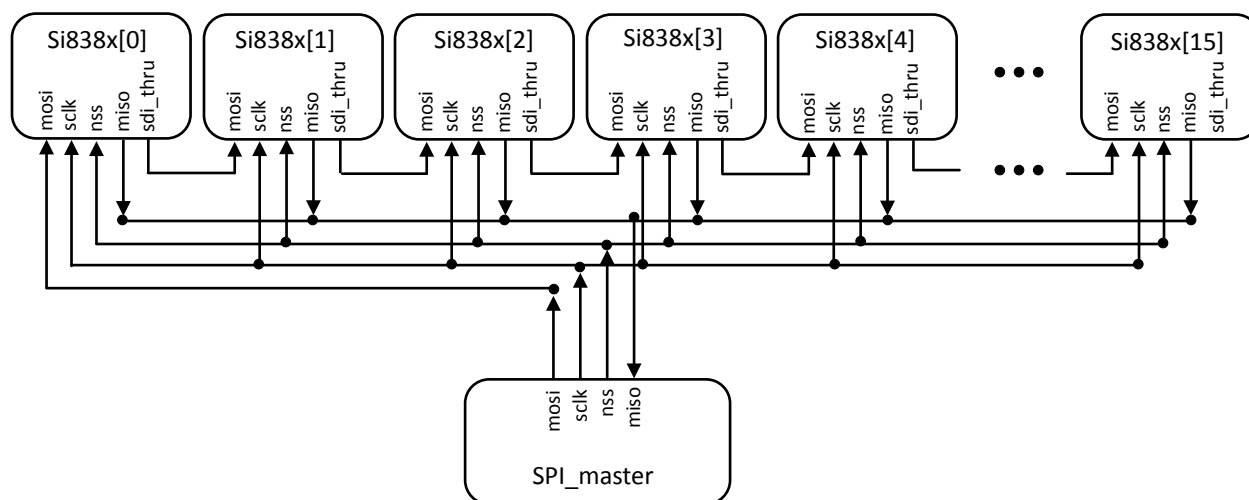

Figure 2.5. SPI Daisy Chain Organization

From the preceding figure, and referring to Figure 2.2 SPI Communication Packet Structure, Write Operation and Control Byte Structure on page 3, in order to read from Si838x[1], the control word would be:

Control[7:0] = 0100_1000.

Similarly, in order to write to Si838x[12], the control word would be:

Control[7:0] = 0000_0011.

Finally, if it were desired to update an internal SPI register of all daisy-chained Si838x devices, the control word would be:

Control[7:0] = 1000_0000.

If the broadcast bit is zero during a write operation, only the Si838x device being addressed using the CID[3:0] field of the control word in a daisy-chain organization will be updated. If the broadcast bit is one during a write operation, the CID[3:0] field is ignored, and all Si838x devices connected in a daisy-chain will be updated. For non-daisy-chain operation, the CID[3:0] field should always be all zeros.

Note that there is a finite combinational delay associated with passing the MOSI input pin of a given Si838x to the SDI_THRU output pin. As a result, the maximum possible SCLK frequency will be reduced based on the number of Si838x devices connected in a daisy-chain organization.

2.2.6 SPI Interface Timing Specification

The timing diagram for the Si838x SPI interface is presented in the figure below.
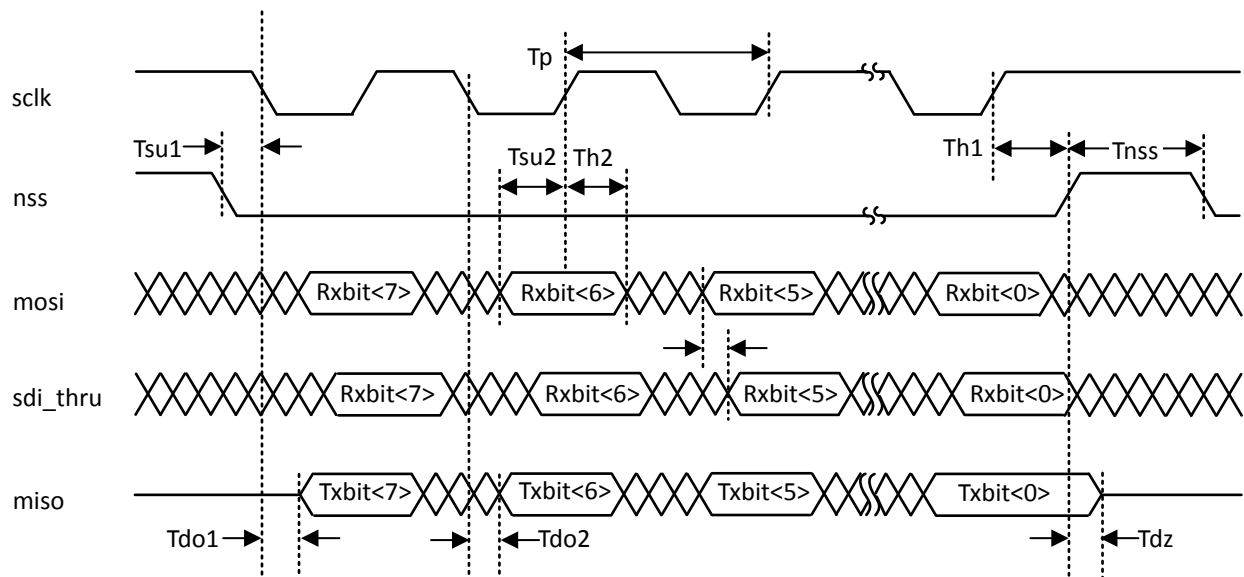

Figure 2.6. SPI Timing Diagram

The timing specifications depicted in this figure apply to each byte of the three byte Si838x SPI communications packet. Refer to the SPI timing specifications in Table 4.2 Electrical Characteristics on page 12.

Although this discussion of the Si838x SPI interface has focused on a preferred organization (separate `MISO`/`MOSI` wires), other options are available with regard to the Si838x control interface. Possible Si838x organizations include:

- MISO/MOSI wired operation
  - MISO/MOSI may be two separate wires, or may be connected together if the SPI master is capable of tri-stating its MOSI during the data byte packet transfer of a read operation.
- Multiple Si838x devices interfaced in a non-daisy-chain format
  - The SPI master provides multiple NSS signals, one for each of a multiple of Si838x slaves.
  - Every Si838x shares a single trace from its MOSI input back to the SPI master (the Si838x SDI_THRU signal is not utilized).

2.3 Debounce Filter

The Si838x includes a user programmable debounce filter, providing the user a mechanism to individually control the debounce behavior for each of the eight Si838x isolation channels. User control of the debounce filter is accomplished via the included Si838x SPI interface. Consequently, user control of this feature is available only on the serial interface accessible Si838x device versions. The debounce filter is incorporated into the path of the input data stream allowing signal conditioning of the PLC inputs.

There are product options available with the parallel output interface with discrete debounce time constants of 0, 10, 30 or 100 ms—these are only available on the low speed channels. The high speed channels have no debounce filtering (See 1. Ordering Guide for more details on part numbers).

2.3.1 Debounce Control Registers

The operation of the Si838x debounce filters is controlled using r/w control registers mapped into the Si838x SPI address space. The details of these registers are covered in the Si838x SPI register map section of this document. The options available using these registers are outlined in the following tables. For each of the eight PLC channels, two data bits are allocated to control the debounce delay, and two bits are used to stipulate the debounce filtering mode. This consumes a total of 32 bits, which are allocated across four individual Si838x SPI control registers of one byte each.

Table 2.2. Debounce Filter Delay Control

dbnc_dly[1:0]	Delay (ms)	Comment
00	0	Bypass debounce
01	10	
10	30	
11	100	

Table 2.3. Debounce Filter Mode Control

dbnc_mode[1:0]	Filter Mode	Comment
00	no filter	Simple trailing edge delay
01	low pass	
1X	leading edge	

2.3.2 Debounce Filtering Modes

In addition to the user specifiable delays, three filtering modes are provided by the debounce function. Like the debounce delay setting, these filtering modes may be unique for each of the eight Si838x PLC channels.

The first of these three modes, corresponding to `dbnc_mode[1:0] == 00`, employs only a simple trailing edge delay. In this mode, once the debounce filter input has been stable for the amount of time specified in the corresponding channel's debounce delay setting, D, the output of the debounce filter assumes the value of the new debounce input. Consequently, any glitches on the debounce input having a duration less than the channel's debounce delay setting, D, will be suppressed.

The second mode, corresponding to `dbnc_mode[1:0] == 01`, performs a low pass filtering function on the input to the debounce filter. When the input to the debounce filter has assumed a new value, a counter begins counting toward the current delay setting, D. If before the count D is reached the debounce input returns to its previous state, this counter is decremented. Assuming that the debounce filter input again assumes the new value before the counter is decremented back to 0 (i.e. glitch width is less than time the input had previously assumed a new value), the counter incrementing resumes from a non-zero value. Once this count has reached the designated delay, D, the debounce filter output assumes the value of the new debounce input. Using this mechanism, any input glitches on the debounce input having a duration less than the channel's debounce delay setting, D, will be suppressed. However unlike mode 0, when the debounce input returns to the new value after this glitch, credit is given for the time this new value was active before the glitch.

The final mode, corresponding to `dbnc_mode[1:0] == 1X`, realizes a leading edge filtering function on the input to the debounce filter. Internally, a counter is initialized to zero. When the input to the debounce filter changes, the output of the debounce filter immediately assumes the new value, and the counter is reset to the current delay setting, D. Independent of what occurs on the input of the debounce filter, the counter begins decrementing after this change. When the counter again reaches zero, the current input of the debounce filter is compared to the current output of the filter. If they are they are different, again the debounce filter immediately assumes the new value. If they are the same, the output of the debounce filter will immediately change on the next new value of the debounce input. In either case, a change on the debounce output filter resets the counter to the current delay setting, D.

A graphical depiction of the operation and characteristics for each these debounce filter modes is provided in the following figure.
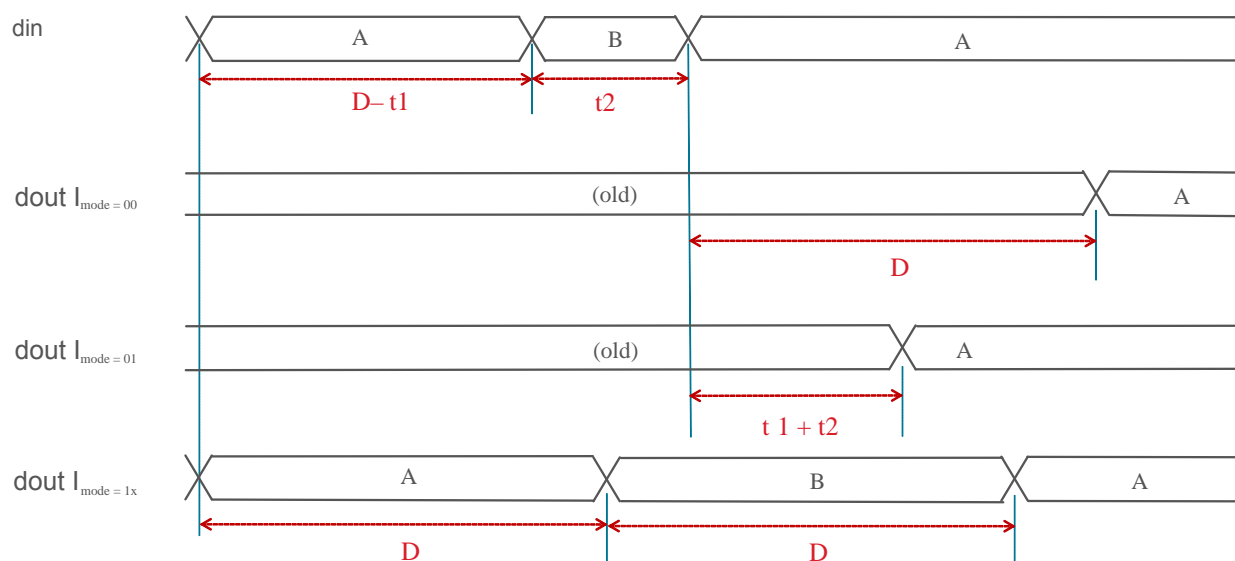

Figure 2.7. Debounce Filter Modes Timing Diagram
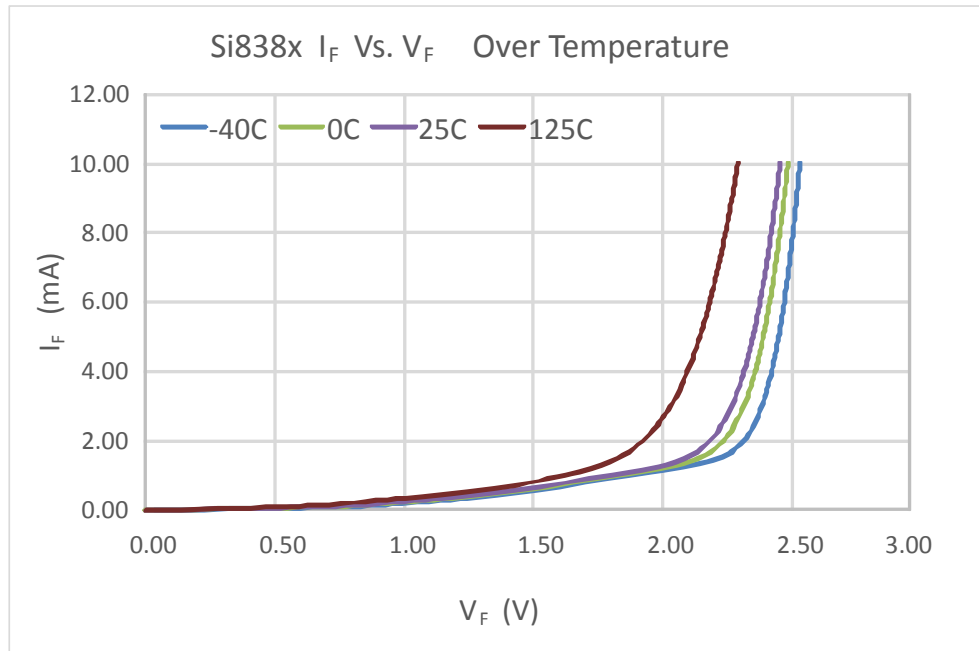
2.4 Typical Operating Characteristics

Figure 2.8. Input Current vs. Input Voltage Over Temperature

3. Device Operation

Table 3.1. Truth Table Summary

VDD	Input, Ax/AHx	Output, Bx/BHx
P[1]	ON	High
P	OFF	Low
UP[2]	X	Low
1. P = powered (> UVLO).		
2. UP = Unpowered (< UVLO).		

3.1 Device Start-up

During start-up, Output Bx/BHx are held low until the VDD is above the UVLO threshold for a time period of at least tSTART. Following this, the output is high when the current flowing from anode to cathode is > IF(ON). Device startup, normal operation, and shutdown behavior is shown in the figure below.
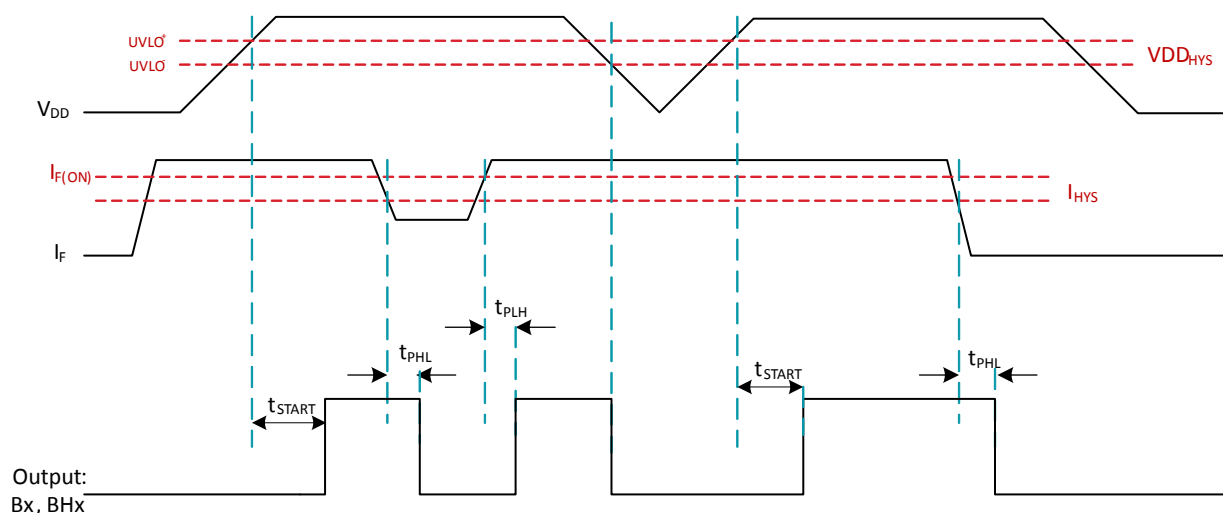

Figure 3.1. Device Start-up

3.2 Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. For example, the output side unconditionally enters UVLO when V_{DD} falls below V_{DDUV-} and exits UVLO when V_{DD} rises above V_{DDUV+}.

3.3 Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 VAC) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 VAC) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 4.4 Insulation and Safety-Related Specifications[1] on page 15 and Table 4.6 VDE 0884-10 Insulation Characteristics[1] on page 16 detail the creepage/clearance and working voltage capabilities of the Si838x. These tables also detail the component standards (UL1577, VDE 0884, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (60950-1, etc.) requirements before starting any design that uses a digital isolator.

3.3.1 Supply Bypass

The Si838x family requires a 0.1 µF bypass capacitor between VDD and GND. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, the user may also include resistors (50–300 Ω) in series with the outputs if the system is excessively noisy.

3.3.2 Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

4. Electrical Specifications

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
V_{DD} Supply Voltage	V_{DD}	2.25	—	5.5	V
Input data rate, low-speed channels (no debounce)	D	—	—	250	Kbps
Input data rate, (10 ms debounce)	D	—	—	0.1	Kbps
Input data rate, (30 ms debounce)	D	—	—	0.033	Kbps
Input data rate, (100 ms debounce)	D	—	—	0.01	Kbps
Input data rate, high-speed channels	DH	—	—	2000	Kbps
Input Current	$I_{F(ON)}$	1.0	—	20	mA
Operating Temperature (Ambient)	T_A	–40	—	+125	°C

Table 4.2. Electrical Characteristics

V_{DD} = 2.25 V –5.5 V; GND = 0 V; T_A = –40 to +125 °C; typical specs at 25 °C; V_{DD} = 5 V

DC Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Current Threshold	$I_{F(TH)}$		460	606	950	µA
Input Current Hysteresis[1]	I_{HYS}		30	76	200	µA
Input Voltage Threshold	$V_{F(TH)}$		1.21	1.38	1.5	V
Input Voltage Hysteresis[2]	V_{HYS}		30	73	130	mV
Input Capacitance	C_I	f = 100 kHz	—	105	—	pF
VDD Undervoltage Threshold	V_{DDUV+}	VDD rising	1.93	2.06	2.19	V
VDD Undervoltage Threshold	V_{DDUV-}	VDD falling	1.79	1.91	2.01	V
VDD Undervoltage Hysterisis	VDD_{HYS}		—	60	—	mV
Low level output voltage	V_{OL}	IOL = 4 mA	—	—	0.4	V
High level output voltage	V_{OH}	IOH = –4 mA	VDD – 0.4	—	—	V
Output Impedance	Z_O		—	50	—	Ω
Output Current	I_{SINK}	Vout = 0.1 V, 50 Ω load	—	2.0	—	mA
	I_{SOURCE}	Vout = VDD–0.1 V, 50 Ω load	—	2.0	—	mA
DC Supply Current (All Inputs 0 or 1)						
IDD		All inputs 0	2.8	4.8	6.7	mA
		All inputs 1	3.6	5.4	7.6	mA
125 kHz Supply Current						
IDD		All inputs switching	3.7	5.5	7.7	mA
1 MHz (2 Mbps) Supply Current						

DC Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
IDD		All inputs switching	3.9	5.6	8.0	mA
AC Switching Parameters (V$_{DD}$ = 5 V, C$_L$ = 15 pF)						
Propagation Delay, Low to High	t$_{PLH}$	AHx channels	49	84	124	ns
		Ax channels	3.8	4.1	4.6	µs
Propagation Delay, High to Low	t$_{PHL}$	AHx channels	47	80	113	ns
		Ax channels	3.75	4.15	4.55	µs
Pulse Width Distortion	PWD	| tPLH – tPHL |				
		AHx channels	—	6	50	ns
		Ax channels	—	80	—	ns
Propagation Delay Skew	t$_{PSK(P-P)}$	Part to part variation				
		AHx channels	—	—	±30	ns
		Ax channels	—	—	±80	ns
Channel–Channel Skew	t$_{PSK}$	Channel to channel variation				
		AHx channels	—	—	±30	ns
		Ax channels	—	—	±80	ns
Rise Time	t$_R$	50 Ω load	—	3.9	—	ns
Fall Time	t$_F$	50 Ω load	—	3.7	—	ns
Device Startup Time	t$_{START}$		—	150	—	µs
Common Mode Transient Immunity Si838x high speed channels (AHx)	CMTI	See Figure 4.1 Common Mode Measurement Circuit on page 14.	25	50	—	kV/µs
Common Mode Transient Immunity Si838x low speed channels (Ax)	CMTI	See Figure 4.1 Common Mode Measurement Circuit on page 14.	200	300	—	kV/µs
Serial Data Interface (See Figure 2.6 SPI Timing Diagram on page 6.)						
Clock rate[3]	SCLK		—	—	10	MHz
Cycle time (SCLK)[4]	T$_p$		100	—	—	ns
Delay time, SCLK fall to MISO active	Tdo1		—	—	20	ns
Delay time, SCLK fall to MISO transition	Tdo2		—	—	20	ns
Delay Time, NSS rise to MISO hi-Z	Tdz		—	—	20	ns
Setup time, NSS fall to SCLK fall	Tsu1		25	—	—	ns
Hold time, SCLK rise to NSS rise	Th1	See Figure 2.6 SPI Timing Diagram on page 6.	20	—	—	ns
Setup time, MOSI to SCLK rise	Tsu2		25	—	—	ns
Hold time, SCLK rise to MOSI transition	Th2		20	—	—	ns

DC Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Delay time between NSS active	Tnss		200	—	—	ns
Propagation delay, MOSI to SDI_THRU[3]	Tdthru		—	—	15	ns

Notes:

1. The current value at which device turns off is determined by $I_{F(OFF)} = I_{F(TH)} - I_{HYS}$.

2. The voltage value at which the device turns off is determined by $V_{F(OFF)} = V_{F(TH)} - V_{HYS}$.

3. See Section 2.2.5 SPI Daisy Chain Organization.

4. For daisy chain operation, see spec for "Propagation delay, MOSI to SDI_THRU" in this table.
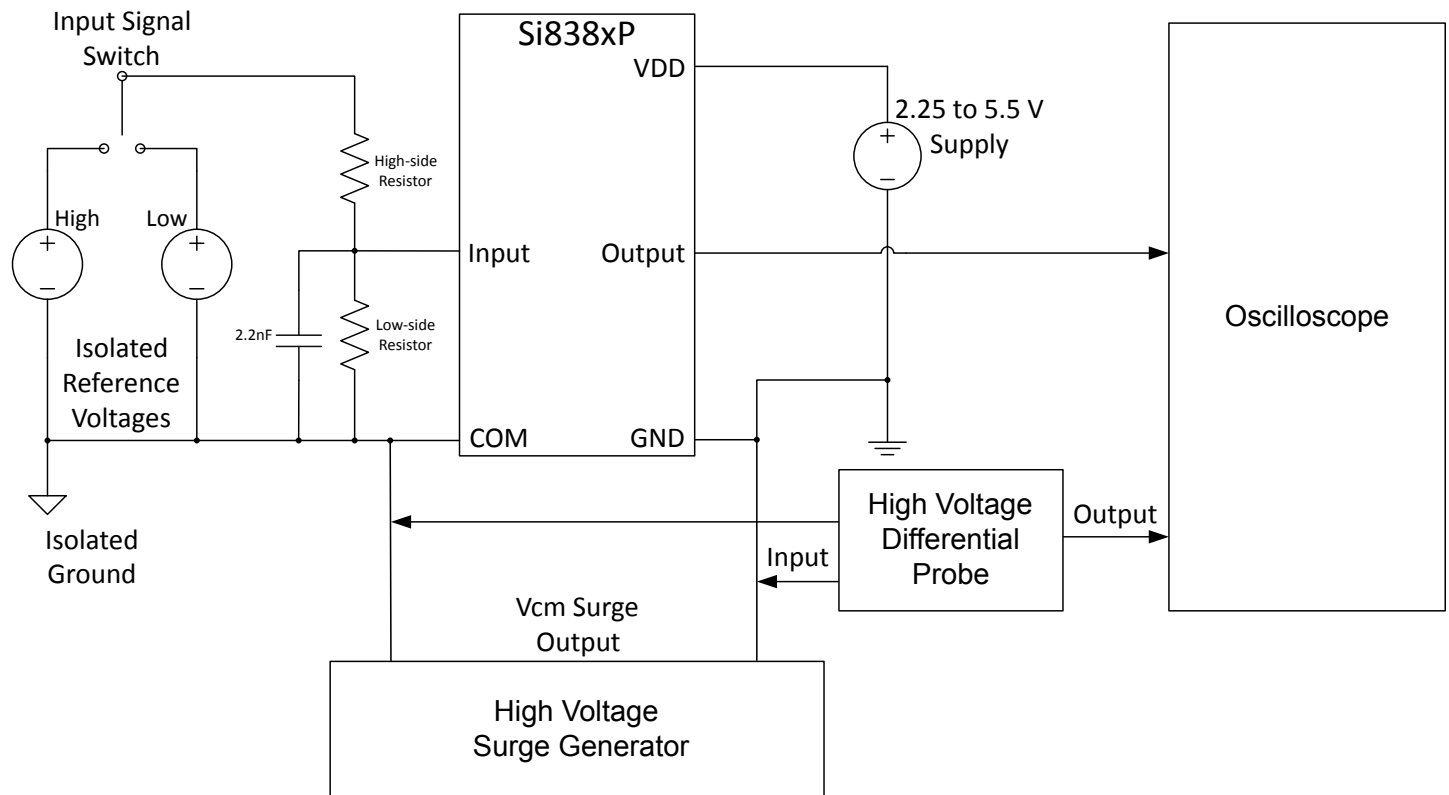
Figure 4.1. Common Mode Measurement Circuit

Table 4.3. Regulatory Information (pending)[1]

CSA
The Si838x is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
60950-1: Up to 130 VRMS reinforced insulation working voltage; up to 1000 VRMS basic insulation working voltage.
VDE
The Si838x is certified according to VDE0884. For more details, see File 5006301-4880-0001.
VDE 0884-10: 560 Vpeak for basic insulation working voltage
UL
The Si838x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 2500 VRMS isolation voltage for single protection.
CQC
The Si838x is certified under GB4943.1-2011.
Rated up to 130 VRMS reinforced insulation working voltage; up to 1000 VRMS basic insulation working voltage.
Note:
1. Regulatory Certifications apply to 2.5 kVRMS rated devices that are production tested to 3.0 kVRMS for 1 s. For more information, see 1. Ordering Guide.

Table 4.4. Insulation and Safety-Related Specifications[1]

Parameter	Symbol	Test Condition	QSOP-20	Unit
Nominal Air Gap (Clearance)	L(IO1)		3.6 min	mm
Nominal External Tracking (Creepage)	L(IO2)		3.6 min	mm
Minimum Internal Gap (Internal Clearance)			0.008	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	V
Erosion Depth	ED		0.057	mm
Resistance (Input-Output)[1]	RIO		10^{12}	Ω
Capacitance (Input-Output)[1]	CIO	f = 1 MHz	1	pF

Note:
1. To determine resistance and capacitance, the Si838x is converted into a 2-terminal device. Pins 1–10 are shorted together to form the first terminal, and pins 11–20 are shorted together to form the second terminal. The parameters are then measured between these two terminals.

Table 4.5. IEC 60664-1 Ratings

Parameter	Test Condition	QSOP-20
Basic Isolation Group	Material Group	I
Installation Classification	Rated Mains Voltages < 150 VRMS	I–IV
	Rated Mains Voltages < 300 VRMS	I-III
	Rated Mains Voltages < 400 VRMS	I-II
	Rated Mains Voltages < 600 VRMS	I-II

Table 4.6. VDE 0884-10 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic QSOP-20	Unit
Maximum Working Insulation Voltage	V_{IORM}		560	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (VIORM x 1.875 = VPR,100%) Production Test, tm = 1 sec, (Partial Discharge < 5 pC)	1050	V peak
Transient Overvoltage	V_{IOTM}	t = 60 s	4000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at TS, V_{IO} = 500 V	R_S		>10^9	Ω

Note:
1. This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si838x provides a climate classification of 40/125/21.

Table 4.7. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Max QSOP-20	Unit
Case Temperature	T_S		150	°C
Safety Current	I_S	θ_{JA} = 105 °C/W V_F = 2.8 V, T_J = 150 °C, T_A = 25 °C	370	mA
Power Dissipation	P_S		1.2	W

Note:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figure 4.2 (QSOP-20) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE 0884 on page 17.

Table 4.8. Thermal Characteristics

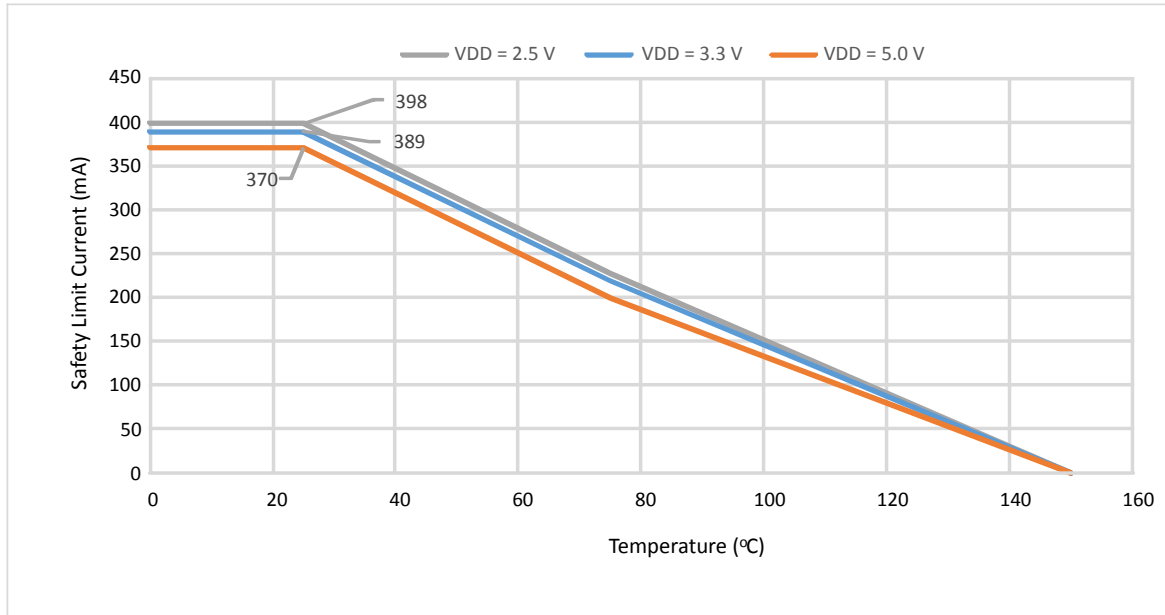| Parameter	Symbol	QSOP-20	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	105	°C/W

Figure 4.2. (QSOP-20) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE 0884

Table 4.9. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	−65	+150	°C
Ambient Temperature	T_A	−40	+125	°C
Junction Temperature	T_J	—	+150	°C
Average Forward Input Current	$I_{F(AVG)}$	—	30	mA
Peak Transient Input Current (< 1 µs pulse width, 300 ps)	I_{FTR}	—	1	A
Input voltage, referred to COM	Ax, AHx	± −0.5	±7	V
Supply Voltage	V_{DD}	−0.5	7	V
Output Voltage	V_{OUT}	−0.5	V_{DD}+0.5	V
Average Output Current	$I_{O(AVG)}$	—	10	mA
Input Power Dissipation	P_I	—	480	mW
Output Power Dissipation (includes 3 mA per channel for status LED)	P_O	—	484	mW
Total Power Dissipation	P_T	—	964	mW
Lead Solder Temperature (10 s)		—	260	°C
HBM Rating ESD		4	—	kV
Machine Model ESD		200	—	V
CDM		500	—	V
Maximum Isolation Voltage (1 s)		—	3000	V_{RMS}

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet.

5. Applications

5.1 System Level Transitions with the Si838x
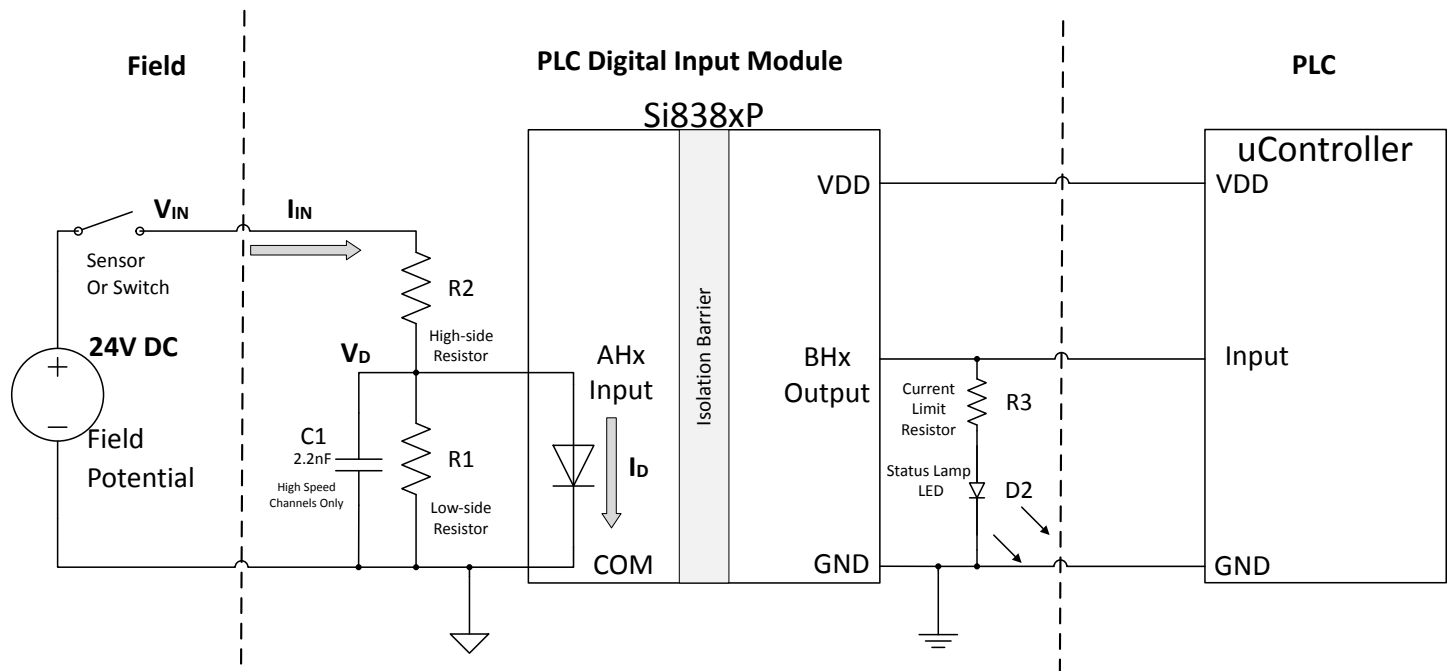
Figure 5.1. System Level Drawing of a High-speed Channel on the Si838xP with the Supporting Bill of Materials

The Si838x combined with an appropriate input resistor network and indication LED will produce a PLC Digital Input Module which adheres to the IEC 61131-2 specification.

Resistors R1 and R2 set the transition voltages and currents for the system, as visualized in the figure below, while capacitor C1, is required only for high-speed channels and serves to improve CMTI performance. Further, resistor R3 is selected based on desired LED, D2, brightness during a system ON condition.
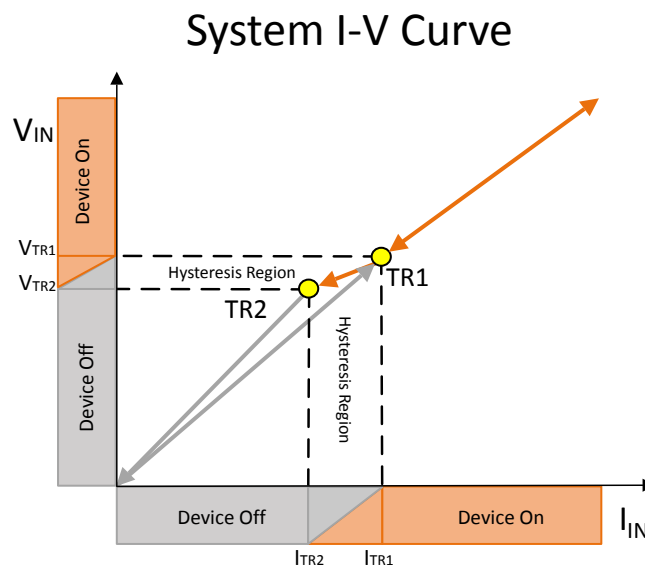
Figure 5.2. Visualization of System Level Transitions when Utilizing a Si838x According to the Recommended Design Process

5.2 IEC 61131-2 Compliance Options

IEC 61131-2 articulates three types of digital inputs for PLC sensing. Each type category dictates boundary conditions on the system level input space, (V_{IN}, I_{IN}), defining the range of values for which the module must output a logic LOW, a logic HIGH, or transition between the two.

More details on the specification can be found on the IEC website: https://webstore.iec.ch/publication/4551.

The table below provides per-input type bill of materials recommendations for plug-n-play designs adhering to the specification or as a starting point for custom designs. These recommendations assume a resistor tolerance of 5%.

Table 5.1. Si838x Recommended Input Bill of Materials and System Level Transition Values[1]

	Input Resistor Values		Nominal TR1 Values		Nominal TR2 Values	
PLC Digital Input Type	R1 (Ω)	R2 (Ω)	I_{IN} (mA)	V_{IN} (V)	I_{IN} (mA)	V_{IN} (V)
Type-1	2400	6200	1.18	8.70	1.07	7.97
Type-2	390	1500	4.14	7.60	3.88	7.13
Type-3	750	2700	2.45	7.98	2.27	7.44
Note:						
1. Based on 24 V DC PLC digital input types.						

5.3 Custom Bill of Materials

A PLC digital input module based on the Si838x can have its transition values customized on a per-channel basis in accordance with the system level equations and tolerances. An extended discussion of this process and an example design are available in "AN970: Design Guide for PLC Digital Input Modules Using the Si838x".

6. Pin and Package Definitions

The Si838x consists of multiple dies in one package. Each package and bond-out serves a customer need and may reflect multiple bond options. The following packages are defined: QSOP-20. 1. Ordering Guide describes the part number and OPN configuration quantities envisioned for these products. Subsequent sections define the pins for each package type.
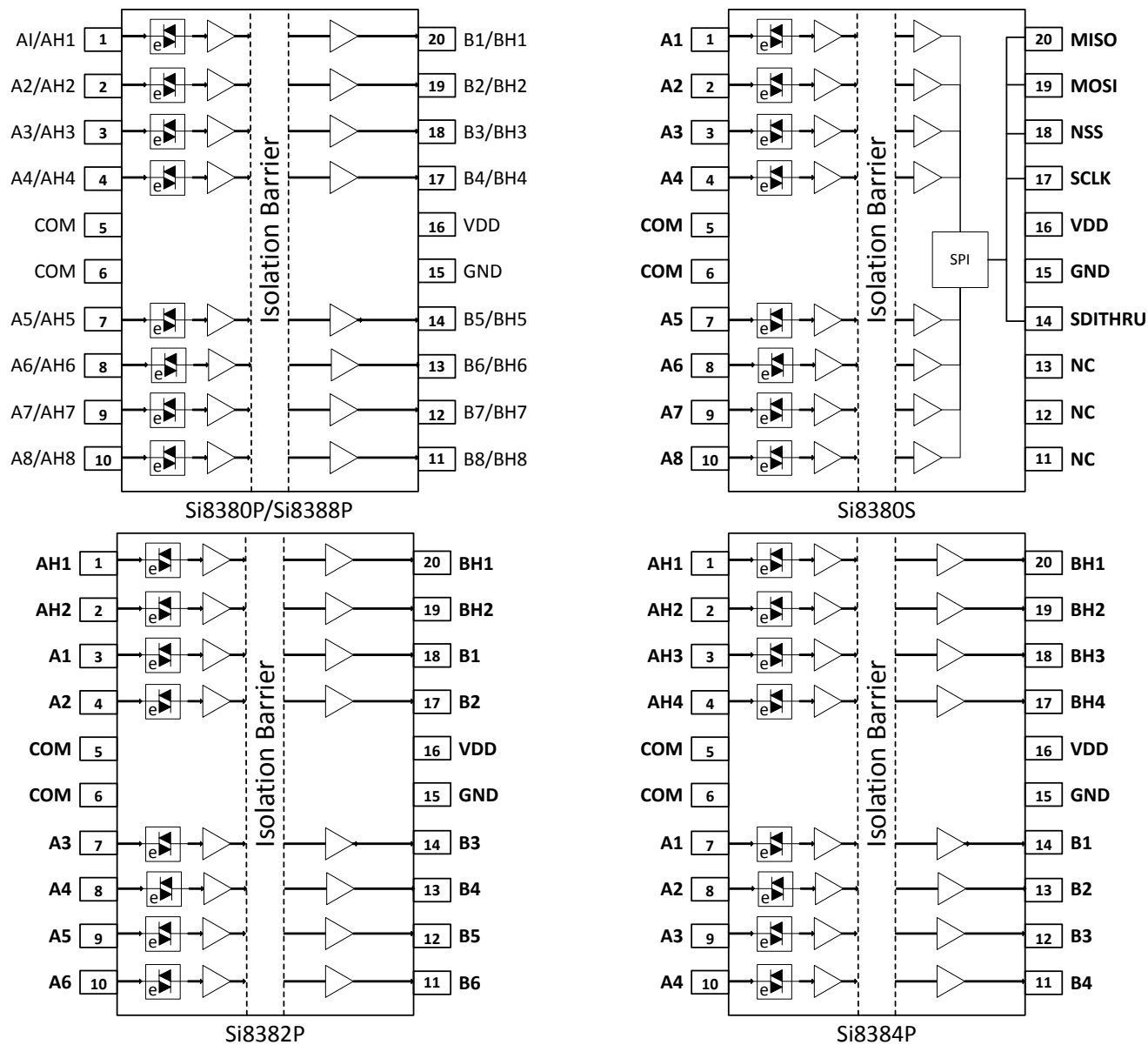
6.1 Pin Descriptions

Figure 6.1. Si838x Pin Assignments

Table 6.1. Si838x Pin Descriptions

Pin Name	Description
A1 – A8	Low-speed input channels
AH1-AH8	High-speed input channels
COM	Common. Can be connected to ground or 24 V
B1-B8	Low-speed output channels
BH1-BH8	High-speed output channels
VDD	Controller side power supply
GND	Controller side ground
MOSI	SPI, input
SCLK	SPI Clock
NSS	SPI Chip select
SDITHRU	SPI Serial data out for cascading multiple Si838x (up to 16)
MISO	SPI, output

7. Package Outline

The figure below illustrates the package details for the 20-pin QSOP package. The table below lists the values for the dimensions shown in the illustration.
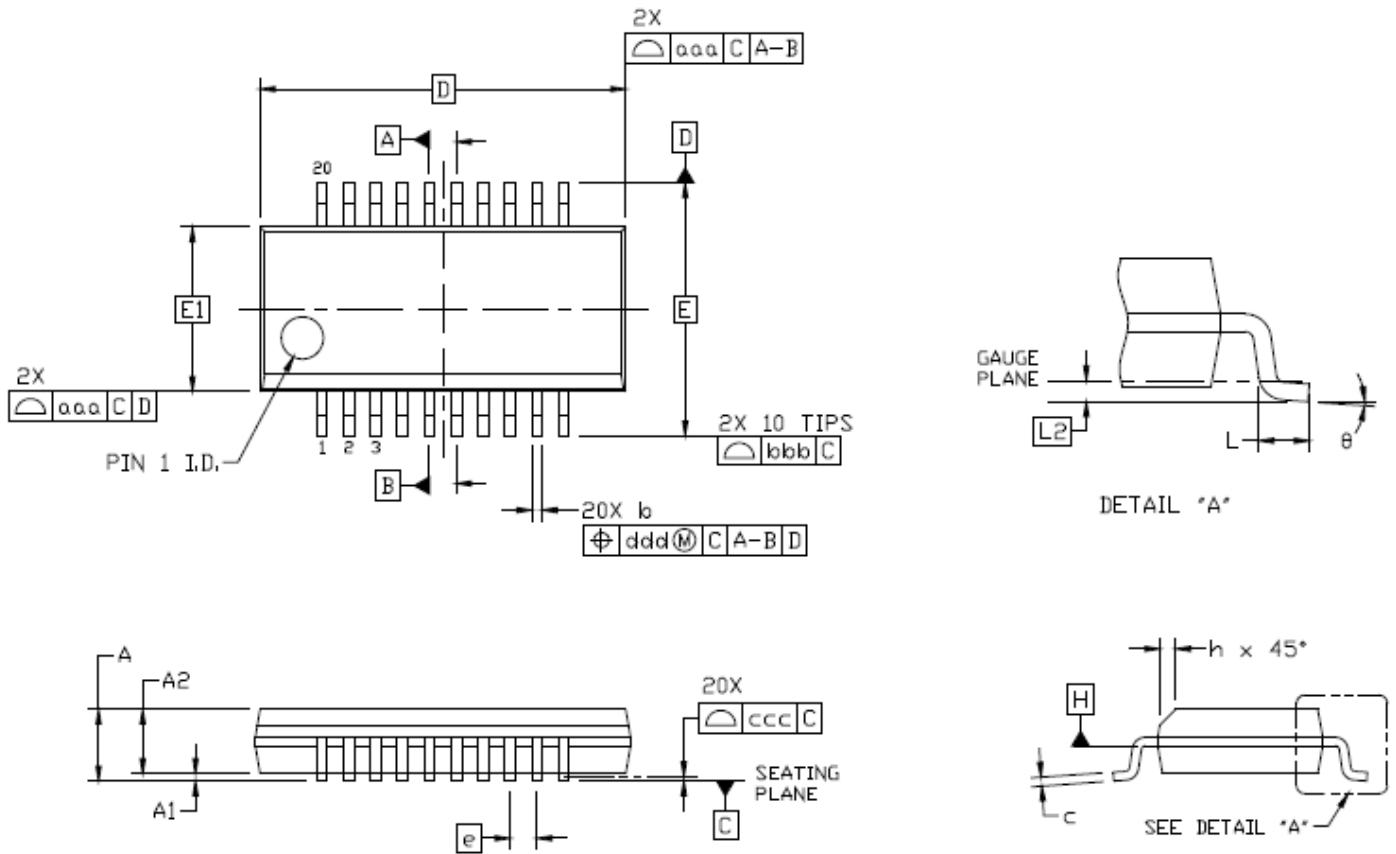

Figure 7.1. 20-Pin QSOP Package Outline

Table 7.1. Package Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.20	0.30
c	0.17	0.25
D	8.66 BSC	
E	6.00 BSC	
E1	3.91 BSC	
e	0.635 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.20	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline M0-137, Variation AD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Land Pattern

The figure below illustrates the PCB land pattern details for the 20-pin QSOP package. The table below lists the values for the dimensions shown in the illustration.
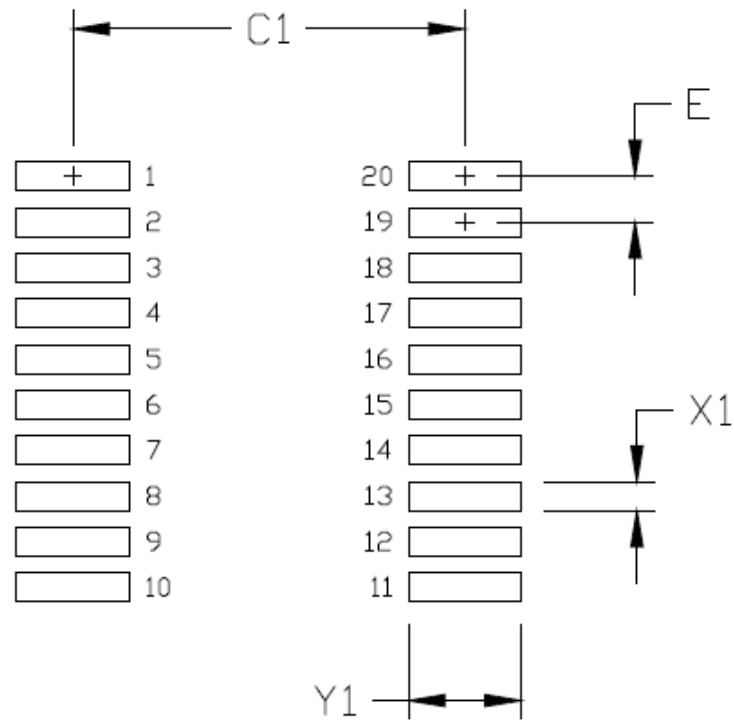
Figure 8.1. 20-Pin QSOP PCB Land Pattern

Table 8.1. 20-Pin QSOP PCB Land Pattern Dimensions

Dimension	Feature	mm
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	0.635
X1	Pad Width	0.40
Y1	Pad Length	1.55
1. This Land Pattern Design is based on IPC-7351 design rules for Density Level B (Median Land Protrusion). 2. All feature sizes shown are at Maximum Material Condition (MMC), and a card fabrication tolerance of 0.05 mm is assumed.		

9. Top Marking
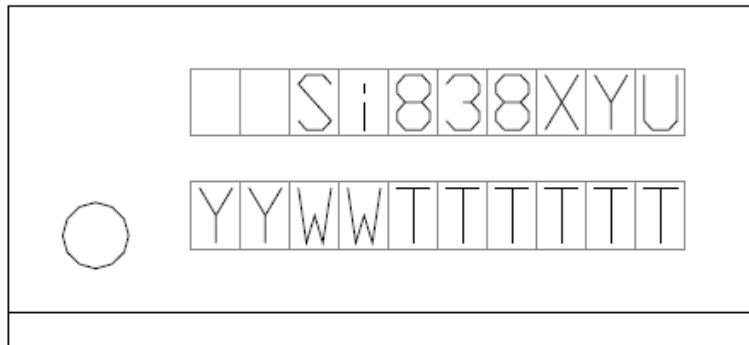
Figure 9.1. Si838x Top Marking (20-Pin QSOP)

Table 9.1. Top Marking Explanation (20-Pin QSOP)

Line 1 Marking:	Base Part Number
	
	Ordering Options
	
	See 1. Ordering Guide for more information.
		Si838 = 8-ch PLC input isolator
		
		X = # of high speed channels
		
		Y = S, P
		
		    S = serial outputs
		
		    P = parallel outputs
		
		U = Debounce option
		
		    F = fast debounce, 10 ms
		
		    M = slower debounce, 30 ms
		
		    S = slow debounce, 100 ms

Line 2 Marking:	YY = Year WW = Workweek TTTTTT = Mfg Code	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date and manufacturing code from Assembly Purchase Order form.

10. Document Change List

10.1 Revision 0.5

April 4, 2016
- Initial release.

Table of Contents

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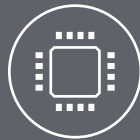
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