256k 32k X 8 bit

FT28HC256

5 Volt, Byte Alterable EEPROM

FEATURES

- **Access time: 90ns**
- **Simple byte and page write**
  - **—Single 5V supply**
  - **—No external high voltages or V_{PP} control circuits**
  - **—Self-timed**
  - **—No erase before write**
  - **—No complex programming algorithms**
  - **—No overerase problem**
- **Low power CMOS**
  - **—Active: 60mA**
  - **—Standby: 500µA**
- **Software data protection**
  - **—Protects data against system level inadvertent writes**
- **High speed page write capability**
- **Highly reliable direct Write**
  - **—Endurance: 1,000,000 cycles**
  - **—Data retention: 100 years**
- **Early end of write detection**
  - **—DATA polling**
  - **—Toggle bit polling**

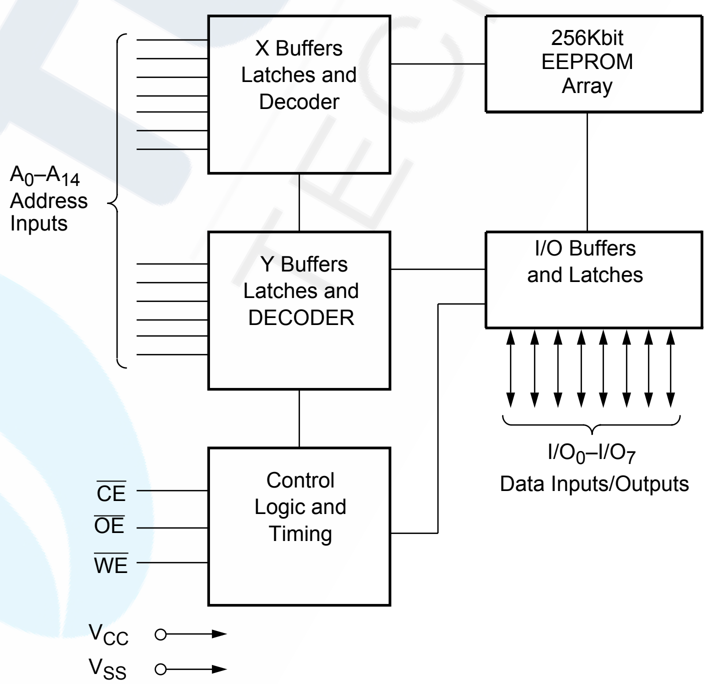
DESCRIPTION

The FT28HC256 is a second generation high performance 32K x 8 EEPROM.

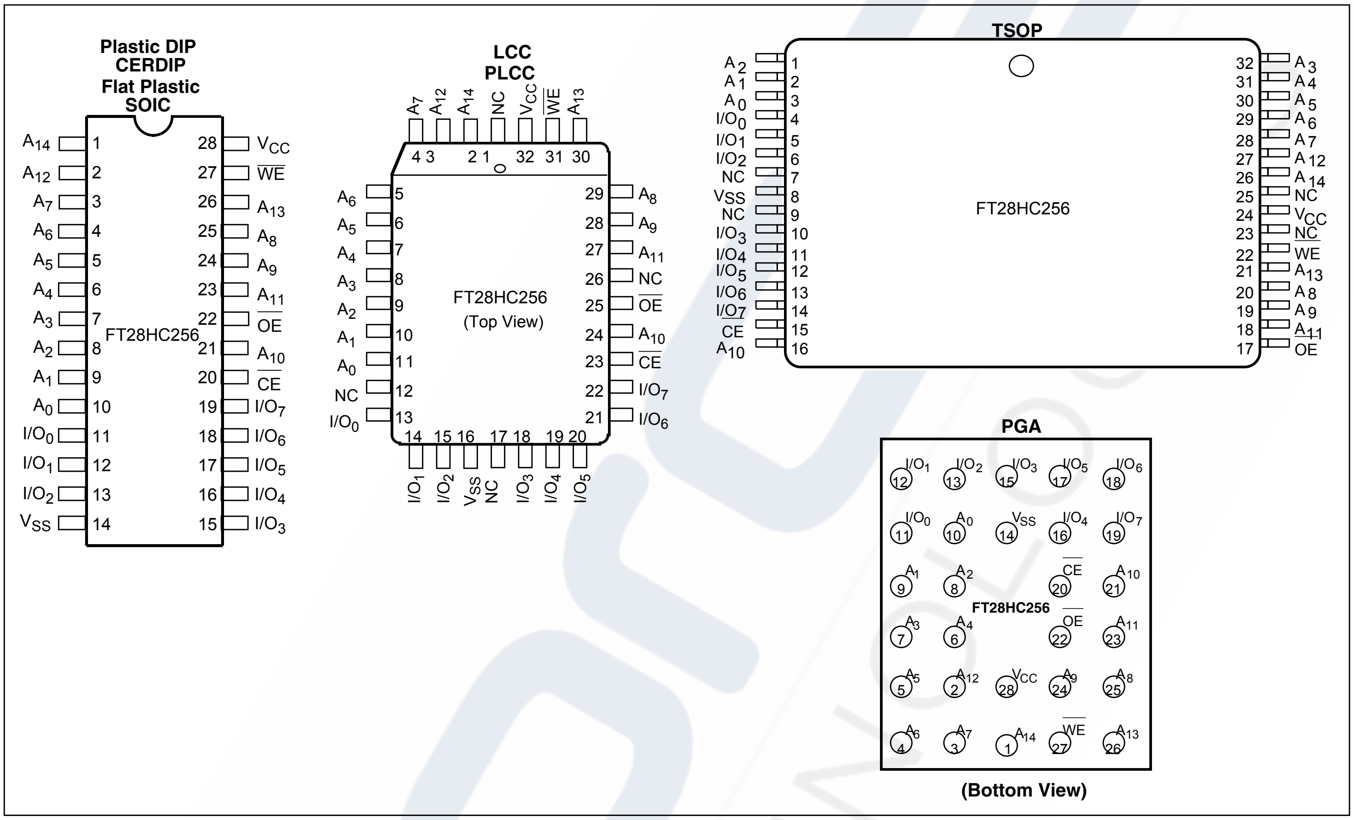
The FT28HC256 supports a 128-byte page write operation, effectively providing a 24µs/byte write cycle, and enabling the entire memory to be typically rewritten in less than 0.8 seconds. The FT28HC256 also features $\overline{\text{DATA}}$ Polling and Toggle Bit Polling, two methods of providing early end of write detection. The FT28HC256 also supports the JEDEC standard Software Data Protection feature for protecting against inadvertent writes during power-up and power-down.

Endurance for the FT28HC256 is specified as a minimum 1,000,000 writecycles per byte and an inherent data retention of 100 years.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTIONS

Addresses (A_0–A_{14})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/ write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers, and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the FT28HC256 through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the FT28HC256.

PIN NAMES

Symbol	Description
A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

DEVICE OPERATION

Read

Read operations are initiated by both OE and CE LOW. The read operation is terminated by either CE or OE returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE or CE is HIGH.

Write

Write operations are initiated when both CE and WE are LOW and OE is HIGH. The FT28HC256 supports both a CE and WE controlled write cycle. That is, the address is latched by the falling edge of either CE or WE, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE or WE, which ever occurs first A byte write operation, once initiated, will automatically continue to completion, typically within 3ms.

Page Write Operation

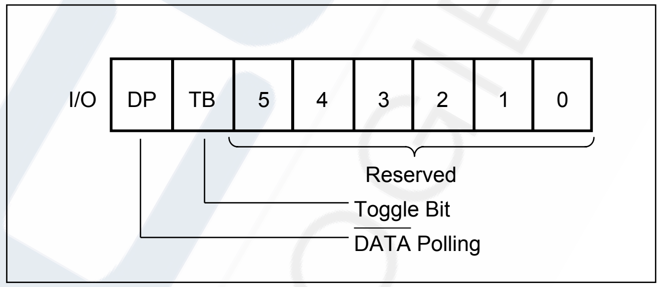
The page write feature of the FT28HC256 allows the entire memory to be written in typically 0.8 seconds . Page write allows up to one hundred twenty-eight bytes of data to be consecutively written to the FT28HC256, prior to the commencement of the internal programming cycle . The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_7 through A_{14}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to one hundred twenty-seven bytes in the same manner as the first byte was written. Each successive byte load cycle , started by the WE HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding WE. If a subsequent WE HIGH to LOW transition is not detected within 100µs , the internal automatic programming cycle will commence . There is no page write window limitation. Effectively the page write window is infinitel wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The FT28HC256 provides the user two write operation status bits. These can be used to optimised a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



DATA Polling (I/O$_7$)

The FT28HC256 features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the FT28HC256. This eliminates additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O$_7$ (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete , I/O$_7$ will reflect true data.

Toggle Bit (I/O$_6$)

The FT28HC256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O$_6$ will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease, and the device will be accessible for additional read and write operations.

$\overline{\text{DATA}}$ POLLING I/O$_7$

Figure 2. $\overline{\text{DATA}}$ Polling Bus Sequence

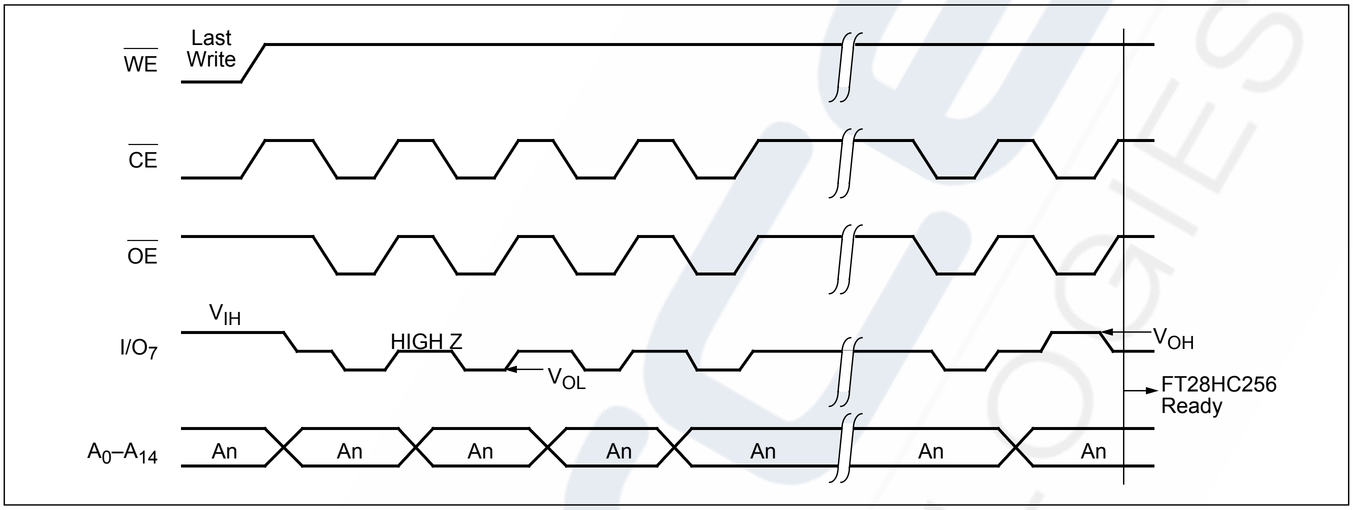
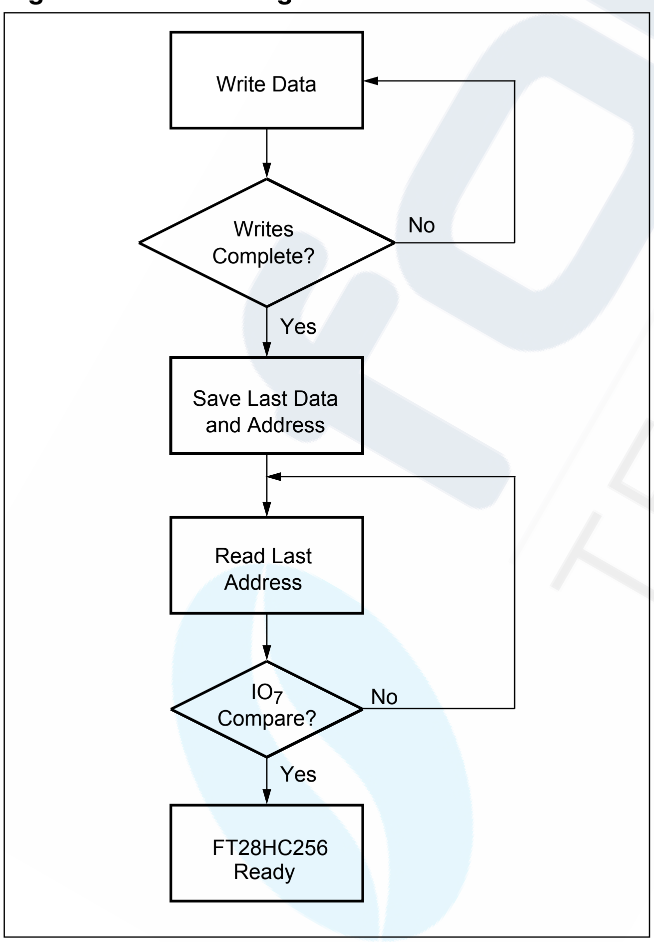


Figure 3. $\overline{\text{DATA}}$ Polling Software Flow



$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the FT28HC256. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diag ram in Figure 3 illustrates one method of implementing the routine.

THE TOGGLE BIT I/O_6

Figure 4. Toggle Bit Bus Sequence

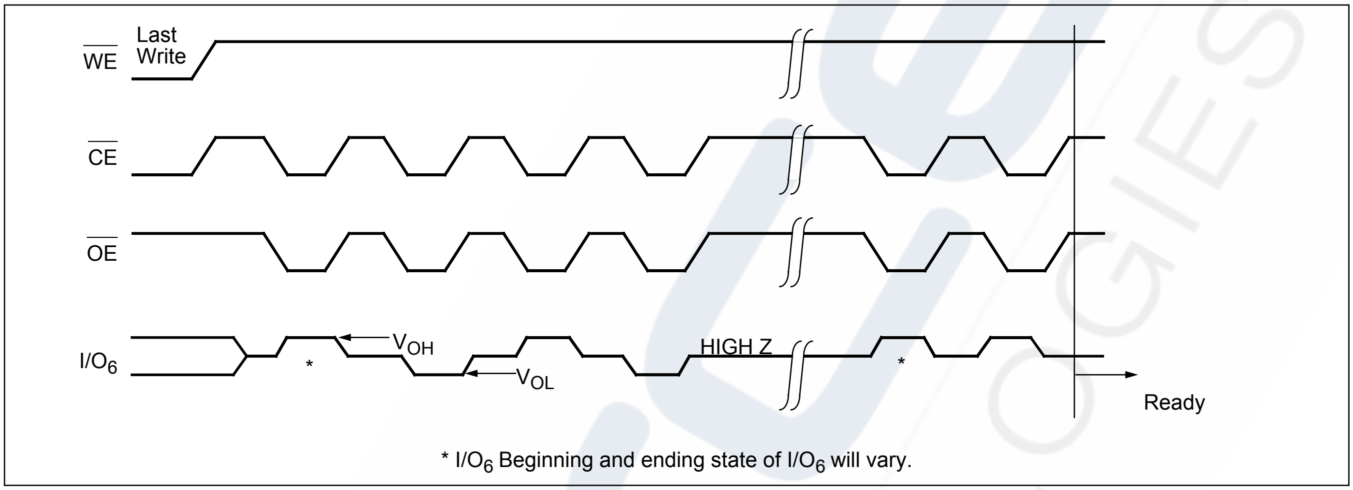
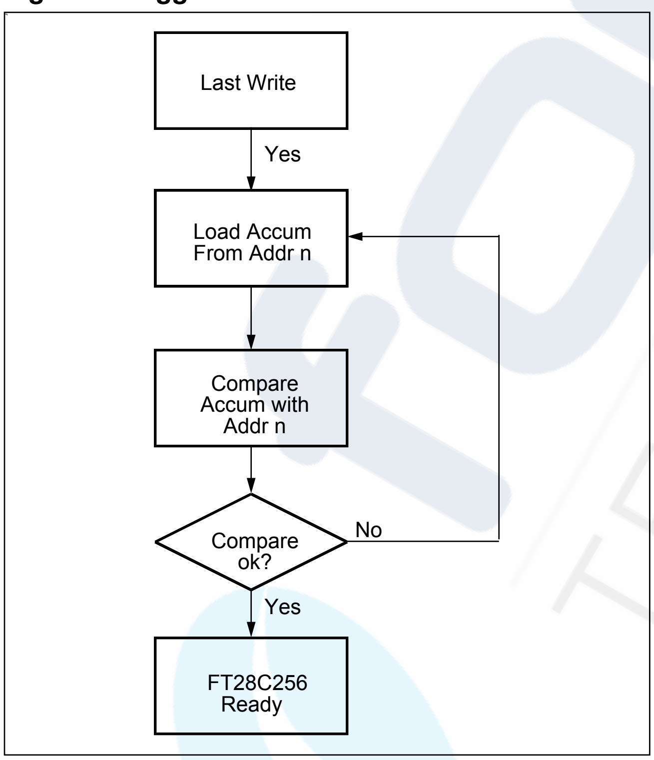


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the chore of saving and fetching the last address and data in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple FT28HC256 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for polling the Toggle Bit.

HARDWARE DATA PROTECTION

The FT28HC256 provides two hardware features that protect nonvolatile data from inadvertent writes.

– Default V_{CC} Sense—All write functions are inhibited when V_{CC} is 3.5V typically.

– Write Inhibit—Holding either OE LOW, WE HIGH, or CE HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

SOFTWARE DATA PROTECTION

The FT28HC256 offers a software-controlled data protection feature. The FT28HC256 is shipped from FT with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The FT28HC256 can be automatically protected during power-up and power-down (without the need for external circuits) by employing the software data protection feature. The internal software data protection circuit is enabled after the first w ite operation, utilising the software algor ithm. This circuit is non volatile, and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the FT28HC256 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence.

The three-byte sequence opens the page write window, enabling the host to write from one to one hundred twenty-eight bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

SOFTWARE DATA PROTECTION

Figure 6. Timing Sequence—Byte or Page Write

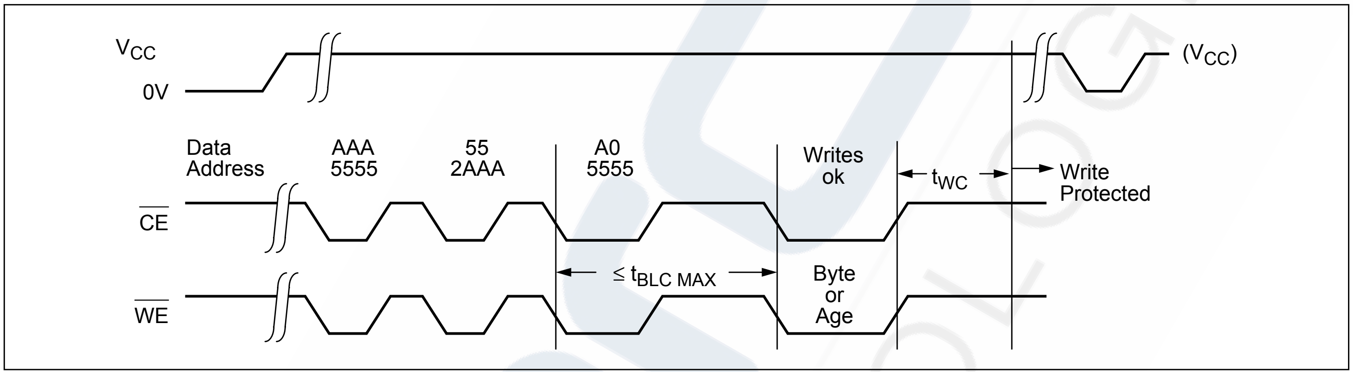
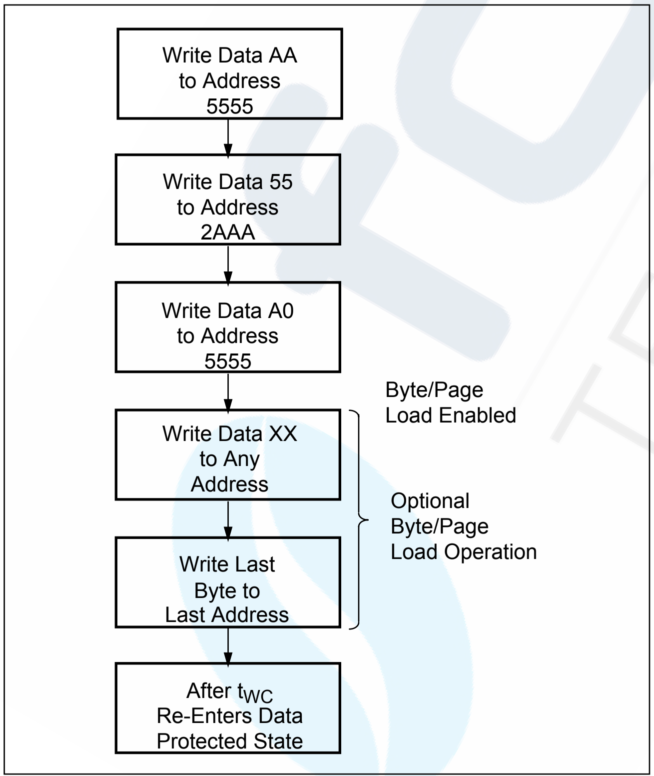


Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the FT28HC256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the FT28HC256 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

RESETTING SOFTWARE DATA PROTECTION

Figure 8. Reset Software Data Protection Timing Sequence

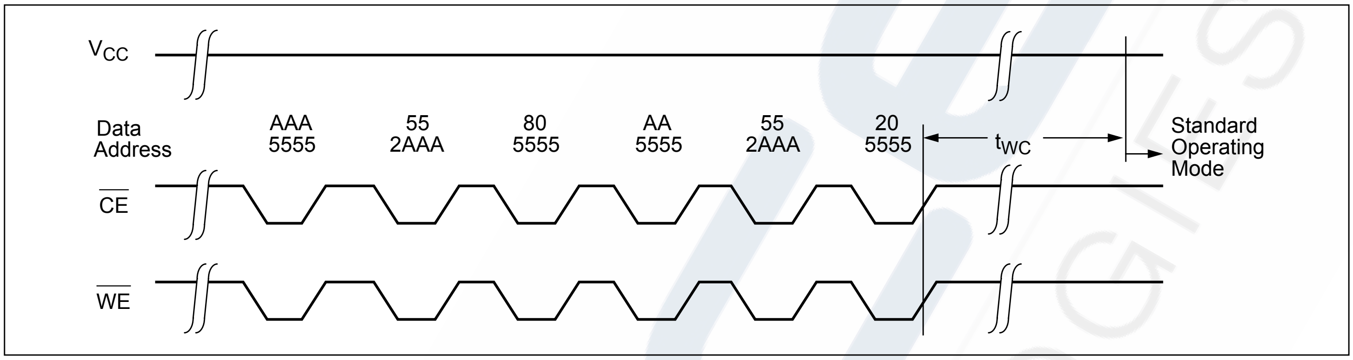
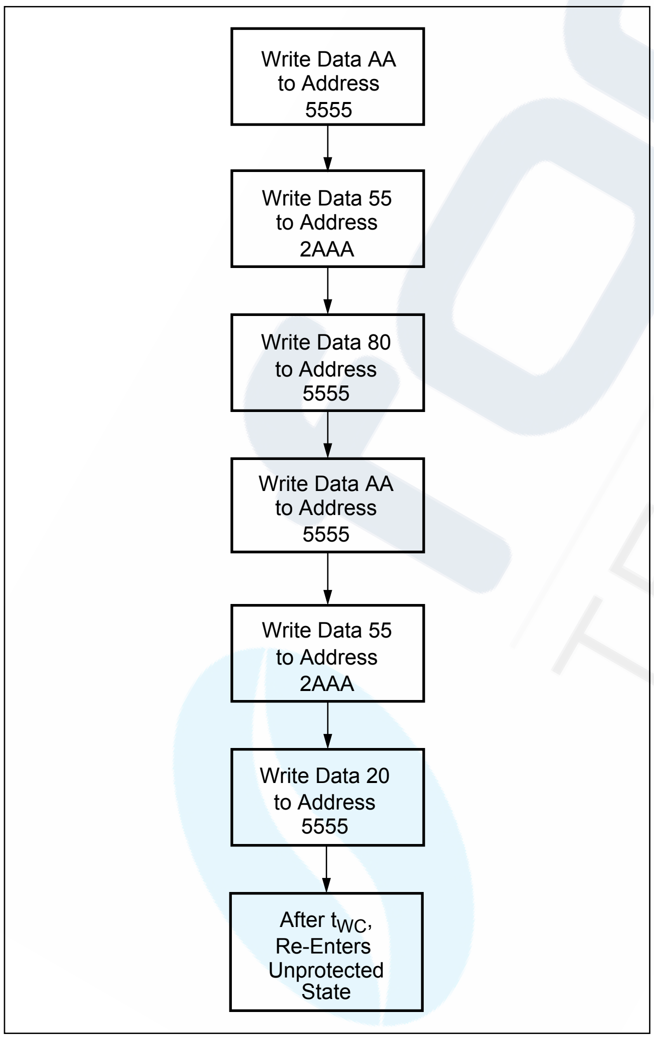


Figure 9. Write Sequence for resetting Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an EEPROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the FT28HC256 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

Because the FT28HC256 is frequently used in large memory arrays, it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation, and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit, it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both OE and WE would then be common among all devices in the array. For a read operation, this assures that all deselected devices are in their standby mode, and that only the selected device(s) is/are outputting data on the bus.

Because the FT28HC256 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling CE will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} fo r each eight de vices emplo yed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

ABSOLUTE MAXIMUM RATINGS

Temperature under bias
FT28HC256 .... –10°C to +85°C
FT28HC256I, FT28HC256M............. –65°C to +135°C
Storage temperature .... –65°C to +150°C
Voltage on any pin with
respect to V_{SS} ....–1V to +7V
D.C. output current 10mA
Lead temperature (soldering, 10 seconds)........ 300°C

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those indicated in the operational sections of this specification) i not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

Supply Voltage	Limits
FT28HC256	5V ±10%

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.(7)	Max.		
I_{CC}	V_{CC} active current (TTL Inputs)		30	60	mA	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, All I/O's = open, address inputs = .4V/2.4V levels @ f = 10MHz
I_{SB1}	V_{CC} standby current (TTL Inputs)		1	2	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$, All I/O's = open, other inputs = V_{IH}
I_{SB2}	V_{CC} standby current (CMOS Inputs)		200	500	µA	$\overline{CE} = V_{CC} - 0.3V$, $\overline{OE}$ = GND, All I/Os = open, other inputs = $V_{CC} - 0.3V$
I_{LI}	Input leakage current			10	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output leakage current			10	µA	$V_{OUT} = V_{SS}$ to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(2)	Input LOW voltage	–1		0.8	V	
V_{IH}(2)	Input HIGH voltage	2		V_{CC} + 1	V	
V_{OL}	Output LOW voltage			0.4	V	I_{OL} = 6mA
V_{OH}	Output HIGH voltage	2.4			V	I_{OH} = –4mA

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

POWER-UP TIMING

Symbol	Parameter	Max.	Unit
t_{PUR}(3)	Power-up to read	100	µs
t_{PUW}(3)	Power-up to write	5	ms

Note: (3) This parameter is periodically sampled and not 100% tested.

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Unit	Conditions
$C_{I/O}$(9)	Input/output capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(9)	Input capacitance	6	pF	V_{IN} = 0V

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Unit
Endurance	1,000,000		Cycles
Data retention	100		Years

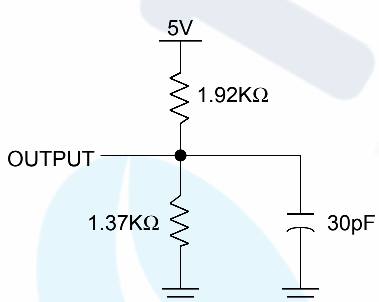
A.C. CONDITIONS OF TEST

Input pulse levels	0V to 3V
Input rise and fall times	5ns
Input and output timing levels	1.5V

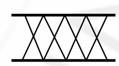
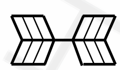
MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	active
L	H	L	Write	D_{IN}	active
H	X	X	Standby and write inhibit	High Z	standby
X	L	X	Write inhibit	—	—
X	X	H	Write inhibit	—	—

EQUIVALENT A.C. LOAD CIRCUIT



SYMBOL TABLE

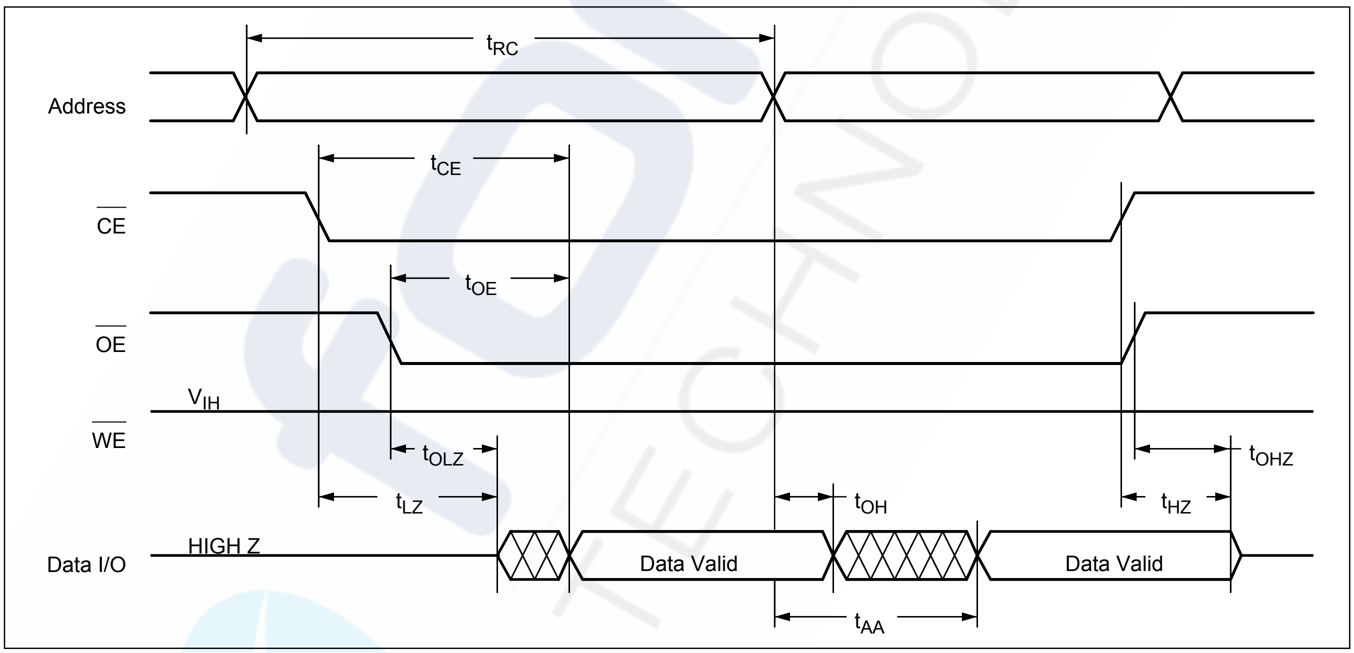
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	FT28HC256-70		FT28HC256-90		FT28HC256-12		FT28HC256-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}(5)	Read cycle time	70		90		120		150		ns
t_{CE}(5)	Chip enable access time		70		90		120		150	ns
t_{AA}(5)	Address access time		70		90		120		150	ns
t_{OE}	Output enable access time		35		40		50		50	ns
t_{LZ}(4)	$\overline{CE}$ LOW to active output	0		0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ LOW to active output	0		0		0		0		ns
t_{HZ}(4)	$\overline{CE}$ HIGH to high Z output		35		40		50		50	ns
t_{OHZ}(4)	$\overline{OE}$ HIGH to high Z output		35		40		50		50	ns
t_{OH}	Output hold from address change	0		0		0		0		ns

Read Cycle



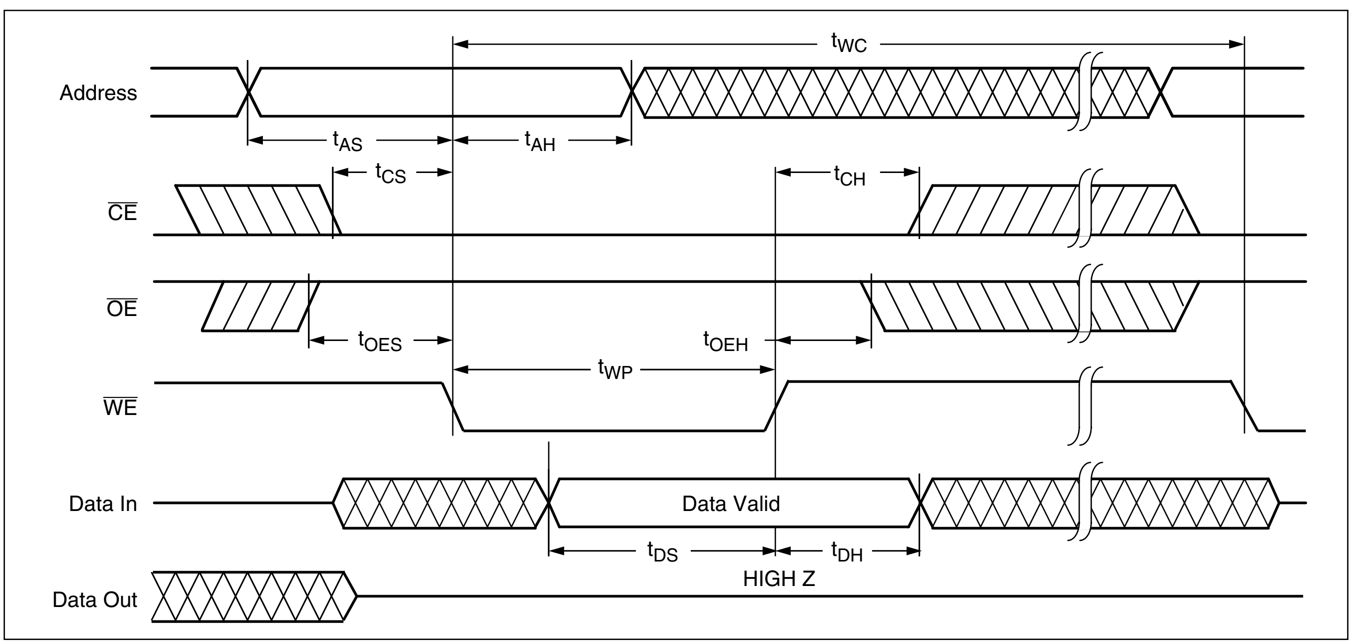
Notes: (4) t_{LZ} min., t_{HZ}, t_{OLZ} min. and t_{OHZ} are periodically sampled and not 100% tested, t_{HZ} and t_{OHZ} are measured with CL = 5pF, from the point when $\overline{CE}$, $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer diven.

Write Cycle Limits

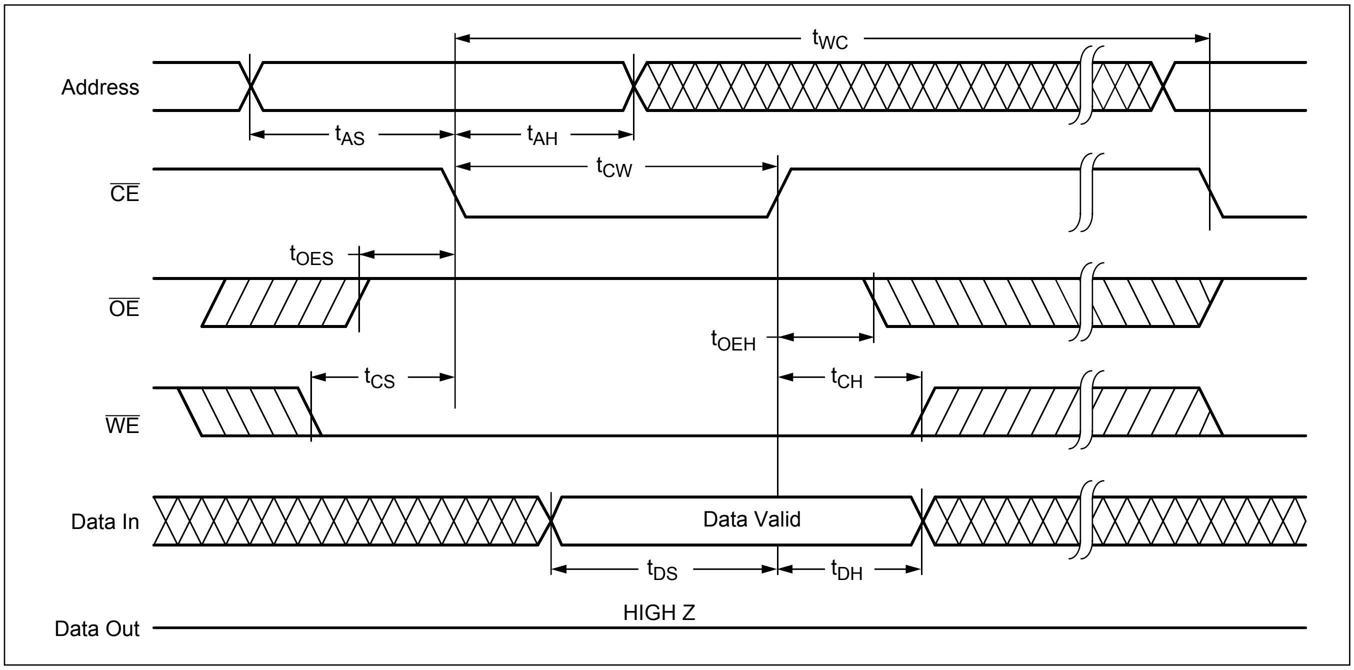
Symbol	Parameter	Min.	Typ.(6)	Max.	Unit
t_{WC}(7)	Write cycle time		3	5	ms
t_{AS}	Address setup time	0			ns
t_{AH}	Address hold time	50			ns
t_{CS}	Write setup time	0			ns
t_{CH}	Write hold time	0			ns
t_{CW}	$\overline{CE}$ pulse width	50			ns
t_{OES}	$\overline{OE}$ HIGH setup time	0			ns
t_{OEH}	$\overline{OE}$ HIGH hold time	0			ns
t_{WP}	$\overline{WE}$ pulse width	50			ns
t_{WPH}(8)	$\overline{WE}$ HIGH recovery (page write only)	50			ns
t_{DV}	Data valid			1	µs
t_{DS}	Data setup	50			ns
t_{DH}	Data hold	0			ns
t_{DW}(8)	Delay to next write after polling is true	10			µs
t_{BLC}	Byte load cycle	0.15		100	µs

Notes: (6) Typical values are for T_A = 25°C and nominal supply voltage.
(7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.
(8) t_{WPH} and t_{DW} are periodically sampled and not 100% tested.

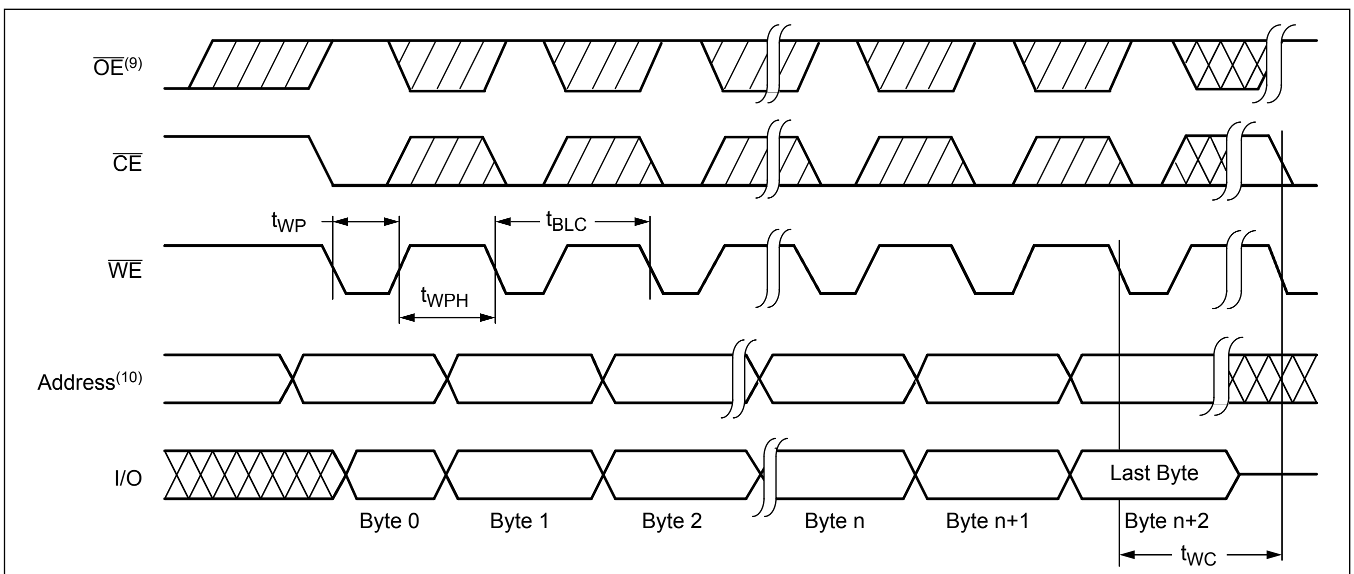
$\overline{WE}$ Controlled Write Cycle



$\overline{CE}$ Controlled Write Cycle



Page Write Cycle

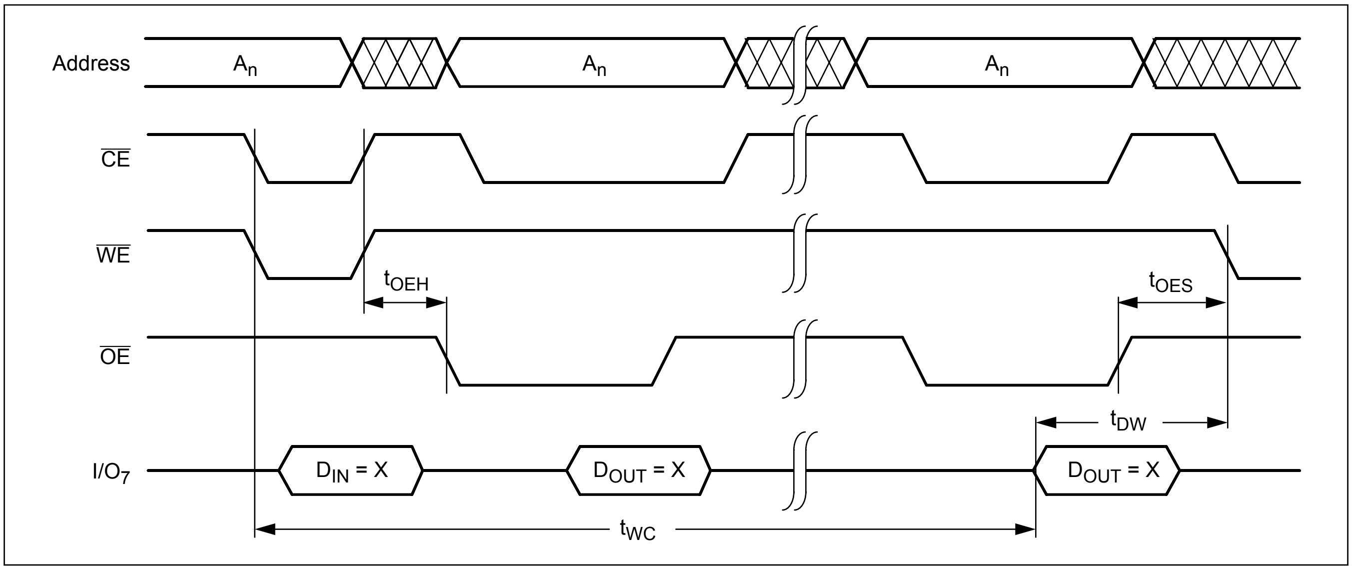


*For each successive write within the page write operation, A_7–A_{15} should be the same or writes to an unknown address could occur.

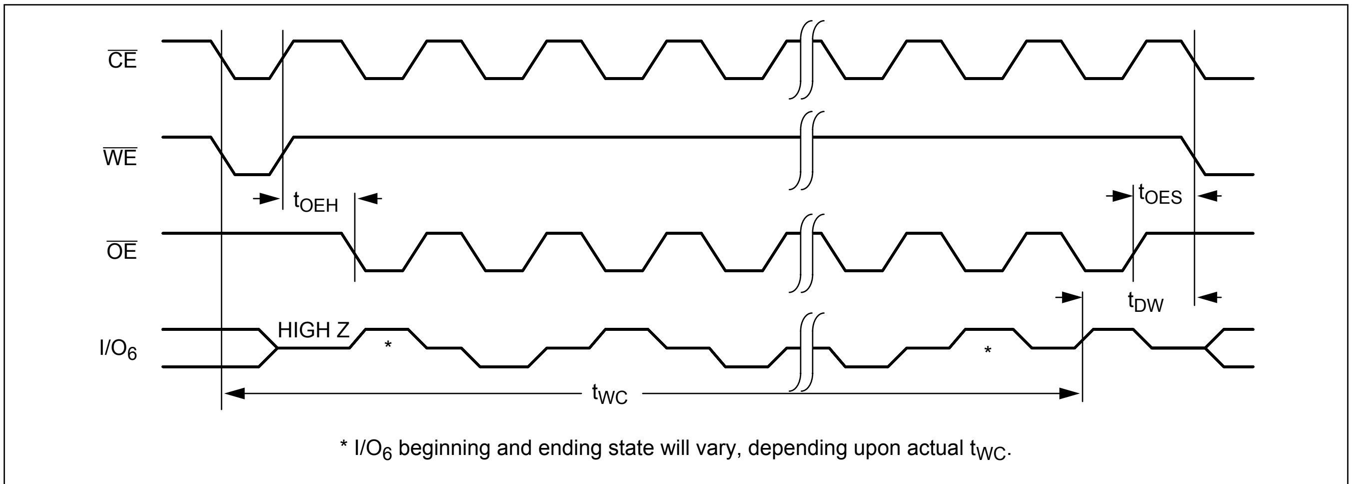
Notes: (9) Between successive byte writes within a page wr ite operation, $\overline{OE}$ can be strobed LO W: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(10) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{DATA}$ Polling Timing Diagram(11)



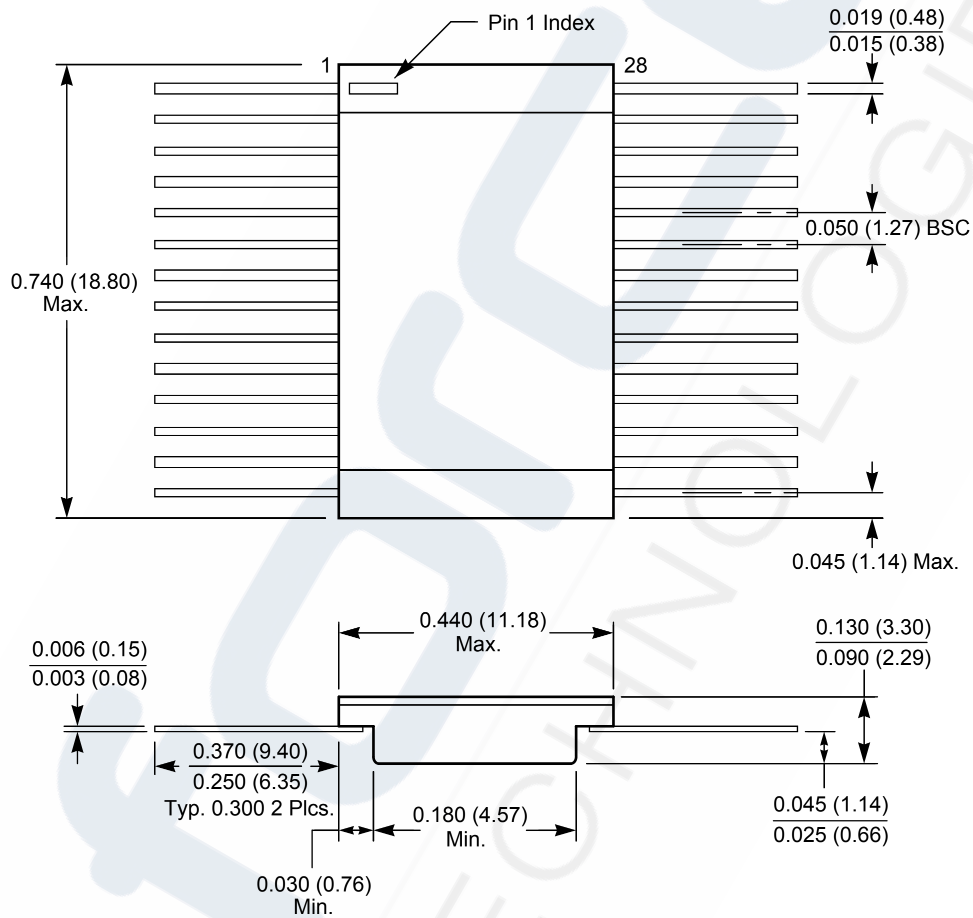
Toggle Bit Timing Diagram(11)



Note: (11)Polling operations are by definition read cycles and are thereore subject to read cycle timings.

PACKAGING INFORMATION

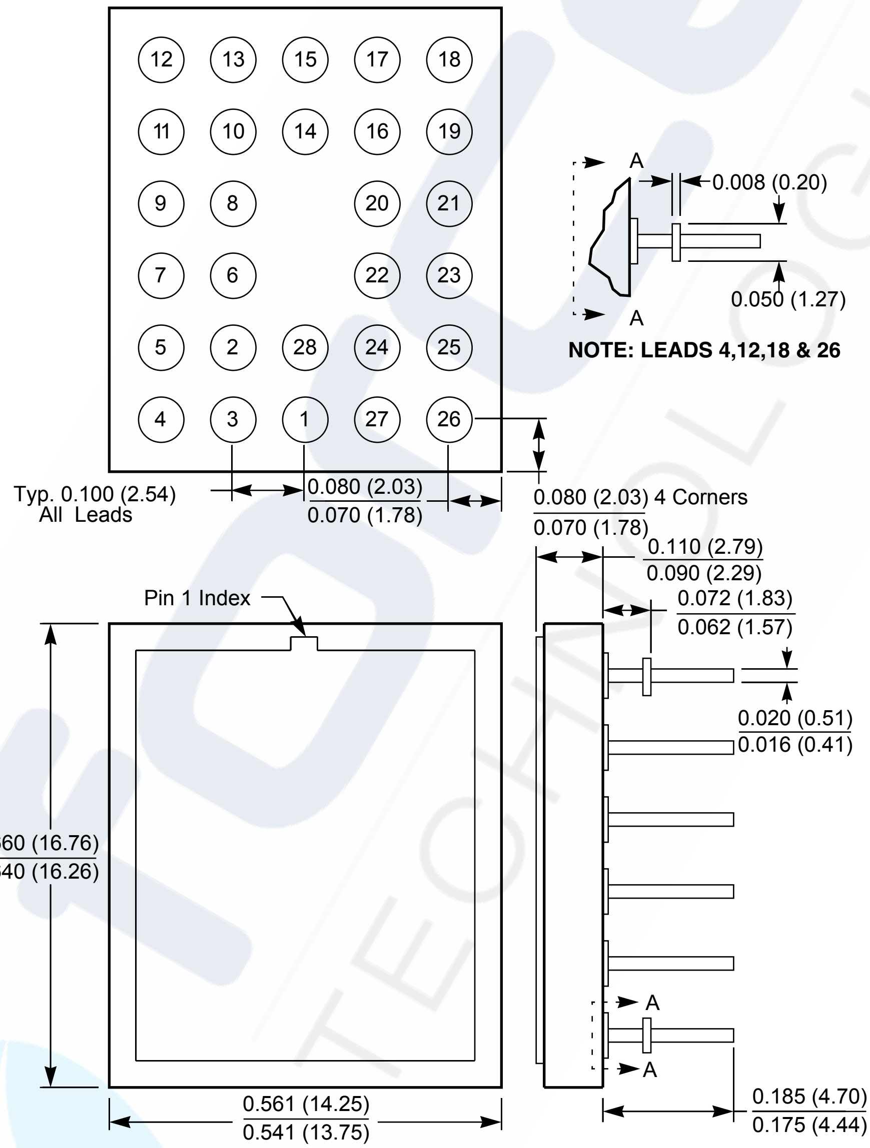
28-Lead Ceramic Flat Pack Type F



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

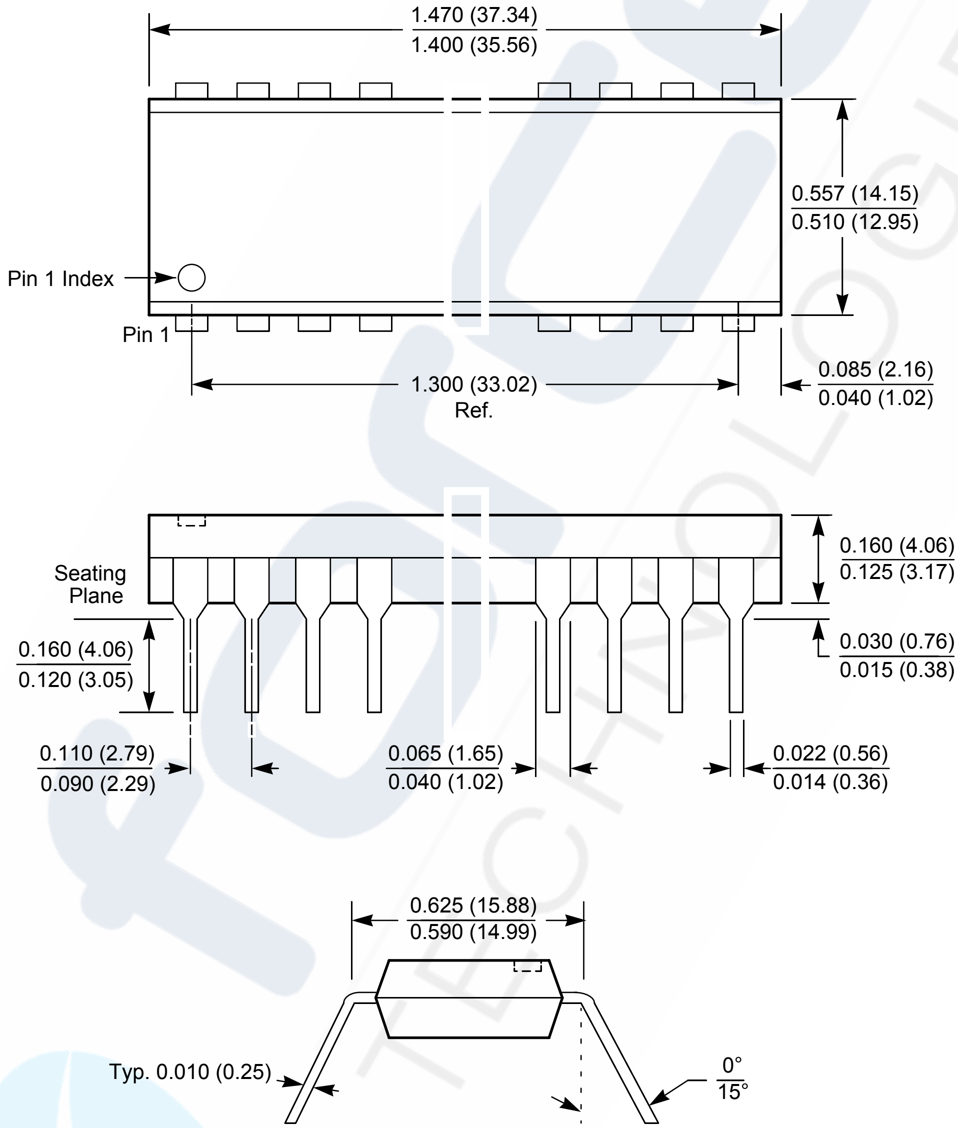
28-Lead Ceramic Pin Grid Array Package Type K



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

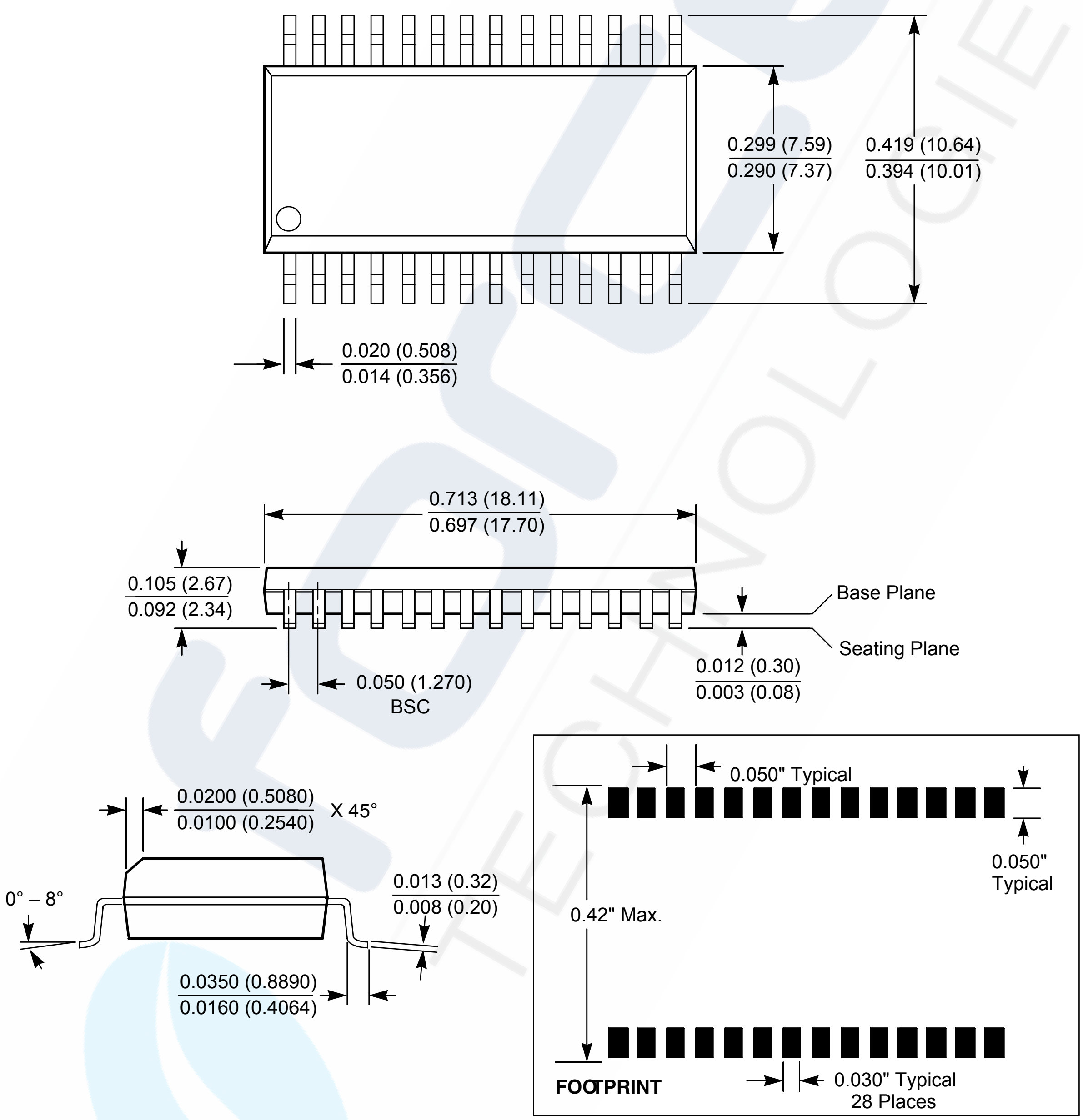
28-Lead Plastic Dual In-Line Package Type P



NOTE:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

PACKAGING INFORMATION

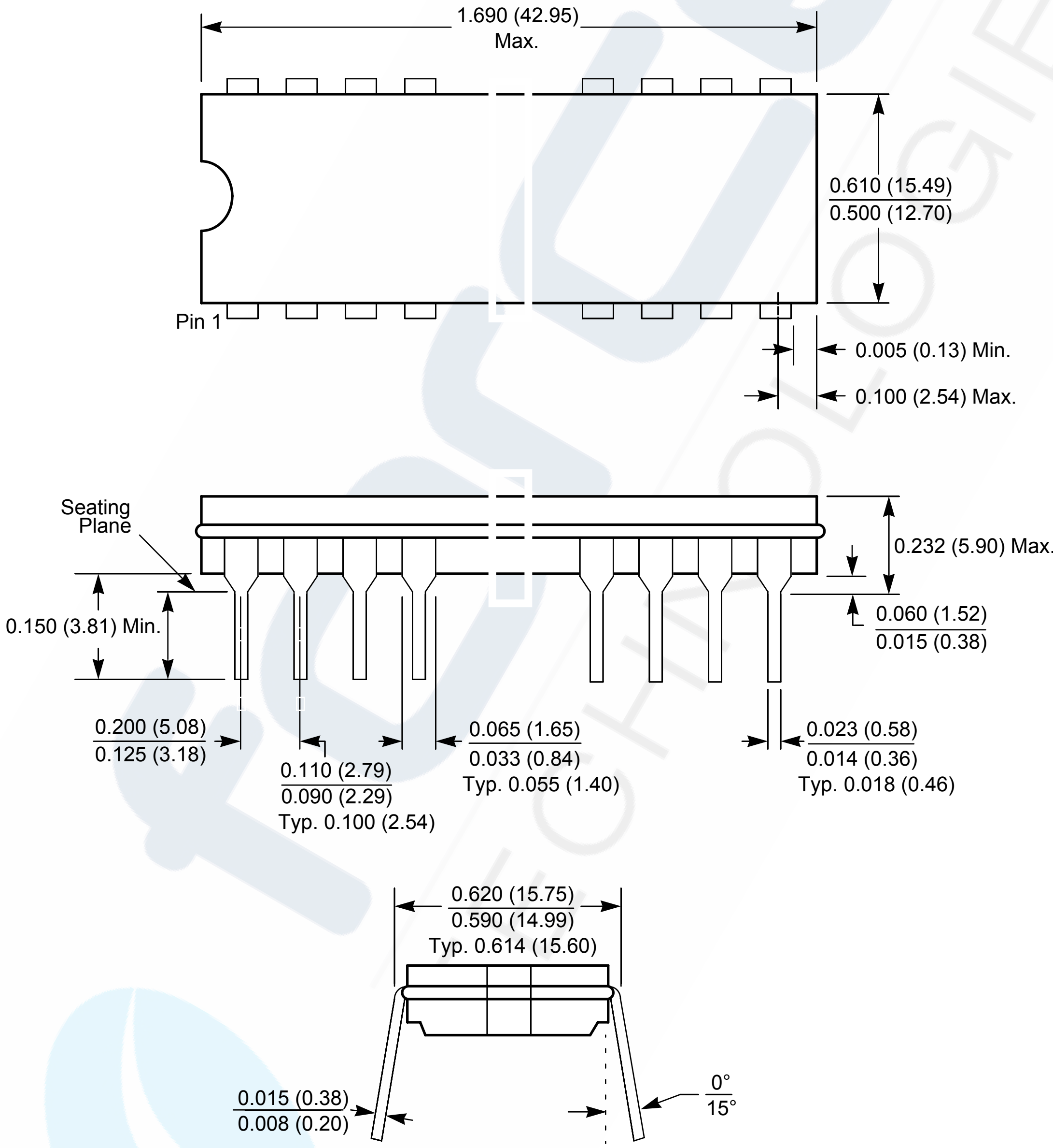
28-Lead Plastic Small Outline Gull Wing Package Type S



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.004 INCHES

PACKAGING INFORMATIN

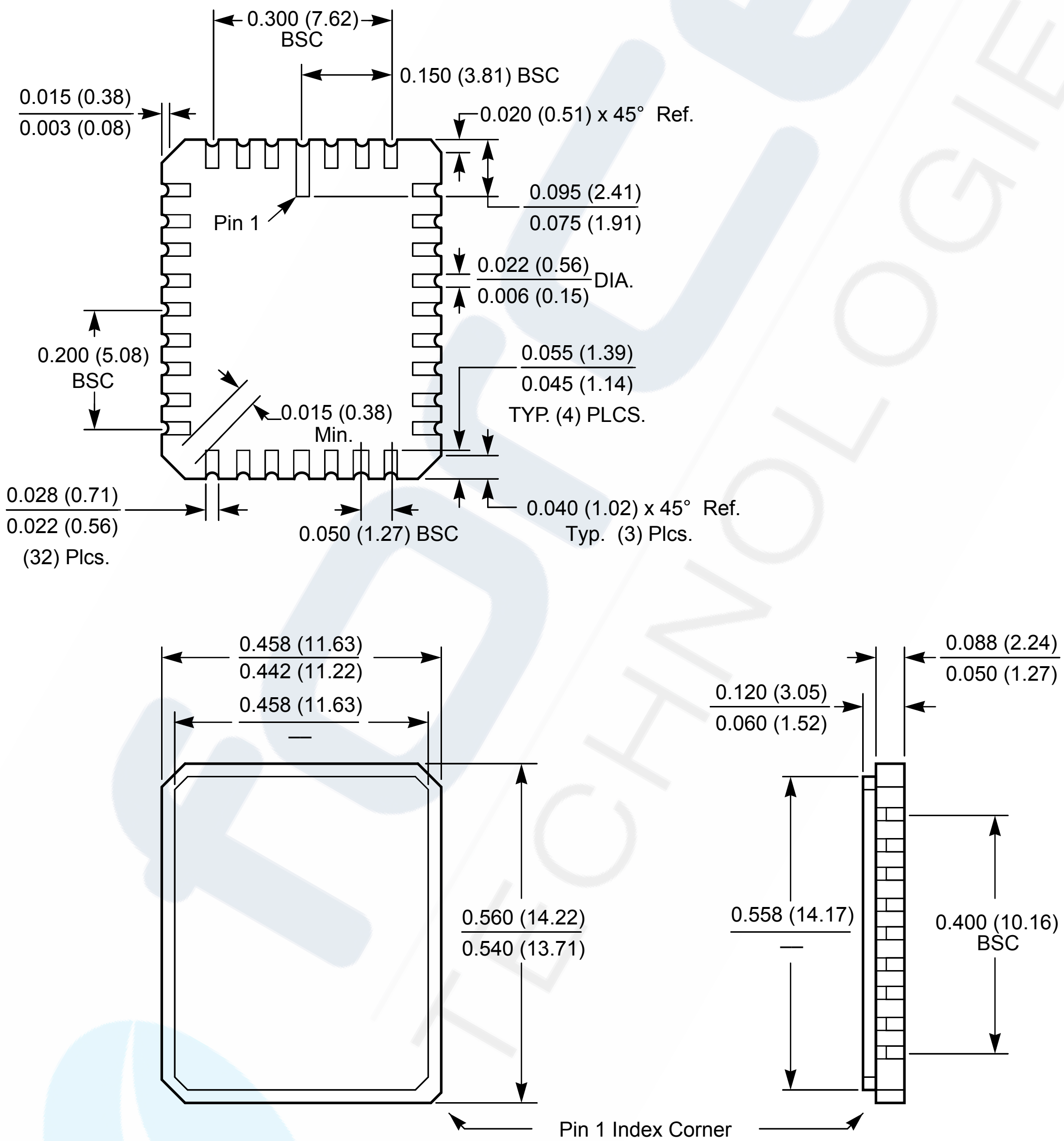
32-Lead Hermetic Dual In-Line Package Type D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

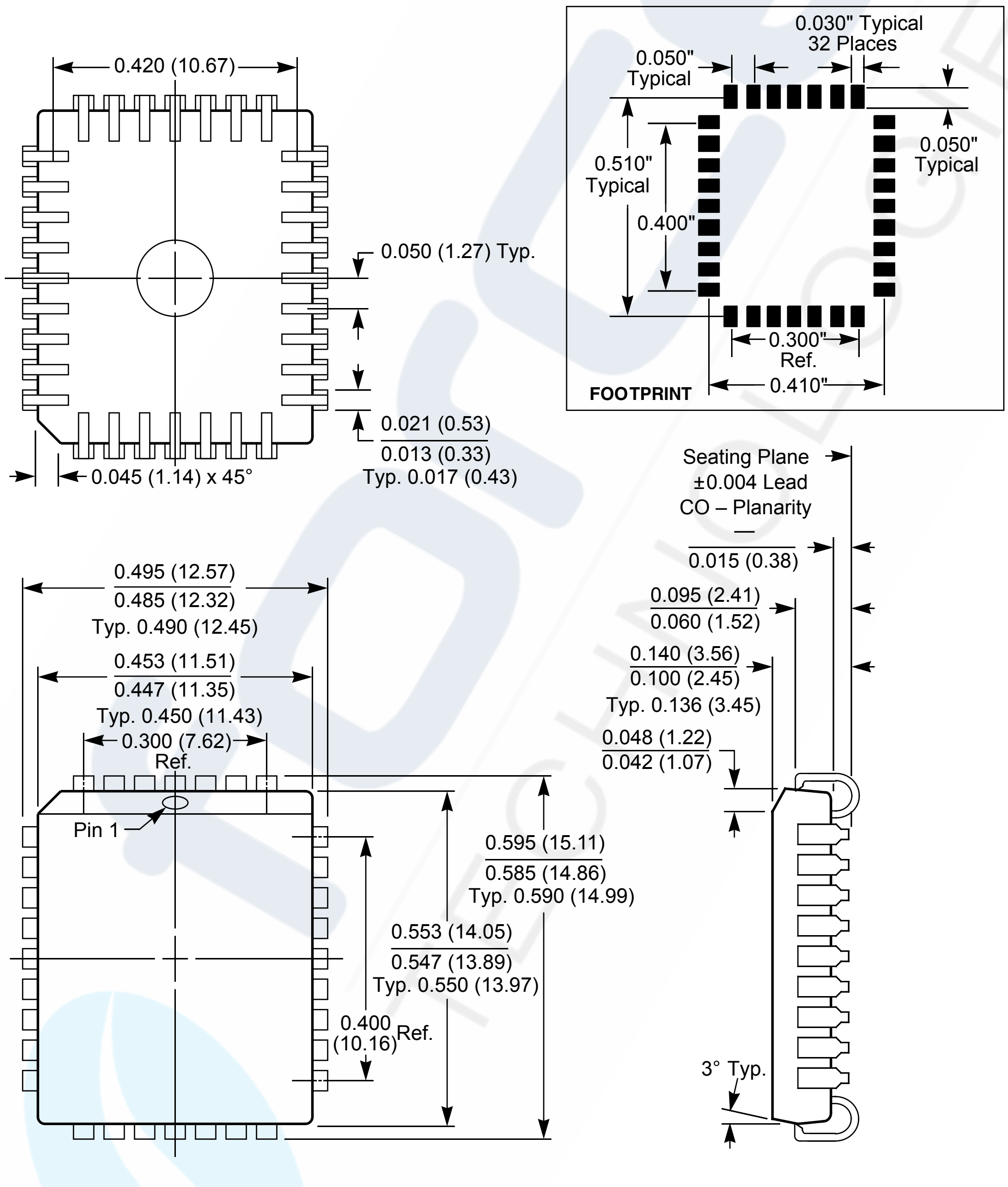
32-Pad Ceramic Leadless Chip Carrier Package Type E



NOTE:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **TOLERANCE: ±1% NLT ±0.005 (0.127)**

PACKAGING INFORMATION

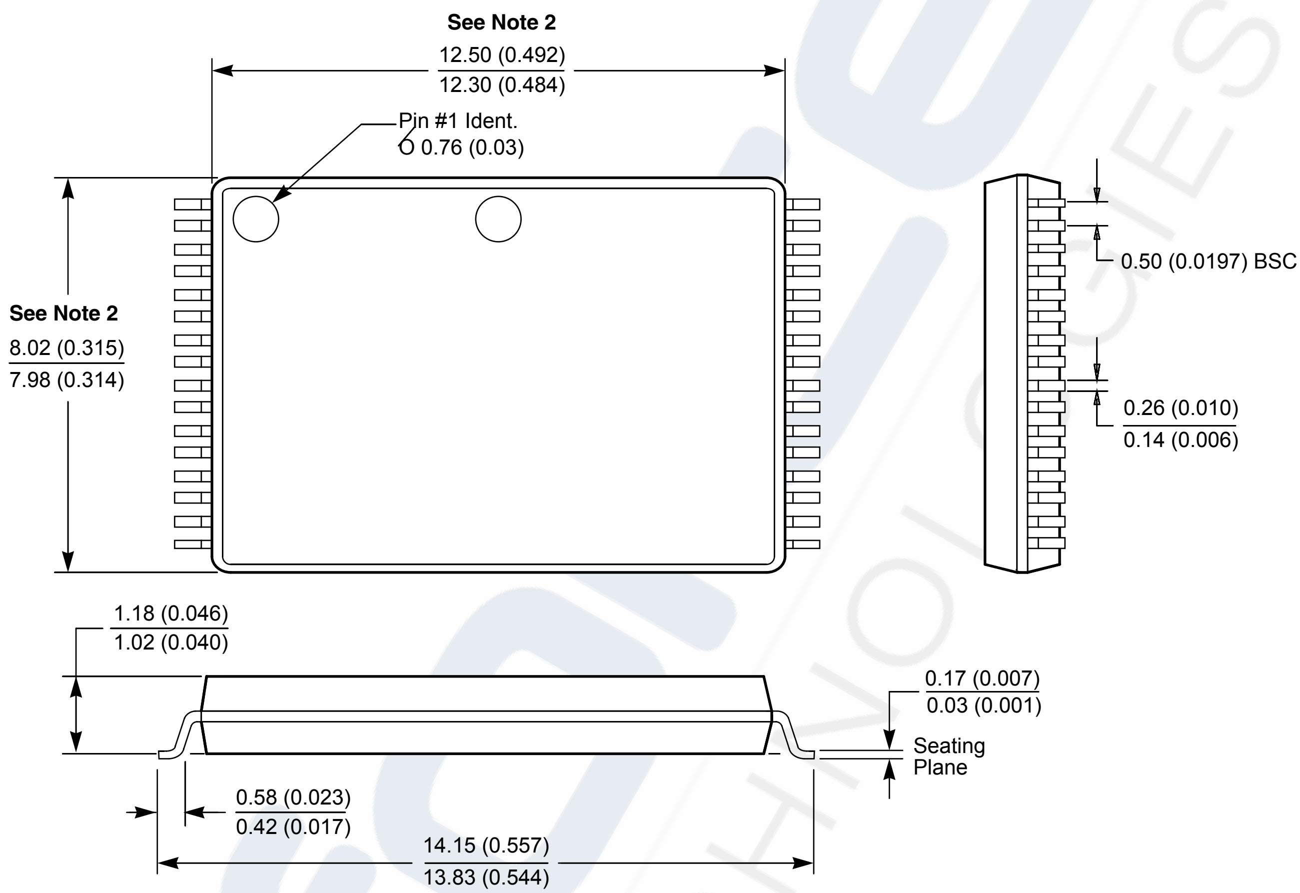
32-Lead Plastic Leaded Chip Carrier Package Type J

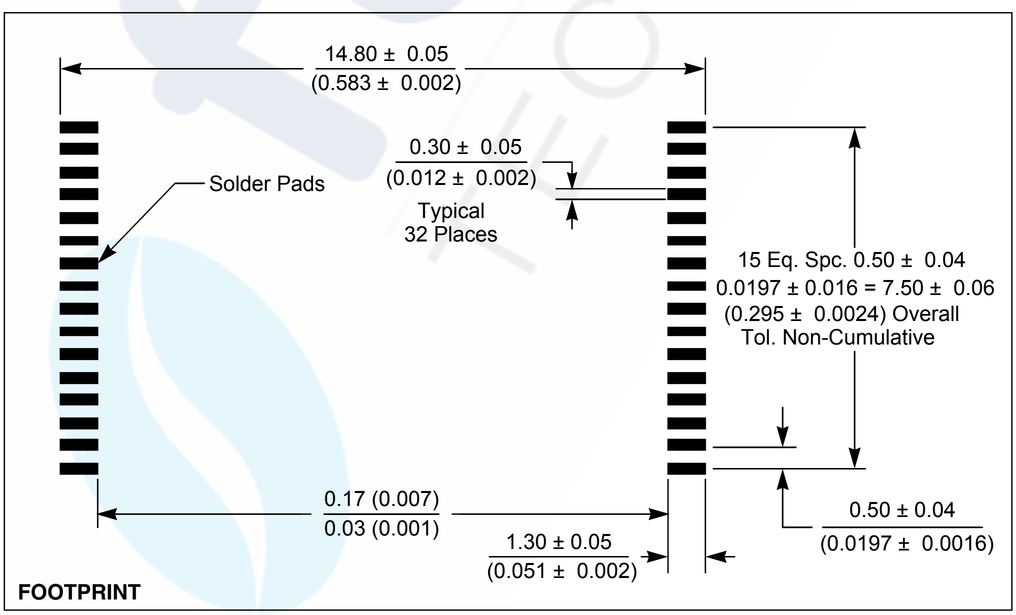


NOTES:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY**

PACKAGING INFORMATION

32-Lead Thin Small Outline Package (TSOP) Type T





NOTE:
1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES IN PARENTHESES).

FT28HC256 X X -X

Device — FT28HC256

Access Time
- –70 = 70ns
- –90 = 90ns
- –12 = 120ns
- –15 = 150ns

Temperature Range
- Blank = Commercial = 0°C to +70°C
- I = Industrial = –40°C to +85°C
- M = Military = –55°C to +125°C
- MB = MIL-STD-883 M5004

Package
- P = 28-Lead Plastic DIP
- D = 28-Lead CERDIP
- J = 32-Lead PLCC
- S = 28-Lead plastic SOIC
- E = 32-Pad LCC
- K = 28-Pin grid array
- F = 28-Lead flat pack
- T = 32-Lead TSOP