

LPM3401 - -20V/4.2A

P-Channel Enhancement Mode Field Effect Transistor

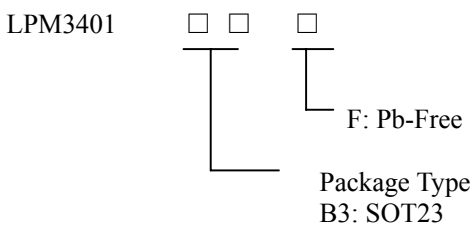
General Description

The LPM3401 is the P-channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

Ordering Information



Features

- -20V/-4.2A, $R_{DC(ON)} \leq 54m\Omega$ (typ.)@ $V_{GS} = -2.5V$
- -20V/-3.0A, $R_{DC(ON)} \leq 60m\Omega$ (typ.)@ $V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DC(ON)}$
- SOT23 Package

Applications

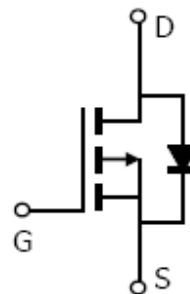
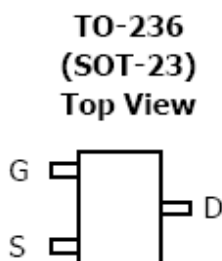
- ◇ Portable Media Players
- ◇ Cellular and Smart mobile phone
- ◇ LCD
- ◇ DSC Sensor
- ◇ Wireless Card

Marking Information

Device	Marking	Package	Shipping
LPM3401B3F	A1XXX	SOT23-3	3K/REEL

XXX : The production cycle and the batch.

Pin Configurations



SOT23L(Top View)

Functional Pin Description

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 8	V
Continuous Drain Current ^A	$T_A=25^\circ\text{C}$	-4.0	A
	$T_A=70^\circ\text{C}$	-3.5	
Pulsed Drain Current ^B	I_{DM}	-30	
Power Dissipation ^A	$T_A=25^\circ\text{C}$	1.4	W
	$T_A=70^\circ\text{C}$	0.9	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-16V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±4.5V			±1	μA
		V _{DS} =0V, V _{GS} =±8V			±10	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-0.3	-0.55	-1	
I _{D(ON)}	On state drain current	V _{GS} =-4.5V, V _{DS} =-5V	-25			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-4.5V, I _D =-4A T _J =125°C		35 48	43 60	mΩ
		V _{GS} =-2.5V, I _D =-4A		45	54	mΩ
		V _{GS} =-1.8V, I _D =-2A		56	73	mΩ
		V _{GS} =-1.5V, I _D =-1A		70		mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-4A	8	16		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.78	-1	V
I _S	Maximum Body-Diode Continuous Current				-2.2	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-10V, f=1MHz		1450		pF
C _{oss}	Output Capacitance		205		pF	
C _{rss}	Reverse Transfer Capacitance		160		pF	
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		6.5		Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =-4.5V, V _{DS} =-10V, I _D =-4A		17.2		nC
Q _{gs}	Gate Source Charge		1.3		nC	
Q _{gd}	Gate Drain Charge		4.5		nC	
t _{D(on)}	Turn-On DelayTime	V _{GS} =-4.5V, V _{DS} =-10V, R _L =2.5Ω, R _{GEN} =3Ω		9.5		ns
t _r	Turn-On Rise Time		17		ns	
t _{D(off)}	Turn-Off DelayTime		94		ns	
t _f	Turn-Off Fall Time		35		ns	
t _{rr}	Body Diode Reverse Recovery Time	I _F =-4A, dI/dt=100A/μs		31		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-4A, dI/dt=100A/μs		13.8		nC

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

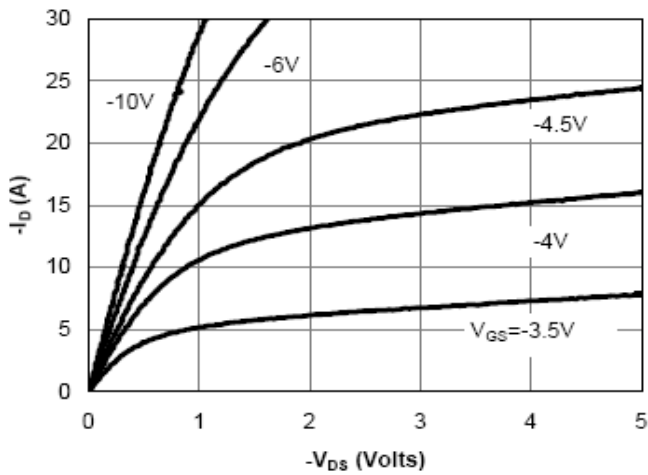


Fig 1: On-Region Characteristics (Note E)

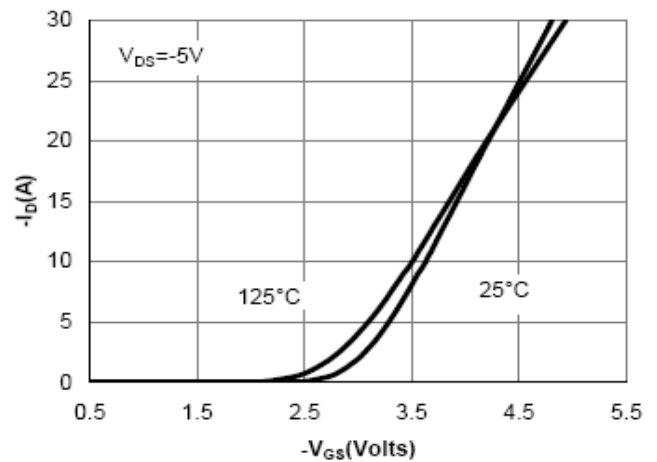


Figure 2: Transfer Characteristics (Note E)

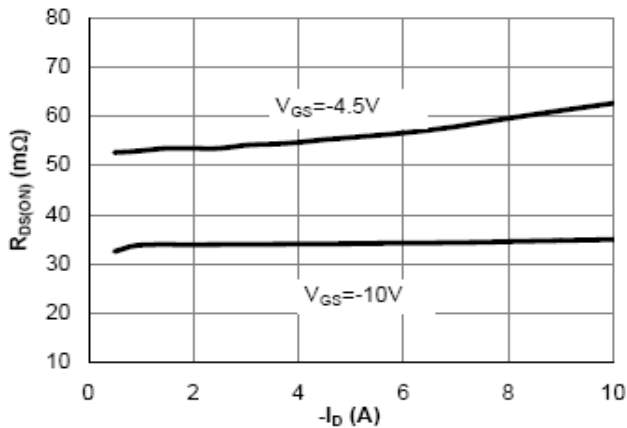


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

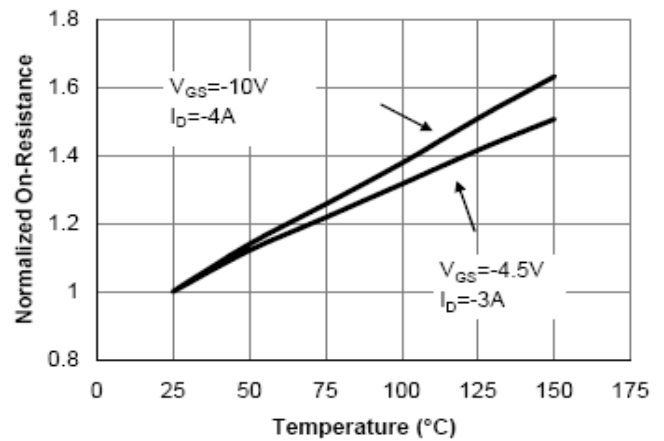


Figure 4: On-Resistance vs. Junction Temperature (Note E)

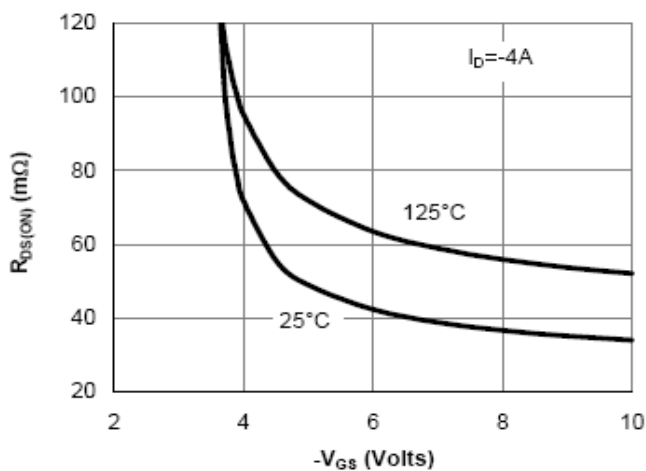


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

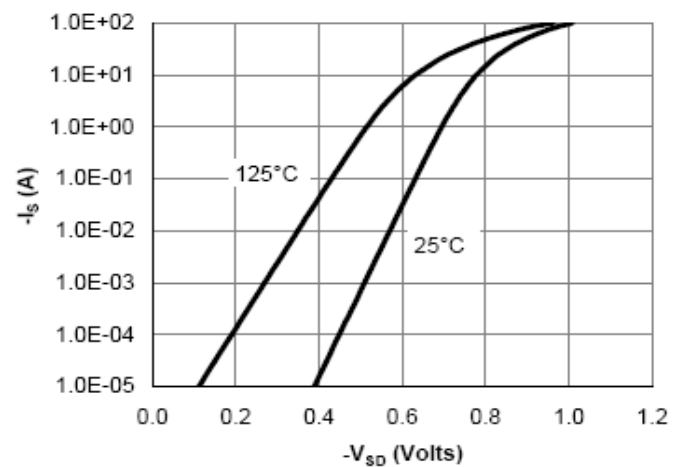


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

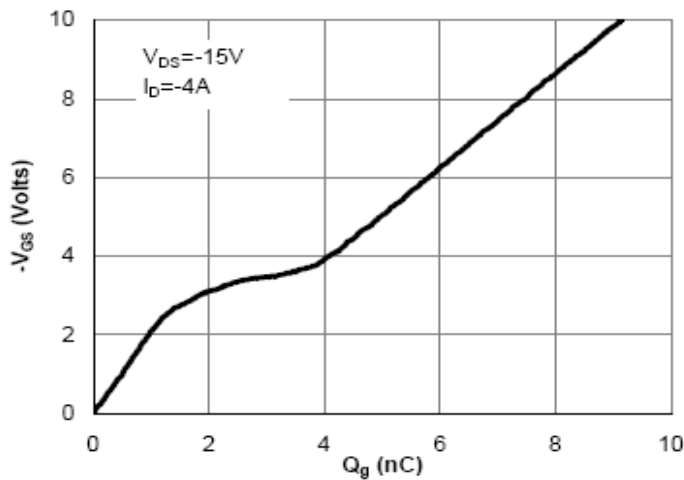


Figure 7: Gate-Charge Characteristics

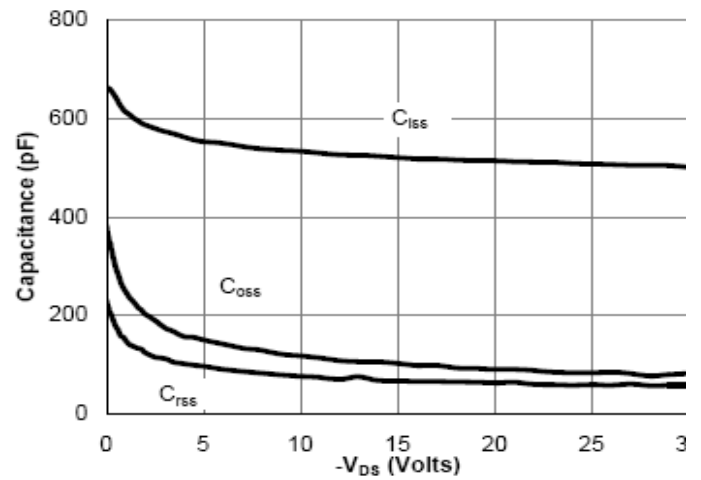


Figure 8: Capacitance Characteristics

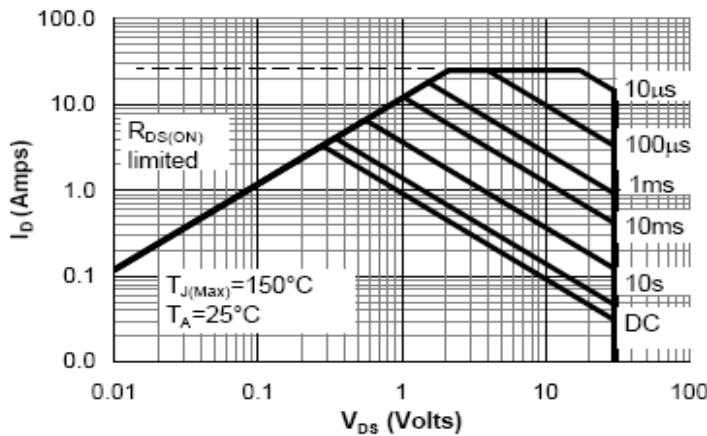


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

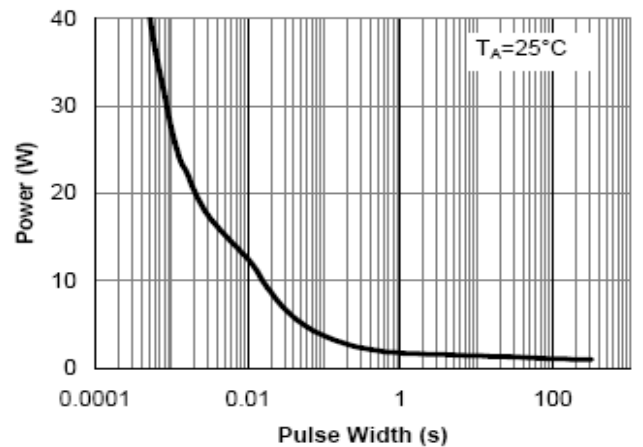


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

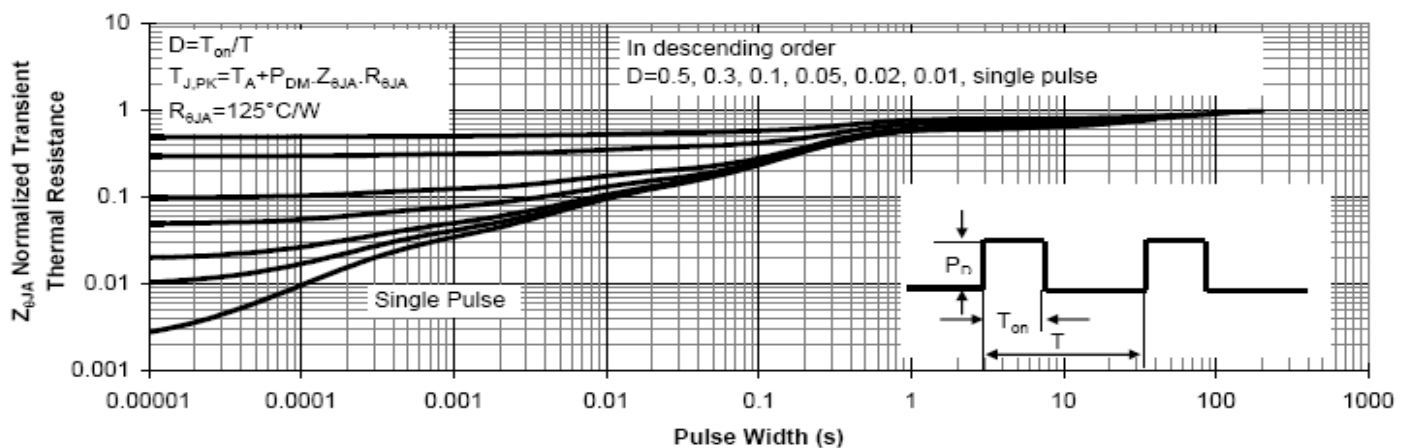
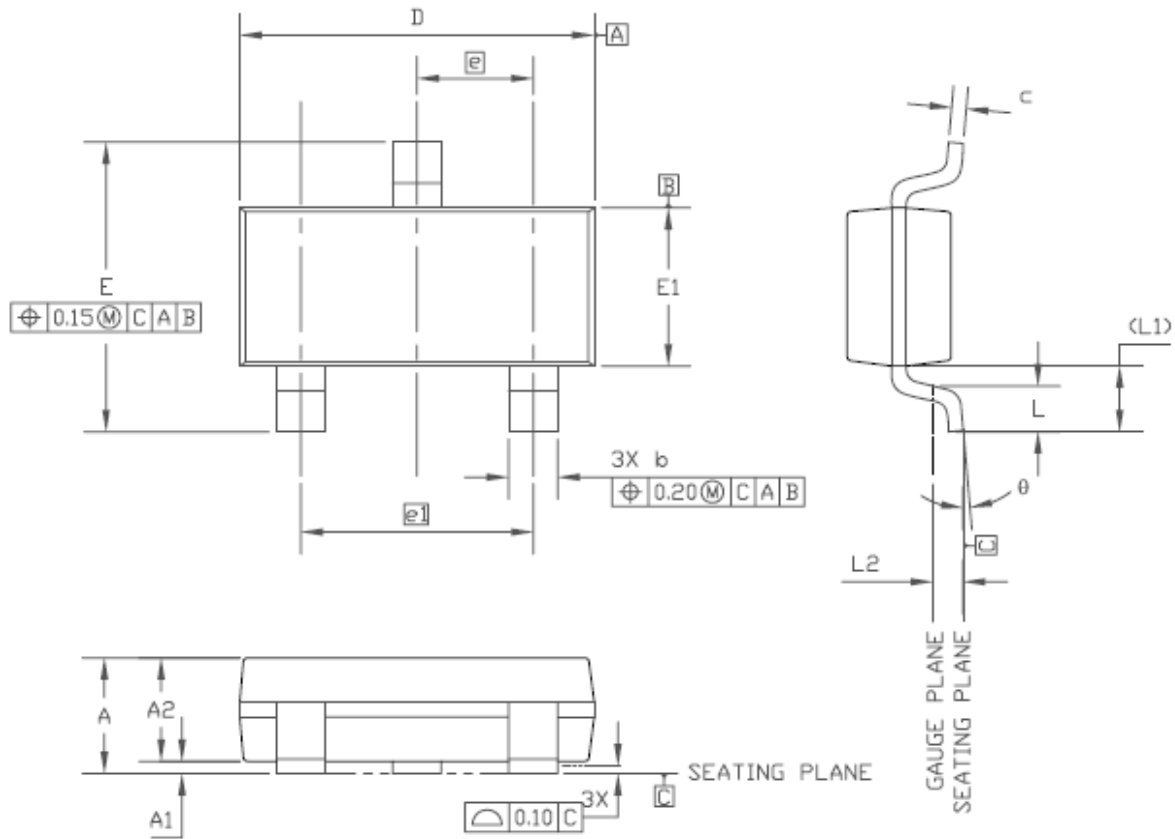


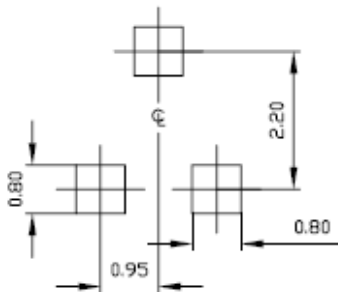
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Packaging Information

SOT-23 STANDARD PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	1.17	0.030	—	0.046
A1	0.05	—	0.15	0.002	—	0.006
A2	0.70	0.85	1.02	0.028	0.033	0.040
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.20	0.003	—	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	2.10	—	2.64	0.083	—	0.104
E1	1.20	1.30	1.40	0.047	0.051	0.055
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.54 REF			0.021 REF		
L2	0.25			0.010		
θ1	0°	—	8°	0°	—	8°