16-Channel, 1 MSPS, 12-Bit ADC with Sequencer in 28-Lead TSSOP

Data Sheet

AD7490-EP

FEATURES

- Fast throughput rate: 1 MSPS
- Specified for V_{DD} of 4.75 V to 5.25 V
- Low power at maximum throughput rates
  - 12.5 mW maximum at 1 MSPS with 5 V supplies
- 16 (single-ended) inputs with sequencer
- Wide input bandwidth
  - 69.5 dB SNR at 50 kHz input frequency
- Flexible power/serial clock speed management
- No pipeline delays
- High speed serial interface, SPI/QSPI™/MICROWIRE™/ DSP compatible
- Full shutdown mode: 0.5 µA maximum
- 28-lead TSSOP package
- Support defense and aerospace applications (AQEC)
- Military temperature range (−55°C to +125°C)
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

FUNCTIONAL BLOCK DIAGRAM

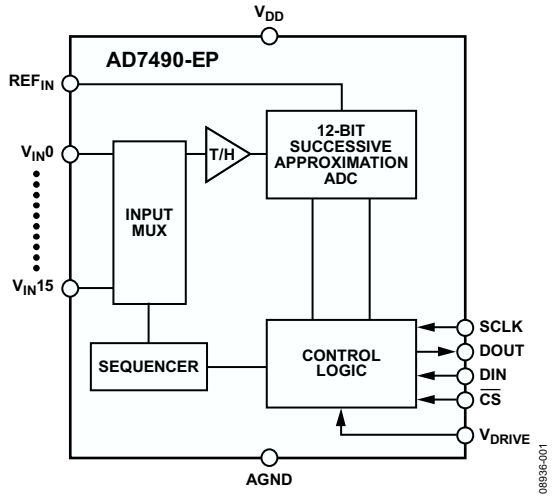

Figure 1.

GENERAL DESCRIPTION

The AD7490-EP is a 12-bit high speed, low power, 16-channel, successive approximation ADC. The part operates from a single 4.75 V to 5.25 V power supply and features throughput rates up to 1 MSPS. The part contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 1 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock signal, allowing the device to easily interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$, and conversion is also initiated at this point. There are no pipeline delays associated with the part.

The AD7490-EP uses advanced design techniques to achieve very low power dissipation at high throughput rates. For maximum throughput rates, the AD7490-EP consumes just 2.5 mA with 5 V supplies.

By setting the relevant bits in the control register, the analog input range for the part can be selected to be a 0 V to REF_{IN} input or a 0 V to 2 × REF_{IN} input, with either straight binary or twos complement output coding. The AD7490-EP features 16 single-ended analog inputs with a channel sequencer to allow a preprogrammed selection of channels to be converted sequentially. The conversion time is determined by the SCLK frequency because this is also used as the master clock to control the conversion.

The AD7490-EP is available in a 28-lead TSSOP package.

Full details about this enhanced product are available in the AD7490 data sheet, which should be consulted in conjunction with this data sheet.

PRODUCT HIGHLIGHTS

1. The AD7490-EP offers up to 1 MSPS throughput rates.
2. A sequence of channels can be selected, through which the AD7490-EP cycles and converts.
3. The AD7490-EP operates from a single 4.75 V to 5.25 V supply. The V_{DRIVE} function allows the serial interface to connect directly to either 3 V or 5 V processor systems independent of V_{DD}.
4. The conversion rate is determined by the serial clock, allowing the conversion time to be reduced through the serial clock speed increase. The part also features various shutdown modes to maximize power efficiency at lower throughput rates. Power consumption is 0.5 µA, maximum, when in full shutdown.
5. The part features a standard successive approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once off conversion control.

Rev. A Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

9/12—Rev. 0 to Rev. A

Changes to Ordering Guide 9

4/10—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 4.75 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V, REF_{IN} = 2.5 V, f_{SCLK}[1] = 20 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Temperature range (EP version): −55°C to +125°C.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE	f_{IN} = 50 kHz sine wave, f_{SCLK} = 20 MHz				
Signal-to-(Noise + Distortion) (SINAD)		69	70.5		dB
Signal-to-Noise Ratio (SNR)		69.5			dB
Total Harmonic Distortion (THD)			−84	−74	dB
Peak Harmonic or Spurious Noise (SFDR)			−86	−75	dB
Intermodulation Distortion (IMD)	fa = 40.1 kHz, fb = 41.5 kHz				
Second-Order Terms			−85		dB
Third-Order Terms			−85		dB
Aperture Delay			10		ns
Aperture Jitter			50		ps
Channel-to-Channel Isolation	f_{IN} = 400 kHz		−82		dB
Full Power Bandwidth	3 dB		8.2		MHz
	0.1 dB		1.6		MHz
DC ACCURACY					
Resolution		12			Bits
Integral Nonlinearity				±1	LSB
Differential Nonlinearity	Guaranteed no missed codes to 12 bits			−0.95/+1.5	LSB
0 V to REF_{IN} Input Range	Straight binary output coding				
Offset Error			±0.6	±8	LSB
Offset Error Match				±0.5	LSB
Gain Error				±2	LSB
Gain Error Match				±0.6	LSB
0 V to 2 × REF_{IN} Input Range	−REF_{IN} to +REF_{IN} biased about REF_{IN} with twos complement output coding offset				
Positive Gain Error				±2	LSB
Positive Gain Error Match				±0.5	LSB
Zero Code Error			±0.6	±8	LSB
Zero Code Error Match				±0.5	LSB
Negative Gain Error				±1	LSB
Negative Gain Error Match				±0.5	LSB
ANALOG INPUT					
Input Voltage Range	RANGE bit set to 1	0		REF_{IN}	V
	RANGE bit set to 0	0		2 × REF_{IN}	V
DC Leakage Current				±1	µA
Input Capacitance			20		pF
REFERENCE INPUT					
REF_{IN} Input Voltage	±1% specified performance		2.5		V
DC Leakage Current				±1	µA
REF_{IN} Input Impedance	f_{SAMPLE} = 1 MSPS		36		kΩ
LOGIC INPUTS					
Input High Voltage, V_{INH}		0.7 × V_{DRIVE}			V
Input Low Voltage, V_{INL}				0.3 × V_{DRIVE}	V
Input Current, I_{IN}	V_{IN} = 0 V or V_{DRIVE}		±0.01	±1	µA
Input Capacitance, C_{IN}+[2]				10	pF

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 200 µA	V_{DRIVE} − 0.2			V
Output Low Voltage, V_{OL}	I_{SINK} = 200 µA			0.4	V
Floating State Leakage Current	WEAK/$\overline{TRI}$ bit set to 0			±10	µA
Floating State Output Capacitance[2]	WEAK/$\overline{TRI}$ bit set to 0			10	pF
Output Coding	Coding bit set to 1		Straight (natural) binary		
	Coding bit set to 0		Twos complement		
CONVERSION RATE					
Conversion Time	16 SCLK cycles, SCLK = 20 MHz			800	ns
Track-and-Hold Acquisition Time	Sine wave input			300	ns
	Full-scale step input			300	ns
Throughput Rate				1	MSPS
POWER REQUIREMENTS					
V_{DD}		4.75		5.25	V
V_{DRIVE}		2.7		5.25	V
I_{DD}	Digital inputs = 0 V or V_{DRIVE}				
Normal Mode (Static)	SCLK on or off		600		µA
Normal Mode (Operational)	f_{SCLK} = 20 MHz			2.5	mA
(f_S = Maximum Throughput)					
Auto Standby Mode	f_{SAMPLE} = 500 kSPS		1.55		mA
	Static			100	µA
Auto Shutdown Mode	f_{SAMPLE} = 250 kSPS		960		µA
	Static			0.5	µA
Full Shutdown Mode	SCLK on or off		0.02	0.5	µA
Power Dissipation					
Normal Mode (Operational)	f_{SCLK} = 20 MHz			12.5	mW
Auto Standby Mode (Static)				460	µW
Auto Shutdown Mode (Static)				2.5	µW
Full Shutdown Mode				2.5	µW

[1] Specifications apply for f_{SCLK} up to 20 MHz. However, for serial interfacing requirements, see the Timing Specifications section.
[2] Guaranteed by characterization.

TIMING SPECIFICATIONS

V_{DD} = 4.75 V to 5.25 V, $V_{DRIVE} \leq V_{DD}$, REF_{IN} = 2.5 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2. Timing Specifications[1]

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCLK}[2]	10	kHz min	
	20	MHz max	
$t_{CONVERT}$	$16 \times t_{SCLK}$		
t_{QUIET}	50	ns min	Minimum quiet time required between bus relinquish and start of next conversion
t_2	10	ns min	$\overline{CS}$ to SCLK setup time
t_3[3]	14	ns max	Delay from $\overline{CS}$ until DOUT three-state disabled
t_3b[4]	20	ns max	Delay from $\overline{CS}$ to DOUT valid
t_4[3]	40	ns max	Data access time after SCLK falling edge
t_5	$0.4 \times t_{SCLK}$	ns min	SCLK low pulse width
t_6	$0.4 \times t_{SCLK}$	ns min	SCLK high pulse width
t_7	15	ns min	SCLK to DOUT valid hold time
t_8[5]	15/50	ns min/max	SCLK falling edge to DOUT high impedance
t_9	20	ns min	DIN setup time prior to SCLK falling edge
t_{10}	5	ns min	DIN hold time after SCLK falling edge
t_{11}	20	ns min	16th SCLK falling edge to $\overline{CS}$ high
t_{12}	1	µs max	Power-up time from full power-down/auto shutdown/auto standby modes

[1] Guaranteed by characterization. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V (see Figure 2).
[2] The mark/space ratio for the SCLK input is 40/60 to 60/40.
[3] Measured with the load circuit of Figure 2 and defined as the time required for the output to cross 0.4 V or 0.7 V_{DRIVE}.
[4] t_3b represents a worst-case figure for having ADD3 available on the DOUT line, that is, if the AD7490-EP goes back into three-state at the end of a conversion and some other device takes control of the bus between conversions, the user has to wait a maximum time of t_3b before having ADD3 valid on the DOUT line. If the DOUT line is weakly driven to ADD3 between conversions, the user typically has to wait 12 ns at 5 V after the $\overline{CS}$ falling edge before seeing ADD3 valid on DOUT.
[5] t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 25 pF capacitor. This means that the time, t_8, quoted in the timing characteristics, is the true bus relinquish time of the part and is independent of the bus loading.

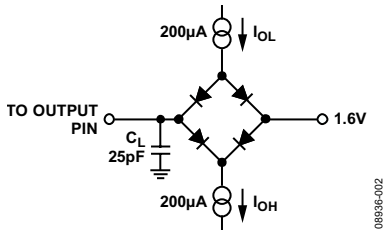

Figure 2. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
V_{DRIVE} to GND	−0.3 V to V_{DD} + 0.3 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
REF_{IN} to GND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Ranges	
Enhanced Plastic (EP Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	97.9°C/W (TSSOP)
θ_{JC} Thermal Impedance	14°C/W (TSSOP)
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	1 kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

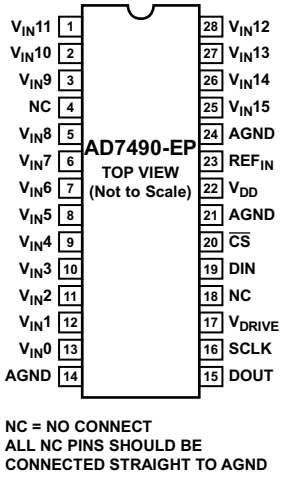

Figure 3. 28-Lead TSSOP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
20	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7490-EP and also frames the serial data transfer.
23	REF_{IN}	Reference Input for the AD7490-EP. An external reference must be applied to this input. The voltage range for the external reference is 2.5 V ± 1% for specified performance.
22	V_{DD}	Power Supply Input. The V_{DD} range for the AD7490-EP is from 2.7 V to 5.25 V. For the 0 V to 2 × REF_{IN} range, V_{DD} should be from 4.75 V to 5.25 V.
14, 21, 24	AGND	Analog Ground. Ground reference point for all circuitry on the AD7490-EP. All analog/digital input signals and any external reference signal should be referred to this AGND voltage. All AGND pins should be connected together.
13 to 5, 3 to 1, 28 to 25	$V_{IN}0$ to $V_{IN}15$	Analog Input 0 through Analog Input 15. Sixteen single-ended analog input channels that are multiplexed into the on chip track-and-hold. The analog input channel to be converted is selected by using the address bits ADD3 through ADD0 of the control register. The address bits, in conjunction with the SEQ and SHADOW bits, allow the sequence register to be programmed. The input range for all input channels can extend from 0 V to REF_{IN} or 0 V to 2 × REF_{IN} as selected via the RANGE bit in the control register. Any unused input channels should be connected to AGND to avoid noise pickup.
19	DIN	Data In. Logic input. Data to be written to the control register of the AD7490-EP is provided on this input and is clocked into the register on the falling edge of SCLK (see the AD7490 data sheet).
15	DOUT	Data Out. Logic output. The conversion result from the AD7490-EP is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream consists of four address bits indicating which channel the conversion result corresponds to, followed by the 12 bits of conversion data, which is provided by MSB first. The output coding can be selected as straight binary or twos complement via the CODING bit in the control register.
16	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the conversion process of the AD7490-EP.
17	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the serial interface of the AD7490-EP operates.

TYPICAL PERFORMANCE CHARACTERISTICS

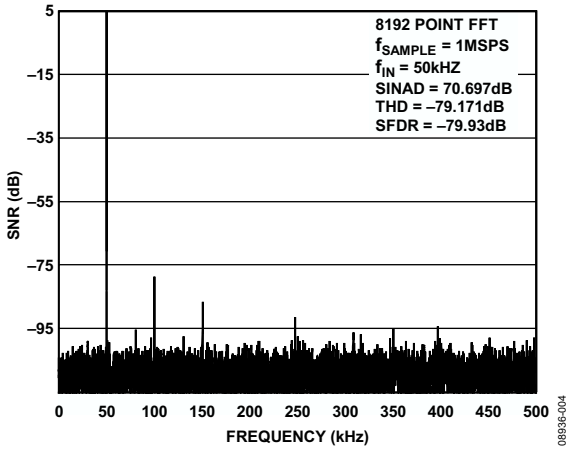

Figure 4. Dynamic Performance at 1 MSPS

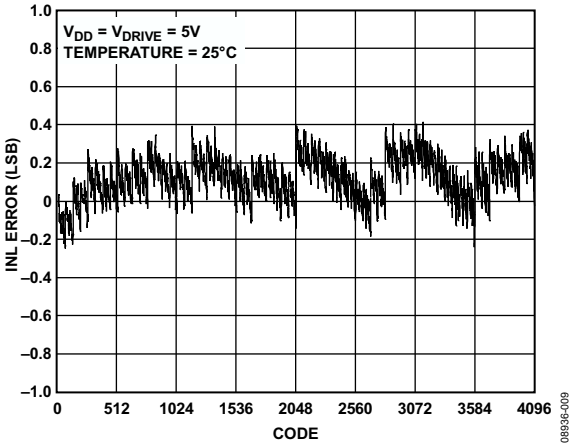

Figure 6. Typical INL

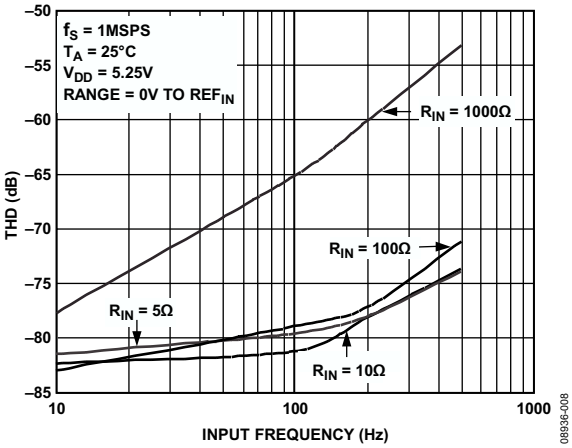

Figure 5. THD vs. Analog Input Frequency for Various Analog Source Impedances

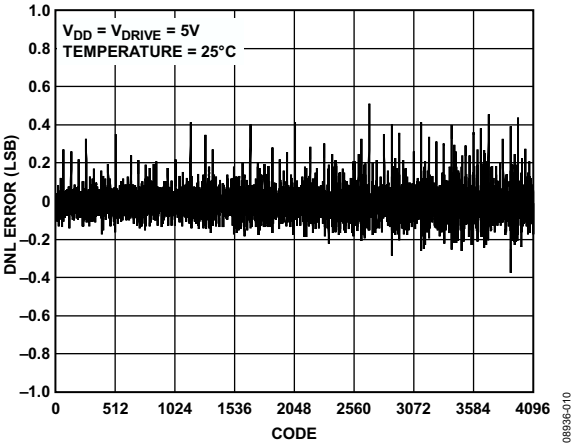

Figure 7. Typical DNL

OUTLINE DIMENSIONS

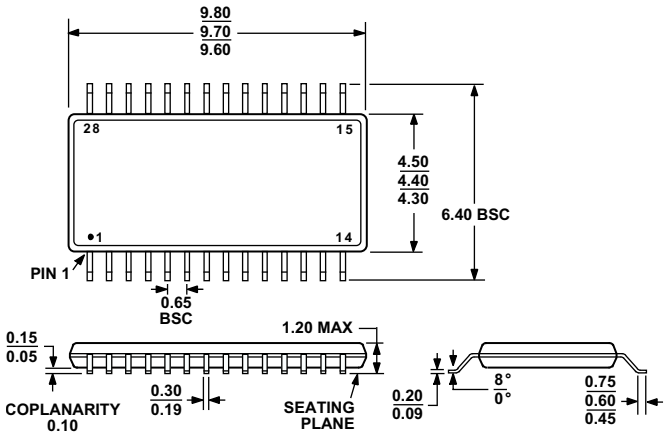

Figure 8. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Integral Linearity Error (LSB)	Package Description	Package Option
AD7490SRU-EP-RL7	−55°C to +125°C	±1	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28

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