



# CLC1005, CLC1015, CLC2005

Low Cost, +2.7V to 5.5V, 260MHz  
Rail-to-Rail Amplifiers

## General Description

The CLC1005 (single), CLC1015 (single with disable), and CLC2005 (dual) are low cost, voltage feedback amplifiers. These amplifiers are designed to operate on +2.7V to +5V, or  $\pm 2.5V$  supplies. The input voltage range extends 300mV below the negative rail and 1.2V below the positive rail.

The CLC1005, CLC1015, and CLC2005 offer superior dynamic performance with 260MHz small signal bandwidth and 145V/ $\mu$ s slew rate. The amplifiers consume only 4.2mA of supply current per channel and the CLC1015 offers a disable supply current of only 127 $\mu$ A. The combination of low power, high output current drive, and rail-to-rail performance make these amplifiers well suited for battery-powered communication/computing systems.

The combination of low cost and high performance make the CLC1005, CLC1015, and CLC2005 suitable for high volume applications in both consumer and industrial applications such as interactive whiteboards, wireless phones, scanners, color copiers, and video transmission.

## FEATURES

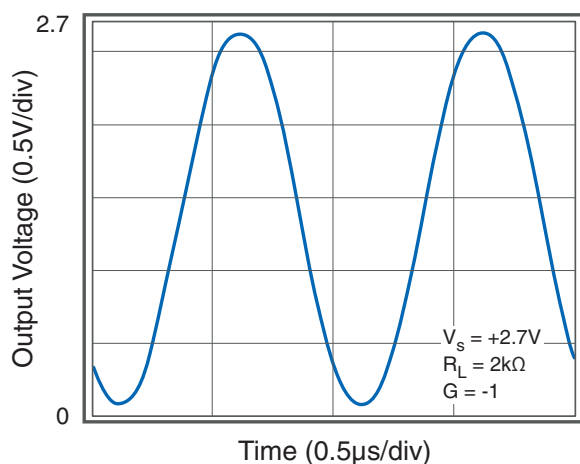
- 260MHz bandwidth
- Fully specified at +2.7V and +5V supplies
- Output voltage range:
  - 0.036V to 4.953V;  $V_S = +5$ ;  $R_L = 2k\Omega$
- Input voltage range:
  - -0.3V to +3.8V;  $V_S = +5$
- 145V/ $\mu$ s slew rate
- 4.2mA supply current
- Power down to 127 $\mu$ A
- $\pm 55$ mA linear output current
- $\pm 85$ mA short circuit current
- CLC2005 directly replaces AD8052/42/92 in single supply applications
- CLC1005 directly replaces AD8051/41/91 in single supply applications

## APPLICATIONS

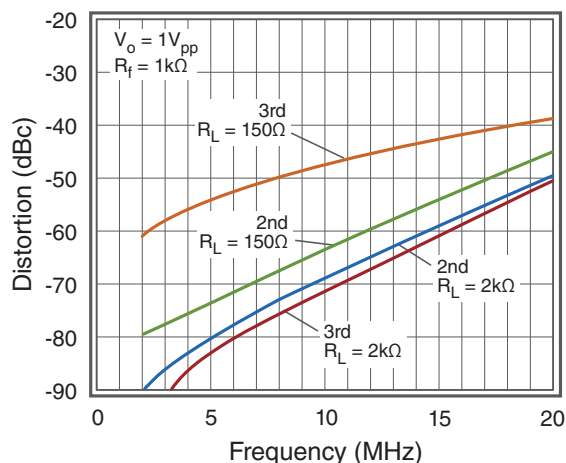
- A/D driver
- Active filters
- CCD imaging systems
- CD/DVD ROM
- Coaxial cable drivers
- High capacitive load driver
- Portable/battery-powered applications
- Twisted pair driver
- Telecom and optical terminals
- Video driver
- Interactive whiteboards

Ordering Information - [backpage](#)

## Output Swing



## 2nd & 3rd Harmonic Distortion; $V_S = +2.7V$



**Absolute Maximum Ratings**

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

V<sub>S</sub> ..... 0V to +6V  
V<sub>IN</sub> ..... -V<sub>S</sub> - 0.5V to +V<sub>S</sub> +0.5V

**Operating Conditions**

Supply Voltage Range .....2.5 to 5.5V  
Operating Temperature Range .....-40°C to 85°C  
Junction Temperature ..... 150°C  
Storage Temperature Range.....-65°C to 150°C  
Lead Temperature (Soldering, 10s) .....260°C

**Package Thermal Resistance**

θ<sub>JA</sub> (SOIC-8) .....150°C/W  
θ<sub>JA</sub> (MSOP-8) ..... 200°C/W  
θ<sub>JA</sub> (TSOT23-5) .....215°C/W  
θ<sub>JA</sub> (TSOT23-6) .....192°C/W  
Package thermal resistance (θ<sub>JA</sub>), JEDEC standard, multi-layer test boards, still air.

**ESD Protection**

SOIC-8 (HBM) .....2.5kV  
ESD Rating for HBM (Human Body Model) and CDM (Charged Device Model).

### Electrical Characteristics at +2.7V

$T_A = 25^\circ\text{C}$ ,  $V_S = +2.7\text{V}$ ,  $R_f = 2\text{k}\Omega$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ;  $G = 2$ ; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
GBWP	-3dB Gain Bandwidth Product			86		MHz
UGBW	Unity Gain Bandwidth <sup>(1)</sup>	$G = +1$ , $V_{OUT} = 0.05V_{pp}$		215		MHz
BW <sub>SS</sub>	-3dB Bandwidth	$G = +2$ , $V_{OUT} = 0.2V_{pp}$		85		MHz
BW <sub>LS</sub>	Large Signal Bandwidth	$G = +2$ , $V_{OUT} = 2V_{pp}$		36		MHz
Time Domain						
$t_R$ , $t_F$	Rise and Fall Time <sup>(1)</sup>	$V_{OUT} = 0.2\text{V}$ step; (10% to 90%)		3.7		ns
$t_S$	Settling Time to 0.1%	$V_{OUT} = 1\text{V}$ step		40		ns
OS	Overshoot	$V_{OUT} = 0.2\text{V}$ step		9		%
SR	Slew Rate	$G = -1$ , $2.7\text{V}$ step		130		V/ $\mu\text{s}$
Distortion/Noise Response						
HD2	2nd Harmonic Distortion <sup>(1)</sup>	5MHz, $V_{OUT} = 1V_{pp}$		79		dBc
HD3	3rd Harmonic Distortion <sup>(1)</sup>	5MHz, $V_{OUT} = 1V_{pp}$		82		dBc
THD	Total Harmonic Distortion <sup>(1)</sup>	5MHz, $V_{OUT} = 1V_{pp}$		77		dB
$e_n$	Input Voltage Noise	>1MHz		16		nV/ $\sqrt{\text{Hz}}$
$i_n$	Input Current Noise	>1MHz		1.3		pA/ $\sqrt{\text{Hz}}$
X <sub>TALK</sub>	Crosstalk <sup>(1)</sup>	CLC2005, 10MHz		65		dB
DC Performance						
$V_{IO}$	Input Offset Voltage			-1.6		mV
$d_{VIO}$	Average Drift			10		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current			3		$\mu\text{A}$
$dI_B$	Average Drift			7		nA/ $^\circ\text{C}$
$I_{OS}$	Input Offset Current			0.1		$\mu\text{A}$
PSRR	Power Supply Rejection Ratio	DC	52	57		dB
$A_{OL}$	Open Loop Gain			75		dB
$I_S$	Supply Current			3.9		mA
Disable Characteristics (CLC1015)						
$T_{ON}$	Turn On Time			150		ns
$T_{OFF}$	Turn Off Time			25		ns
OFF <sub>ISO</sub>	Off Isolation	5MHz, $R_L = 100\Omega$		75		dB
$I_{SD}$	Disable Supply Current	$\overline{DIS}$ tied to GND		58	100	$\mu\text{A}$
Input Characteristics						
$R_{IN}$	Input Resistance			4.3		M $\Omega$
$C_{IN}$	Input Capacitance			1.8		pF
CMIR	Common Mode Input Range			-0.3 to 1.5		V
CMRR	Common Mode Rejection Ratio	DC, $V_{CM} = 0$ to $V_S - 1.5\text{V}$		87		dB
Output Characteristics						
$V_{OUT}$	Output Swing	$R_L = 10\text{k}\Omega$ to $V_S/2$		0.023 to 2.66		V
		$R_L = 2\text{k}\Omega$ to $V_S/2$		0.025 to 2.653		V
		$R_L = 150\Omega$ to $V_S/2$		0.065 to 2.55		V
$I_{OUT}$	Output Current			$\pm 55$		mA
		-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$		$\pm 50$		mA
$I_{SC}$	Short Circuit Current	$V_{OUT} = V_S/2$		$\pm 85$		mA
$V_S$	Power Supply Operating Range		2.5	2.7	5.5	V

**Notes:**

1.  $R_f = 1\text{k}\Omega$  was used for optimal performance. (For  $G = +1$ ,  $R_f = 0$ )

**Electrical Characteristics at +5V**

$T_A = 25^\circ\text{C}$ ,  $V_S = +5\text{V}$ ,  $R_f = 2\text{k}\Omega$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ;  $G = 2$ ; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>Frequency Domain Response</b>						
GBWP	-3dB Gain Bandwidth Product			90		MHz
UGBW	Unity Gain Bandwidth <sup>(1)</sup>	$G = +1$ , $V_{OUT} = 0.05V_{pp}$		260		MHz
BW <sub>SS</sub>	-3dB Bandwidth	$G = +2$ , $V_{OUT} = 0.2V_{pp}$		90		MHz
BW <sub>LS</sub>	Large Signal Bandwidth	$G = +2$ , $V_{OUT} = 2V_{pp}$		40		MHz
<b>Time Domain</b>						
$t_R$ , $t_F$	Rise and Fall Time <sup>(1)</sup>	$V_{OUT} = 0.2\text{V}$ step		3.6		ns
$t_S$	Settling Time to 0.1%	$V_{OUT} = 2\text{V}$ step		40		ns
OS	Overshoot	$V_{OUT} = 0.2\text{V}$ step		7		%
SR	Slew Rate	$G = -1$ , 5V step		145		V/ $\mu\text{s}$
<b>Distortion/Noise Response</b>						
HD2	2nd Harmonic Distortion <sup>(1)</sup>	5MHz, $V_{OUT} = 2V_{pp}$		71		dBc
HD3	3rd Harmonic Distortion <sup>(1)</sup>	5MHz, $V_{OUT} = 2V_{pp}$		78		dBc
THD	Total Harmonic Distortion <sup>(1)</sup>	5MHz, $V_{OUT} = 2V_{pp}$		70		dB
DG	Differential Gain	NTSC (3.85MHz), AC-Coupled, $R_L = 150\Omega$		0.06		%
		NTSC (3.85MHz), DC-Coupled, $R_L = 150\Omega$		0.08		%
DP	Differential Phase	NTSC (3.85MHz), AC-Coupled, $R_L = 150\Omega$		0.07		$^\circ$
		NTSC (3.85MHz), DC-Coupled, $R_L = 150\Omega$		0.06		$^\circ$
$e_n$	Input Voltage Noise	>1MHz		16		nV/ $\sqrt{\text{Hz}}$
$i_n$	Input Current Noise	>1MHz		1.3		pA/ $\sqrt{\text{Hz}}$
$X_{TALK}$	Crosstalk <sup>(1)</sup>	CLC2005, 10MHz		62		dB
<b>DC Performance</b>						
$V_{IO}$	Input Offset Voltage		-8	1.4	8	mV
$d_{VIO}$	Average Drift			10		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current		-8	3	8	$\mu\text{A}$
$dI_B$	Average Drift			7		nA/ $^\circ\text{C}$
$I_{OS}$	Input Offset Current		-0.8	0.1	0.8	$\mu\text{A}$
PSRR	Power Supply Rejection Ratio	DC	52	57		dB
$A_{OL}$	Open Loop Gain		68	78		dB
$I_S$	Supply Current			4.2	5.2	mA
<b>Disable Characteristics (CLC1015)</b>						
$T_{ON}$	Turn On Time			150		ns
$T_{OFF}$	Turn Off Time			25		ns
OFF <sub>ISO</sub>	Off Isolation	5MHz, $R_L = 100\Omega$		75		dB
$I_{SD}$	Disable Supply Current	$\overline{DIS}$ tied to GND		127	170	$\mu\text{A}$
<b>Input Characteristics</b>						
$R_{IN}$	Input Resistance			4.3		M $\Omega$
$C_{IN}$	Input Capacitance			1.8		pF
CMIR	Common Mode Input Range			-0.3 to 3.8		V
CMRR	Common Mode Rejection Ratio	DC, $V_{CM} = 0$ to $V_S - 1.5\text{V}$	72	87		dB

**Electrical Characteristics at +5V Continued**

$T_A = 25^\circ\text{C}$ ,  $V_S = +5\text{V}$ ,  $R_f = 2\text{k}\Omega$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ;  $G = 2$ ; unless otherwise noted.

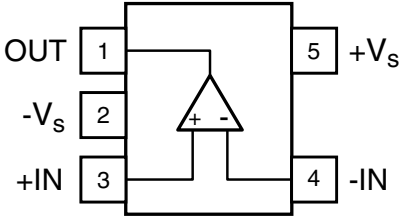
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Output Characteristics						
$V_{OUT}$	Output Swing	$R_L = 10\text{k}\Omega$ to $V_S / 2$		0.027 to 4.97		V
		$R_L = 2\text{k}\Omega$ to $V_S / 2$		0.036 to 4.953		V
		$R_L = 150\Omega$ to $V_S / 2$	0.3	0.12 to 4.8	4.625	V
$I_{OUT}$	Output Current			$\pm 55$		mA
		$-40^\circ\text{C}$ to $+85^\circ\text{C}$		$\pm 50$		mA
$I_{SC}$	Short Circuit Current	$V_{OUT} = V_S / 2$		$\pm 85$		mA
$V_S$	Power Supply Operating Range		2.5	5	5.5	V

**Notes:**

1.  $R_f = 1\text{k}\Omega$  was used for optimal performance. (For  $G = +1$ ,  $R_f = 0$ )

**CLC1005 Pin Configurations**

TSOT-5

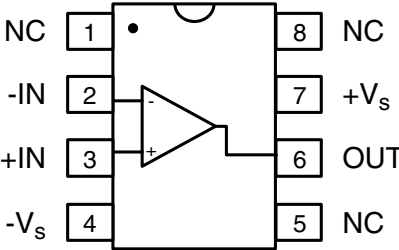


**CLC1005 Pin Assignments**

TSOT-5

Pin No.	Pin Name	Description
1	OUT	Output
2	-V <sub>S</sub>	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	+V <sub>S</sub>	Positive supply

SOIC-8

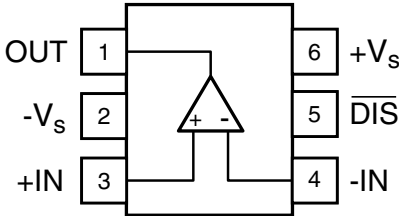


SOIC-8

Pin No.	Pin Name	Description
1	NC	No Connect
2	-IN	Negative input
3	+IN	Positive input
4	-V <sub>S</sub>	Negative supply
5	NC	No Connect
6	OUT	Output
7	+V <sub>S</sub>	Positive supply
8	NC	No Connect

**CLC1015 Pin Configurations**

TSOT-6



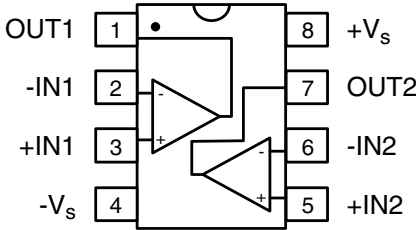
**CLC1015 Pin Assignments**

TSOT-6

Pin No.	Pin Name	Description
1	OUT	Output
2	-V <sub>S</sub>	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	$\overline{\text{DIS}}$	Disable pin. Enabled if pin is left open or tied to +V <sub>S</sub> , disabled if pin is tied to -V <sub>S</sub> (which is GND in a single supply application.)
6	+V <sub>S</sub>	Positive supply

**CLC2005 Pin Configuration**

SOIC-8 / MSOP-8



**CLC2005 Pin Assignments**

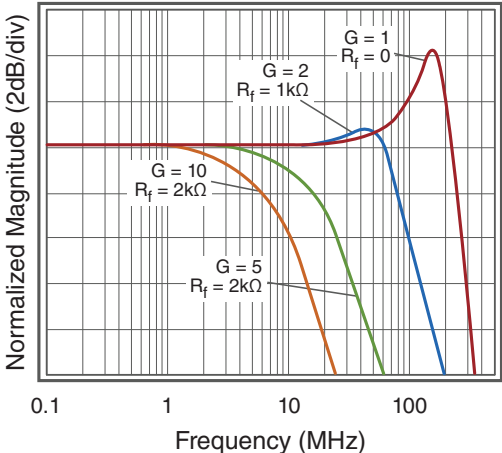
SOIC-8 / MSOP-8

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	-V <sub>s</sub>	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	+V <sub>s</sub>	Positive supply

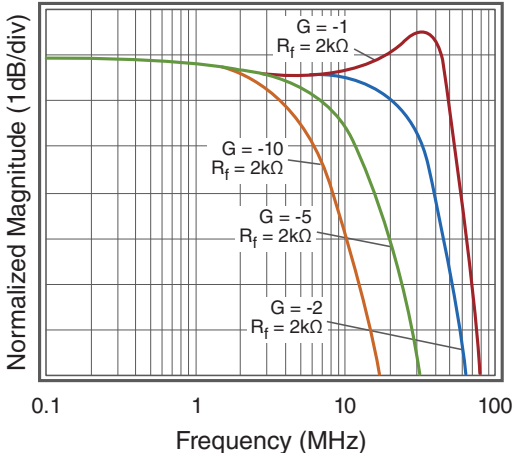
**Typical Performance Characteristics**

$T_A = 25^\circ\text{C}$ ,  $V_S = +5\text{V}$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ,  $G = +2$ ,  $R_F = 2\text{k}\Omega$ ; unless otherwise noted.

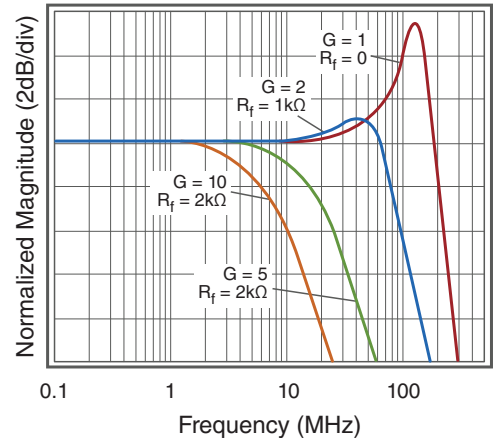
Non-Inverting Frequency Response  $V_S = +5\text{V}$



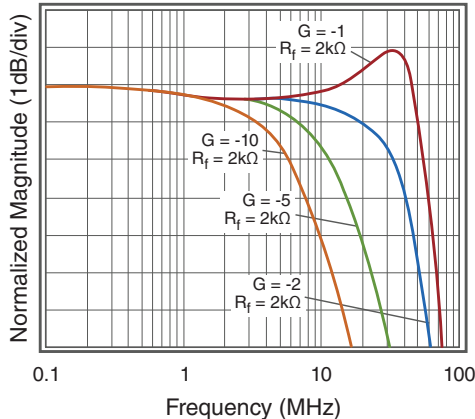
Inverting Frequency Response  $V_S = +5\text{V}$



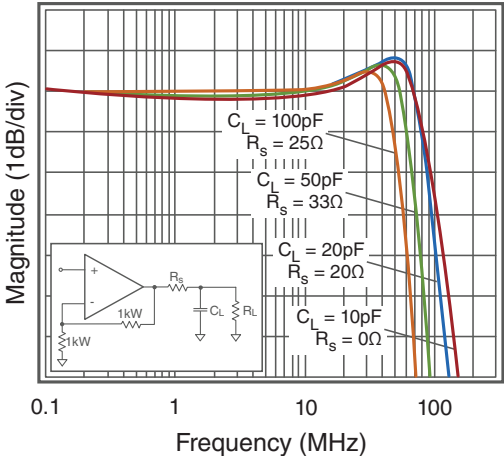
Non-Inverting Frequency Response  $V_S = +2.7\text{V}$



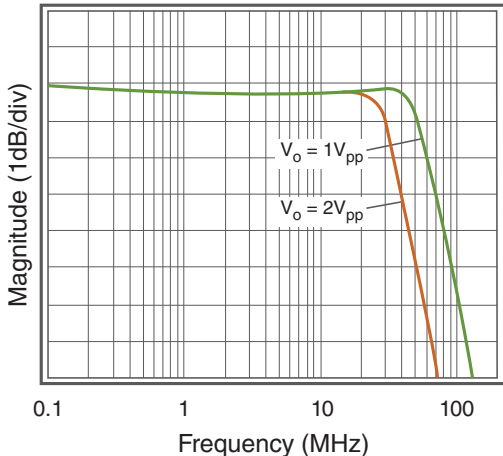
Inverting Frequency Response  $V_S = +2.7\text{V}$



Frequency Response vs  $C_L$



Large Signal Frequency Response

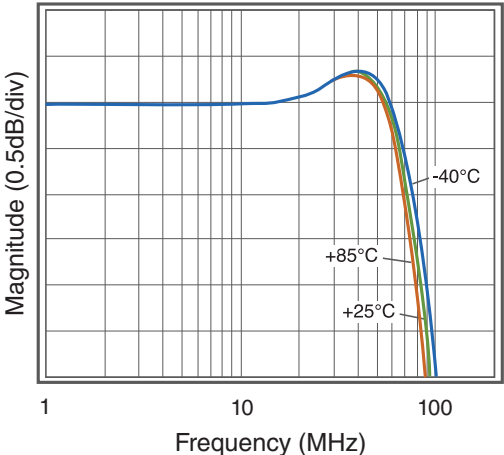




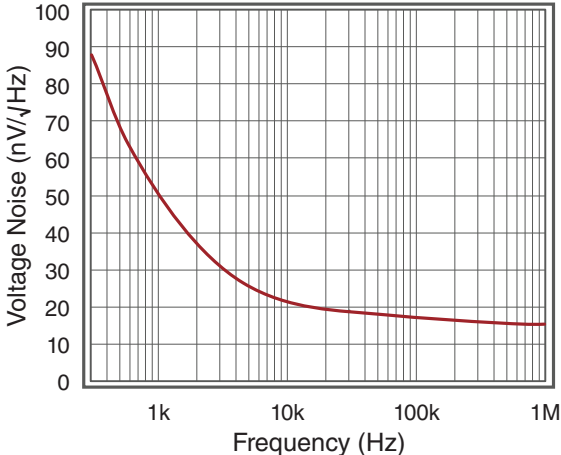
**Typical Performance Characteristics**

$T_A = 25^\circ\text{C}$ ,  $V_S = +5\text{V}$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ,  $G = +2$ ,  $R_F = 2\text{k}\Omega$ ; unless otherwise noted.

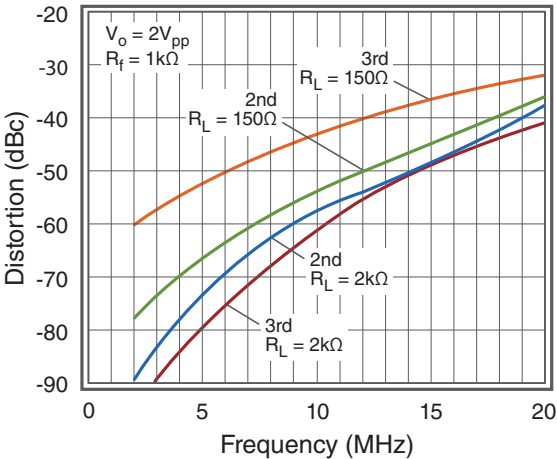
Frequency Response vs. Temperature



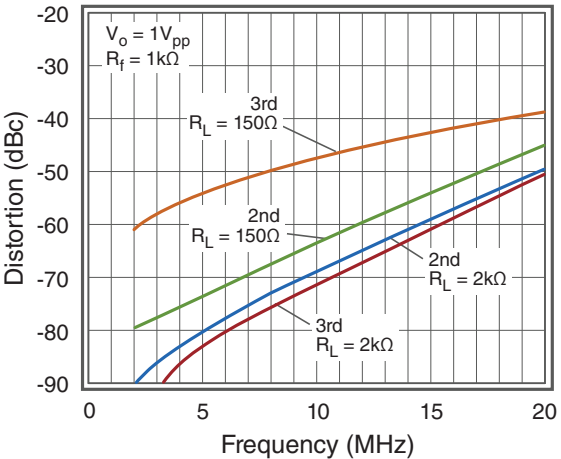
Input Voltage Noise vs Frequency



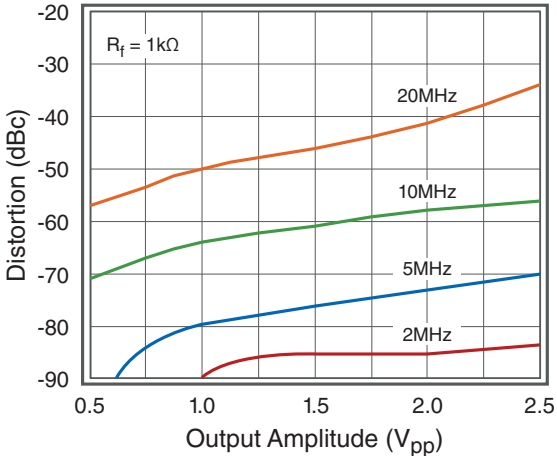
2nd & 3rd Harmonic Distortion  $V_S = +5\text{V}$



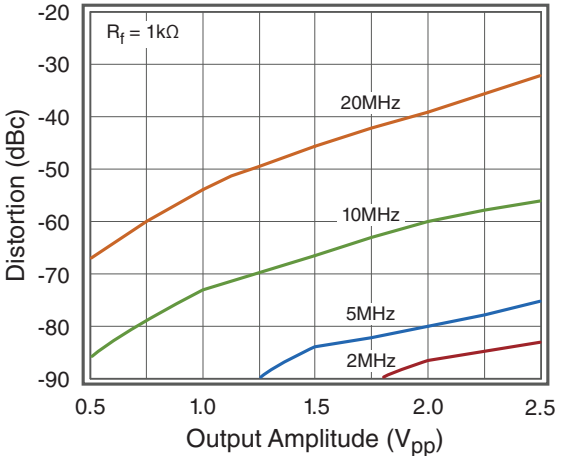
2nd & 3rd Harmonic Distortion  $V_S = +2.7\text{V}$



2nd Harmonic Distortion vs  $V_O$



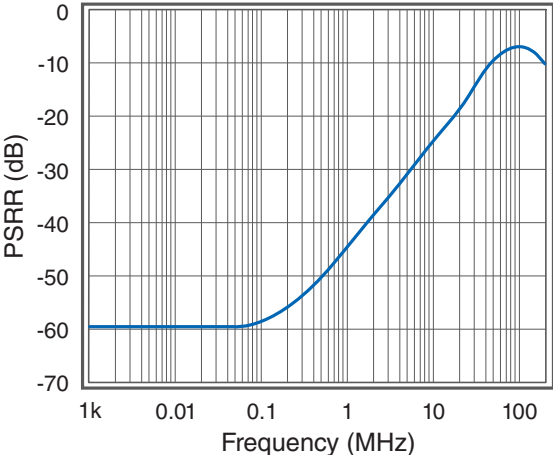
3rd Harmonic Distortion vs  $V_O$



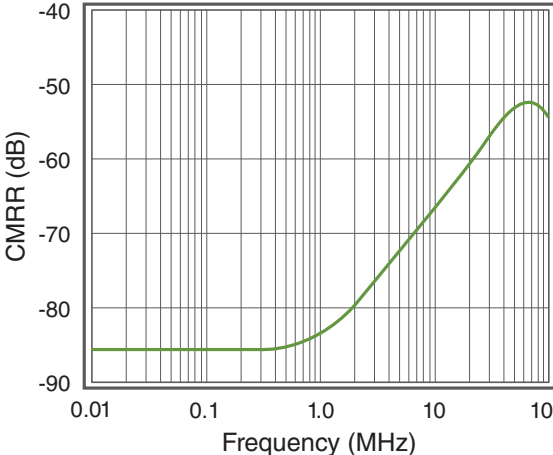
**Typical Performance Characteristics**

$T_A = 25^\circ\text{C}$ ,  $V_S = +5\text{V}$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ,  $G = +2$ ,  $R_F = 2\text{k}\Omega$ ; unless otherwise noted.

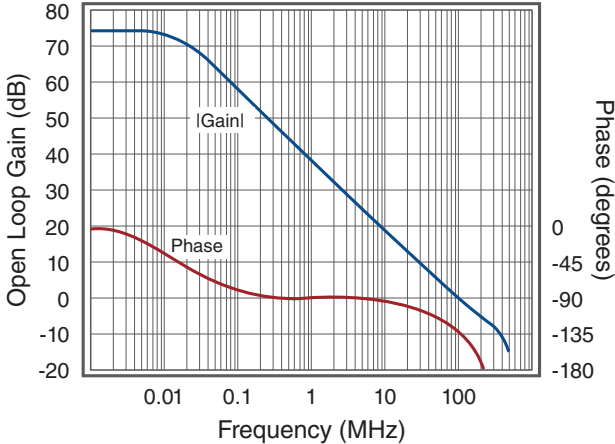
PSRR



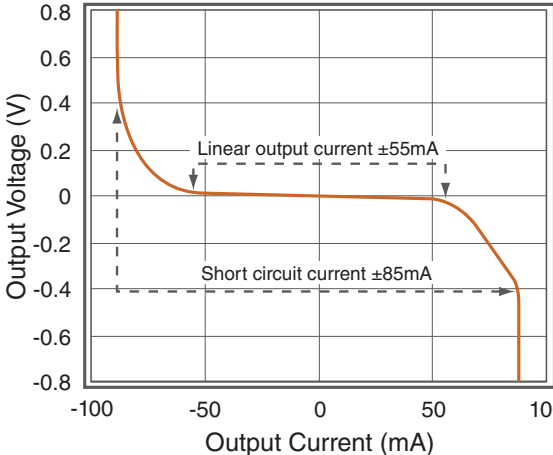
CMRR



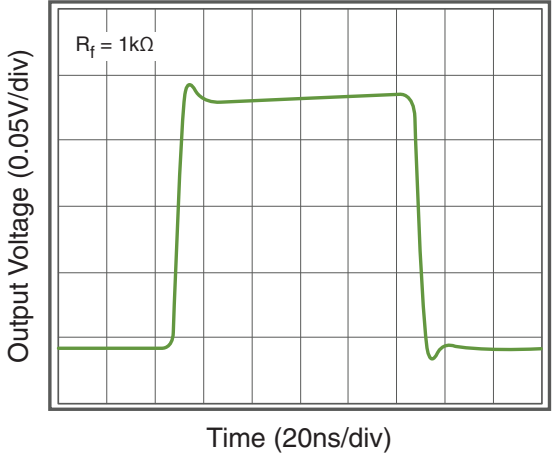
Open Loop Gain & Phase vs. Frequency



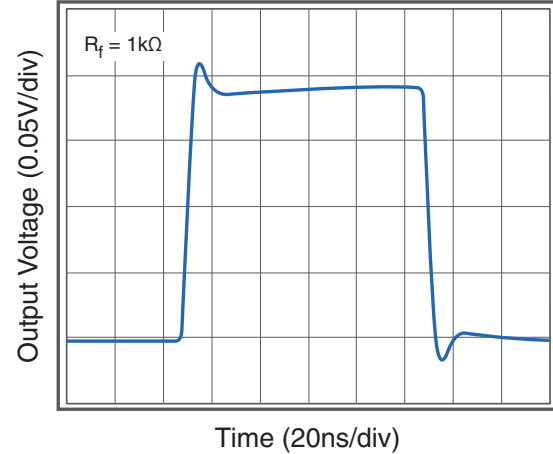
Output Current



Small Signal Pulse Response  $V_S = +5\text{V}$



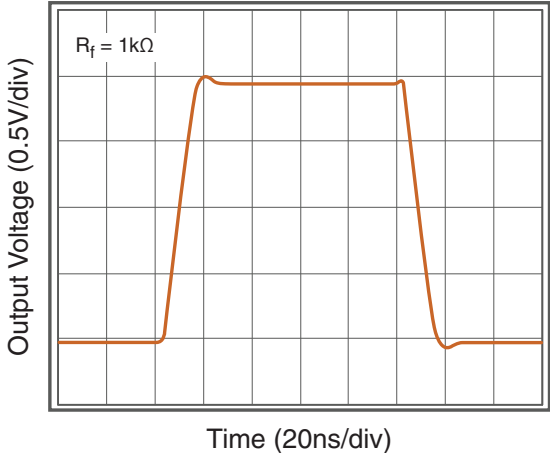
Small Signal Pulse Response  $V_S = +2.7\text{V}$



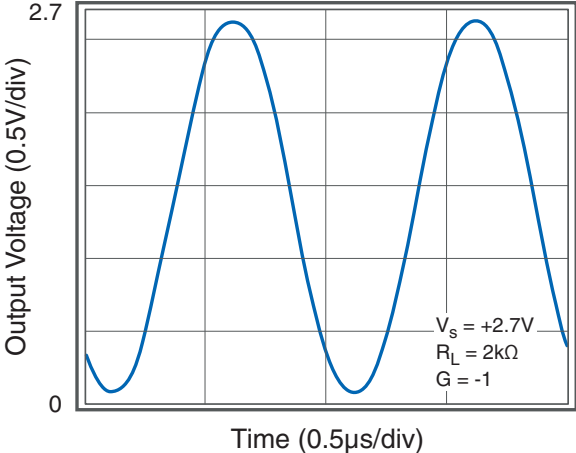
Typical Performance Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_S = +5\text{V}$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$ ,  $G = +2$ ,  $R_F = 2\text{k}\Omega$ ; unless otherwise noted.

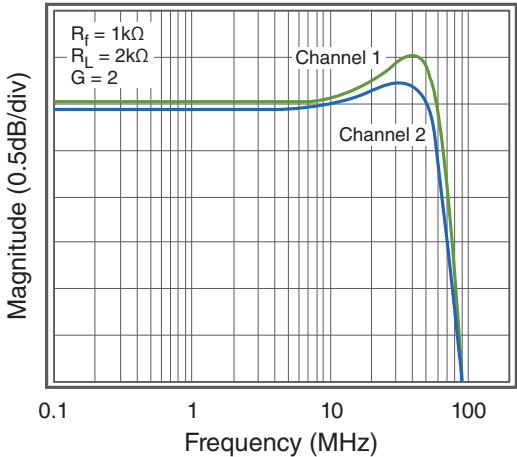
Large Signal Pulse Response  $V_S = +5\text{V}$



Output Swing



Channel Matching  $V_S = +5\text{V}$



Application Information

General Description

The CLC1005, CLC1015, and CLC2005 are single supply, general purpose, voltage-feedback amplifiers fabricated on a complementary bipolar process using a patented topography. They feature a rail-to-rail output stage and are unity gain stable. Both gain bandwidth and slew rate are insensitive to temperature.

The common mode input range extends to 300mV below ground and to 1.2V below  $V_{s+}$ . Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition.

The design is short circuit protected and offers “soft” saturation protection that improves recovery time.

Figures 1, 2, and 3 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations. Figure 4 shows the typical non-inverting gain circuit for single supply applications.

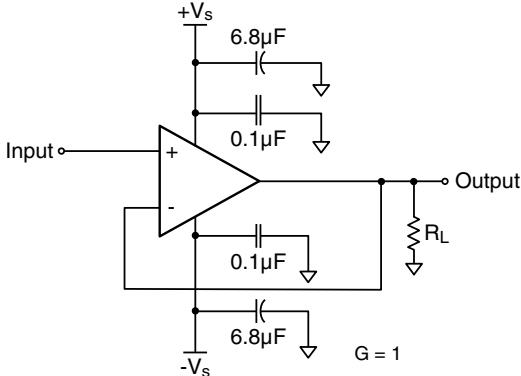


Figure 3: Unity Gain Circuit

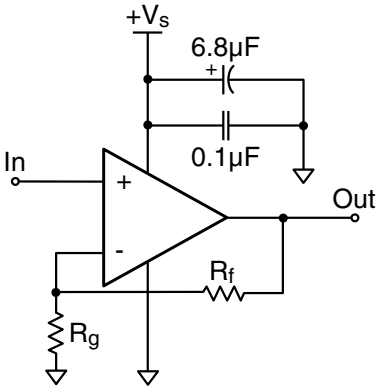


Figure 4: Single Supply Non-Inverting Gain Circuit

At non-inverting gains other than  $G = +1$ , keep  $R_g$  below 1kΩ to minimize peaking; thus for optimum response at a gain of +2, a feedback resistor of 1kΩ is recommended. Figure 5 illustrates the CLC1005, CLC1015 and CLC2005 frequency response with both 1kΩ and 2kΩ feedback resistors.

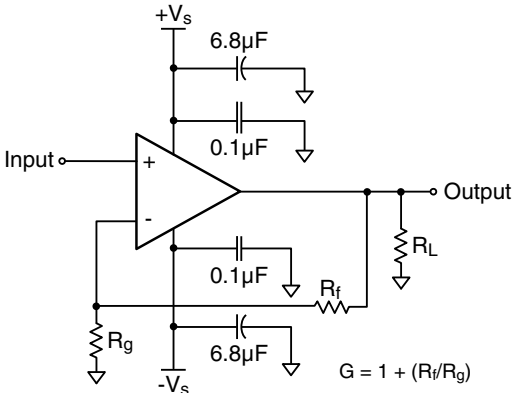


Figure 1: Typical Non-Inverting Gain Circuit

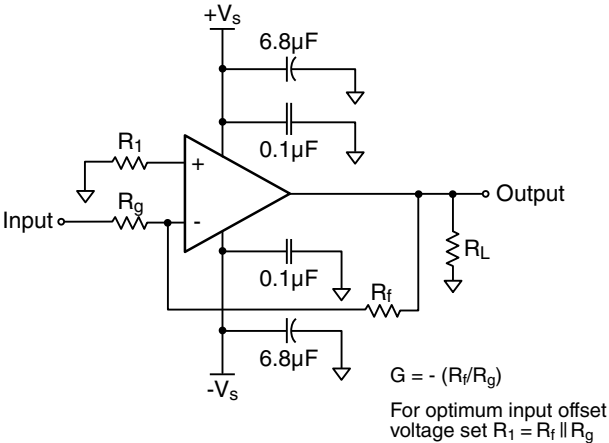


Figure 2: Typical Inverting Gain Circuit

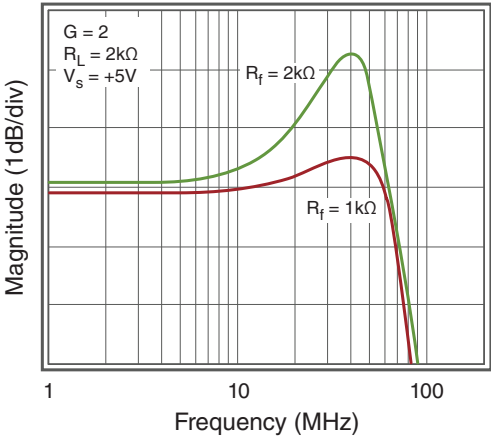


Figure 5: Frequency Response vs.  $R_f$

**Overdrive Recovery**

For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The CLC1005, CLC1015, and CLC2005 will typically recover in less than 20ns from an overdrive condition. Figure 6 shows the CLC2005 in an overdriven condition.

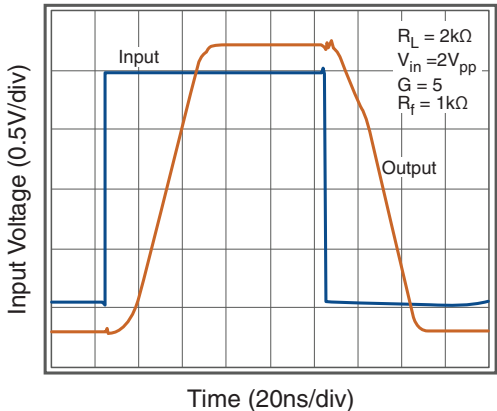


Figure 6: Overdrive Recovery

**Enable/Disable Function**

The CLC1015 offers an active-low disable pin that can be used to lower its supply current. Leave the pin floating to enable to part. Pull the disable pin to the negative supply (which is ground in a single supply application) to disable the output. During the disable condition, the nominal supply current will drop below 127µA and the output will be at a high impedance with about 2pF capacitance.

**Power Dissipation**

Power dissipation should not be a factor when operating under the stated 2kΩ load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value ThetaJA (θJA) is used along with the total die power dissipation.

$$T_{\text{Junction}} = T_{\text{Ambient}} + (\theta_{\text{JA}} \times P_{\text{D}})$$

Where T<sub>Ambient</sub> is the temperature of the working environment.

In order to determine P<sub>D</sub>, the power dissipated in the load

needs to be subtracted from the total power delivered by the supplies.

$$P_{\text{D}} = P_{\text{supply}} - P_{\text{load}}$$

Supply power is calculated by the standard power equation.

$$P_{\text{supply}} = V_{\text{supply}} \times I_{\text{RMSsupply}}$$

$$V_{\text{supply}} = V_{\text{S+}} - V_{\text{S-}}$$

Power delivered to a purely resistive load is:

$$P_{\text{load}} = ((V_{\text{load}})_{\text{RMS}}^2) / R_{\text{loadeff}}$$

The effective load resistor (R<sub>load<sub>eff</sub></sub>) will need to include the effect of the feedback network. For instance,

R<sub>load<sub>eff</sub></sub> in Figure 3 would be calculated as:

$$R_{\text{L}} \parallel (R_{\text{f}} + R_{\text{g}})$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P<sub>D</sub> can be found from

$$P_{\text{D}} = P_{\text{Quiescent}} + P_{\text{Dynamic}} - P_{\text{load}}$$

Quiescent power can be derived from the specified I<sub>S</sub> values along with known supply voltage, V<sub>supply</sub>. Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{\text{load}})_{\text{RMS}} = V_{\text{peak}} / \sqrt{2}$$

$$(I_{\text{load}})_{\text{RMS}} = (V_{\text{load}})_{\text{RMS}} / R_{\text{loadeff}}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{\text{Dynamic}} = (V_{\text{S+}} - V_{\text{load}})_{\text{RMS}} \times (I_{\text{load}})_{\text{RMS}}$$

Assuming the load is referenced in the middle of the power rails or V<sub>supply</sub>/2.

The CLC1015 is short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. Figure 7 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

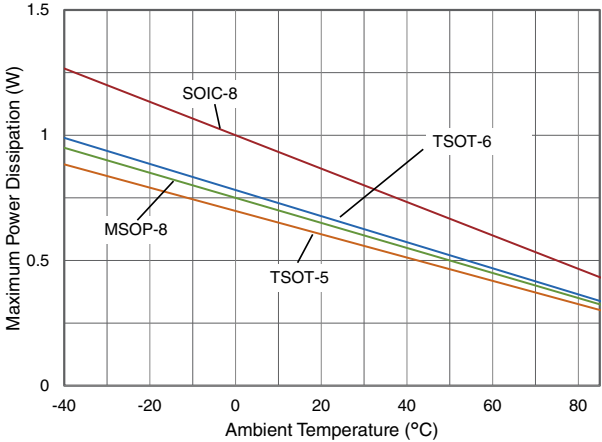


Figure 7. Maximum Power Derating

**Driving Capacitive Loads**

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance,  $R_S$ , between the amplifier and the load to help improve stability and settling performance. Refer to Figure 8.

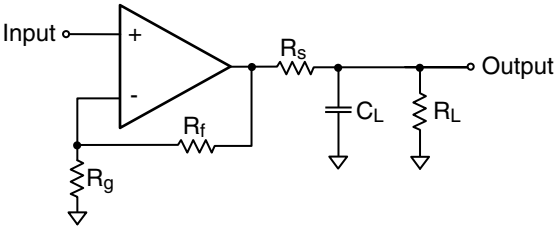


Figure 8. Addition of  $R_S$  for Driving Capacitive Loads

Table 1 provides the recommended  $R_S$  for various capacitive loads. The recommended  $R_S$  values result in approximately <1dB peaking in the frequency response.

$C_L$ (pF)	$R_S$ ( $\Omega$ )	-3dB BW (MHz)
22pF	0	118
47pF	15	112
100pF	15	91
492pF	6.5	59

Table 1: Recommended  $R_S$  vs.  $C_L$

For a given load capacitance, adjust  $R_S$  to optimize the tradeoff between settling time and bandwidth. In general, reducing  $R_S$  will increase bandwidth at the expense of additional overshoot and ringing.

**Layout Considerations**

General layout and supply bypassing play major roles in high frequency performance. Exar has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8 $\mu$ F and 0.1 $\mu$ F ceramic capacitors for power supply decoupling
- Place the 6.8 $\mu$ F capacitor within 0.75 inches of the power pin
- Place the 0.1 $\mu$ F capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

**Evaluation Board Information**

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board #	Products
CEB002	CLC1005 and CLC1015 in TSOT
CEB003	CLC1005 in SOIC
CEB006	CLC2005 in SOIC
CEB010	CLC2005 in MSOP

**Evaluation Board Schematics**

Evaluation board schematics and layouts are shown in Figures 9-18. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short  $-V_S$  to ground.
2. Use C3 and C4, if the  $-V_S$  pin of the amplifier is not directly connected to the ground plane.

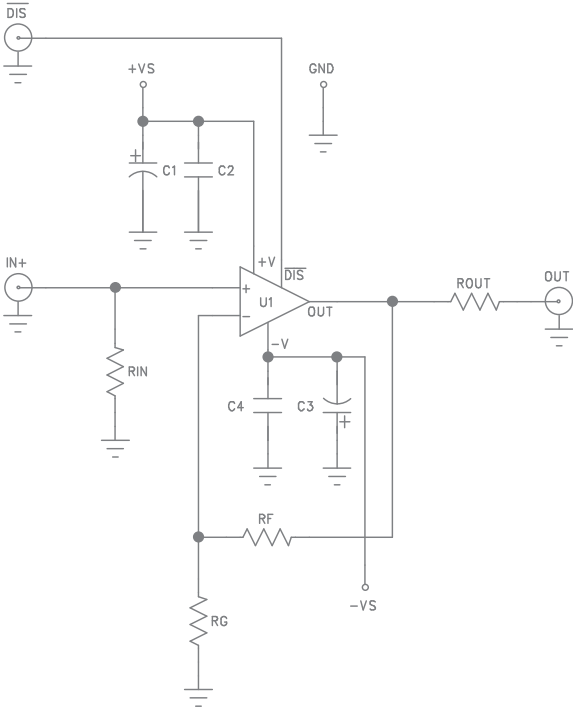


Figure 9. CEB002 and CEB003 Schematic

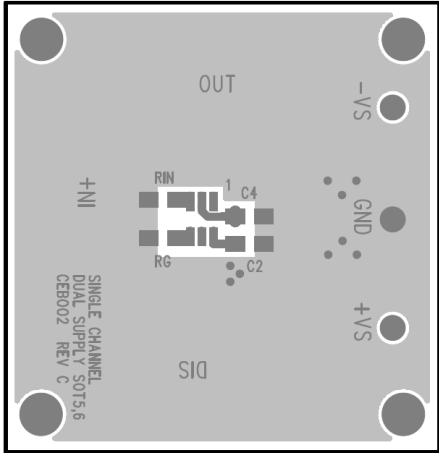


Figure 10. CEB002 Top View

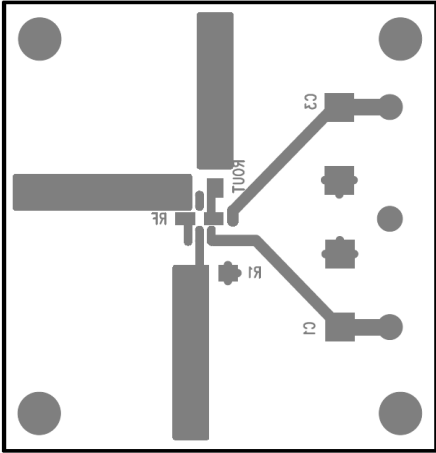


Figure 11. CEB002 Bottom View

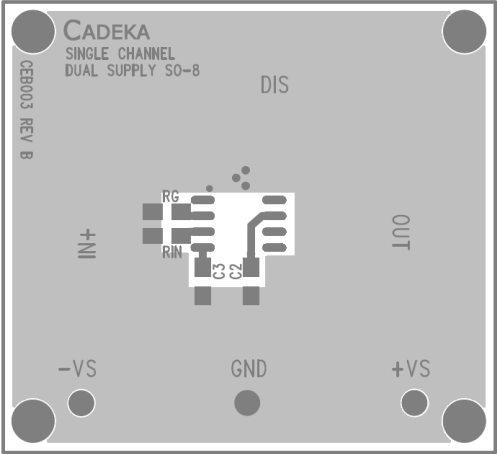


Figure 12. CEB003 Top View

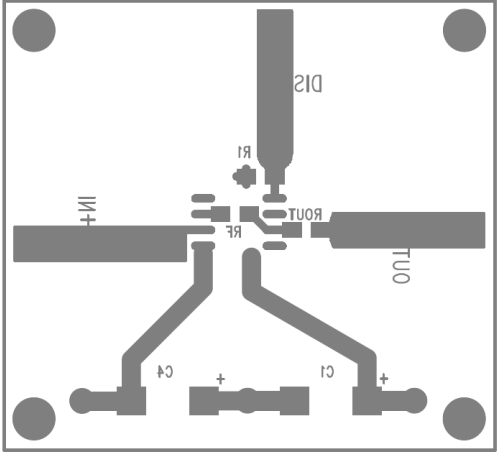


Figure 13. CEB003 Bottom View

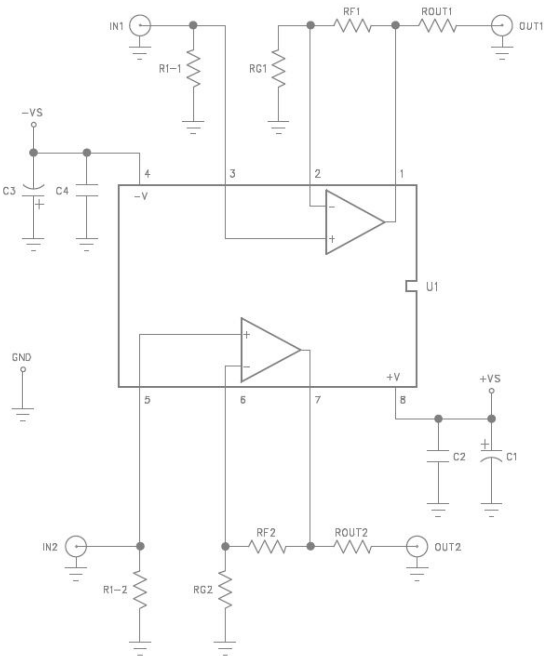


Figure 14. CEB006 & CEB010 Schematic

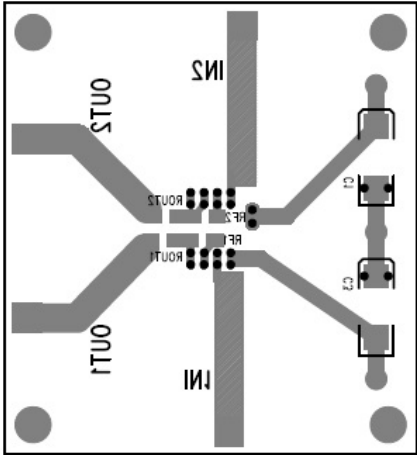


Figure 16. CEB006 Bottom View

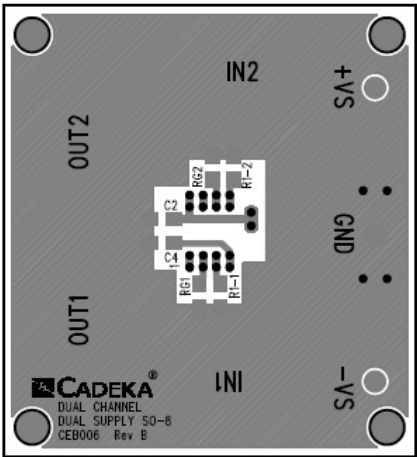


Figure 15. CEB006 Top View

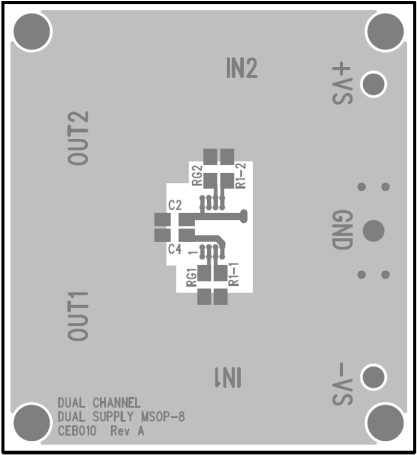


Figure 17. CEB010 Top View

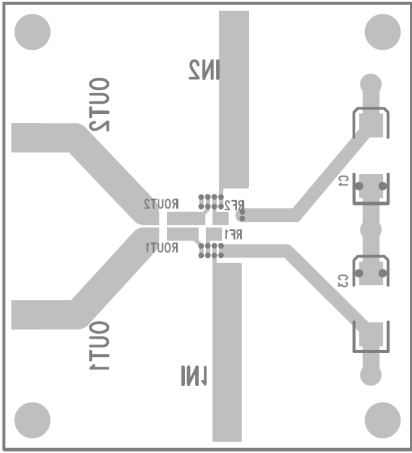
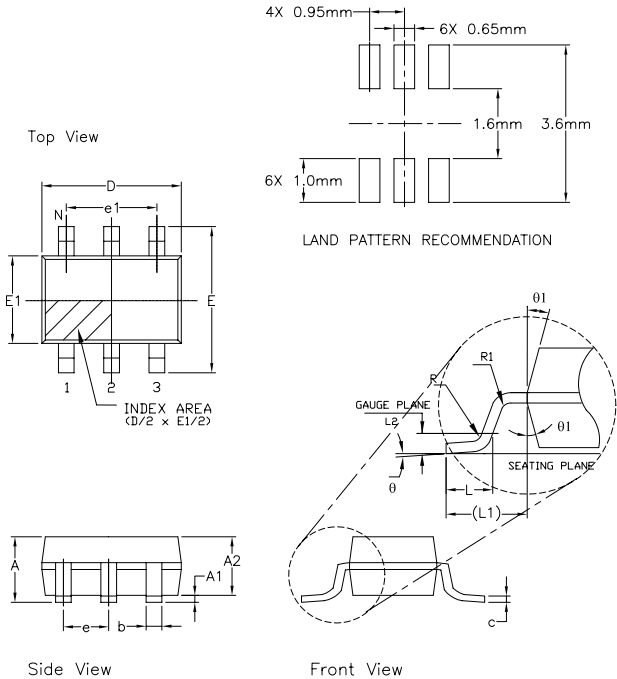


Figure 18. CEB010 Bottom View



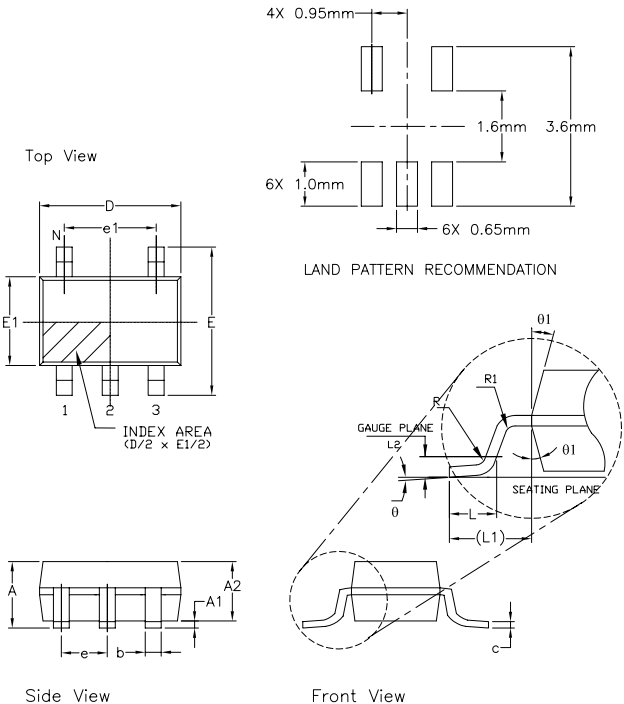
Mechanical Dimensions

TSOT-6 Package



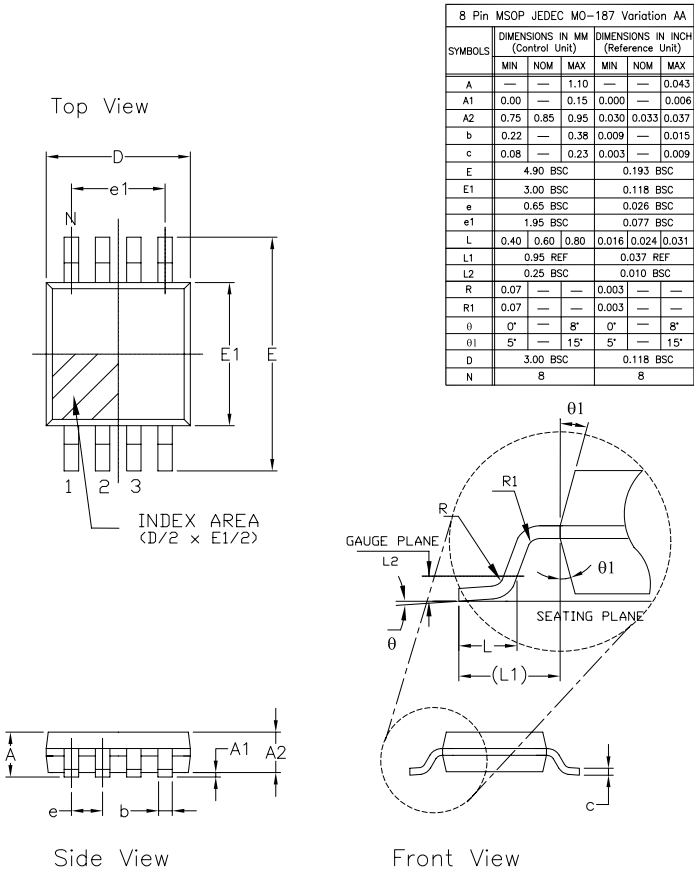
6 PIN TSOT (OPTION 2)						
SYMBOLS	DIMENSION IN MM (Control Unit)			DIMENSION IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	0.80	0.030	—	0.031
A1	0.00	—	0.05	0.000	—	0.002
A2	0.70	0.75	0.78	0.028	0.036	0.031
b	0.35	—	0.50	0.012	—	0.020
c	0.10	—	0.20	0.003	—	0.008
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.063 BSC		
e	0.95 BSC			0.038 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.37	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
R1	0.10	—	0.25	0.004	—	0.010
θ	0°	4°	8°	0°	4°	8°
θ1	4°	10°	12°	4°	10°	12°
N	6			6		

TSOT-5 Package

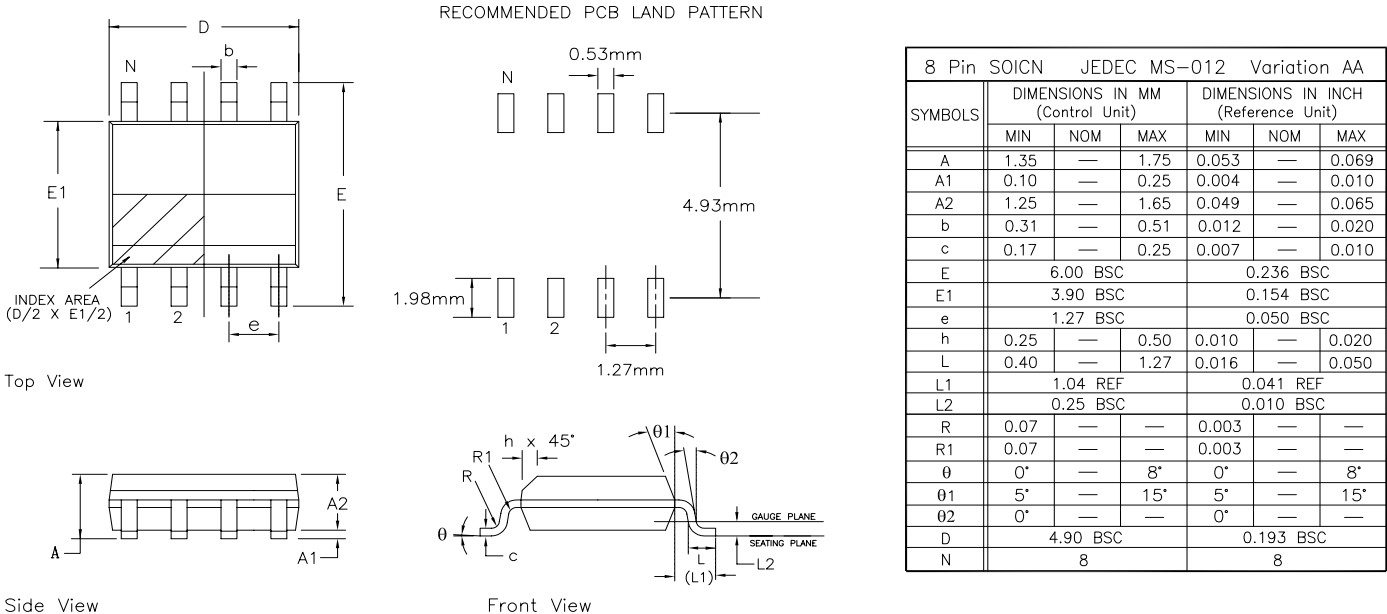


5 Pin TSOT (OPTION 2)						
SYMBOLS	DIMENSION IN MM (Control Unit)			DIMENSION IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.75	—	0.80	0.030	—	0.031
A1	0.00	—	0.05	0.000	—	0.002
A2	0.70	0.75	0.78	0.028	0.030	0.031
b	0.35	—	0.50	0.012	—	0.020
c	0.10	—	0.20	0.003	—	0.008
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.063 BSC		
e	0.95 BSC			0.038 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.37	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
R1	0.10	—	0.25	0.004	—	0.010
θ	0°	4°	8°	0°	4°	8°
θ1	4°	10°	12°	4°	10°	12°
N	5			5		

MSOP-8 Package



SOIC-8 Package



## Ordering Information

Part Number	Package	Green	Operating Temperature Range	Packaging
CLC1005 Ordering Information				
CLC1005IST5X	TSOT-5	Yes	-40°C to +85°C	Tape & Reel
CLC1005IST5MTR	TSOT-5	Yes	-40°C to +85°C	Mini Tape & Reel
CLC1005IST5EVB	Evaluation Board	N/A	N/A	N/A
CLC1005ISO8X	SOIC-8	Yes	-40°C to +85°C	Tape & Reel
CLC1005ISO8MTR	SOIC-8	Yes	-40°C to +85°C	Mini Tape & Reel
CLC1005ISO8EVB	Evaluation Board	N/A	N/A	N/A
CLC1015 Ordering Information				
CLC1015IST6X	TSOT-6	Yes	-40°C to +85°C	Tape & Reel
CLC1015IST6MTR	TSOT-6	Yes	-40°C to +85°C	Mini Tape & Reel
CLC1015IST6EVB	Evaluation Board	N/A	N/A	N/A
CLC2005 Ordering Information				
CLC2005ISO8X	SOIC-8	Yes	-40°C to +85°C	Tape & Reel
CLC2005ISO8MTR	SOIC-8	Yes	-40°C to +85°C	Mini Tape & Reel
CLC2005ISO8EVB	Evaluation Board	N/A	N/A	N/A
CLC2005IMP8X	MSOP-8	Yes	-40°C to +85°C	Tape & Reel
CLC2005IMP8MTR	MSOP-8	Yes	-40°C to +85°C	Mini Tape & Reel
CLC2005IMP8EVB	Evaluation Board	N/A	N/A	N/A

Moisture sensitivity level for all parts is MSL-1. Mini tape and reel quantity is 250.

## Revision History

Revision	Date	Description
2D (ECN 1513-01)	March 2015	Reformat into Exar data sheet template. Updated ordering information table to include MTR and EVB part numbers. Updated thermal resistance numbers and package outline drawings. Added CLC1015 back into data sheet.

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