KSMD7N20 / KSMU7N20

200V N-Channel MOSFET

KERSEMI ELECTRONIC CO.,LTD.

Features

- 5.3A, 200V, $R_{DS(on)}$ = 0.69Ω @V_{GS} = 10 V
- Low gate charge (typical 8.0 nC)
- Low Crss (typical 9.0 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
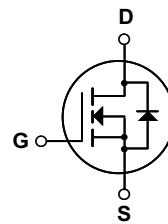
TO-252   TO-251

General Description

These N-Channel enhancement mode power field effect transistors are produced using Kersemi proprietary planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supply, DC-AC converters for uninterrupted power supply, motor control.

Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter			KSMD7N20 / KSMU7N20	Units
V_{DSS}	Drain-Source Voltage			200	V
I_D	Drain Current	- Continuous (T_C = 25°C)		5.3	A
		- Continuous (T_C = 100°C)		3.4	A
I_{DM}	Drain Current	- Pulsed	(Note 1)	21	A
V_{GSS}	Gate-Source Voltage			± 30	V
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	73	mJ
I_{AR}	Avalanche Current		(Note 1)	5.3	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	4.5	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	5.5	V/ns
P_D	Power Dissipation (T_A = 25°C) *			2.5	W
	Power Dissipation (T_C = 25°C)			45	W
	- Derate above 25°C			0.36	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds			300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.78	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_C = 25°C$ unless otherwise noted

| Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ µA	200	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C	--	0.27	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 200$ V, $V_{GS} = 0$ V	--	--	1	µA
		$V_{DS} = 160$ V, $T_C = 125°C$	--	--	10	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30$ V, $V_{DS} = 0$ V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30$ V, $V_{DS} = 0$ V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ µA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 2.65$ A	--	0.55	0.69	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40$ V, $I_D = 2.65$ A (Note 4)	--	3.6	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1.0 MHz	--	300	400	pF
C_{oss}	Output Capacitance		--	60	75	pF
C_{rss}	Reverse Transfer Capacitance		--	9	12	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100$ V, $I_D = 6.6$ A, $R_G = 25$ Ω	--	8	25	ns
t_r	Turn-On Rise Time		--	65	140	ns
$t_{d(off)}$	Turn-Off Delay Time		--	15	40	ns
t_f	Turn-Off Fall Time	(Note 4, 5)	--	35	80	ns
Q_g	Total Gate Charge	$V_{DS} = 160$ V, $I_D = 6.6$ A, $V_{GS} = 10$ V	--	8.0	10	nC
Q_{gs}	Gate-Source Charge		--	2.4	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4, 5)	--	3.3	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	5.3	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	21	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 5.3$ A	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0$ V, $I_S = 6.6$ A, $dI_F / dt = 100$ A/µs	--	115	--	ns
Q_{rr}	Reverse Recovery Charge	(Note 4)	--	0.51	--	µC
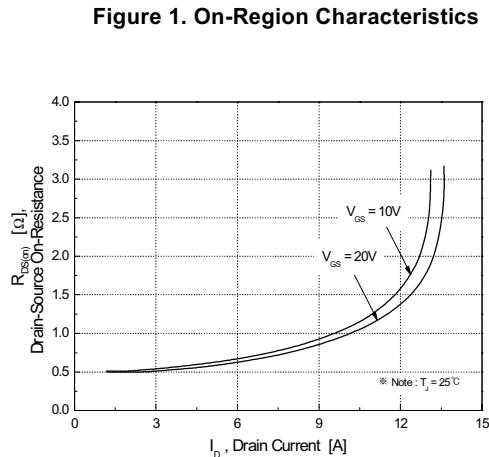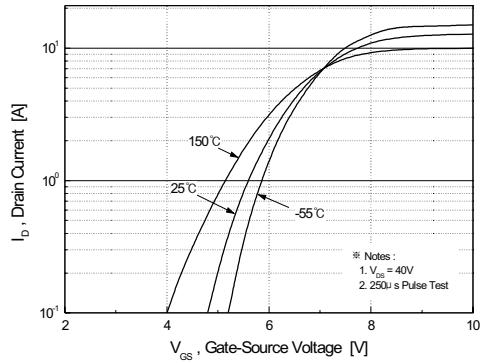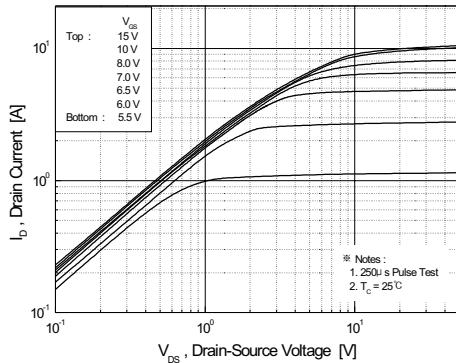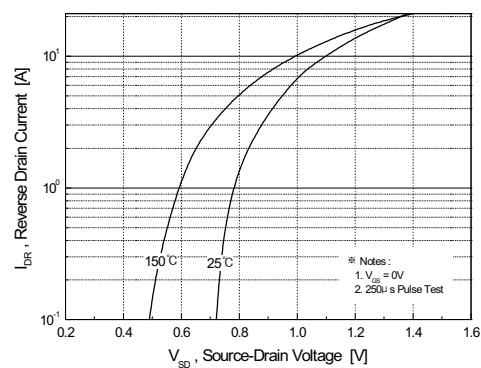
Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 3.9mH, $I_{AS} = 5.3$A, $V_{DD} = 50$V, $R_G = 25$ Ω, Starting $T_J = 25°C$
3. $I_{SD} \leq 6.6$A, di/dt ≤ 300A/µs, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25°C$
4. Pulse Test : Pulse width ≤ 300µs, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

Figure 1. On-Region Characteristics
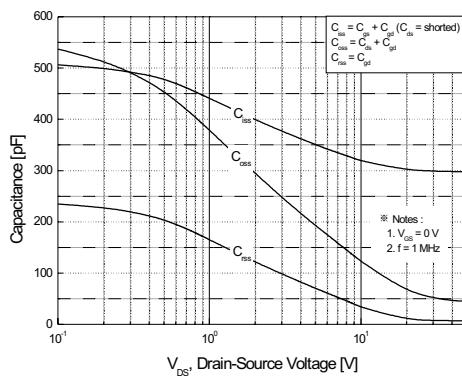
Figure 2. Transfer Characteristics
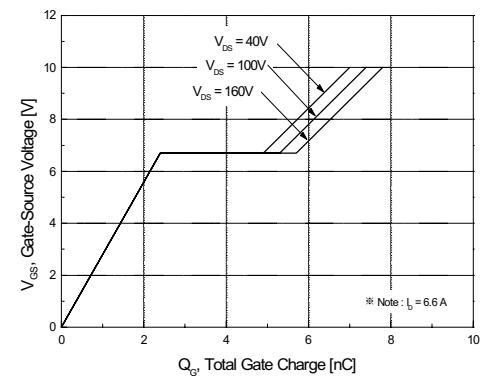
Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

Figure 4. Body Diode Forward Voltage
Variation vs. Source Current
and Temperature
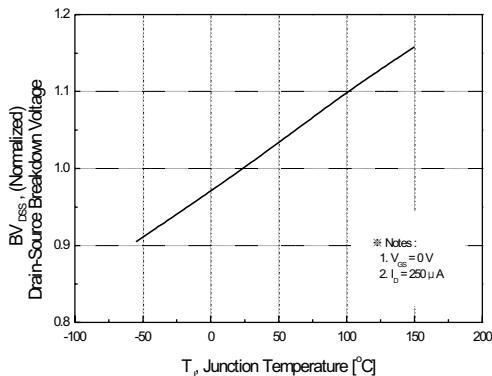
Figure 5. Capacitance Characteristics
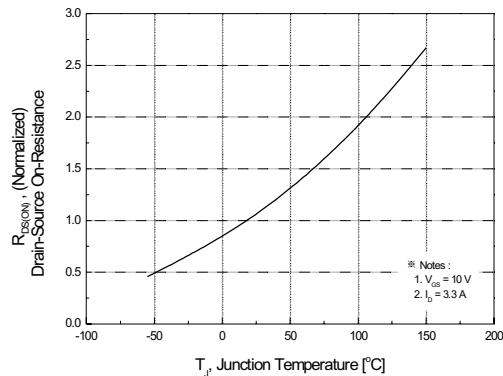
Figure 6. Gate Charge Characteristics
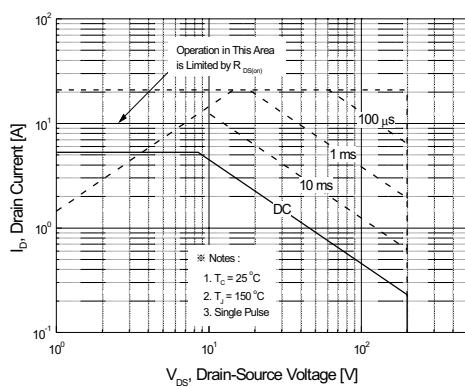
Typical Characteristics (Continued)
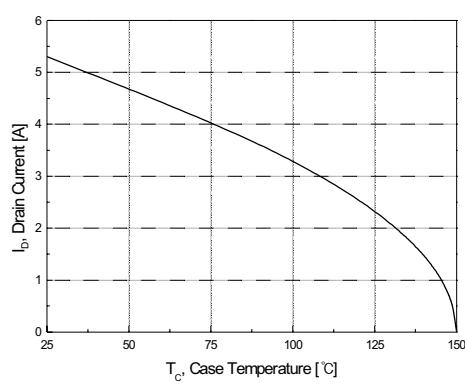
Figure 7. Breakdown Voltage Variation vs. Temperature
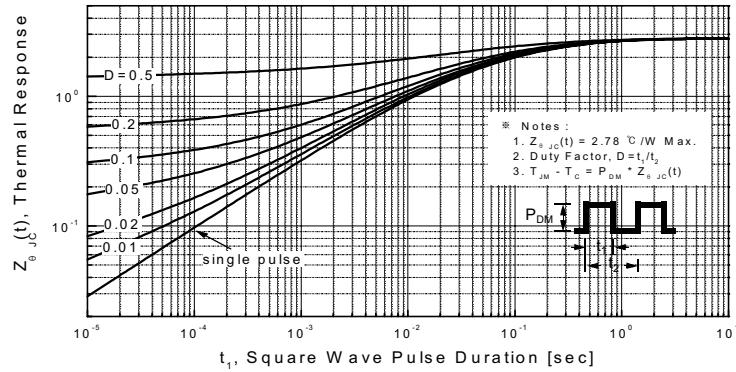
Figure 8. On-Resistance Variation vs. Temperature
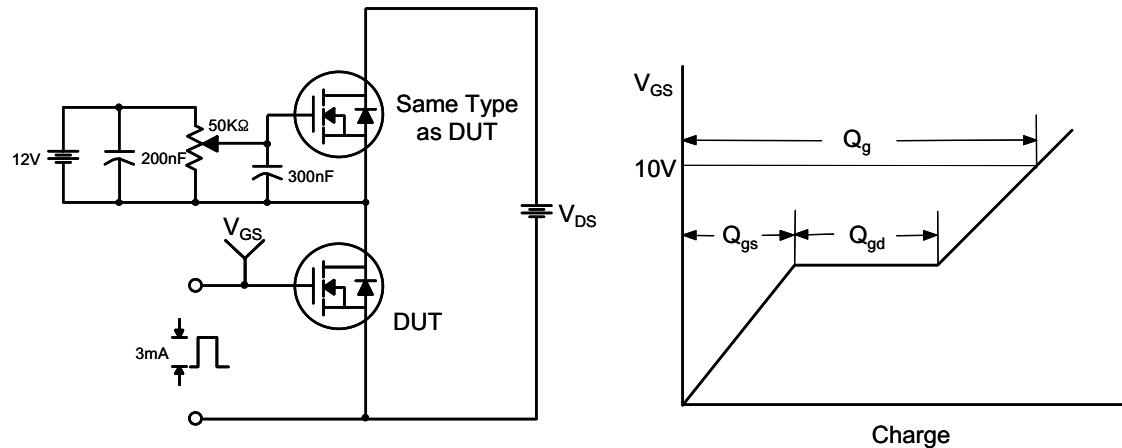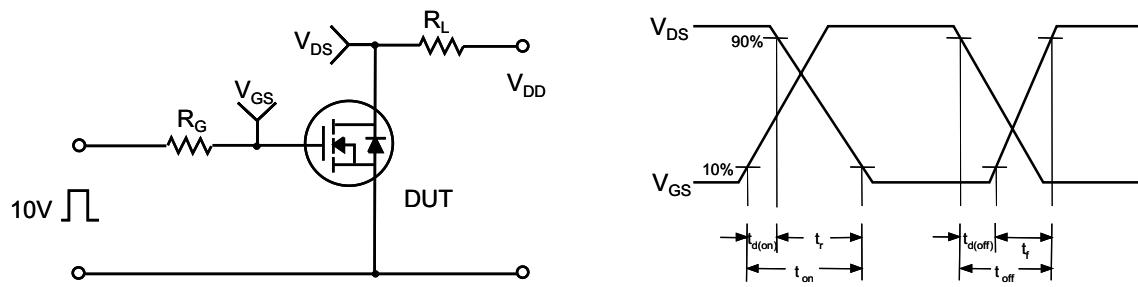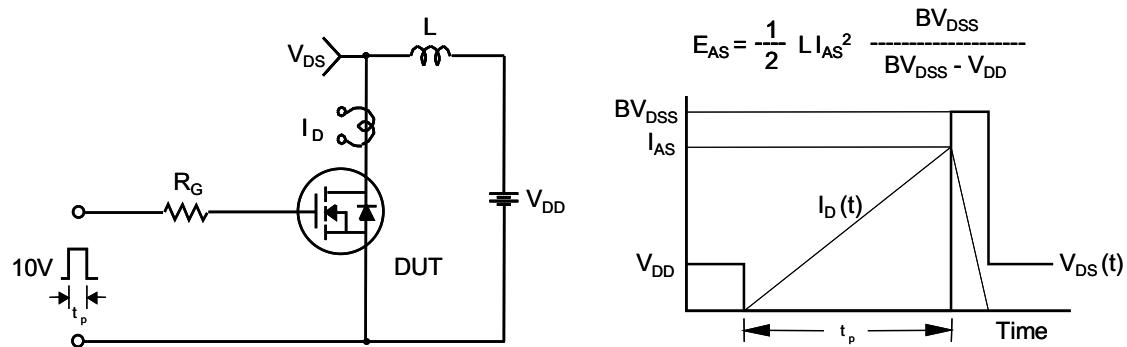
Figure 9. Maximum Safe Operating Area
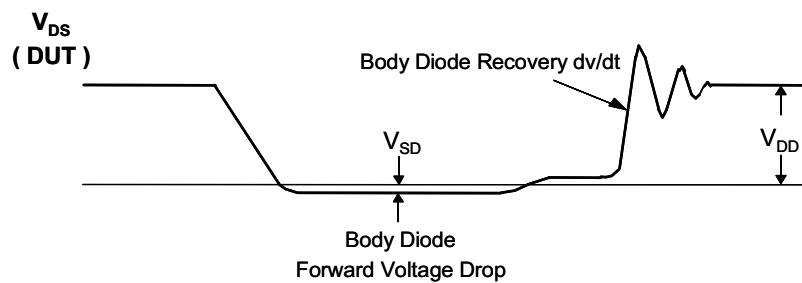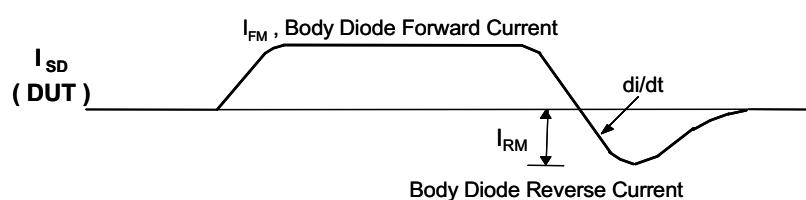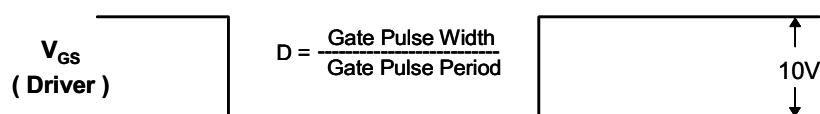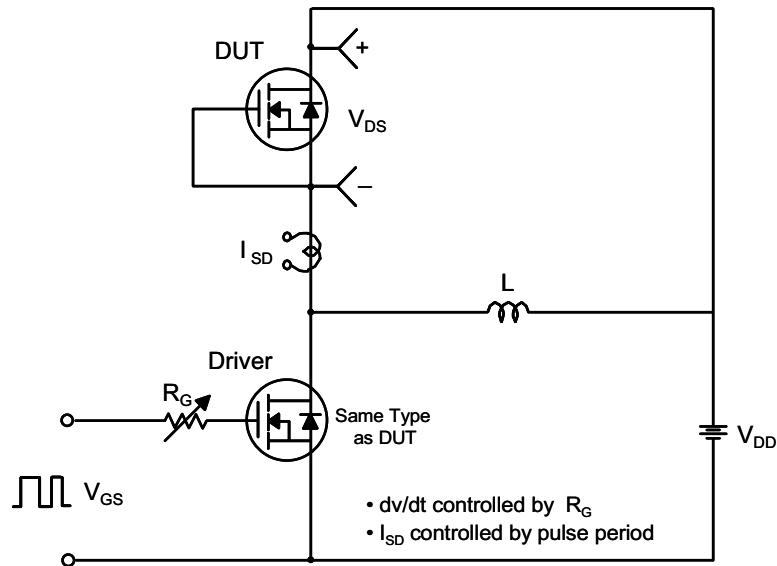
Figure 10. Maximum Drain Current vs. Case Temperature
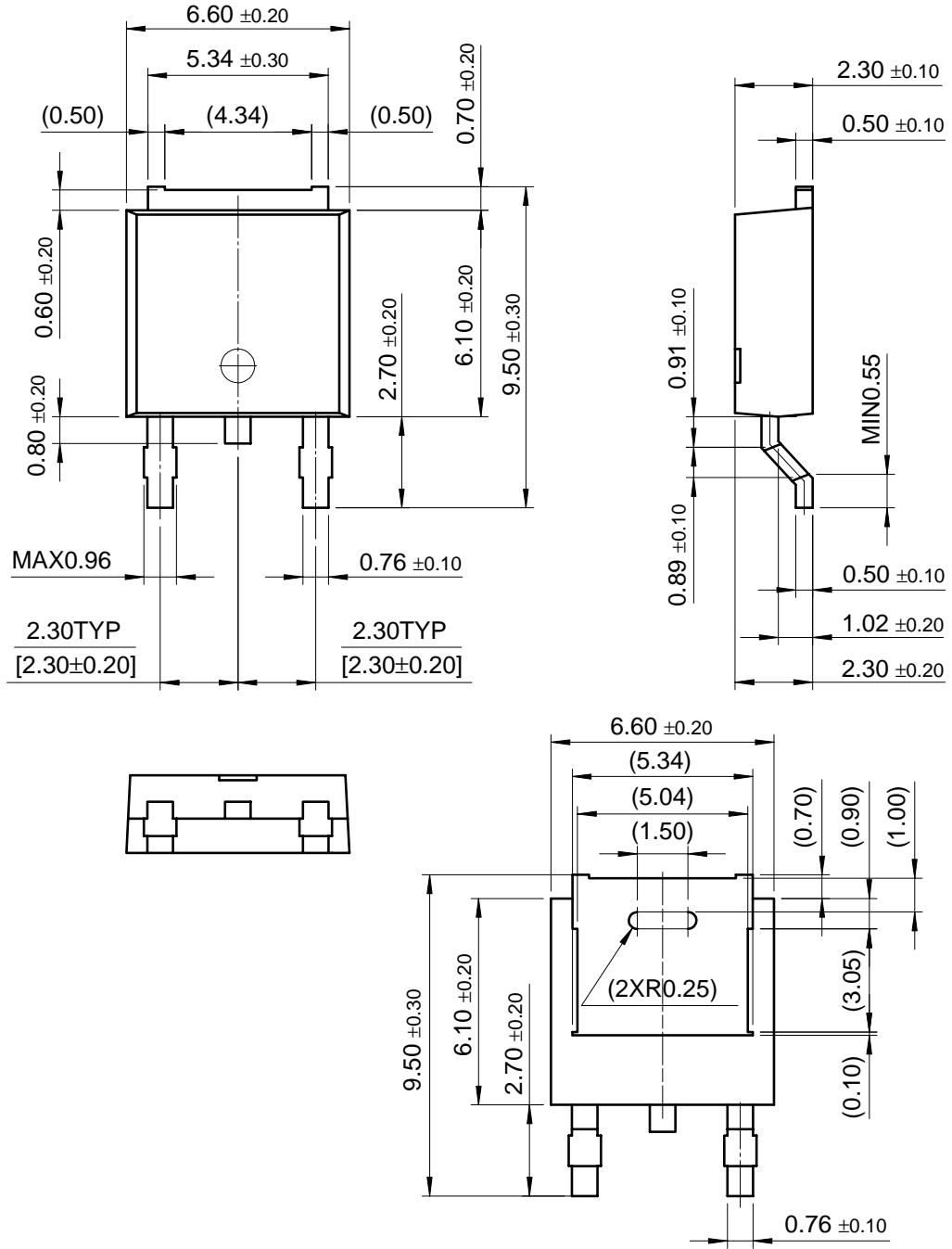
Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \; \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

Peak Diode Recovery dv/dt Test Circuit & Waveforms

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

- dv/dt controlled by R_G
- I_{SD} controlled by pulse period

Package Dimensions

DPAK

Package Dimensions (Continued)

IPAK

6.60 ±0.20
5.34 ±0.20
(0.50) (4.34) (0.50)
0.60 ±0.20
0.70 ±0.20
6.10 ±0.20
0.80 ±0.10
MAX0.96
1.80 ±0.20
9.30 ±0.30
0.76 ±0.10
2.30TYP [2.30±0.20]
2.30TYP [2.30±0.20]

2.30 ±0.20
0.50 ±0.10
16.10 ±0.30
0.50 ±0.10