



Multiple Channel Capacitive Touch Sensor and LED Driver

PRODUCT FEATURES

Datasheet

General Description

The CAP1014 is a multiple channel Capacitive Touch sensor and LED Driver.

The CAP1014 contains up to fourteen (14) individual Capacitive Touch sensor inputs with programmable sensitivity for use in touch button and slider switch applications. Each sensor also contains automatic recalibration with programmable time delays.

The CAP1014 also contains eleven (11) low side LED drivers that offer full-on / off, variable rate blinking, dimmness controls, and breathing. Capacitive buttons can be linked to LED outputs.

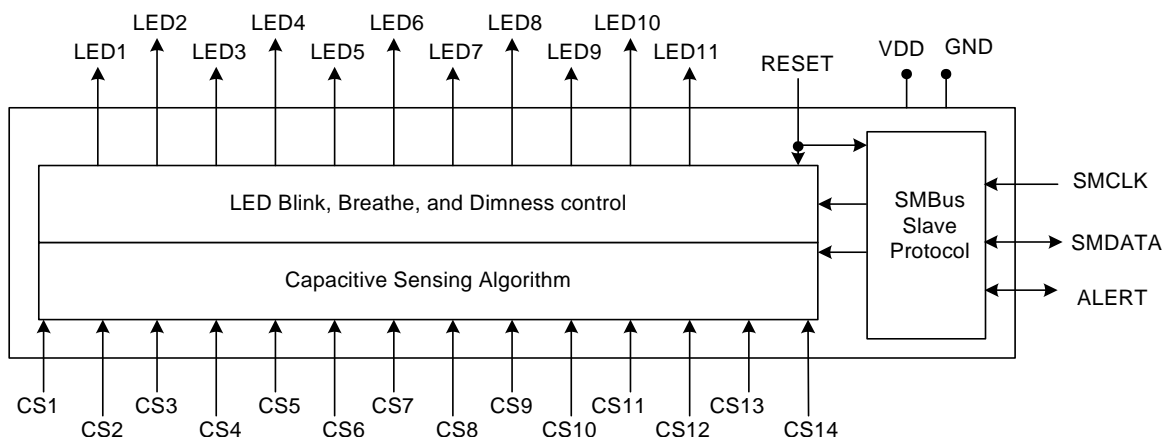
Applications

- Consumer Electronics
- Desktop and Notebook PC's
- LCD Monitors

Features

- Fourteen (14) Capacitive Touch Sensor inputs
 - Programmable sensitivity
 - High SNR allows for easy tuning
 - Automatic recalibration
 - Slider Acceleration Detection
 - Slider positional detection
- Low Power operation
 - 150uA quiescent current in Deep Sleep
 - 250uA quiescent current in Sleep mode while monitoring 2 buttons.
- Alert to signal touch to host processor
- User controlled reset
- Low External Component Count
- SMBus 2.0 compliant interface to change operating parameters to work in a wide variety of systems
 - Block Read and Write function for quick tasking
- Eleven (11) LED Driver outputs
 - Programmable blink, breathe, and dimmness controls
 - 8 Configurable as GPIOs
 - Buttons can be linked to LED responses
- Development boards and software available
- Available in 32-pin 5mm x 5mm QFN Lead-free RoHS Compliant package

Block Diagram



ORDER NUMBERS:

| ORDERING NUMBER | PACKAGE | FEATURES |
|------------------------|--|---|
| CAP1014-1-EZK-TR | 32-pin QFN 5mm x 5mm (Lead Free RoHS compliant) | 14 Capacitive Touch Sensors, 11 LED drivers. Lid Closure. SMBus address 0101_000b |
| CAP1014-2-EZK-TR | 32-pin QFN 5mm x 5mm (Lead Free RoHS compliant) | 14 Capacitive Touch Sensors, 11 LED drivers. Lid Closure. SMBus address 0101_100b |

REEL SIZE IS 4,000 PIECES

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Chapter 1 Pin Description

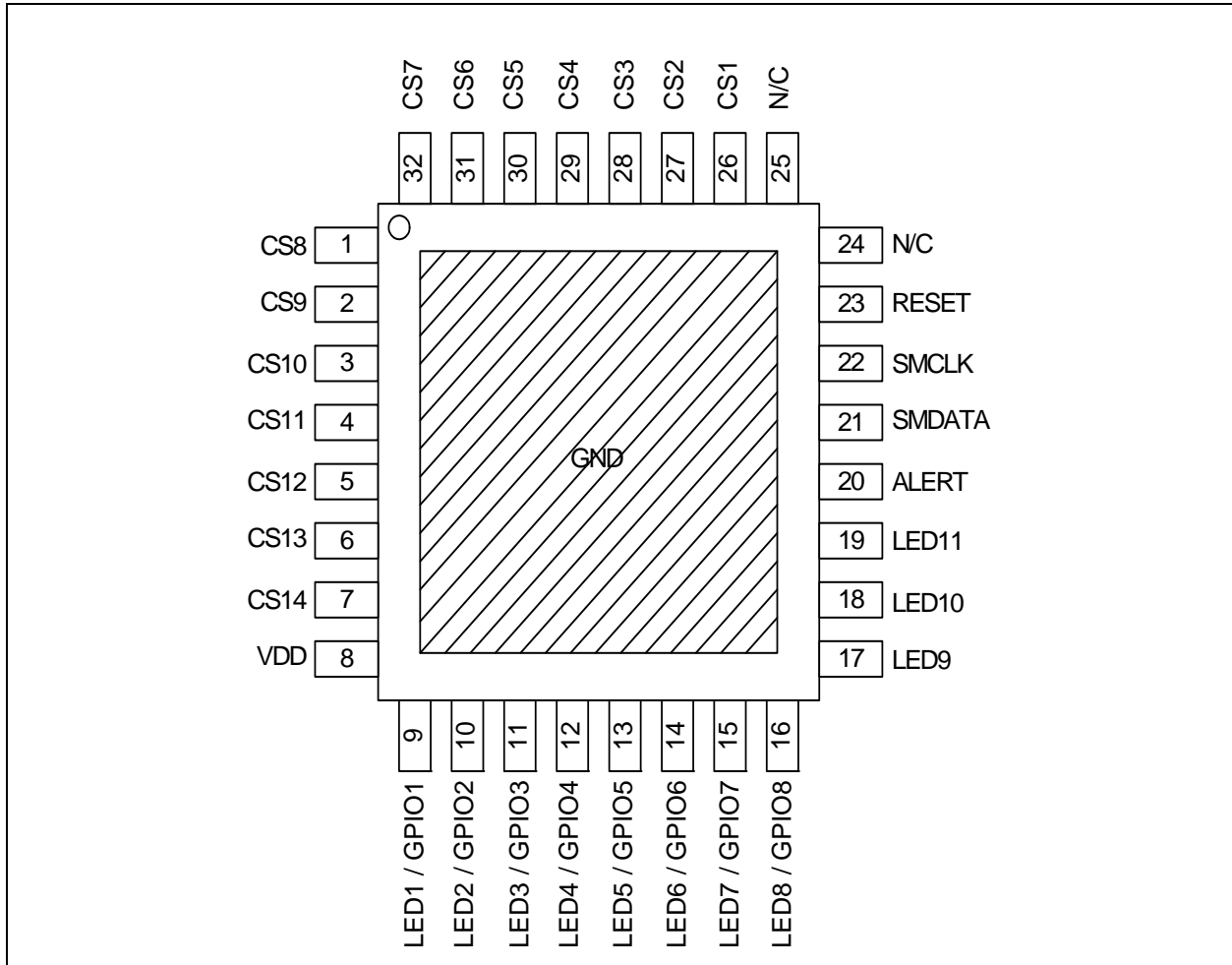


Figure 1.1 CAP1014 Pin Diagram (32-Pin QFN)

Table 1.1 Pin Description for CAP1014

| PIN NUMBER | PIN NAME | PIN FUNCTION | PIN TYPE |
|------------|----------|----------------------------|----------|
| 1 | CS8 | Capacitive Touch Sensor 8 | AIO |
| 2 | CS9 | Capacitive Touch Sensor 9 | AIO |
| 3 | CS10 | Capacitive Touch Sensor 10 | AIO |
| 4 | CS11 | Capacitive Touch Sensor 11 | AIO |
| 5 | CS12 | Capacitive Touch Sensor 12 | AIO |
| 6 | CS13 | Capacitive Touch Sensor 13 | AIO |
| 7 | CS14 | Capacitive Touch Sensor 14 | AIO |

Table 1.1 Pin Description for CAP1014 (continued)

| PIN NUMBER | PIN NAME | PIN FUNCTION | PIN TYPE |
|------------|---------------|---|-----------|
| 8 | VDD | Positive Power supply | Power |
| 9 | LED1 / GPIO1 | LED1 - Open drain LED driver (default) | OD (5V) |
| | | GPI1 - GPIO 1 Input | DI (5V) |
| | | GPO1 - GPIO 1 push-pull output | DO |
| 10 | LED2 / GPIO 2 | LED2 - Open drain LED driver (default) | OD (5V) |
| | | GPI2 - GPIO 2 Input | DI (5V) |
| | | GPO2 - GPIO 2 push-pull output | DO |
| 11 | LED3 / GPIO3 | LED3 - Open drain LED driver (default) | OD (5V) |
| | | GPI3 - GPIO 3 Input | DI (5V) |
| | | GPO3 - GPIO 3 push-pull output | DO |
| 12 | LED4 / GPIO4 | LED4 - Open drain LED driver (default) | OD (5V) |
| | | GPI4 - GPIO 4 Input | DI (5V) |
| | | GPO4 - GPIO 4 push-pull output | DO |
| 13 | LED5 / GPIO5 | LED5 - Open drain LED driver (default) | OD (5V) |
| | | GPI5 - GPIO 5 Input | DI (5V) |
| | | GPO5 - GPIO 5 push-pull output | DO |
| 14 | LED6 / GPIO6 | LED6 - Open drain LED driver (default) | OD (5V) |
| | | GPI6 - GPIO 6 Input | DI (5V) |
| | | GPO6 - GPIO 6 push-pull output | DO |
| 15 | LED7 / GPIO7 | LED7 - Open drain LED driver (default) | OD (5V) |
| | | GPI7 - GPIO 7 Input | DI (5V) |
| | | GPO7 - GPIO 7 push-pull output | DO |
| 16 | LED8 / GPIO8 | LED8 - Open drain LED driver (default) | OD (5V) |
| | | GPI8 - GPIO 8 Input | DI (5V) |
| | | GPO8 - GPIO 8 push-pull output | DO |
| 17 | LED9 | LED9 - Open drain LED driver | OD (5V) |
| 18 | LED10 | LED10 - Open drain LED driver | OD (5V) |
| 19 | LED11 | LED11 - Open drain LED driver | OD (5V) |
| 20 | ALERT | Active High Interrupt / Wake Up Input | DIO |
| 21 | SMDATA | Bi-directional SMBus data - requires pull-up resistor | DIOD (5V) |
| 22 | SMCLK | SMBus clock input - requires pull-up resistor | DI (5V) |

Table 1.1 Pin Description for CAP1014 (continued)

| PIN NUMBER | PIN NAME | PIN FUNCTION | PIN TYPE |
|--------------|----------|--|----------|
| 23 | RESET | Soft reset for system - resets all registers to default values | DI (5V) |
| 24 | N/C | Not Connected - connect to gnd | N/A |
| 25 | N/C | Not Connected - connect to gnd | N/A |
| 26 | CS1 | Capacitive Touch Sensor 1 | AIO |
| 27 | CS2 | Capacitive Touch Sensor 2 | AIO |
| 28 | CS3 | Capacitive Touch Sensor 3 | AIO |
| 29 | CS4 | Capacitive Touch Sensor 4 | AIO |
| 30 | CS5 | Capacitive Touch Sensor 5 | AIO |
| 31 | CS6 | Capacitive Touch Sensor 6 | AIO |
| 32 | CS7 | Capacitive Touch Sensor 7 | AIO |
| Bottom Plate | GND | Power Ground | Power |

The pin types are described in detail below. All pins labelled with (5V) are 5V tolerant.

Note: For all 5V tolerant pins that require a pull-up resistor, the voltage difference between VDD and the pull-up voltage must never exceed 3.6V.

Table 1.2 Pin Types

| PIN TYPE | DESCRIPTION |
|----------|--|
| Power | This pin is used to supply power or ground to the device. |
| DI | Digital Input - this pin is used as a digital input. This pin is 5V tolerant. |
| DIO | Digital Input Output - this pin is used as a digital input / output. |
| AIO | Analog Input / Output - this pin is used as an I/O for analog signals. |
| DIOD | Digital Input / Open Drain Output - this pin is used as an digital I/O. When it is used as an output, It is open drain and requires a pull-up resistor. This pin is 5V tolerant. |
| OD | Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant. |
| DO | Push-pull Digital Output - this pin is used as a digital output and can sink and source current |

Chapter 2 Electrical Specifications

Table 2.1 Absolute Maximum Ratings

| | | |
|---|------------------------|--------------------|
| Voltage on VDD pin | -0.3 to 4 | V |
| Voltage on 5V tolerant pins (V_{5VT_pin}) | -0.3 to 5.5 | V |
| Voltage on 5V tolerant pins ($ V_{5VT_pin} - V_{DD} $) (see Note 2.1) | 0 to 3.6 | V |
| Voltage on any other pin to GND | -0.3 to $V_{DD} + 0.3$ | V |
| Package Power Dissipation up to $T_A = 85^\circ\text{C}$ (see Note 2.2) | 1 | W |
| Junction to Ambient (θ_{JA}) (see Note 2.3) | 48 | $^\circ\text{C/W}$ |
| Operating Ambient Temperature Range | -40 to 125 | $^\circ\text{C}$ |
| Storage Temperature Range | -55 to 150 | $^\circ\text{C}$ |
| ESD Rating, All Pins, HBM | 8000 | V |

Note: Stresses above those listed could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note 2.1 For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the device is unpowered.

Note 2.2 The Package Power Dissipation specification assumes a thermal via design with the thermal landing be soldered to the PCB ground plane with 0.3mm (12mil) diameter vias in a 4x4 matrix at 0.9mm (35.4mil) pitch.

Note 2.3 Junction to Ambient (θ_{JA}) is dependent on the design of the thermal vias. Without thermal vias and a thermal landing, the θ_{JA} is approximately 60°C/W including localized PCB temperature increase.

Table 2.2 Electrical Specifications

| $V_{DD} = 3\text{V to } 3.6\text{V}, T_A = 0^\circ\text{C to } 100^\circ\text{C}$, all Typical values at $T_A = 27^\circ\text{C}$ unless otherwise noted. | | | | | | |
|--|--------------|-----|------|-----|---------------|---|
| CHARACTERISTIC | SYMBOL | MIN | TYP | MAX | UNIT | CONDITIONS |
| DC Power | | | | | | |
| Supply Voltage | V_{DD} | 3.0 | 3.3 | 3.6 | V | |
| Supply Current | I_{SLEEP} | | 220 | 300 | μA | Sleep Mode active, 2 sensors monitored |
| | I_{DSLEEP} | | 150 | 200 | μA | Deep Sleep or Deact modes active |
| | I_{DD} | | 0.42 | 1 | mA | Average current Capacitive Sensing Active, LEDs enabled |

Table 2.2 Electrical Specifications (continued)

| V _{DD} = 3V to 3.6V, T _A = 0°C to 100°C, all Typical values at T _A = 27°C unless otherwise noted. | | | | | | |
|--|---------------------|-----------------------|-----|-----|------|---|
| CHARACTERISTIC | SYMBOL | MIN | TYP | MAX | UNIT | CONDITIONS |
| Capacitive Touch Sensor | | | | | | |
| Base Capacitance | C _{BASE} | 5 | 15 | 50 | pF | Pad untouched |
| Detectable Capacitive Shift | ΔC _{TOUCH} | 0.1 | 0.4 | 2 | pF | Pad touched |
| Sample Time | t _{TOUCH} | | 2.5 | | ms | |
| Update Time | Δt _{TOUCH} | | 35 | | ms | |
| Recalibration Interval | Δt _{CAL} | | 8 | | s | Automatic Recalibration active, no touch active, Default settings |
| LED / GPIO Drivers (LED / GPIO 1 - 8) | | | | | | |
| Duty Cycle | DUTY _{LED} | 0 | | 100 | % | Programmable |
| Sinking Current | I _{SINK} | | | 24 | mA | V _{OL} = 0.4 |
| Sourcing Current | I _{SOURCE} | | | 24 | mA | V _{OH} = V _{DD} - 0.4 |
| Input High Voltage | V _{IH} | 2.0 | | | V | LED / GPIO configured as input |
| Input Low Voltage | V _{IL} | | | 0.8 | V | LED / GPIO configured as input |
| LED Drivers (LED 9 - LED 10) | | | | | | |
| Duty Cycle | DUTY _{LED} | 0 | | 100 | % | Programmable |
| Sinking Current | I _{SINK} | | | 24 | mA | |
| Output Low Voltage | V _{OL} | | | 0.4 | V | I _{SINK} = 24mA |
| LED11 Driver | | | | | | |
| Duty Cycle | DUTY _{LED} | 0 | | 100 | % | Programmable |
| Sinking Current | I _{SINK} | | | 48 | mA | |
| Output Low Voltage | V _{OL} | | | 0.4 | V | I _{SINK} = 48mA |
| I/O Pins - SMDATA, SMCLK, and ALERT Pins | | | | | | |
| Output Low Voltage | V _{OL} | | | 0.4 | V | I _{SINK_IO} = 8mA |
| Output High Voltage | V _{OH} | V _{DD} - 0.4 | | | V | ALERT pin active high and asserted I _{SOURCE_IO} = 8mA |
| Input High Voltage | V _{IH} | 2.0 | | | V | |
| Input Low Voltage | V _{IL} | | | 0.8 | V | |
| Leakage Current | I _{LEAK} | | | ±5 | uA | powered or unpowered T _A < 85°C pull-up voltage ≤ 3.6V |
| RESET Pin | | | | | | |
| Input High Voltage | V _{IH} | 2.0 | | | V | |

Table 2.2 Electrical Specifications (continued)

| V _{DD} = 3V to 3.6V, T _A = 0°C to 100°C, all Typical values at T _A = 27°C unless otherwise noted. | | | | | | |
|--|----------------------|-----|-----|-----|------|----------------------------------|
| CHARACTERISTIC | SYMBOL | MIN | TYP | MAX | UNIT | CONDITIONS |
| Input Low Voltage | V _{IL} | | | 0.8 | V | |
| RESET Pin assertion to device reset | t _{RST_OFF} | | 1 | 10 | us | |
| RESET Pin release to fully active operation | t _{RST_ON} | | 400 | 500 | ms | |
| SMBus Timing | | | | | | |
| Input Capacitance | C _{IN} | | 5 | | pF | |
| Clock Frequency | f _{SMB} | 10 | | 400 | kHz | |
| Spike Suppression | t _{SP} | | | 50 | ns | |
| Bus free time Start to Stop | t _{BUF} | 1.3 | | | us | |
| Setup Time: Start | t _{SU:STA} | 0.6 | | | us | |
| Setup Time: Stop | t _{SU:STP} | 0.6 | | | us | |
| Data Hold Time | t _{HD:DAT} | 0.6 | | 6 | us | |
| Data Setup Time | t _{SU:DAT} | 0.6 | | 72 | us | |
| Clock Low Period | t _{LOW} | 1.3 | | | us | |
| Clock High Period | t _{HIGH} | 0.6 | | | us | |
| Clock/Data Fall time | t _{FALL} | | | 300 | ns | Min = 20+0.1C _{LOAD} ns |
| Clock/Data Rise time | t _{RISE} | | | 300 | ns | Min = 20+0.1C _{LOAD} ns |
| Capacitive Load | C _{LOAD} | | | 400 | pF | per bus line |

Chapter 3 Communications

The CAP1014 communicates via the SMBus or I²C communications protocols.

APPLICATION NOTE: Upon power up, the CAP1014 will not respond to any SMBus communications for 10ms. After this time, full functionality is available.

3.1 System Management Bus Protocol

The CAP1014 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 3.1. Stretching of the SMCLK signal is supported, however the CAP1014 will not stretch the clock signal.

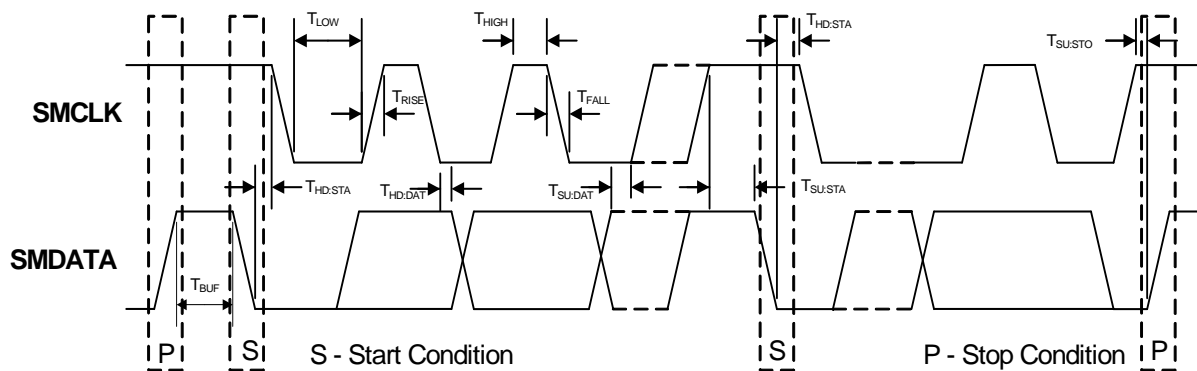


Figure 3.1 SMBus Timing Diagram

3.1.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic '1' state to a logic '0' state while the SMBus Clock line is in a logic '1' state.

3.1.2 SMBus Address and $\overline{RD/WR}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by the $\overline{RD/WR}$ indicator bit. If this $\overline{RD/WR}$ bit is a logic '0', then the SMBus Host is writing data to the client device. If this $\overline{RD/WR}$ bit is a logic '1', then the SMBus Host is reading data from the client device.

The CAP1014-1 responds to the slave address 0101_000xb. The CAP1014-2 responds to slave address 0101_100xb.

Multiple addressing options are available. For more information contact SMSC.

3.1.3 SMBus Data Bytes

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

3.1.4 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives. This is done by the client device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted. This applies to both the Write Byte and Block Write protocols

The Host will NACK (not acknowledge) the last data byte to be received from the client by holding the SMBus data line high after the 8th data bit has been sent. For the Block Read protocol, the Host will ACK each data byte that it receives except the last data byte.

3.1.5 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the CAP1014 detects an SMBus Stop bit, and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

3.1.6 SMBus Time-out

The CAP1014 includes an SMBus time-out feature. Following a 30ms period of inactivity on the SMBus where the SMCLK pin is held low, the device will time-out and reset the SMBus interface.

The time-out function defaults to disabled. It can be enabled by setting the TIMEOUT bit in the Configuration register (see [Section 5.14](#)).

3.1.7 SMBus and I²C Compliance

The major difference between SMBus and I²C devices is highlighted here. For complete compliance information refer to the SMBus 2.0 specification.

1. Minimum frequency for SMBus communications is 10kHz.
2. The client protocol will reset if the clock is held low longer than 30ms.
3. The client protocol will reset if both the clock and the data line are high for longer than 150us (idle condition).
4. I²C devices do not support the Alert Response Address functionality (which is optional for SMBus).

3.2 SMBus Protocols

The CAP1014 is SMBus 2.0 compatible and supports Send Byte, Read Byte, Block Read, Receive Byte as valid protocols as shown below. The CAP1014 also supports the I²C block read and block write protocols. Finally, it will respond to the Alert Response Address protocol but is not in full compliance.

All of the below protocols use the convention in [Table 3.1](#).

Table 3.1 Protocol Format

| DATA SENT TO DEVICE | DATA SENT TO THE HOST |
|---------------------|-----------------------|
| Data sent | Data sent |

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3.2.1 SMBus Write Byte

The Write Byte is used to write one byte of data to a specific register as shown in [Table 3.2](#).

Table 3.2 Write Byte Protocol

| START | CLIENT ADDRESS | WR | ACK | REGISTER ADDRESS | ACK | REGISTER DATA | ACK | STOP |
|--------|----------------|----|-----|------------------|-----|---------------|-----|--------|
| 1 -> 0 | 0101_000 | 0 | 0 | XXh | 0 | XXh | 0 | 0 -> 1 |

3.2.2 Block Write

The Block Write is used to write multiple data bytes to a group of contiguous registers as shown in [Table 3.3](#). It is an extension of the Write Byte Protocol.

APPLICATION NOTE: When using the Block Write protocol, the internal address pointer will be automatically incremented after every data byte is received. It will wrap from FFh to 00h.

Table 3.3 Block Write Protocol

| START | CLIENT ADDRESS | WR | ACK | REGISTER ADDRESS | ACK | REGISTER DATA | ACK |
|---------------|----------------|---------------|-----|------------------|---------------|---------------|--------|
| 1 -> 0 | 0101_000 | 0 | 0 | XXh | 0 | XXh | 0 |
| REGISTER DATA | ACK | REGISTER DATA | ACK | ... | REGISTER DATA | ACK | STOP |
| XXh | 0 | XXh | 0 | ... | XXh | 0 | 0 -> 1 |

3.2.3 SMBus Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in [Table 3.4](#).

Table 3.4 Read Byte Protocol

| START | CLIENT ADDRESS | WR | ACK | REGISTER ADDRESS | ACK | START | CLIENT ADDRESS | RD | ACK | REGISTER DATA | NACK | STOP |
|-------|----------------|----|-----|------------------|-----|-------|----------------|----|-----|---------------|------|--------|
| 1->0 | 0101_000 | 0 | 0 | XXh | 0 | 1->0 | 0101_000 | 1 | 0 | XXh | 1 | 0 -> 1 |

3.2.4 Block Read

The Block Read is used to read multiple data bytes from a group of contiguous registers as shown in [Table 3.5](#). It is an extension of the Read Byte Protocol.

APPLICATION NOTE: When using the Block Read protocol, the internal address pointer will be automatically incremented after every data byte is received. It will wrap from FFh to 00h.

Table 3.5 Block Read Protocol

| START | CLIENT ADDRESS | WR | ACK | REGISTER ADDRESS | ACK | START | CLIENT ADDRESS | RD | ACK | REGISTER DATA |
|-------|----------------|-----|---------------|------------------|---------------|-------|----------------|---------------|------|---------------|
| 1->0 | 0101_000 | 0 | 0 | XXh | 0 | 1->0 | 0101_000 | 1 | 0 | XXh |
| ACK | REGISTER DATA | ACK | REGISTER DATA | ACK | REGISTER DATA | ACK | ... | REGISTER DATA | NACK | STOP |
| 0 | XXh | 0 | XXh | 0 | XXh | 0 | ... | XXh | 1 | 0->1 |

3.2.5 SMBus Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in [Table 3.6](#).

Table 3.6 Send Byte Protocol

| START | CLIENT ADDRESS | WR | ACK | REGISTER ADDRESS | ACK | STOP |
|-------|----------------|----|-----|------------------|-----|------|
| 1->0 | 0101_000 | 0 | 0 | XXh | 0 | 0->1 |

3.2.6 SMBus Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in [Table 3.7](#).

Table 3.7 Receive Byte Protocol

| START | CLIENT ADDRESS | RD | ACK | REGISTER DATA | NACK | STOP |
|-------|----------------|----|-----|---------------|------|------|
| 1->0 | 0101_000 | 1 | 0 | XXh | 1 | 0->1 |

Chapter 4 Product Description

The CAP1014 is a multiple channel Capacitive Touch sensor and LED Driver.

The CAP1014 contains up to 14 individual Capacitive Touch sensor inputs with programmable sensitivity for use in touch button and slider switch applications. Each sensor also contains automatic recalibration.

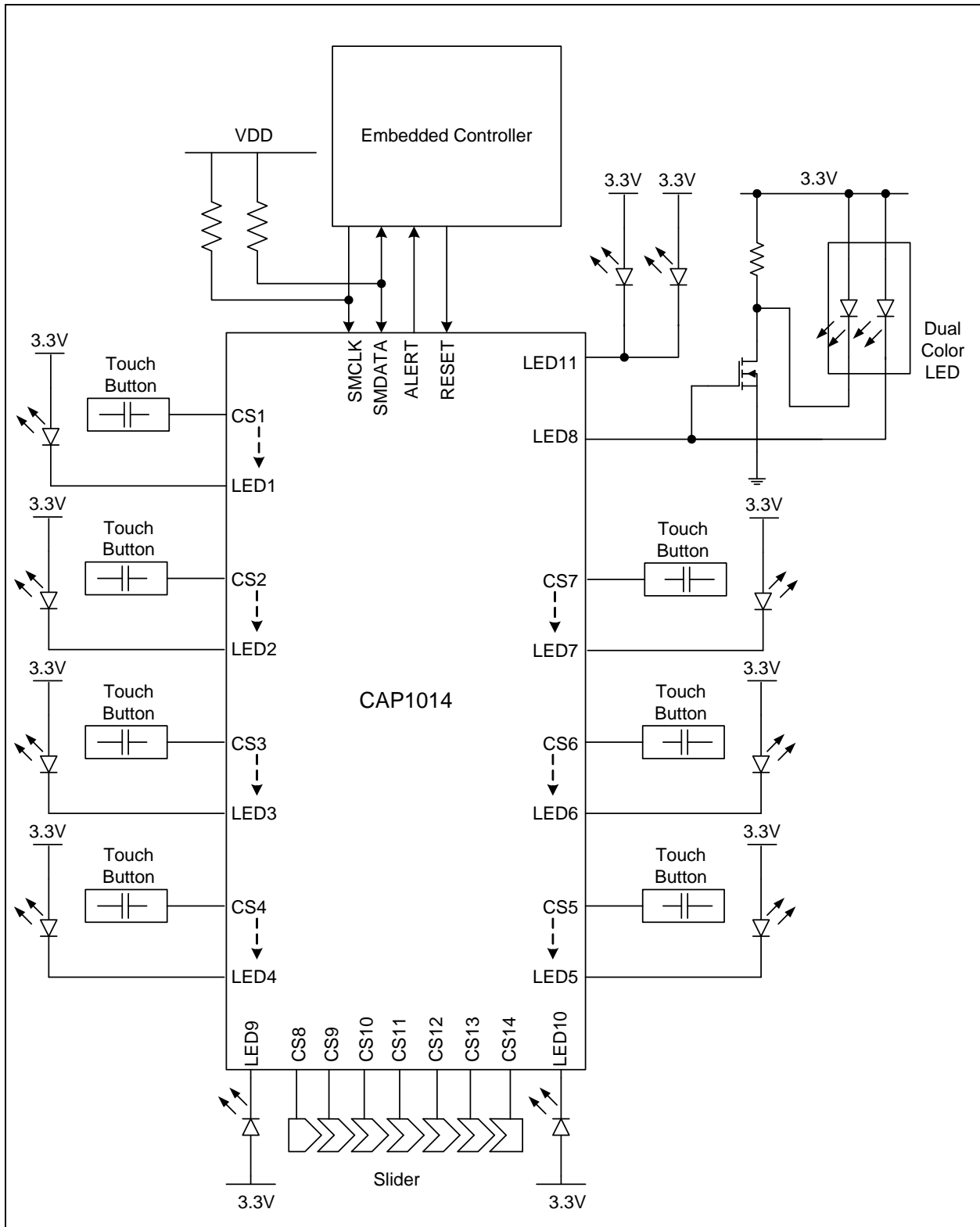
The CAP1014 also contains eleven (11) open drain LED drivers that offer full-on / off, variable rate breathing, and dimness controls. Eight (8) of these LEDs can double as GPIOs and support open-drain or push-pull operation. Capacitive buttons can be linked to LED outputs. Additionally, LEDs 1-7 may be optionally linked to Buttons 1-7 so that when a touch is detected, the LED is actuated.

The device communicates with a host controller using SMBus. The host controller may poll the device for updated information at any time or it may configure the device to flag an interrupt whenever a press is detected on any sensor.

Each sensor is polled by the device approximately every 35 ms. The host may also initiate a recalibration routine for one or more sensors or set up times and conditions so that the device automatically invokes the re-calibration routine.

The CAP1014 contains multiple power states including several low power operating modes. In addition, it contains a user driven RESET pin to force the device to reset.

A typical system diagram is shown in [Figure 4.1](#).


Figure 4.1 System Diagram for CAP1014

4.1 Power States

The CAP1014 has four operating states depending on the status of the SLEEP, DEACT, and DSLEEP bits (see [Section 5.1](#)). They are described below and summarized in [Table 4.1](#). When the device transitions between power states, previously detected touches (for deactivated channels) are cleared and the status bits reset.

1. Fully Active - The device is fully active. It is monitoring all active Capacitive Sensor channels and driving all LED channels as defined.
2. Sleep - The device is in Sleep Mode. It is monitoring a limited number of Capacitive Sensor channels (default 0). Interrupts will still be generated based on the active channels. The device will still respond to SMBus commands normally and can be returned to the Fully Active mode by clearing the SLEEP bit. The LED11 channel is controlled via the PWR_LED control (see [Section 5.1](#)). All other LEDs will not be affected.
3. Deep Sleep - The device is in Deep Sleep mode. It is not monitoring any Capacitive Sensor channels or the SMBus. The LED11 channel is controlled via the PWR_LED control (see [Section 5.1](#)). All other LEDs will have PWM controls suspended so they should be disabled prior to entering this mode. If these LEDs are not disabled, then the system will show excess current draw from these LEDs.

When the device leaves the Deep Sleep mode (by externally driving the ALERT pin to its active state), then it automatically returns to its defined state and clears the DSLEEP bit. When the device enters the Deep Sleep mode, it will release control to the ALERT pin and will change the direction of the ALERT pin (i.e. the device will monitor the ALERT pin instead of driving it).

4. Inactive - The device is inactive. It is not monitoring any Capacitive Sensor channels. The device will still respond to SMBus commands normally and can be returned to Fully Active Mode by clearing the DEACT bit. All LEDs will have PWM controls suspended so they should be disabled prior to entering this mode. If these LEDs are not disabled, then the system will show excess current draw from these LEDs.

Table 4.1 Power Modes

| POWER MODE | DEACT | SLEEP | DSLEEP |
|-----------------------------------|-------|-------|--------|
| Fully Active | 0 | 0 | 0 |
| Deep Sleep waking to Fully Active | 0 | 0 | 1 |
| Sleep | 0 | 1 | 0 |
| Deep Sleep waking to Sleep | 0 | 1 | 1 |
| Inactive | 1 | 0 | 0 |
| Deep Sleep waking to Inactive | 1 | 0 | 1 |
| Inactive | 1 | 1 | 0 |
| Deep Sleep waking to Inactive | 1 | 1 | 1 |

The priority of power control signals is:

1. DSLEEP - when set will override DEACT, disable all LEDs except LED11 then disable SMBus communications.
2. DEACT - when set, will override the SLEEP controls. It will disable sensor measurement and all LEDs.
3. SLEEP - when set, will enable Sleep mode.

4.2 RESET Pin

The RESET pin is an active high reset that is driven from an external source. While it is asserted high, all the internal blocks will be held in reset including the SMBus. All configuration settings will be reset to default states and all readings will be cleared. Once the RESET pin is pulled low, the CAP1014 will begin operation as if a power-on-reset had occurred.

4.3 LED Drivers

The CAP1014 contains eleven (11) LED Drivers. Each LED Driver is controlled independently of the others and may be linked to the corresponding Capacitive Touch Sensor inputs. In addition, LED drivers 1 - 8 can be configured to operate in one of the following modes with either push-pull or open-drain drive. LED drivers 9 - 11 will only operate in as an open-drain driver.

1. Direct - The LED is configured to be on or off when the corresponding button is pressed or not pressed. The dimness of both “on” states and “off” states can be programmed as well as the rising and falling ramp times and delay when the corresponding button is released
2. Breathe - The LED is configured to breathe. Over the course of the programmed cycle the LED will transition from the programmed minimum to the programmed maximum and then back off again. This mode operates independently of any stimuli or may be linked so that the LED breathes when the stimuli is asserted (or deasserted). This feature is commonly used for power LEDs when in standby mode.
3. Pulse - The LED is configured to breathe 5 times with a programmable rate and dimness controls. This mode is linked to a button press detection or release.

LED11 operates differently than the other LED outputs in three ways. First, it is configured to drive up to two external LED channels simultaneously. Second, it is not disabled during the Sleep or Deep Sleep modes of operation (see [Section 5.1](#)) and allows for different behaviors when the device is in Fully Active Mode versus when the device is in Sleep or Deep Sleep mode.

4.3.1 Linking LEDs to Capacitive Touch Sensors

LEDs 1 - 7 can be optionally linked to Capacitive Touch Sensors 1-7 so that when the sensor detects a button press, the corresponding LED will be actuated at one of the programmed responses.

4.4 Capacitive Touch Sensing

The CAP1014 contains 14 independent Capacitive Touch Sensor inputs. Each sensor has dynamic range to detect a change of capacitance due to a touch. Additionally, each sensor can be configured to be automatically and routinely re-calibrated.

4.4.1 Multiple Button Presses

If multiple sensor buttons (with a programmable threshold - see [Section 5.23](#)) are simultaneously detected, then only the first N buttons that are detected are flagged. All other buttons are ignored. Furthermore, the device remembers which buttons were legitimate so new touches are not detected so long as N buttons are pressed.

Likewise, if too many (based on the programmed threshold - see [Section 5.23](#)) grouped sensor presses are detected, then the device will block all press detections on the grouped buttons and cancel any current presses as if the sensor had been released.

4.4.2 Lid Closure

To detect lid closure or other similar events, lid closure sensor thresholds can be set. A Lid Closure Event can be flagged based on either a minimum number of sensors or on specific sensors

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simultaneously exceeding the lid closure threshold. An interrupt can also be generated. During a Lid Closure Event all touches are blocked.

4.4.3 Grouped Sensors

Capacitive Touch Sensors 8 through 14 inclusive are automatically grouped as a single entity. Each sensor is sampled independently, however for purposes of activation, recalibration, and repeat rates, all of them are treated as one group. The Group also has different controls and allows for different behavior such as sliding, tapping, or press and hold.

4.4.4 Sensing Cycle

Each Capacitive Touch Sensor has controls to be activated and included in the sensing cycle. When the device is active, it automatically initiates a sensing cycle and repeats the cycle every time it finishes. The cycle polls through each active Sensor starting with CS1 and extending through CS14. As each Capacitive Touch Sensor is polled, its measurement is compared against a baseline “not touched” measurement. If the delta measurement is large enough, then a touch is detected and an interrupt generated.

4.4.5 Recalibrating Sensors

Each sensor is regularly recalibrated at an adjustable rate. By default, the recalibration routine stores the average 256 previous measurements and periodically updates the base “Not Touched” setting for the Capacitive Touch Sensor input. This routine is disabled automatically if a touch is detected so the touch does not factor into the base “Not Touched” setting.

4.5 Grouped Sensor Behavior

The CAP1014 Grouped sensors function as a single entity that operates differently than the individual button sensors. This group functions as a slider and offers three different interface functions associated with it.

4.5.1 Tap

If a touch on any Grouped sensor is detected and held for less than or equal to the M_PRESS bit settings (default 245ms), then a group press is detected, the TAP bit is set, and an interrupt is generated. Furthermore, the relative position on the slider is determined and the appropriate UP or DOWN status bits are set and the appropriate LED is actuated.

No further action is taken. If a slide is subsequently detected, then the TAP status bit is cleared.

4.5.2 Press and Hold

If a touch on any Grouped sensor is held for longer than the M_PRESS bit settings (default 245ms), then a Group Touch is detected and an interrupt is generated. Furthermore, the relative position on the slider is determined and the appropriate UP or DOWN status bits are set, the PH bit is set, and the appropriate LED is actuated.

So long as the Grouped sensor is held, it will flag an interrupt at the programmed repeat rate (as determined by the RPT_RATE_PH bit settings) indefinitely. Once the touch has been removed, then the Group is returned to its normal operating condition.

The M_PRESS setting is important to distinguish between Tap, Press & Hold and Sliding. If M_PRESS is set too low, a Press & Hold may be detected during a slow slide. This will cause user confusion as the Slide direction and LED may change. Longer M_PRESS settings will ensure that the 3 Group behaviors are reliably distinct and will add more delay prior to the Press & Hold repeat interrupt generation.

4.5.3 Slider

The Grouped sensors have the capability to detect a slide in either the “Up” or “Down” direction as referenced by the sensor numbers that are used. For example, an “Up” direction slide would be detected if CS8 detected a touch, followed by CS9, then by CS10 etc. Likewise, a “Down” direction slide would be detected if CS10 detected a touch, followed by CS9, then by CS8 etc.

Slides in either direction are configured to flag an interrupt and to cause an LED to be actuated (separate for each direction). The Slide is detected independently of a Press and Hold or a Tap condition and only one condition may be present at any one time.

So long as a slide is maintained in either direction, it will flag an interrupt at the programmed repeat rate (as determined by the RPT_RATE_SL bit settings). If the slide is removed or changes direction, then it will reset and return to normal operation.

4.5.4 Relative Position

The CAP1014 has the option to indicate the relative position of a touch on the Grouped sensors. This value is stored either as a scaled number from 2 to 98 indicating where a tap, press and hold, or the end of a slide was detected or as a 8-bit number that represents volumetric data. When configured to store volumetric data, the user may write a base setting at any time that is modified based on Grouped sensor behavior (see [Section 5.4](#)).

4.5.5 Slider Velocity

The repeat rate can be dynamically increased based on the speed of a slide. This permits slow sliding motions to have precise, step-by-step volume control and faster motions to generate increasingly fast volume changes.

Two techniques are employed to make increase the number of interrupts generated based on speed. First, the slide speed is measured and the repeat rate is increased to provide more interrupts for the same distance traveled relative to a slower slide. Second, additional interrupts are generated immediately after the slide ends to further increase the change in volume. The number of additional interrupts is based on slide speed; both of these dynamic slider behaviors are controlled by the Slider Velocity Register.

4.6 ALERT Pin

The ALERT pin is an active high output that is driven high when an interrupt event is detected. It is also used to wake the device from Deep Sleep mode.

Whenever an interrupt is generated, the INT bit (see [Section 5.1](#)) is set. The ALERT pin is cleared when INT bit is cleared by the user. Additionally, when the INT bit is cleared by the user status bits are cleared only if no press is detected.

4.6.1 Button Interrupt Behavior

For non-grouped buttons, an interrupt is generated when a touch is detected. If the repeat rate is enabled (see [Section 5.14](#)), then, so long as the touch is held, another interrupt will be generated based on the programmed repeat rate (see [Figure 4.2](#)). An interrupt will be generated whenever a release is detected (see [Figure 4.3](#)).

4.6.2 Grouped Sensor Interrupt Behavior

For grouped sensors, an interrupt is generated upon initial detection of a tap, slide, or press and hold event. Then, subsequent interrupts are generated as follows:

1. For a slide event, an interrupt is generated based on the programmed repeat rate as well as the velocity of the slide operation. See [Figure 4.6](#) and [Figure 4.7](#). Additionally, additional interrupts are

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generated after the slide has finished. These extra interrupts are generated every round robin cycle (~35ms) and the number is determined by the speed of the slide.

- For a tap event there are no further interrupts. See [Figure 4.4](#).
- For a press and hold event, interrupts are generated based on the programmed repeat rate. If the repeat rate is disabled, then no further interrupts are generated. See [Figure 4.5](#).

4.6.3 Wake from Deep Sleep

This pin is also used to wake the device from the Deep Sleep power state if it is driven high from an external source. When the device enters the Deep Sleep power state, the ALERT pin output is put into a High Z mode. It requires a pull-down resistor to pull it to the inactive state. Furthermore, the CAP1014 will wait 5ms before it samples the ALERT pin for wake activity.

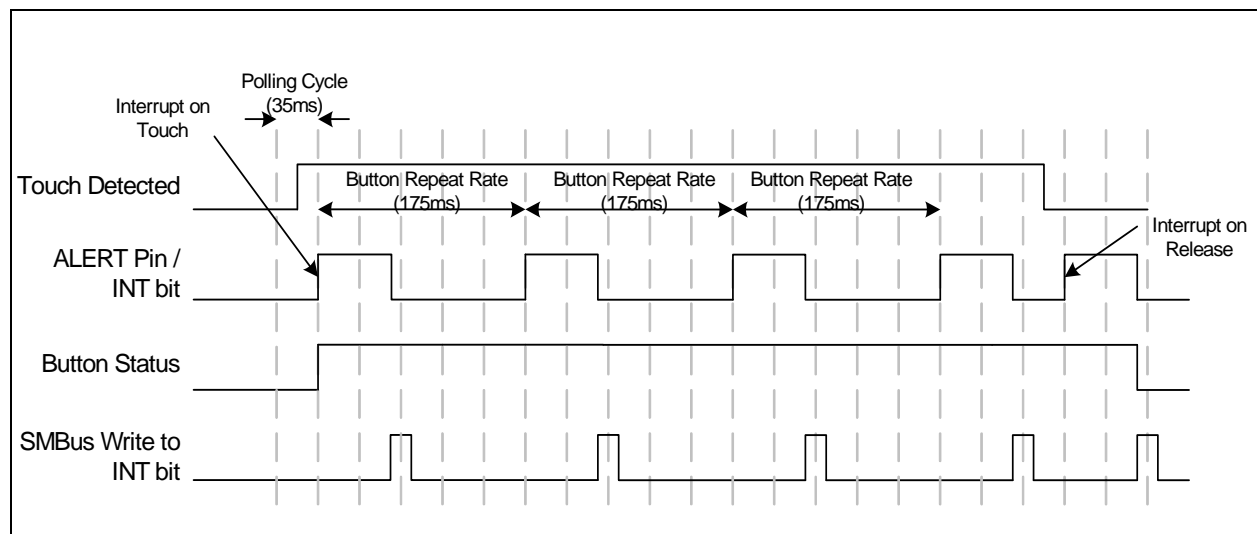


Figure 4.2 Button Interrupt Behavior - Repeat Rate Enabled (default)

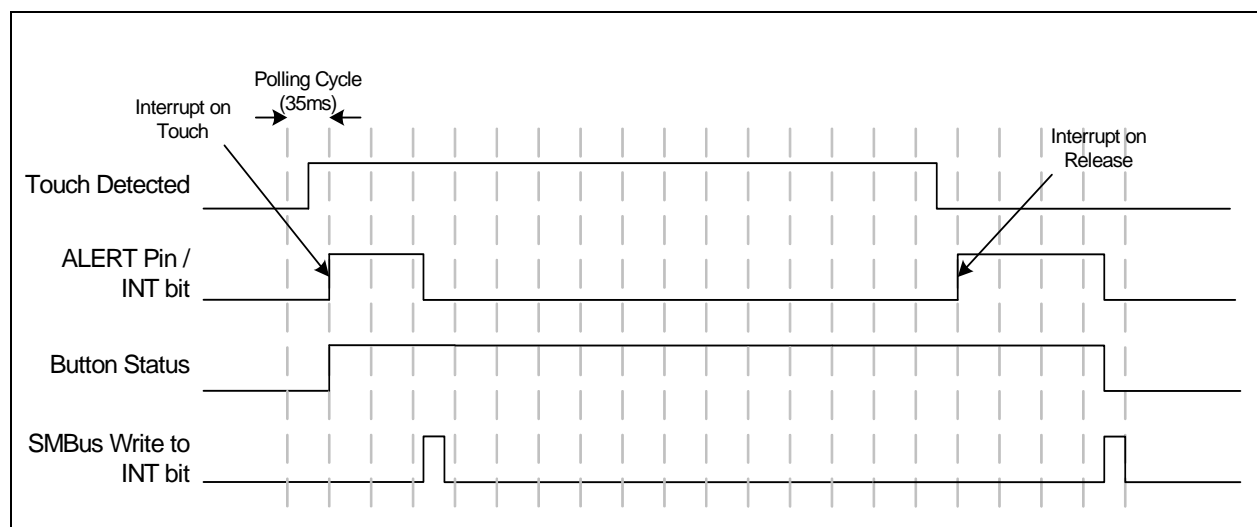
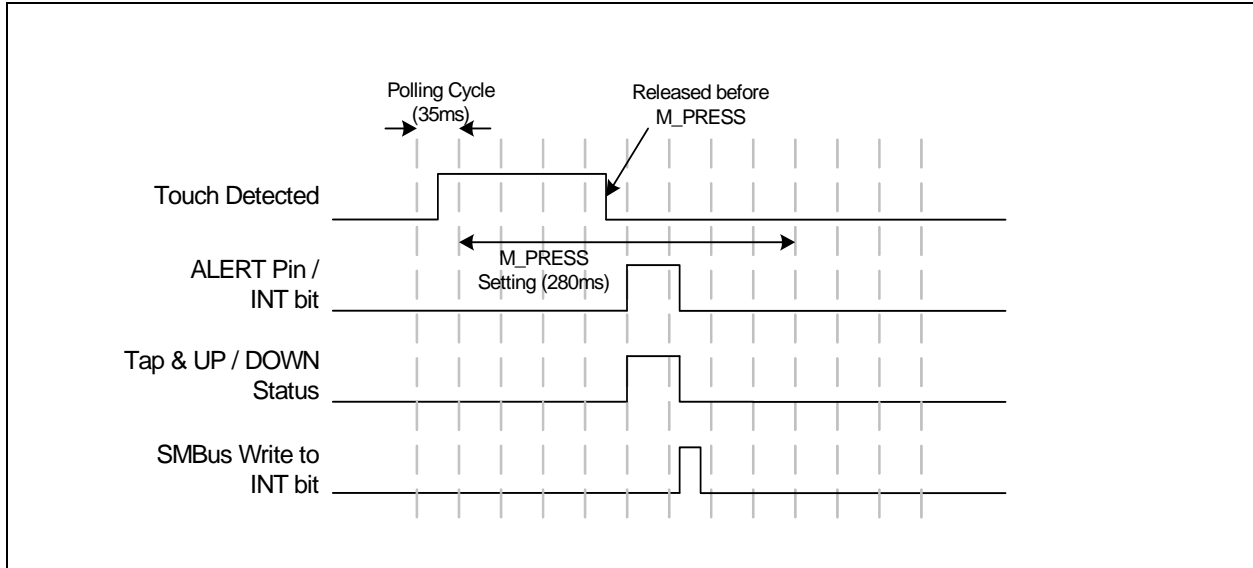
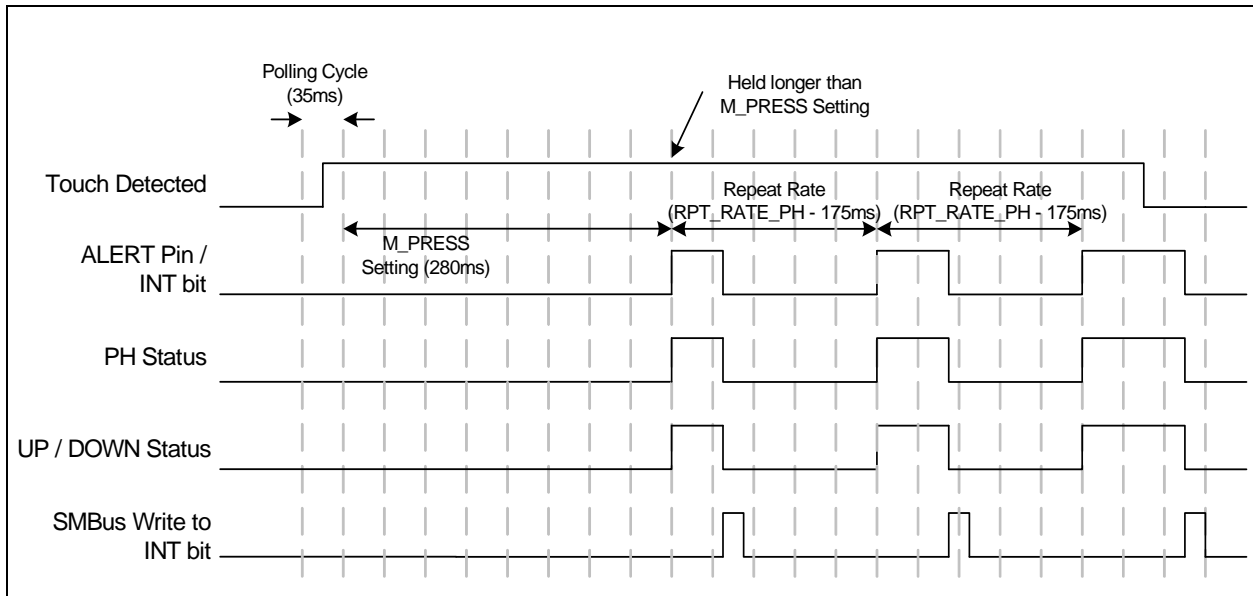


Figure 4.3 Button Interrupt Behavior - No Repeat Rate Enabled


Figure 4.4 Tap Interrupt Behavior

Figure 4.5 Press and Hold Interrupt Behavior

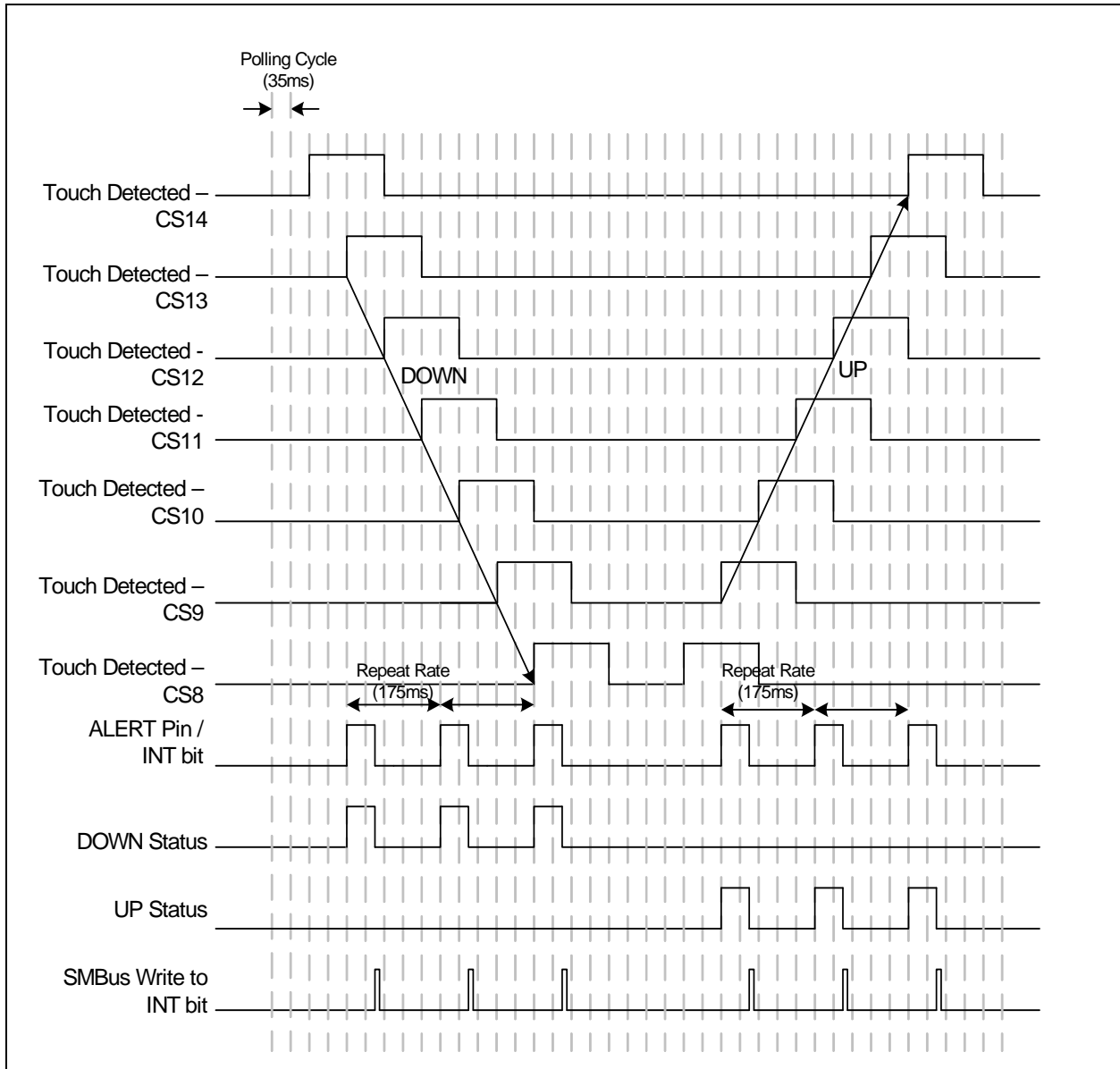
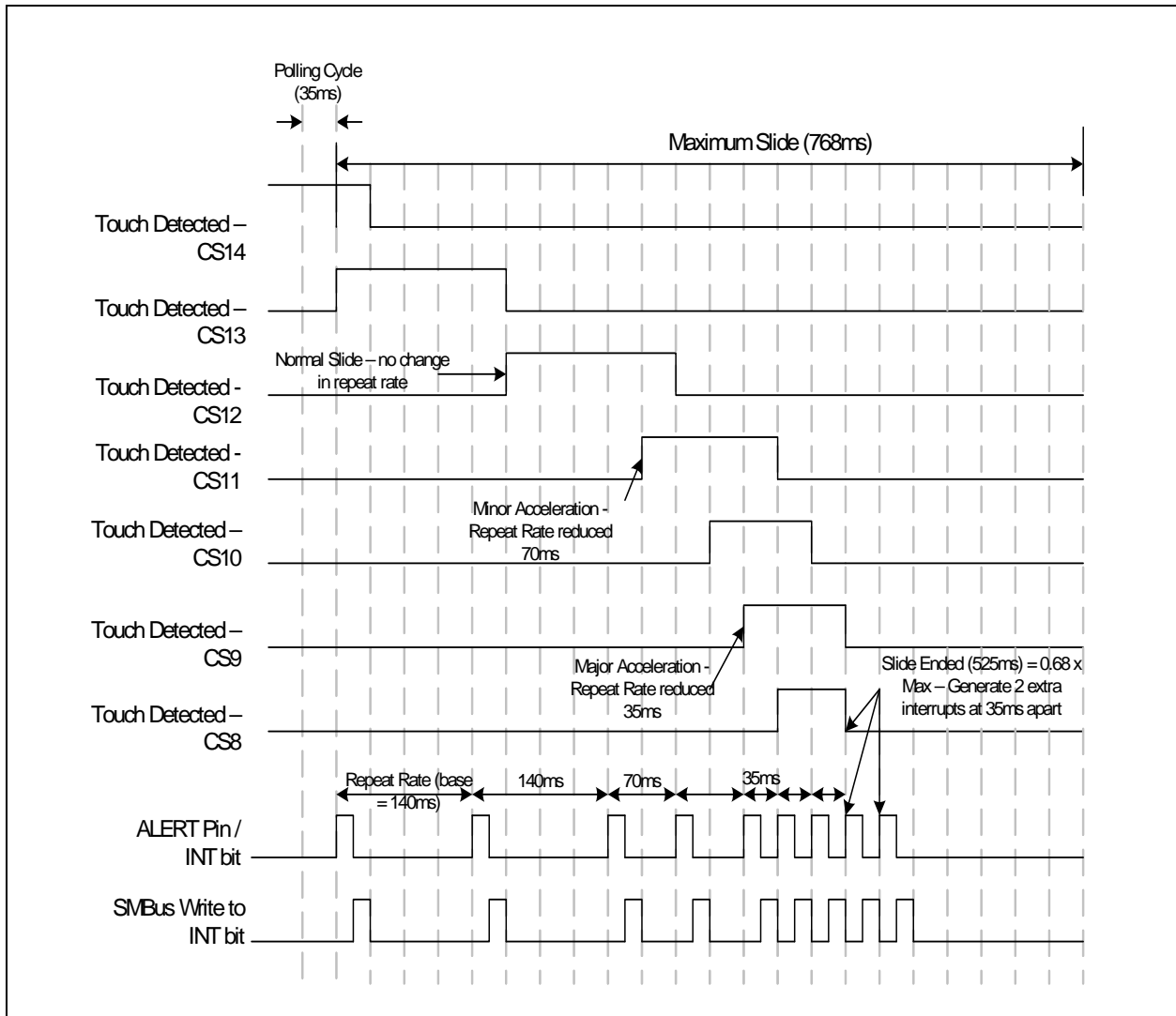


Figure 4.6 Slide Interrupt Behavior - No Acceleration


Figure 4.7 Slide Interrupt Behavior - Acceleration Example

Chapter 5 Register Description

The registers shown in [Table 5.1](#) are accessible through the SMBus. An entry of '-' indicates that the bit is not used and will always read '0'.

Table 5.1 Register Set in Hexadecimal Order

| REGISTER ADDRESS | R/W | REGISTER NAME | FUNCTION | DEFAULT VALUE | PAGE |
|------------------|-----------|-----------------------------------|---|---------------|-------------------------|
| 00h | R/W | Main Status Control | Controls general sleep states and power dissipation | 00h | Page 34 |
| 03h | R | Button Status 1 | Returns the state of the Cap Sensor group and buttons 1 - 6 and slider controls | 00h | Page 35 |
| 04h | R | Button Status 2 | Returns the state of buttons 7 - 14 | 00h | Page 35 |
| 05h | R | Build Revision | Stores the functional revision of the device build | 1Xh | Page 36 |
| 06h | R-C / R/W | Slider Position / Volumetric Data | Returns the relative position of a press on the slider or volumetric data | 00h | Page 37 |
| 08h | R | Vendor ID | Stores a fixed value that Identifies SMSC | 5Dh | Page 38 |
| 09h | R/W | Volumetric Step | Controls the step used for volumetric data increases for a slide | 01h | Page 38 |
| 0Ah | R | Noise Flag Status 1 | Stores the noise flags for sensors 1 - 7 | 00h | Page 39 |
| 0Bh | R | Noise Flag Status 2 | Stores the noise flags for sensors 8 - 14 | 00h | Page 39 |
| 0Ch | R | Lid Closure Status 1 | Stores lid closure status bits for sensors 1 - 7 | 00h | Page 39 |
| 0Dh | R | Lid Closure Status 2 | Stores lid closure status bits for sensors 8 - 14 | 00h | Page 39 |
| 0Eh | R-C | GPIO Status | Stores the status of LED1 / GPIO1 through LED8 / GPIO8 pins | 00h | Page 40 |
| 0Fh | R-C | Group Status | Returns the state of the Grouped sensors | 00h | Page 40 |
| 10h | R | Sensor 1 Delta Count | Stores the delta count for CS1 | 00h | Page 41 |
| 11h | R | Sensor 2 Delta Count | Stores the delta count for CS2 | 00h | Page 41 |
| 12h | R | Sensor 3 Delta Count | Stores the delta count for CS3 | 00h | Page 41 |
| 13h | R | Sensor 4 Delta Count | Stores the delta count for CS4 | 00h | Page 41 |

Table 5.1 Register Set in Hexadecimal Order (continued)

| REGISTER ADDRESS | R/W | REGISTER NAME | FUNCTION | DEFAULT VALUE | PAGE |
|------------------|-----|-----------------------|--|---------------|-------------------------|
| 14h | R | Sensor 5 Delta Count | Stores the delta count for CS5 | 00h | Page 41 |
| 15h | R | Sensor 6 Delta Count | Stores the delta count for CS 6 | 00h | Page 41 |
| 16h | R | Sensor 7 Delta Count | Stores the delta count for CS7 | 00h | Page 41 |
| 17h | R | Sensor 8 Delta Count | Stores the delta count for CS8 | 00h | Page 41 |
| 18h | R | Sensor 9 Delta Count | Stores the delta count for CS9 | 00h | Page 41 |
| 19h | R | Sensor 10 Delta Count | Stores the delta count for CS10 | 00h | Page 41 |
| 1Ah | R | Sensor 11 Delta Count | Stores the delta count for CS11 | 00h | Page 41 |
| 1Bh | R | Sensor 12 Delta Count | Stores the delta count for CS12 | 00h | Page 41 |
| 1Ch | R | Sensor 13 Delta Count | Stores the delta count for CS13 | 00h | Page 41 |
| 1Dh | R | Sensor 14 Delta Count | Stores the delta count for CS14 | 00h | Page 41 |
| 1Eh | R/W | Queue Control | Controls how many samples must exceed touch threshold for Button press detections | 03h | Page 42 |
| 1Fh | R/W | Data Sensitivity | Controls the sensitivity of the threshold and delta counts and data scaling of the base counts | 2Fh | Page 42 |
| 20h | R/W | Configuration | Controls some recalibration and LED controls | 2Dh | Page 44 |
| 21h | R/W | Sensor Enable | Controls whether the Capacitive Touch Sensor group and button inputs 1 - 7 are sampled | FFh | Page 45 |
| 22h | R/W | Button Configuration | Controls reset delay and auto-repeat delay for buttons | A4h | Page 46 |
| 23h | R/W | Group Configuration 1 | Controls the detection dwell time before a press is detected within the group | 47h | Page 47 |
| 24h | R/W | Group Configuration 2 | Controls reset delay and auto-repeat delay for grouped sensors | D4h | Page 48 |
| 25h | R/W | Calibration Enable | Controls automatic calibration for grouped sensors and sensors 1 - 7 | FFh | Page 48 |
| 26h | R/W | Calibration Activate | Activates manual re-calibration for grouped sensors and sensors 1 - 7 | 00h | Page 49 |

Table 5.1 Register Set in Hexadecimal Order (continued)

| REGISTER ADDRESS | R/W | REGISTER NAME | FUNCTION | DEFAULT VALUE | PAGE |
|------------------|-----|------------------------------|---|---------------|-------------------------|
| 27h | R/W | Interrupt Enable 1 | Enables Interrupts associated with the grouped sensors and sensors 1 - 7 | FFh | Page 49 |
| 28h | R/W | Interrupt Enable 2 | Enables Interrupts associated with GPIOs 1 - 8 | 00h | Page 49 |
| 29h | R/W | Sleep Channel Control | Determines the number and which channels are measured during Sleep Mode | 00h | Page 51 |
| 2Ah | R/W | Multiple Press Configuration | Determines the number of simultaneous presses to flag a multiple press condition | 82h | Page 51 |
| 2Bh | R/W | Lid Closure Configuration | Controls Lid Closure detection and operation | 00h | Page 52 |
| 2Ch | R/W | Lid Closure Queue Control | Controls how many samples must exceed the lid closure threshold for Button and Slider operation | 02h | Page 53 |
| 2Dh | R/W | Lid Closure Pattern 1 | Stores pattern bits for lid closure detection for channels 1 - 7 | 7Fh | Page 53 |
| 2Eh | R/W | Lid Closure Pattern 2 | Stores pattern bits for lid closure detection for channels 8 - 14 | 7Fh | Page 53 |
| 2Fh | R/W | Recalibration Configuration | Determines re-calibration timing and sampling window | 93h | Page 54 |
| 30h | R/W | Sensor 1 Threshold | Stores the delta count threshold to determine a touch for Capacitive Touch Sensor 1 | 40h | Page 55 |
| 31h | R/W | Sensor 2 Threshold | Stores the delta count threshold to determine a touch for Capacitive Touch Sensor 2 | 40h | Page 55 |
| 32h | R/W | Sensor 3 Threshold | Stores the delta count threshold to determine a touch for Capacitive Touch Sensor 3 | 40h | Page 55 |
| 33h | R/W | Sensor 4 Threshold | Stores the delta count threshold to determine a touch for Capacitive Touch Sensor 4 | 40h | Page 55 |
| 34h | R/W | Sensor 5 Threshold | Stores the delta count threshold to determine a touch for Capacitive Touch Sensor 5 | 40h | Page 55 |
| 35h | R/W | Sensor 6 Threshold | Stores the delta count threshold to determine a touch for Capacitive Touch Sensor 6 | 40h | Page 55 |
| 36h | R/W | Sensor 7 Threshold | Stores the delta count threshold to determine a touch for Capacitive Touch Sensor 7 | 40h | Page 55 |
| 37h | R/W | Group Threshold | Stores the delta count threshold to determine a touch on any of the Grouped Sensors | 40h | Page 55 |

Table 5.1 Register Set in Hexadecimal Order (continued)

| REGISTER ADDRESS | R/W | REGISTER NAME | FUNCTION | DEFAULT VALUE | PAGE |
|------------------|--------------|-------------------------------|---|---------------|-------------------------|
| 38h | R/W (unlock) | Button Noise Threshold 1 | Stores controls for selecting the noise threshold for buttons 1 - 4 | 55h | Page 56 |
| 39h | R/W (unlock) | Button Noise Threshold 2 | Stores controls for selecting the noise threshold for buttons 5 - 7 and the Grouped sensors | 55h | Page 56 |
| 3Ah | R/W (unlock) | Lid Closure Threshold 1 | Stores controls for selecting the lid closure threshold for buttons 1 - 4 | AAh | Page 57 |
| 3Bh | R/W (unlock) | Lid Closure Threshold 2 | Stores controls for selecting the lid closure threshold for buttons 5 - 8 | AAh | Page 57 |
| 3Ch | R/W (unlock) | Lid Closure Threshold 3 | Stores controls for selecting the lid closure threshold for buttons 9 - 12 | AAh | Page 57 |
| 3Dh | R/W (unlock) | Lid Closure Threshold 4 | Stores controls for selecting the lid closure threshold for buttons 13 - 14 | 0Ah | Page 57 |
| 3Eh | R/W | Slider Velocity Configuration | Determines speed parameters for the slider | C5 | Page 59 |
| 4Fh | R/W | Sampling Configuration | Changes the sampling time for one or more input channels | 00h | Page 60 |
| 50h | R | Sensor 1 Base Count | Stores the reference count value for sensor 1 | 00h | Page 61 |
| 51h | R | Sensor 2 Base Count | Stores the reference count value for sensor 2 | 00h | Page 61 |
| 52h | R | Sensor 3 Base Count | Stores the reference count value for sensor 3 | 00h | Page 61 |
| 53h | R | Sensor 4 Base Count | Stores the reference count value for sensor 4 | 00h | Page 61 |
| 54h | R | Sensor 5 Base Count | Stores the reference count value for sensor 5 | 00h | Page 61 |
| 55h | R | Sensor 6 Base Count | Stores the reference count value for sensor 6 | 00h | Page 61 |
| 56h | R | Sensor 7 Base Count | Stores the reference count value for sensor 7 | 00h | Page 61 |
| 57h | R | Sensor 8 Base Count | Stores the reference count value for sensor 8 | 00h | Page 61 |
| 58h | R | Sensor 9 Base Count | Stores the reference count value for sensor 9 | 00h | Page 61 |
| 59h | R | Sensor 10 Base Count | Stores the reference count value for sensor 10 | 00h | Page 61 |
| 5Ah | R | Sensor 11 Base Count | Stores the reference count value for sensor 11 | 00h | Page 61 |
| 5Bh | R | Sensor 12 Base Count | Stores the reference count value for sensor 12 | 00h | Page 61 |

Table 5.1 Register Set in Hexadecimal Order (continued)

| REGISTER ADDRESS | R/W | REGISTER NAME | FUNCTION | DEFAULT VALUE | PAGE |
|------------------|-----|------------------------|---|---------------|-------------------------|
| 5Ch | R | Sensor 13 Base Count | Stores the reference count value for sensor 13 | 00h | Page 61 |
| 5Dh | R | Sensor 14 Base Count | Stores the reference count value for sensor 14 | 00h | Page 61 |
| 70h | R/W | LED / GPIO Direction | Controls the direction for LED1 / GPIO1 through LED8 / GPIO8 | 00h | Page 62 |
| 71h | R/W | LED / GPIO Output Type | Controls the output type for LED1 / GPIO1 through LED8 / GPIO8 | 00h | Page 62 |
| 72h | R | GPIO Input | Stores the pin state of LED1 / GPIO1 through LED8 / GPIO8 | 00h | Page 63 |
| 73h | R/W | LED Output Control 1 | Controls the output state of the LED drivers 1 - 8 | 00h | Page 63 |
| 74h | R/W | LED Output Control 2 | Controls the output state of the LED drivers 9 - 11 | 00h | Page 63 |
| 75h | R/W | LED Polarity 1 | Controls the output polarity of LEDs 1 - 8 | 00h | Page 64 |
| 76h | R/W | LED Polarity 2 | Controls the output polarity of LEDs 9 - 11 | 00h | Page 64 |
| 80h | R/W | Sensor LED Linking | Controls linking of CS1 - CS7 to LED channels | 00h | Page 66 |
| 81h | R/W | LED Behavior 1 | Controls the behavior and response of LEDs 1 - 4 | 00h | Page 67 |
| 82h | R/W | LED Behavior 2 | Controls the behavior and response of LEDs 5 - 8 | 00h | Page 67 |
| 83h | R/W | LED Behavior 3 | Controls the behavior and response of LEDs 9 - 11 | 00h | Page 67 |
| 84h | R/W | LED Pulse 1 Period | Controls the period of each breathe during a pulse | 20h | Page 69 |
| 85h | R/W | LED Pulse 2 Period | Controls the period of breath and pulse release operation | 14h | Page 71 |
| 86h | R/W | LED Breathe Period | Controls the period of an LED breathe operation | 5Dh | Page 72 |
| 88h | R/W | LED Pulse Config | Controls the number of pulses for the Pulse 1 and Pulse 2 LED behaviors | 24h | Page 72 |
| 90h | R/W | LED Pulse 1 Duty Cycle | Determines the min and max duty cycle for the pulse operation | F0h | Page 73 |
| 91h | R/W | LED Pulse 2 Duty Cycle | Determines the min and max duty cycle for the breathe and pulse release operation | F0h | Page 73 |
| 92h | R/W | LED Breathe Duty Cycle | Determines the min and max duty cycle for the breathe operation | F0h | Page 73 |

Table 5.1 Register Set in Hexadecimal Order (continued)

| REGISTER ADDRESS | R/W | REGISTER NAME | FUNCTION | DEFAULT VALUE | PAGE |
|------------------|-----|-----------------------|---|---------------|-------------------------|
| 93h | R/W | LED Direct Duty Cycle | Determines the min and max duty cycle for Direct mode LED operation | F0h | Page 73 |
| 94h | R/W | LED Direct Ramp Rates | Determines the rising and falling edge ramp rates of the LED | 00h | Page 74 |
| 95h | R/W | LED Off Delay | Determines the off delay for all LED behaviors | 00h | Page 75 |
| FDh | R | Product ID | Stores a fixed value that identifies each product | 2Dh | Page 77 |
| FFh | R | Revision | Stores a fixed value that represents the revision number | 81h | Page 77 |

During Power-On-Reset (POR), the default values are stored in the registers. A POR is initiated when power is first applied to the part and the voltage on the VDD supply surpasses the POR level as specified in the electrical characteristics. Any reads to undefined registers will return 00h. Writes to undefined registers will not have an effect.

5.1 Main Status Control Register

Table 5.2 Main Status Control Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|---------------------|----|-------|-------|--------|----|----|---------|-----|---------|
| 00h | R/W | Main Status Control | - | DEACT | SLEEP | DSLEEP | - | - | PWR_LED | INT | 00h |

The Main Status and Control register controls the primary power state of the device.

Bit 6 - DEACT - Deactivates all sensor scanning and LED activity.

- '0' - (default) - Sensor scanning is active and LEDs are functional.
- '1' - All sensor scanning is disabled and all linked LEDs are disabled (see [Section 5.39](#)). The only way to restart scanning is to clear this bit. The status registers are automatically cleared and the INT bit is cleared.

Bit 5 - SLEEP - Enables Sleep mode by deactivating the LED activity.

- '0' (default) - Sensor scanning is active and LEDs are functional.
- '1' - All LEDs are disabled (except LED11) and the Capacitive Touch Sensor scanning is limited to the sensors set in the Sleep Channel Control register (see [Section 5.22](#)). The status registers will not be cleared.

Bit 4 - DSLEEP - Enables the Deep Sleep mode by deactivating all functions.

- '0' (default) - Sensor scanning is active and LEDs are functional.
- '1' - All sensor scanning is disabled and all LEDs are disabled (except LED11). The device will return to its previous power state when the ALERT pin is driven to its active level (see [Section 4.1](#)). The status registers are automatically cleared and the INT bit is cleared.

Bit 1 - PWR_LED - Controls the output of LED11 based on the state of bits 5 and 4.

- '0' (default) - The LED11 output is in the "inactive" or off state.

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- '1' - The LED11 output is active in one of the following conditions:
 - a. Both bits 4 and 5 are set to a logic '0' (normal mode). The LED will behave as defined the the LED11_CTL bits (see [Section 5.40](#)).
 - b. Either bit 4 or bit 5 are set to a logic '1' (sleep mode). The LED will behave as defined by the LED11_ALT bits (see [Section 5.40](#)).

Bit 0 - INT - Indicates that there is an interrupt. This bit is only set if the ALERT pin has been asserted. If a channel detects a press and its associated interrupt enable bit is not set to a logic '1' then no action is taken.

This bit is cleared by writing a logic '0' to it. When this bit is cleared, the ALERT pin will be deasserted and all status registers will be cleared if the condition has been removed.

- '0' - No interrupt pending.
- '1' - A button press has been detected on one or more channels and the interrupt has been asserted.

5.2 Button Status Registers

Table 5.3 Button Status Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-----------------|------|------|------|------|------|-----|-----|-----|---------|
| 03h | R | Button Status 1 | UP | DOWN | CS6 | CS5 | CS4 | CS3 | CS2 | CS1 | 00h |
| 04h | R | Button Status 2 | CS14 | CS13 | CS12 | CS11 | CS10 | CS9 | CS8 | CS7 | 00h |

The Button Status Registers store status bits that indicate a button press has been detected. A value of '0' in any bit indicates that no button press has been detected. A value of '1' in any bit indicates that a button press has been detected.

All status bits are cleared when the device enters the Deep Sleep or Inactive states (DSLEEP = '1' or DEACT = '1' - see [Section 5.1](#)). All status bits are cleared when the INT bit is cleared and if a touch on the respective Capacitive Touch Sensor is no longer present. If a touch is still detected, then the bits will not be cleared (but this will not cause the interrupt to be asserted - see [Section 5.14](#))

APPLICATION NOTE: When the Button Status 1 Register is read, the Group Status register will be automatically cleared. Therefore, the Group Status register should be read prior to reading the Button Status Registers

5.2.1 Button Status 1

Bit 7 - UP - Indicates that a slide was detected on increasing sensors (i.e. Sensor 8 -> Sensor 9 -> Sensor 10). This bit is also set if a press is detected on the "Up" portion of the slider. If the Group auto-repeat is enabled, then the ALERT pin will be periodically asserted while a slide or press and hold event is still detected. This bit is sticky and will remain set until cleared. Once cleared, it will be re-set when another interrupt is generated in the "UP" direction. This bit is automatically cleared if the DOWN bit is set.

Bit 6 - DOWN - Indicates that a slide was detected on decreasing sensors (i.e. Sensor 14 -> Sensor 13-> Sensor 12). This bit is also set if a press is detected on the "Down" portion of the slider. If the Group auto-repeat is enabled, then the ALERT pin will be periodically asserted while a slide or press and hold event is still detected. This bit is sticky and will remain set until cleared. Once cleared, it will be re-set when another interrupt is generated in the "DOWN" direction. This bit is automatically cleared if the UP bit is set.

Bit 5 - CS6 - Indicates that a press was detected on Sensor 6. This sensor can be linked to LED6.

- '0' - A touch was not detected on the corresponding button.
- '1' - A touch was detected on the corresponding button.

Bit 4 - CS5 - Indicates that a press was detected on Sensor 5. This sensor can be linked to LED5.

Bit 3 - CS4 - Indicates that a press was detected on Sensor 4. This sensor can be linked to LED4.

Bit 2 - CS3 - Indicates that a press was detected on Sensor 3. This sensor can be linked to LED3.

Bit 1 - CS2 - Indicates that a press was detected on Sensor 2. This sensor can be linked to LED2.

Bit 0 - CS1 - Indicates that a press was detected on Sensor 1. This sensor can be linked to LED1.

5.2.2 Button Status 2

Bit 7 - CS14 - Indicates that press was detected on Sensor 14. This sensor is part of the group which can be linked to LED9 and LED10.

Bit 6 - CS13 - Indicates that press was detected on Sensor 13. This sensor is part of the group which can be linked to LED9 and LED10.

Bit 5 - CS12 - Indicates that press was detected on Sensor 12. This sensor is part of the group which can be linked to LED9 and LED10.

Bit 4 - CS11 - Indicates that press was detected on Sensor 11. This sensor is part of the group which can be linked to LED9 and LED10.

Bit 3 - CS10 - Indicates that press was detected on Sensor 10. This sensor is part of the group which can be linked to LED9 and LED10.

Bit 2 - CS9 - Indicates that press was detected on Sensor 9. This sensor is part of the group which can be linked to LED9 and LED10.

Bit 1 - CS8 - Indicates that press was detected on Sensor 8. This sensor is part of the group which can be linked to LED9 and LED10.

Bit 0 - CS7 - Indicates that a press was detected on Sensor 7. This sensor can be linked to LED7.

5.3 Build Revision Register

Table 5.4 Firmware Revision Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-----------------------------|----|----|----|----|----|----|----|----|---------|
| 05h | R | CAP1014-1 Build Revision | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11h |
| 05h | R | CAP1014-2 Build Revision | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12h |

The Build Revision register indicates hardware defined settings that are used.

Table 5.5 Build History

| BUILD | DEVICE | REASON FOR CHANGE |
|-------|-----------|--|
| 10h | CAP1014 | Initial Development |
| 11h | CAP1014-1 | Activated Lid Closure circuitry |
| 12h | CAP1014-2 | Activated Lid Closure circuitry and changed SMBus address to 0101_100b |

5.4 Slider Position / Volumetric Data Register

Table 5.6 Slider Position / Volumetric Data Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----------|-----------------------------------|----|----------|----|----|----|----|----|-----|---------|
| 06h | R-C / R/W | Slider Position / Volumetric Data | - | POS[6:0] | | | | | | 00h | |

The Slider Position register indicates the absolute position of a Tap, Slide, or Press and Hold event detected on the Grouped sensors (slider). Alternately, the register stores volumetric data that increases or decreased based on detected operations on the Grouped sensors (slider).

Bits 6-0 - POS[6:0] - Indicate absolute position or volumetric data as determined by the POS_VOL bit (see [Section 5.14](#)).

5.4.1 Absolute Position

The absolute position of a single touch is available from this register. By interpolating information from up to 3 adjacent buttons, 16 different positions are calculated by the CAP1014 from the center of one button to the center of each adjacent button. The bits will encode a range from 2 to 98 indicative of where the touch occurred. [Table 5.7](#) shows an example of the settings assuming a single button is pressed.

If a slide is detected on the Grouped sensors, then the POS[6:0] bits will indicate the most recently touched sensor (i.e. where the slide ended) however will not indicate where the slide originated.

APPLICATION NOTE: The register will be cleared to a value of 00h when it is read. It will be set to a valid position when the next ALERT is generated. It will be updated at the respective repeat rate for a slide or press and hold event regardless of whether it has been read or not. Therefore, it will only show the position of the last touch detected at the time of the interrupt.

Table 5.7 Example Slider Absolute Position Decode

| TOUCH POSITION | POS[6:0] SETTINGS |
|----------------|-------------------|
| CS8 | 02h (2d) |
| CS9 | 12h (18d) |
| CS10 | 22h (34d) |
| CS11 | 32h (50d) |

Table 5.7 Example Slider Absolute Position Decode (continued)

| TOUCH POSITION | POS[6:0] SETTINGS |
|----------------|-------------------|
| CS12 | 42h (68d) |
| CS13 | 52h (82d) |
| CS14 | 62h (98d) |

5.4.2 Volumetric Data

If they are setup to present Volumetric Data (see [Section 5.14](#)) then the bits will encode a range from 0 to 100. This value is updated based on the Grouped sensor activity:

- A slide in the “UP” direction will increase the volumetric data by the Volumetric Step setting (see [Section 5.6](#)) whenever an interrupt is generated (including extra interrupts generated after the slide is complete).
- A slide in the “DOWN” direction will decrease the volumetric data by the Volumetric Step setting (see [Section 5.6](#)) whenever an interrupt is generated (including extra interrupts generated after the slide is complete)
- A tap (see [Section 4.5.1](#)) on the “UP” side will increase the volumetric data by a value of 1.
- A tap on the “DOWN” side will decrease the volumetric data by a value of 1.
- A press and hold (see [Section 4.5.2](#)) on the “UP” side will increase the volumetric data by a value of 1 at every repeat rate interval.
- A press and hold (see [Section 4.5.2](#)) on the “DOWN” side will decrease the volumetric data by a value of 1 at every repeat rate interval.

The bits are read / write.

5.5 Vendor ID Register

Table 5.8 Vendor ID Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-----------|----|----|----|----|----|----|----|----|---------|
| 08h | R | Vendor ID | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 5Dh |

The Vendor ID register stores an 8-bit value that represents SMSC.

5.6 Volumetric Step Register

Table 5.9 Volumetric Step Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-----------------|----|----|----|----|---------------|----|----|-----|---------|
| 09h | R/W | Volumetric Step | - | - | - | - | VOL_STEP[3:0] | | | 01h | |

The Volumetric Step register controls the size of a step to the volumetric data when a slide is detected in the UP and DOWN directions.

Bits 3 - 0 - VOL_STEP[3:0] - Determines the volumetric data step when a slide is detected. Each LSB corresponds to a value of ± 1 .

5.7 Noise Flag Status Registers

Table 5.10 Noise Flag Status Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|---------------------|----|-----------|-----------|-----------|-----------|-----------|----------|----------|---------|
| 0Ah | R | Noise Flag Status 1 | - | S7_NOISE | S6_NOISE | S5_NOISE | S4_NOISE | S3_NOISE | S2_NOISE | S1_NOISE | 00h |
| 0Bh | R | Noise Flag Status 2 | - | S14_NOISE | S13_NOISE | S12_NOISE | S11_NOISE | S10_NOISE | S9_NOISE | S8_NOISE | 00h |

The Noise Flag Status registers store status bits that are generated from the analog block if the detected noise is above the operating region of the analog detector. These bits indicate that the most recently received data from the sensor is invalid and should not be used for touch detection. Furthermore, so long as the bit is set for a particular channel, no decisions are made with the data. The queues are not updated, a touch is not detected, and a release is not detected.

These bits are not sticky and will be cleared automatically if the analog block does not report a noise error.

5.8 Lid Closure Status Registers

Table 5.11 Lid Closure Status Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------------------|----|---------|---------|---------|---------|---------|--------|--------|---------|
| 0Ch | R | Lid Closure Status 1 | - | S7_LID | S6_LID | S5_LID | S4_LID | S3_LID | S2_LID | S1_LID | 00h |
| 0Dh | R | Lid Closure Status 2 | - | S14_LID | S13_LID | S12_LID | S11_LID | S10_LID | S9_LID | S8_LID | 00h |

The Lid Closure Status registers bits are only set if the lid closure detection circuitry is enabled (see [Section 5.24, "Lid Closure Configuration Register"](#)). These status bits indicate that the corresponding Capacitive Touch Sensor exceeded the Lid Closure threshold. These bits will be set if a button press is detected, because the Lid Closure threshold is a percentage of the Sensor Threshold.

These bits are used in combination with the Lid Closure Pattern register settings to determine when a Lid Closure Event is flagged (see [Section 5.26, "Lid Closure Pattern Registers"](#)).

These bits are not sticky and will be cleared automatically when the corresponding sensor count drops below the lid closure count threshold. The device does not flag a sensor as above or below the threshold until it has cycled through the queue (see [Section 5.25, "Lid Closure Queue Control Register"](#)).

APPLICATION NOTE: It is likely that recalibration will occur while the lid is closed, resulting in negative delta counts until recalibration takes place.

5.9 GPIO Status Register

Table 5.12 GPIO Status Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------|
| 0Eh | R-C | GPIO Status | GPIO8_ STS | GPIO7_ STS | GPIO6_ STS | GPIO5_ STS | GPIO4_ STS | GPIO3_ STS | GPIO2_ STS | GPIO1_ STS | 00h |

The GPIO Status register bits are set whenever one of the GPIO inputs changes states. If the LEDx / GPIOx pin is not configured as a GPIO or as an input, then the respective bit will be set to a logic '0'.

The bits are cleared when the register is read.

5.10 Group Status Register

Table 5.13 GPIO Status Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|--------------|-----|------|----|----|----|------|-----|----|---------|
| 0Fh | R-C | Group Status | LID | MULT | - | - | UP | DOWN | TAP | PH | 00h |

The Group Status register indicates that one or more actions was detected on the Grouped sensors. The detectable actions are described in [Section 4.5](#).

Bit 7 - LID - Indicates that a Lid Closure Event has been detected. This bit is sticky. When it is set, it will remain set until read. When a Lid Closure Event is detected, all new touches will be blocked.

Bit 6 - MULT - This bit is asserted if one or more touches are being blocked because greater than N buttons are simultaneously pressed.

Bit 3 - UP - Indicates that a slide was detected on increasing sensors (i.e. Sensor 1 -> Sensor 2 -> Sensor 3). This bit is also set if a touch (tap or press and hold event) is detected on the "Up" portion of the slider. If the Group auto-repeat is enabled, then the ALERT pin will be periodically asserted while a slide or press and hold event is detected. This bit will be cleared when read and re-set when another interrupt is generated. This bit is cleared automatically if the DOWN bit is set.

Bit 2 - DOWN - Indicates that a slide was detected on decreasing sensors (i.e. Sensor 6 -> Sensor 5 -> Sensor 4). This bit is also set if a touch (tap or press and hold event) is detected on the "Down" portion of the slider. If the Group auto-repeat is enabled, then the ALERT pin will be periodically asserted while a slide or press and hold event is detected. This bit will be cleared when read and re-set when another interrupt is generated. This bit is automatically cleared if the UP bit is set.

Bit 1 - TAP - Indicates that a tap was detected on one of the sensors within the Group. The relative position of the tap is indicated by the UP and DOWN bits so that a tap on the "UP" side of the group will assert the UP bit as well as the TAP bit. If the tap event is detected in the "center" of the slider that is neither "UP" nor "DOWN" then the bit will be set however no interrupt will be generated. This bit is sticky and will remain set until read.

Bit 0 - PH - Indicates that a press and hold event was detected on one of the sensors within the Group. the relative position of the press is indicated by the UP and DOWN bits so a touch and hold on the "UP" side of the group will assert the UP bit as well as the PH bit. If the press and hold event is detected in the "center" of the slider that is neither "UP" nor "DOWN" then the bit will be set however no interrupt will be generated. This bit is sticky and will remain set until read. If the condition is still present, then this bit will be re-set when the interrupt is generated.

5.11 Sensor Delta Count Registers

Table 5.14 Sensor Delta Count Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-----------------------|------|----|----|----|----|----|----|----|---------|
| 10h | R | Sensor 1 Delta Count | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 11h | R | Sensor 2 Delta Count | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 12h | R | Sensor 3 Delta Count | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 13h | R | Sensor 4 Delta Count | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 14h | R | Sensor 5 Delta Count | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 15h | R | Sensor 6 Delta Count | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 16h | R | Sensor 7 Delta Count | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 17h | R | Sensor 8 Delta Count | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 18h | R | Sensor 9 Delta Count | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 19h | R | Sensor 10 Delta Count | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 1Ah | R | Sensor 11 Delta Count | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 1Bh | R | Sensor 12 Delta Count | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 1Ch | R | Sensor 13 Delta Count | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 1Dh | R | Sensor 14 Delta Count | Sign | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |

The Sensor Delta Count registers store the delta count that is compared against the threshold used to determine if a touch has been detected. The count value represents a change in input due to the capacitor associated with a touch on one of the sensors and is referenced to a calibrated base “Not touched” count value. The delta is an instantaneous change and is updated once per sensor per sensing cycle (see [Section 4.4.4](#) - sensor cycle).

The value presented is a standard 2's complement number. In addition, the value is capped at a value of 7Fh. A reading of 7Fh indicates that the sensitivity settings are too high and should be adjusted accordingly (see [Section 5.13](#)).

The value is also capped at a negative value of FFh for negative delta counts which may result upon a release.

5.12 Queue Control Register

Table 5.15 Queue Control Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------------------|----|----|----|----|----|--------------|----|----|---------|
| 1Eh | R/W | Button Queue Control | - | - | - | - | - | QUEUE_B[2:0] | | | 03h |

The Queue Control register determines the number of consecutive samples for which a single sensor output is above the Sensor Threshold before a touch is detected. This is also used to determine the number of consecutive samples used to detect a button release. The queue applies independently to all channels.

Bits 2 - 0 - QUEUE_B[2:0] - The number of consecutive samples necessary to detect a touch. Default is 3 consecutive samples. See [Table 5.16](#).

Table 5.16 QUEUE_B Bit Decode

| QUEUE_B[3:0] | | | NUMBER OF CONSECUTIVE READINGS > THRESHOLD |
|--------------|---|---|--|
| 2 | 1 | 0 | |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

5.13 Data Sensitivity Register

Table 5.17 Data Scaling Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|------------------|----|------------|----|----|------------|----|----|-----|---------|
| 1Fh | R/W | Data Sensitivity | - | D_DSP[2:0] | | | C_DSP[3:0] | | | 2Fh | |

The Data Sensitivity register controls the sensitivity of a touch detection.

Bits 6- 4 D_DSP[2:0] - Controls the sensitivity of a touch detection. The sensitivity settings act to scale the relative delta count value higher or lower based on the system parameters. A setting of 0000b is the most sensitive while a setting of 1111b is the least sensitive. At the more sensitive settings, touches are detected for a smaller delta C corresponding to a "lighter" touch. These settings are more sensitive to noise however and a noisy environment may flag more false touches than higher sensitivity levels.

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APPLICATION NOTE: A value of 128x is the most sensitive setting available. At the most sensitive settings, the MSB of the Delta Count register represents 64 out of ~25,000 which corresponds to a touch of approximately 0.25% of the base capacitance (or a ΔC of 25fF from a 10pF base capacitance). Conversely a value of 1x is the least sensitive setting available. At these settings, the MSB of the Delta Count register corresponds to a delta count of 8192 counts out of ~25,000 which corresponds to a touch of approximately 33% of the base capacitance (or a ΔC of 3.33pF from a 10pF base capacitance).

Table 5.18 D_DSP Bit Decode

| D_DSP[2:0] | | | SENSITIVITY MULTIPLIER |
|------------|---|---|------------------------|
| 2 | 1 | 0 | |
| 0 | 0 | 0 | 128x (most sensitive) |
| 0 | 0 | 1 | 64x |
| 0 | 1 | 0 | 32x (default) |
| 0 | 1 | 1 | 16x |
| 1 | 0 | 0 | 8x |
| 1 | 0 | 1 | 4x |
| 1 | 1 | 0 | 2x |
| 1 | 1 | 1 | 1x - (least sensitive) |

Bits 3 - 0 - C_DSP[3:0] - Controls the scaling and data presentation of the Base Count registers. The higher the value of these bits, the larger the range and the lower the resolution of the data presented. The scale factor represents the multiplier to the bit-weighting presented in these register descriptions.

APPLICATION NOTE: The C_DSP[3:0] bits normally do not need to be updated. These settings will not affect touch detection or sensitivity. These bits are sometimes helpful in analyzing the Cap Sensing board performance and stability.

Table 5.19 C_DSP Bit Decode

| C_DSP[3:0] | | | | DATA SCALING FACTOR |
|------------|---|---|---|---------------------|
| 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | 1x |
| 0 | 0 | 0 | 1 | 2x |
| 0 | 0 | 1 | 0 | 4x |
| 0 | 0 | 1 | 1 | 8x |
| 0 | 1 | 0 | 0 | 16x |
| 0 | 1 | 0 | 1 | 32x |
| 0 | 1 | 1 | 0 | 64x |
| 0 | 1 | 1 | 1 | 128x |

Table 5.19 C_DSP Bit Decode (continued)

| C_DSP[3:0] | | | | DATA SCALING FACTOR |
|------------|---|---|---|---------------------------|
| 3 | 2 | 1 | 0 | |
| 1 | 0 | 0 | 0 | 256x |
| All others | | | | 256x (default = 1111b) |

5.14 Configuration Register

Table 5.20 Configuration Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|---------------|----------|---------|--------------|---------------|--------------|----------|--------------|----------|---------|
| 20h | R/W | Configuration | TIME OUT | POS_VOL | BLK_NOISE_TH | BLK_NOISE_DIS | MAX_DUR_EN_B | RPT_EN_B | MAX_DUR_EN_G | RPT_EN_G | 2Dh |

The Configuration register controls general global functionality that affects the entire device.

Bit 7 - TIMEOUT - Enables the timeout and idle functionality of the SMBus protocol.

- '0' (default) - The SMBus timeout and idle functionality are disabled. The SMBus interface will not time out if the clock line is held low. Likewise, it will not reset if both the data and clock lines are held high for longer than 150us. This is used for I²C compliance.
- '1' - The SMBus timeout and idle functionality are enabled. The SMBus interface will time out if the clock line is held low for longer than 30ms. Likewise, it will reset if both the data and clock lines are held high for longer than 150us.

Bit 6 - POS_VOL - Determines the behavior of the POS[6:0] status bits when a Grouped sensor is activated - see [Section 5.4](#).

- '0' (default) - The POS[6:0] bits represent position information that indicates which sensor was touched or the last sensor touched during a slide.
- '1' - The POS[6:0] bits represent volumetric data. The Position / Volumetric Data register is read / write.

Bit 5 - BLK_DIG_NOISE - Determines whether the noise threshold is checked when determining whether to discard samples.

- '0' - The noise threshold is enabled and checked. If a sample is above the noise threshold, it is not included in the re-calibration routine.
- '1' (default) - The noise threshold is disabled. No samples are excluded from the re-calibration routine.

Bit 4 - BLK_ANA_NOISE - Determines whether the noise flag setting will block a touch detection as well as the analog calibration routine.

- '0' (default) - If the analog noise bit is set, then a touch is blocked on the corresponding channel and will force the analog calibration routine to retry.
- '1' - A touch is not blocked even if the analog noise bit is set. Likewise, the analog calibration routine will not retry if the analog noise bit is set.

Bit 3 - MAX_DUR_EN_B - Determines whether the maximum duration recalibration is enabled for non-grouped sensors.

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- '0' - The maximum duration recalibration functionality is disabled. A press may be held indefinitely and no re-calibration will be performed on any button.
- '1' (default) - The maximum duration recalibration functionality is enabled. If a press is held for longer than the MAX_DUR_B bit settings, then the re-calibration routine will be restarted (see [Section 5.16](#)).

APPLICATION NOTE: If the RPT_EN_B bit is updated while a touch is present on a button, then no changes will be made to the interrupts until that button has been released.

Bit 2 - RPT_EN_B - Determines the interrupt mechanism used when a press is detected on a non-grouped sensor (button)

- '0' - An interrupt will be generated when a touch is detected and again when a release is detected.
- '1' (default) - An interrupt will be generated when a touch is detected and at the programmed repeat rate so long as the button is pressed.

Bit 1 - MAX_DUR_EN_G - Determines whether the maximum duration recalibration is enabled for grouped sensors.

- '0' (default) - The maximum duration recalibration functionality is disabled. A press may be held indefinitely and no re-calibration will be performed on any button.
- '1' - The maximum duration recalibration functionality is enabled. If a press is held for longer than the MAX_DUR_G bit settings, then the re-calibration routine will be restarted (see [Section 5.18](#)).

Bit 0 - RPT_EN_G - Determines the interrupt mechanism used when a Press and Hold event is detected on a grouped sensor

- '0' (default) - An interrupt will be generated when a Press and Hold event is detected.
- '1' - An interrupt will be generated when a Press and Hold event is detected and at the programmed repeat rate so long as the sensor is pressed.

5.15 Sensor Enable Registers

Table 5.21 Sensor Enable Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|---------------|------|-------|-------|-------|-------|-------|-------|-------|---------|
| 21h | R/W | Sensor Enable | G_EN | S7_EN | S6_EN | S5_EN | S4_EN | S3_EN | S2_EN | S1_EN | FFh |

The Sensor Enable registers determine whether a Capacitive Touch Sensor input is included in the sampling cycle. The length of the sampling cycle is not affected by the number of sensors measured.

Bit 7 - G_EN - Enables all Capacitive Touch Sensors that are grouped to be included during the sampling cycle.

- '0' - None of the The grouped sensors are included in the sampling cycle.
- '1' (default) - All of the grouped sensors are included in the sampling cycle.

Bit 6 - S7_EN - Enables the CS7 input to be included during the sampling cycle.

- '0' - The CS7 input is not included in the sampling cycle.
- '1' - The CS7 input is included in the sampling cycle.

Bit 5 - S6_EN - Enables the CS6 input to be included during the sampling cycle.

Bit 4 - S5_EN - Enables the CS5 input to be included during the sampling cycle.

Bit 3 - S4_EN - Enables the CS4 input to be included during the sampling cycle.

Bit 2 - S3_EN - Enables the CS3 input to be included during the sampling cycle.

Bit 1 - S2_EN - Enables the CS2 input to be included during the sampling cycle.

Bit 0 - S1_EN - Enables the CS1 input to be included during the sampling cycle.

5.16 Button Configuration Register

Table 5.22 Button Configuration Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------------------|----------------|----|----|----|-----------------|----|----|----|---------|
| 22h | R/W | Button Configuration | MAX_DUR_B[3:0] | | | | RPT_RATE_B[3:0] | | | | A4h |

The Button Configuration Register controls timings associated with the Capacitive Sensor channels 1 - 7 that are not Grouped.

Bits 7 - 4 - MAX_DUR_B [3:0] - (default 1010b) - Determines the maximum time that a button is allowed to be pressed until the Capacitive Touch sensor is recalibrated as shown in [Table 5.23](#).

Table 5.23 MAX_DUR_B and MAX_DUR_G Bit Decode

| MAX_DUR_B[3:0] AND MAX_DUR_G[3:0] | | | | TIME BEFORE RECALIBRATION |
|-----------------------------------|---|---|---|---------------------------|
| 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | 560ms |
| 0 | 0 | 0 | 1 | 840ms |
| 0 | 0 | 1 | 0 | 1120ms |
| 0 | 0 | 1 | 1 | 1400ms |
| 0 | 1 | 0 | 0 | 1680ms |
| 0 | 1 | 0 | 1 | 2240ms |
| 0 | 1 | 1 | 0 | 2800ms |
| 0 | 1 | 1 | 1 | 3360ms |
| 1 | 0 | 0 | 0 | 3920ms |
| 1 | 0 | 0 | 1 | 4480ms |
| 1 | 0 | 1 | 0 | 5600ms |
| 1 | 0 | 1 | 1 | 6720ms |
| 1 | 1 | 0 | 0 | 7840ms |
| 1 | 1 | 0 | 1 | 8906ms |
| 1 | 1 | 1 | 0 | 10080ms |
| 1 | 1 | 1 | 1 | 11200ms |

Bits 3 - 0 - RPT_RATE_B[3:0] - (default 0100b) Determines the time duration between interrupt assertions when auto repeat is enabled. The resolution is 35ms the range is from 35ms to 560ms as shown in [Table 5.24](#).

Table 5.24 RPT_RATE_B / SL / PH and M_PRESS Bit Decode

| RPT_RATE_B / RPT_RATE_SL / RPT_RATE_PH / M_PRESS[3:0] | | | | INTERRUPT REPEAT RATE OR M_PRESS TIME |
|---|---|---|---|---------------------------------------|
| 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | 35ms |
| 0 | 0 | 0 | 1 | 70ms |
| 0 | 0 | 1 | 0 | 105ms |
| 0 | 0 | 1 | 1 | 140ms |
| 0 | 1 | 0 | 0 | 175ms |
| 0 | 1 | 0 | 1 | 210ms |
| 0 | 1 | 1 | 0 | 245ms |
| 0 | 1 | 1 | 1 | 280ms |
| 1 | 0 | 0 | 0 | 315ms |
| 1 | 0 | 0 | 1 | 350ms |
| 1 | 0 | 1 | 0 | 385ms |
| 1 | 0 | 1 | 1 | 420ms |
| 1 | 1 | 0 | 0 | 455ms |
| 1 | 1 | 0 | 1 | 490ms |
| 1 | 1 | 1 | 0 | 525ms |
| 1 | 1 | 1 | 1 | 560ms |

5.17 Group Configuration Register 1

Table 5.25 Group Configuration Register 1

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-----------------------|------------------|----|----|----|--------------|----|----|----|---------|
| 23h | R/W | Group Configuration 1 | RPT_RATE_PH[3:0] | | | | M_PRESS[3:0] | | | | 47h |

Bits 7-4 - RPT_RATE_PH[3:0] - (default 0100b) Determines the time duration between interrupt assertions when auto repeat is enabled. This setting applies when a press and hold condition is detected on the on the Grouped Sensors (see [Section 4.5.2](#)). The resolution is 35ms the range is from 35ms to 560ms as shown in [Table 5.24](#).

Bits 3- 0 - M_PRESS[3:0] - (default 0111b) - Determines the minimum amount of time that a sensor in the Group must detect a button press to detect a Press and Hold event. If the sensor detects a touch for longer than the M_PRESS[3:0] settings, then a Press and Hold event is detected. This has no affect on whether a slide is detected within the group. If a slide is detected before or after the press has been confirmed, it is treated as a separate event.

This is the maximum amount of time that a sensor in the Group can detect a button press to differentiate between a tap and a press and hold. If a sensor detects a touch for less than or equal to the M_PRESS[3:0] settings then, a Tap event is detected.

The resolution is 35ms the range is from 35ms to 560ms as shown in [Table 5.24](#).

5.18 Group Configuration Register 2

Table 5.26 Group Configuration Register 2

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-----------------------|----------------|----|----|----|------------------|----|----|----|---------|
| 24h | R/W | Group Configuration 2 | MAX_DUR_G[3:0] | | | | RPT_RATE_SL[3:0] | | | | D4h |

The Group Configuration 2 register controls timings associated with the Capacitive Sensor channels 8 - 14 that are included in the group.

Bits 7 - 4 - MAX_DUR_G [3:0] - (default 1101b) - Determines the maximum time that a button is allowed to be pressed until the Capacitive Touch sensor is recalibrated as shown in [Table 5.23](#).

Bits 3 - 0 - RPT_RATE_SL[3:0] - (default 0100b) Determines the time duration between interrupt assertions when auto repeat is enabled. This setting applies when a slide is detected on the Grouped Sensors and acts as the base repeat rate that is adjusted based on the slide speed (see [Section 4.5.3](#)). The resolution is 35ms the range is from 35ms to 560ms as shown in [Table 5.24](#).

5.19 Calibration Enable Registers

Table 5.27 Calibration Enable Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|--------------------|-------|--------|--------|--------|--------|--------|--------|--------|---------|
| 25h | R/W | Calibration Enable | G_CEN | S7_CEN | S6_CEN | S5_CEN | S4_CEN | S3_CEN | S2_CEN | S1_CEN | FFh |

The Calibration Enable registers control whether the indicated Capacitive Touch Sensor input is automatically re-calibrated. If a sensor is not enabled then the corresponding calibration enable bit is ignored.

Bit 7- G_CEN - Enables all sensors in the group to be re-calibrated simultaneously.

- '0' - None of the grouped channels are automatically re-calibrated. They can be re-calibrated manually by setting the G_CAL bit.
- '1' (default) - All of the grouped channels are automatically re-calibrated as the CAP1014 samples.

Bit 6 - S7_CEN - Enables the CS7 input to be re-calibrated automatically.

- '0' - The CS7 input is not automatically re-calibrated.
- '1' (default) - The CS7 input is automatically re-calibrated as the CAP1014 samples.

Bit 5 - S6_CEN - Enables the CS6 input to be re-calibrated automatically.

Bit 4 - S5_CEN - Enables the CS5 input to be re-calibrated automatically.

Bit 3 - S4_CEN - Enables the CS4 input to be re-calibrated automatically.

Bit 2 - S3_CEN - Enables the CS3 input to be re-calibrated automatically.

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Bit 1 - S2_CEN - Enables the CS2 input to be re-calibrated automatically.

Bit 0 - S1_CEN - Enables the CS1 input to be re-calibrated automatically.

5.20 Calibration Activate Registers

Table 5.28 Calibration Activate Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------------------|-------|--------|--------|--------|--------|--------|--------|--------|---------|
| 26h | R/W | Calibration Activate | G_CAL | S7_CAL | S6_CAL | S5_CAL | S4_CAL | S3_CAL | S2_CAL | S1_CAL | 00h |

The Calibration Activate register force the respective sensors to be re-calibrated. When a bit is set, the corresponding Capacitive Touch Sensor will be re-calibrated and the bit will be automatically cleared once the re-calibration routine has finished. During the re-calibration routine, the sensors will not detect a press for up to 600ms and the Sensor Base Count register values will be invalid. During this time, any press on the corresponding sensors will invalidate the re-calibration.

Bit 7 - G_CAL - When set, all sensors in the group are re-calibrated. This bit is automatically cleared once all of the sensors in the group have been re-calibrated successfully.

Bit 6 - S7_CAL - When set, the CS7 input is re-calibrated. This bit is automatically cleared once the sensor has been re-calibrated successfully.

Bit 5 - S6_CAL - When set, the CS6 input is re-calibrated. This bit is automatically cleared once the sensor has been re-calibrated successfully.

Bit 4 - S5_CAL - When set, the CS5 input is re-calibrated. This bit is automatically cleared once the sensor has been re-calibrated successfully.

Bit 3 - S4_CAL - When set, the CS4 input is re-calibrated. This bit is automatically cleared once the sensor has been re-calibrated successfully.

Bit 2 - S3_CAL - When set, the CS3 input is re-calibrated. This bit is automatically cleared once the sensor has been re-calibrated successfully.

Bit 1 - S2_CAL - When set, the CS2 input is re-calibrated. This bit is automatically cleared once the sensor has been re-calibrated successfully.

Bit 0 - S1_CAL - When set, the CS1 input is re-calibrated. This bit is automatically cleared once the sensor has been re-calibrated successfully.

5.21 Interrupt Enable Registers

Table 5.29 Interrupt Enable Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|--------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|---------|
| 27h | R/W | Interrupt Enable 1 | G_INT_EN | S7_INT_EN | S6_INT_EN | S5_INT_EN | S4_INT_EN | S3_INT_EN | S2_INT_EN | S1_INT_EN | FFh |
| 28h | R/W | Interrupt Enable 2 | GPIO8_INT_EN | GPIO7_INT_EN | GPIO6_INT_EN | GPIO5_INT_EN | GPIO4_INT_EN | GPIO3_INT_EN | GPIO2_INT_EN | GPIO1_INT_EN | 00h |

The Interrupt Enable registers determine whether a button press or GPIO input changing state causes the interrupt pin to be asserted.

5.21.1 Interrupt Enable 1

Bit 7 - G_INT_EN - Enables the interrupt pin to be asserted if a slide, tap, or press and hold action is detected on the grouped sensors.

- '0' - The interrupt pin will not be asserted if a slide, tap, or press and hold action is detected on the grouped sensors (associated with the UP, DOWN, TAP, and PH status bits).
- '1' (default) - The interrupt pin will be asserted if a slide, tap, or press and hold event is detected on the grouped sensors (associated with the UP, DOWN, TAP, and PH status bits).

Bit 6 - S7_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS7 (associated with the CS7 status bit).

- '0' - The interrupt pin will not be asserted if a touch is detected on CS7 (associated with the CS7 status bit).
- '1' (default) - The interrupt pin will be asserted if a touch is detected on CS7 (associated with the CS7 status bit).

Bit 5 - S6_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS6 (associated with the CS6 status bit).

Bit 4 - S5_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS5 (associated with the CS5 status bit).

Bit 3 - S4_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS4 (associated with the CS4 status bit).

Bit 2 - S3_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS3 (associated with the CS3 status bit).

Bit 1 - S2_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS2 (associated with the CS2 status bit).

Bit 0 - S1_INT_EN - Enables the interrupt pin to be asserted if a touch is detected on CS1 (associated with the CS1 status bit).

5.21.2 Interrupt Enable 2

These bits enable the interrupt pin to be asserted when the GPIOx status bit has been set.

Bit 7 - GPIO8_INT_EN - Enables the interrupt pin to be asserted if the GPIO8 status bit has been set.

- '0' - The interrupt pin will not be asserted if the GPIO8 status bit has been set.
- '1' (default) - The interrupt pin will be asserted if the GPIO8 status bit has been set.

Bit 6 - GPIO7_INT_EN - Enables the interrupt pin to be asserted if the GPIO7 status bit has been set.

Bit 5 - GPIO6_INT_EN - Enables the interrupt pin to be asserted if the GPIO6 status bit has been set.

Bit 4 - GPIO5_INT_EN - Enables the interrupt pin to be asserted if the GPIO5 status bit has been set.

Bit 3 - GPIO4_INT_EN - Enables the interrupt pin to be asserted if the GPIO4 status bit has been set.

Bit 2 - GPIO3_INT_EN - Enables the interrupt pin to be asserted if the GPIO3 status bit has been set.

Bit 1 - GPIO2_INT_EN - Enables the interrupt pin to be asserted if the GPIO2 status bit has been set.

Bit 0 - GPIO1_INT_EN - Enables the interrupt pin to be asserted if the GPIO1 status bit has been set.

5.22 Sleep Channel Control Register

Table 5.30 Sleep Channel Control

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-----------------------|----------|----------|----------|----------|----------|----------|----------|----------|---------|
| 29h | R/W | Sleep Channel Control | GR_SLEEP | S7_SLEEP | S6_SLEEP | S5_SLEEP | S4_SLEEP | S3_SLEEP | S2_SLEEP | S1_SLEEP | 00h |

The Sleep Channel control register determine which sensors are sampled when the device is placed into sleep mode.

APPLICATION NOTE: If this register is updated while the device is in Sleep Mode, then the conversion cycle may be extended or for the first measurement of the new Capacitive Touch Sensors. It will correct itself on subsequent measurement cycles.

APPLICATION NOTE: If this register is updated while the device is in Sleep Mode, it is recommended that force a recalibration routine on newly activated channels.

Bit 7 - GR_SLEEP - Enables the Grouped sensors to be sampled when the device is placed into sleep mode.

- '0' (default) - The Grouped Sensors are not sampled when the device is in Sleep mode
- '1' - The Grouped Sensors are sampled when the device is in Sleep mode. If a tap, slide, or touch and hold is detected then the appropriate status bit is set and an interrupt generated.

Bit 6 - S7_SLEEP - Enables the CS7 sensor to be sampled when the device is placed into sleep mode.

- '0' (default) - The CS7 input is not sampled when the device is in Sleep mode
- '1' - The CS7 input is sampled when the device is in Sleep mode. If a touch is detected then the status bit is set and an interrupt generated.

Bit 5 - S6_SLEEP - Enables the CS6 sensor to be sampled when the device is placed into sleep mode.

Bit 4 - S5_SLEEP - Enables the CS5 sensor to be sampled when the device is placed into sleep mode.

Bit 3 - S4_SLEEP - Enables the CS4 sensor to be sampled when the device is placed into sleep mode.

Bit 2 - S3_SLEEP - Enables the CS3 sensor to be sampled when the device is placed into sleep mode.

Bit 1 - S2_SLEEP - Enables the CS2 sensor to be sampled when the device is placed into sleep mode.

Bit 0 - S1_SLEEP - Enables the CS1 sensor to be sampled when the device is placed into sleep mode.

5.23 Multiple Touch Configuration Register

Table 5.31 Multiple Touch Configuration

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-----------------------|-------------|----|----|----|---------------|----|---------------|----|---------|
| 2Ah | R/W | Multiple Touch Config | MULT_BLK_EN | - | - | - | B_MULT_T[1:0] | | G_MULT_T[1:0] | | 82h |

The Multiple Touch Configuration register controls the settings for the multiple touch detection circuitry. These settings determine the sensitivity of this detection and the CAP1014 device behavior.

Bit 7 - MULT_BLK_EN - Enables the multiple button blocking circuitry.

- '0' - The multiple touch circuitry is disabled. The device will not block multiple touches.
- '1' (default)- The multiple touch circuitry is enabled. The device will accept the number of touches equal to programmed multiple touch threshold and block all others. It will remember which sensor is valid and block all others until that sensor has been released.

Bits 3 - 2 - B_MULT_T[1:0] - Determines the number of simultaneous touches on all buttons (excluding the Grouped buttons) before a Multiple Touch Event is flagged. If the number of multiple buttons touches is greater than the threshold value then a Multiple Touch Event is flagged. The bit decode is given by [Table 5.32](#).

Table 5.32 B_MULT_T Bit Decode

| B_MULT_T[1:0] | | NUMBER OF SIMULTANEOUS TOUCHES |
|---------------|---|--------------------------------|
| 1 | 0 | |
| 0 | 0 | 1 (default) |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

Bits 1 - 0 - G_MULT_T[1:0] - Determines the number of simultaneous touches on all Grouped buttons before a Multiple Touch Event is flagged. If the number of multiple buttons touches is greater than the threshold value then a Multiple Touch Event is flagged. The bit decode is given by [Table 5.33](#).

Table 5.33 G_MULT_T Bit Decode

| G_MULT_T[1:0] | | NUMBER OF SIMULTANEOUS TOUCHES |
|---------------|---|--------------------------------|
| 1 | 0 | |
| 0 | 0 | 2 |
| 0 | 1 | 3 |
| 1 | 0 | 4 (default) |
| 1 | 1 | 5 |

5.24 Lid Closure Configuration Register

Table 5.34 Lid Closure Configuration

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|--------------------|-----------|----|----|----|----|----|-----------|----------|---------|
| 2Bh | R/W | Lid Closure Config | LID_CLOSE | - | - | - | - | - | COMP_PTRN | LID_ALRT | 00h |

The Lid Closure Configuration register controls the settings for the lid closure detection circuitry.

Bit 7 - LID_CLOSE - Enables the lid closure circuitry.

- '0' (default) - The lid closure circuitry is disabled.

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- '1' The lid closure circuitry is enabled. The device will use the Lid Closure Status registers in combination with the Lid Closure Pattern register settings to determine when a Lid Closure Event is flagged. In addition, the Noise Status bits are associated with lid closure.

Bit 1 - COMP_PTRN - Determines how the Lid Closure Status registers are compared against the Lid Closure Pattern registers. See [Section 5.26, "Lid Closure Pattern Registers"](#) for details on how the Lid Closure Pattern registers are used.

- '0' (default) - The Lid Closure Status registers are not compared directly against the Lid Closure Pattern registers. Instead, the number of bits in the Lid Closure Status registers is compared to the number of bits in the Lid Closure Pattern registers to determine whether a Lid Closure Event is flagged.
- '1' - The Lid Closure Status registers are compared directly against the Lid Closure Pattern registers. If the bits set in the Lid Closure Pattern are also set in the Lid Status registers, then a Lid Closure Event is flagged.

Bit 0 - LID_ALERT - Enables an interrupt if a Lid Closure Event occurs.

- '0' (default) - If a Lid Closure Event occurs, the ALERT pin is not asserted.
- '1' - If a Lid Closure Event occurs, the ALERT pin will be asserted.

5.25 Lid Closure Queue Control Register

Table 5.35 Lid Closure Queue Control Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|---------------------------|----|----|----|----|----|----------------|----|----|---------|
| 2Ch | R/W | Lid Closure Queue Control | - | - | - | - | - | QUEUE_L_B[2:0] | | | 02h |

The Lid Closure Queue Control register determines the number of consecutive samples for which a single sensor output is above the Lid Closure Threshold before it is flagged.

A value of 0000b is decoded as 1.

Bits 2 - 0 - QUEUE_B[2:0] - The number of consecutive samples from an individual sensor necessary to set the Lid Closure status bit associated with the sensor. The queue applies individually to all sensors (including both buttons and grouped sensors) and applies to setting and clearing the respective status bit. Default is 2 consecutive samples.

5.26 Lid Closure Pattern Registers

Table 5.36 Lid Closure Pattern Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-----------------------|----|--------|--------|--------|--------|--------|-------|-------|---------|
| 2Dh | R/W | Lid Closure Pattern 1 | - | S7_LM | S6_LM | S5_LM | S4_LM | S3_LM | S2_LM | S1_LM | 7Fh |
| 2Eh | R/W | Lid Closure Pattern 2 | | S14_LM | S13_LM | S12_LM | S11_LM | S10_LM | S9_LM | S8_LM | 7Fh |

The Lid Closure Pattern registers act as a pattern to identify an expected sensor profile that is consistent with lid closure. They are only used when lid closure is enabled (see [Section 5.24, "Lid Closure Configuration Register"](#)). There are two methods for how the Lid Closure Status Registers are used with the Lid Closure Pattern registers: as specific sensors that must exceed the lid closure threshold or as the number of sensors that must exceed the lid closure threshold. Which method is

used is based on bit 1 in the Lid Closure Configuration Register. The methods are described below. A Lid Closure Event is flagged in the Group Status register (see [Section 5.10, "Group Status Register"](#)).

1. Specific Sensors: If the bits set in the Lid Closure Pattern are also set in the Lid Status registers, then a Lid Closure Event is flagged.
2. Number of Sensors: The number of bits in the Lid Closure Status registers is compared to the number of bits in the Lid Closure Pattern registers to determine whether a Lid Closure Event is flagged. If any one of the conditions below is met, the Lid Closure Event is flagged.
 - If the number of bits in Lid Closure Status 1 register equals or exceeds the number of bits in the Lid Closure Pattern 1 register, a Lid Closure Event is flagged. In other words, if the number of simultaneous sensors 1-7 exceeding the lid closure threshold meets or exceeds the number of bits in the Lid Closure Pattern 1 register, a Lid Closure Event is flagged.
 - If the number of bits in Lid Closure Status 2 register equals or exceeds the number of bits in the Lid Closure Pattern 2 register, a Lid Closure Event is flagged. In other words, if the number of simultaneous grouped sensors 8-14 exceeding the lid closure threshold meets or exceeds the number of bits in the Lid Closure Pattern 2 register, a Lid Closure Event is flagged.
 - If the total number of bits in both the Lid Closure Status 1 and 2 registers equals or exceeds the total number of bits in both the Lid Closure Pattern 1 and 2 registers, a Lid Closure Event is flagged. In other words, if the total number of sensors above the lid closure threshold is greater than or equal to the number of sensors required for both Lid Closure Patterns, a Lid Closure Event is flagged.

5.27 Recalibration Configuration Register

Table 5.37 Recalibration Configuration Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-----------------------------|-----------|----------|----|--------------|----|--------------|----|----|---------|
| 2Fh | R/W | Recalibration Configuration | BUT_LD_TH | GP_LD_TH | - | ACAL_RT[1:0] | | CAL_CFG[2:0] | | | 93h |

The Recalibration Configuration register controls the automatic re-calibration routine settings as well as advanced controls to program the Sensor Threshold register settings.

Bit 7 - BUT_LD_TH - Enables setting all button Sensor Threshold registers by writing to the Sensor 1 Threshold register.

- '0' - Each Sensor X Threshold register is updated individually.
- '1' (default) - Writing the Sensor 1 Threshold register will automatically overwrite the Sensor Threshold registers for all buttons (Sensor Threshold 1 through Sensor Threshold 7). The individual Sensor X Threshold registers (Sensor 2 Threshold through Sensor 7 Threshold) can be individually updated at any time.

Bit 6 - GP_LD_TH - Enables setting the Group Threshold register by writing to the Sensor 1 Threshold register.

- '0' (default) - The Group Threshold register is updated independently of the Sensor 1 Threshold register.
- '1' - Writing the Sensor 1 Threshold register automatically overwrites the Group Threshold register settings.

Bits 4-3 - ACAL_RT[1:0] - Determines the number of retries the digital logic will perform on the analog calibration routine before it accepts the previous setting.

Table 5.38 ACAL_RT[1:0] Bit Decode

| ACAL_RT[1:0] | | ANALOG CALIBRATION RETRIES |
|--------------|---|----------------------------|
| 1 | 0 | |
| 0 | 0 | Infinite |
| 0 | 1 | 1 |
| 1 | 0 | 3 (default) |
| 1 | 1 | 7 |

Bits 2 - 0 - CAL_CFG[2:0] - Determines the update time and number of samples of the automatic re-calibration routine. The settings applies to all sensors universally (though individual sensors and the group can be configured to support re-calibration - see [Section 5.19](#)).

Table 5.39 CAL_CFG Bit Decode

| CAL_CFG[2:0] | | | RECALIBRATION SAMPLES (SEE Note 5.1) | UPDATE TIME (SEE Note 5.2) |
|--------------|---|---|---|---|
| 2 | 1 | 0 | | |
| 0 | 0 | 0 | 16 | 16 |
| 0 | 0 | 1 | 32 | 32 |
| 0 | 1 | 0 | 64 | 64 |
| 0 | 1 | 1 | 256 | 256 (default) |
| 1 | 0 | 0 | 256 | 1024 |
| 1 | 0 | 1 | 256 | 2048 |
| 1 | 1 | 0 | 256 | 4096 |
| 1 | 1 | 1 | 256 | 7936 |

Note 5.1 Recalibration Samples refers to the number of samples that are measured and averaged before the Base Count is updated.

Note 5.2 Update Time refers to the amount of time (in polling cycle periods) that elapses before the Base Count is updated.

5.28 Sensor Threshold Registers

Table 5.40 Sensor Threshold Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|--------------------|----|----|----|----|----|----|----|----|---------|
| 30h | R/W | Sensor 1 Threshold | - | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 40h |
| 31h | R/W | Sensor 2 Threshold | - | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 40h |

Table 5.40 Sensor Threshold Registers (continued)

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|--------------------|----|----|----|----|----|----|----|----|---------|
| 32h | R/W | Sensor 3 Threshold | - | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 40h |
| 33h | R/W | Sensor 4 Threshold | - | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 40h |
| 34h | R/W | Sensor 5 Threshold | - | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 40h |
| 35h | R/W | Sensor 6 Threshold | - | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 40h |
| 36h | R/W | Sensor 7 Threshold | - | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 40h |
| 37h | R/W | Group Threshold | - | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 40h |

The Sensor Threshold registers store the delta threshold that is used to determine if a touch has been detected. When a touch occurs, the input signal of the corresponding sensor changes due to the capacitance associated with a touch. If the sensor input change exceeds the threshold settings, then a touch is detected.

When the BUT_LD_TH bit is set (see [Section 5.27](#) - bit 7), writing data to the Sensor 1 Threshold register will update all of the button threshold registers (31h - 36h inclusive).

When the GP_LD_TH bit is set (see [Section 5.27](#) - bit 6), writing data to the Sensor 1 Threshold register (30h) will update the Group Threshold register (37h). Individual button registers may be updated independently of the Sensor 1 Threshold settings.

5.29 Button Noise Threshold Registers

Table 5.41 Button Noise Threshold Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|--------------------------|-----------------|----|-----------------|----|-----------------|----|-----------------|----|---------|
| 38h | R/W | Button Noise Threshold 1 | CS4_BN_TH [1:0] | | CS3_BN_TH [1:0] | | CS2_BN_TH [1:0] | | CS1_BN_TH [1:0] | | 55h |
| 39h | R/W | Button Noise Threshold 2 | GR_BN_TH [1:0] | | CS7_BN_TH [1:0] | | CS6_BN_TH [1:0] | | CS5_BN_TH [1:0] | | 55h |

The Button Noise Threshold registers control the value of a secondary internal threshold to detect noise and improve the automatic recalibration routine. If a Capacitive Touch Sensor output exceeds the Button Noise Threshold but does not exceed the sensor threshold, then it is determined to be caused by a noise spike. That sample is not used by the automatic re-calibration routine.

The Button Noise Threshold is proportional to the programmed threshold as shown in [Table 5.42](#).

Table 5.42 CSx_BN_TH Bit Decode

| CSX_BN_TH[1:0] | | THRESHOLD DIVIDE SETTING |
|----------------|---|--------------------------|
| 1 | 0 | |
| 0 | 0 | 6.25% |
| 0 | 1 | 12.5% (default) |
| 1 | 0 | 25% |
| 1 | 1 | 50% |

5.29.1 Button Noise Threshold 1 Register

The Button Noise Threshold 1 register controls the noise threshold for Capacitive Touch Sensors 1-4.

Bits 7-6 - CH4_BN_TH[1:0] - Controls the noise threshold for Capacitive Touch Sensor 4.

Bits 5-4 - CH3_BN_TH[1:0] - Controls the noise threshold for Capacitive Touch Sensor 3.

Bits 3-2 - CH2_BN_TH[1:0] - Controls the noise threshold for Capacitive Touch Sensor 2.

Bits 1-0 - CH1_BN_TH[1:0] - Controls the noise threshold for Capacitive Touch Sensor 1.

5.29.2 Button Noise Threshold 2 Register

The Button Noise Threshold 2 register controls the noise threshold for Capacitive Touch Sensors 5 - 7 and the Grouped sensors.

Bits 7-6 - GR_BN_TH[1:0] - Controls the noise threshold for all grouped Capacitive Touch Sensors.

Bits 5-4 - CH7_BN_TH[1:0] - Controls the noise threshold for Capacitive Touch Sensor 7.

Bits 3-2 - CH6_BN_TH[1:0] - Controls the noise threshold for Capacitive Touch Sensor 6.

Bits 1-0 - CH5_BN_TH[1:0] - Controls the noise threshold for Capacitive Touch Sensor 5.

5.30 Lid Closure Threshold Registers

Table 5.43 Lid Closure Threshold Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-------------------------|------------------|----|------------------|----|------------------|----|------------------|----|---------|
| 3Ah | R/W | Lid Closure Threshold 1 | CS4_LD_TH [1:0] | | CS3_LD_TH [1:0] | | CS2_LD_TH [1:0] | | CS1_LD_TH [1:0] | | AAh |
| 3Bh | R/W | Lid Closure Threshold 2 | CS8_LD_TH [1:0] | | CS7_LD_TH [1:0] | | CS6_LD_TH [1:0] | | CS5_LD_TH [1:0] | | AAh |
| 3Ch | R/W | Lid Closure Threshold 3 | CS12_LD_TH [1:0] | | CS11_LD_TH [1:0] | | CS10_LD_TH [1:0] | | CS9_LD_TH [1:0] | | AAh |
| 3Dh | R/W | Lid Closure Threshold 4 | - | - | - | - | CS14_LD_TH [1:0] | | CS13_LD_TH [1:0] | | 0Ah |

The Lid Closure Threshold registers control the value of a secondary internal threshold to detect noise potentially generated by lid closure. If a Capacitive Touch Sensor output exceeds the Lid Closure

Threshold, the appropriate status bit is set in the Lid Closure Status register (see [Section 5.8, "Lid Closure Status Registers"](#)).

The Lid Closure Threshold is proportional to the programmed Sensor Threshold as shown in [Table 5.42](#).

Table 5.44 CSx_LD_TH Bit Decode

| CSX_LD_TH[1:0] | | THRESHOLD DIVIDE SETTING |
|----------------|---|--------------------------|
| 1 | 0 | |
| 0 | 0 | 6.25% |
| 0 | 1 | 12.5% |
| 1 | 0 | 25% (default) |
| 1 | 1 | 50% |

5.30.1 Lid Closure Threshold 1 Register

The Lid Closure Threshold 1 register controls the lid closure threshold for Capacitive Touch Sensors 1-4.

Bits 7-6 - CS4_LD_TH[1:0] - Controls the lid closure threshold for Capacitive Touch Sensor 4.

Bits 5-4 - CS3_LD_TH[1:0] - Controls the lid closure threshold for Capacitive Touch Sensor 3.

Bits 3-2 - CS2_LD_TH[1:0] - Controls the noise threshold for Capacitive Touch Sensor 2.

Bits 1-0 - CS1_LD_TH[1:0] - Controls the noise threshold for Capacitive Touch Sensor 1.

5.30.2 Lid Closure Threshold 2 Register

The Lid Closure Threshold 2 register controls the lid closure threshold for Capacitive Touch Sensors 5 - 8.

Bits 7-6 - CS8_LD_TH[1:0] - Controls the lid closure threshold for Capacitive Touch Sensor 8 (one of the grouped sensors).

Bits 5-4 - CS7_LD_TH[1:0] - Controls the lid closure threshold for Capacitive Touch Sensor 7.

Bits 3-2 - CS6_LD_TH[1:0] - Controls the lid closure threshold for Capacitive Touch Sensor 6.

Bits 1-0 - CS5_LD_TH[1:0] - Controls the lid closure threshold for Capacitive Touch Sensor 5.

5.30.3 Lid Closure Threshold 3 Register

The Lid Closure Threshold 3 register controls the lid closure threshold for Capacitive Touch Sensors 9 - 12.

Bits 7-6 - CS12_LD_TH[1:0] - Controls the lid closure threshold for Capacitive Touch Sensor 12 (one of the grouped sensors).

Bits 5-4 - CS11_LD_TH[1:0] - Controls the lid closure threshold for Capacitive Touch Sensor 11 (one of the grouped sensors).

Bits 3-2 - CS10_LD_TH[1:0] - Controls the lid closure threshold for Capacitive Touch Sensor 10 (one of the grouped sensors).

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Bits 1-0 - CS9_LD_TH[1:0] - Controls the lid closure threshold for Capacitive Touch Sensor 9 (one of the grouped sensors).

5.30.4 Lid Closure Threshold 4 Register

The Lid Closure Threshold 4 register controls the lid closure threshold for Capacitive Touch Sensors 13 - 14.

Bits 3-2 - CS14_LD_TH[1:0] - Controls the lid closure threshold for Capacitive Touch Sensor 14 (one of the grouped sensors).

Bits 1-0 - CS13_LD_TH[1:0] - Controls the lid closure threshold for Capacitive Touch Sensor 13 (one of the grouped sensors).

5.31 Slider Velocity Configuration Register

Table 5.45 Slider Velocity Configuration Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-------------------------------|------------|--------------|----|------------------|----|-----------------|----|-----|---------|
| 3Eh | R/W | Slider Velocity Configuration | ACC_INT_EN | MAX_INT[2:0] | | SLIDE_TIME [1:0] | | RPT_SCALE [1:0] | | C5h | |

The Slider Velocity Configuration Register also controls the speed sensitive behaviors of the slider, allowing the number of interrupts to be increased as the slide speed increases

Bit 7 - ACC_INT_EN - Enables the device to generate extra interrupts after an accelerated slide has been detected.

- '0' - The device will not generate extra interrupts during or after the slide has been detected.
- '1' (default) - The device will generate extra interrupts after an accelerated slide is detected. The number of extra interrupts generated will be proportional to the speed of the accelerated slide but will not exceed the maximum number of extra interrupts as determined by the MAX_INT bits.

Bits 6-4 - MAX_INT[2:0] - (default 100b) Determine the maximum number of extra interrupts that will be generated after a single slide (regardless of length). The variable "T" is the actual slide time and the parameter SLIDE_TIME is set by bits [3:2] of this register.

Table 5.46 MAX_INT Bit Decode

| MAX_INT[2:0] | | | MAX # INTERRUPTS | # INTERRUPTS FOR T < 1/2 SLIDE_TIME | # INTERRUPTS FOR 1/2 < T < 3/4 SLIDE_TIME | # INTERRUPTS FOR 3/4 < T < FULL SLIDE_TIME |
|--------------|---|---|------------------|-------------------------------------|---|--|
| 2 | 1 | 0 | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 2 | 2 | 1 | 0 |
| 0 | 1 | 1 | 3 | 3 | 1 | 0 |
| 1 | 0 | 0 | 4 | 4 | 2 | 1 |
| 1 | 0 | 1 | 5 | 5 | 2 | 1 |
| 1 | 1 | 0 | 6 | 6 | 3 | 1 |
| 1 | 1 | 1 | 7 | 7 | 3 | 1 |

Bits 3-2 - SLIDE_TIME[1:0] - (default 01b) - Determines how fast a slide must be to generate extra interrupts. This is the maximum slide time that will result in extra interrupts being generated. If the slide time is greater than SLIDE_TIME, no extra interrupts will be generated.

Table 5.47 SLIDE_TIME Bit Decode

| SLIDE_TIME[1:0] | | APPROXIMATE SLIDE TIME (MSEC) |
|-----------------|---|-------------------------------|
| 1 | 0 | |
| 0 | 0 | 350 |
| 0 | 1 | 560 (default) |
| 1 | 0 | 770 |
| 1 | 1 | 980 |

Bits 1 - 0 - RPT_SCALE[1:0] - (default 01b) - Determines how much to increase the Repeat Rate based on slide speed. The slide speed is determined by counting how many sensors are touched in approximately 100msec. The Repeat Rate is then increased various amounts based on the RPT_SCALE parameter.

When read in [Table 5.48](#), the repeat rate given is the number of measurement cycles between interrupts generated.

Table 5.48 RPT_SCALE Bit Decode

| NUMBER OF SENSORS IN 100MSEC | REPEAT RATE (MSEC) RPT_SCALE[1:0] | | | |
|------------------------------|--------------------------------------|----|-----|-----|
| | 00 | 01 | 10 | 11 |
| >=5 | 35 | 35 | 35 | 35 |
| 4 | 35 | 35 | 35 | 70 |
| 3 | 35 | 35 | 70 | 105 |
| 2 | 35 | 70 | 105 | 140 |
| 1 | RPT_RATE_SL | | | |

Note 5.3 If the repeat rate for the slider is set at 105msec or lower, then the 11b case will use the fixed values of 140, 105 and 70msec, respectively.

5.32 Sampling Configuration Register

Table 5.49 Sampling Configuration Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|------------------------|----|----|----|----|----|--------------------|----|----|---------|
| 4Fh | R/W | Sampling Configuration | - | - | - | - | - | OVERSAMP_RATE[2:0] | | | 00h |

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The Sampling Configuration register controls the length of the sampling window of selected Captive Touch Sensor channels as indicated in the Sampling Channel Select register.

Increasing the sampling window time will have two effects. The first effect will be to increase the effective sensitivity of that particular channel so that a touch may be detected with a smaller ΔC or to allow for degrees of proximity detection. However, at the larger sampling times, the resolution of the measurement is reduced.

The second effect will be increase the overall round robin rate (and all timing associated with the round robin rate such as re-calibration times, repeat rate times, and maximum duration times).

All Capacitive Touch Sensors default to a sampling time of 2.5ms. Increasing the sampling time of any single channel will increase the overall polling cycle by the same amount.

Bits 2 - 0 - OVERSAMP_RATE[2:0] - Determine the sample window of all selected sensors.

5.33 Sensor Base Count Registers

Table 5.50 Sensor Base Count Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------------------|-----|----|----|----|----|----|----|----|---------|
| 50h | R | Sensor 1 Base Count | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 51h | R | Sensor 2 Base Count | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 52h | R | Sensor 3 Base Count | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 53h | R | Sensor 4 Base Count | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 54h | R | Sensor 5 Base Count | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 55h | R | Sensor 6 Base Count | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 56h | R | Sensor 7 Base Count | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 57h | R | Sensor 8 Base Count | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 58h | R | Sensor 9 Base Count | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 59h | R | Sensor 10 Base Count | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 5Ah | R | Sensor 11 Base Count | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 5Bh | R | Sensor 12 Base Count | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 5Ch | R | Sensor 13 Base Count | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |
| 5Dh | R | Sensor 14 Base Count | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 | 00h |

The Sensor Base Count registers store the calibrated “Not Touched” input value from the Capacitive Touch Sensor inputs. These registers are periodically updated by the re-calibration routine.

The routine uses an internal adder to add the current count value for each reading to the sum of the previous readings until sample size has been reached. At this point, the upper 16 bits are taken and used as the Sensor Base Count. The internal adder is then reset and the re-calibration routine continues.

The data presented is determined by the C_DSP bits (see [Section 5.13](#)).

5.34 LED / GPIO Direction Registers

Table 5.51 LED / GPIO Direction Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------------------|----------|----------|----------|----------|----------|----------|----------|----------|---------|
| 70h | R/W | LED / GPIO Direction | LED8_DIR | LED7_DIR | LED6_DIR | LED5_DIR | LED4_DIR | LED3_DIR | LED2_DIR | LED1_DIR | 00h |

The LED / GPIO Direction registers control the data flow direction for the LED / GPIO pins. Each pin is controlled by a single bit.

Bit 7 - LED8_DIR - Controls the direction of the LED8 / GPIO8 pin.

- '0' (default) - The LED8 / GPIO8 pin is configured as an input and cannot be used to drive an LED.
- '1' - The LED8 / GPIO8 pin is configured as an output.

Bit 6 - LED7_DIR - Controls the direction of the LED7 / GPIO7 pin.

Bit 5 - LED6_DIR - Controls the direction of the LED6 / GPIO6 pin.

Bit 4 - LED5_DIR - Controls the direction of the LED5 / GPIO5 pin.

Bit 3 - LED4_DIR - Controls the direction of the LED4 / GPIO4 pin.

Bit 2 - LED3_DIR - Controls the direction of the LED3 / GPIO3 pin.

Bit 1 - LED2_DIR - Controls the direction of the LED2 / GPIO2 pin.

Bit 0 - LED1_DIR - Controls the direction of the LED1 / GPIO1 pin.

5.35 LED / GPIO Output Type Registers

Table 5.52 LED / GPIO Output Type Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|--------------------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| 71h | R/W | LED / GPIO Output Type 1 | LED8_OT | LED8_OT | LED6_OT | LED5_OT | LED4_OT | LED3_OT | LED2_OT | LED1_OT | 00h |

The LED / GPIO Output Type registers control the type of output for the LEDx / GPIOx pins that are configured to operate as outputs. Each pin is controlled by a single bit.

- '0' (default) - The LEDx / GPIOx pin is an open-drain output with an external pull-up resistor. When the appropriate pin is set to the “active” state (logic ‘1’) then the pin will be driven low. Conversely, when the pin is set to the “inactive” state (logic ‘0’), then the pin will be left in a High Z state and pulled high via an external pull-up resistor.

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- '1' - The LEDx / GPIOx pin is a push-pull output. When driving a logic '1' the pin is driven high. When driving a logic '0' the pin is driven low.

5.36 GPIO Input Register

Table 5.53 GPIO Input Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|------------|-------|-------|-------|-------|-------|-------|-------|-------|---------|
| 72h | R | GPIO Input | GPIO8 | GPIO7 | GPIO6 | GPIO5 | GPIO4 | GPIO3 | GPIO2 | GPIO1 | 00h |

The GPIO Input registers reflect the state of the LEDx / GPIOx pins. These bits are updated whenever the pin state changes regardless of the operation of the pin. If a LEDx / GPIOx pin is configured as an input, then when a pin changes states, the GPIOx_STS bit is set. If the corresponding interrupt enable bit is also set, then an interrupt will be asserted.

5.37 LED Output Control Registers

Table 5.54 LED Output Control Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------------------|---------|---------|---------|---------|---------|----------|----------|---------|---------|
| 73h | R/W | LED Output Control 1 | LED8_DR | LED7_DR | LED6_DR | LED5_DR | LED4_DR | LED3_DR | LED2_DR | LED1_DR | 00h |
| 74h | R/W | LED Output Control 2 | | | | | | LED11_DR | LED10_DR | LED9_DR | 00h |

The LED Output Control Registers control the output state of the LED pins when they are configured as outputs. For all LED outputs, the "active" state is with the output driven low and the disabled state is with the output in a high Z state (or driven high). These bits are OR'd with the individual control bits defined in the LED Control Register (see [Section 5.37](#)).

All LEDs that are associated with a Capacitive Touch Sensor channel are automatically enabled and will be actuated per the LED Behavior (if enabled as outputs - see [Section 5.34](#)).

For those LEDs that are associated with a dual-color LED outputs, then the inactive state indicates that the LED connected between the drive pin and ground will be on. Likewise, the active state indicates that the LED connected between VDD and the drive in will be on.

For those LEDs that are not linked with a Capacitive Touch Sensor channel, then the bit state determines whether the LED is active (or breathing - see [Section 5.40](#)) or inactive.

5.37.1 LED Output Control 1

Bit 7 - LED8_DR - Determines whether the LED8 output is driven high or low. This LED cannot be linked to a Capacitive Touch Sensor.

- '0' (default) - The LED8 output is driven low.
- '1' - The LED8 output is High Z or driven high.

Bit 6 - LED7_DR - Determines whether LED7 output is driven high or low.

- '0' (default) - The LED7 output is driven low.
- '1' - The LED7 output is High Z or driven high.

Bit 5 - LED6_DR - Determines whether LED6 output is driven high or low.

Bit 4 - LED5_DR - Determines whether LED5 output is driven high or low.

Bit 3 - LED4_DR - Determines whether LED4 output is driven high or low.

Bit 2 - LED3_DR - Determines whether LED3 output is driven high or low.

Bit 1 - LED2_DR - Determines whether LED2 output is driven high or low.

Bit 0 - LED1_DR - Determines whether LED1 output is driven high or low.

5.37.2 LED Output Control 2

Bit 2 - LED11_DR - Determines whether LED11 is active or not. This LED cannot be linked to a Capacitive Touch Sensor.

- '0' (default) - The LED11 output is in High Z and LED will be inactive.
- '1' - The LED11 output is driven low and the LED will be active.

Bit 1 - LED10_DR - Determines whether LED10 is active or not. If this LED is linked to the Group of sensors, then LED9 is automatically linked to the Group if sensors.

- '0' (default) - The LED10 output is in High Z and LED will be inactive. If linked to the Group of Capacitive Touch sensors, then it will remain inactive when actuated.
- '1' - The LED10 output is driven low and the LED will be active. If linked to Group of Capacitive Touch sensors, it will be in High-Z until it is actuated. At this point it will be driven low and the LED will be active.

Bit 0 - LED9_DR - Determines whether LED9 is active or not.

- '0' (default) - The LED9 output is in High Z and LED will be inactive. If linked to the Group of Capacitive Touch sensors, then it will remain inactive when actuated.
- '1' - The LED9 output is driven low and the LED will be active. If linked to Group of Capacitive Touch sensors, it will be in High-Z until it is actuated. At this point it will be driven low and the LED will be active.

5.38 LED Polarity Registers

Table 5.55 LED Polarity Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------------|----------|----------|----------|----------|----------|-----------|-----------|----------|---------|
| 75h | R/W | LED Polarity 1 | LED8_POL | LED7_POL | LED6_POL | LED5_POL | LED4_POL | LED3_POL | LED2_POL | LED1_POL | 00h |
| 76h | R/W | LED Polarity 2 | - | - | - | - | - | LED11_POL | LED10_POL | LED9_POL | 00h |

The LED Polarity registers control the logical polarity of the LED outputs.

APPLICATION NOTE: The polarity controls determine the final LED pin drive. A touch on a linked Capacitive Touch Sensor is treated in the same way as the LED Output Control bit being set to a logic '1'.

APPLICATION NOTE: For LED operation, the duty cycle settings determine the % of time that the LED pin will be driven to a logic '1' state in a non-inverted system or to a logic '0' state in an inverted system. The duty cycle settings operate independently of the polarity controls. Therefore, the Max Duty Cycle settings define the maximum % of time that the LED pin will be driven high in a non-inverted system while the Min Duty Cycle settings determine the minimum % of time that the LED pin will be driven high in a non-inverted system.

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The LED drive assumes that the LEDs are configured such that if the LED pin is driven to a logic '0' then the LED will be on and that the CAP1014 LED pin is sinking the LED current. Conversely, if the LED pin is driven to a logic '1' then the LED will be off and there is no current flow.

Finally, the breathe operations will always ramp the duty cycle from the minimum duty cycle to the maximum duty cycle and then back down to the minimum duty cycle.

The LED Polarity controls lead to two conditions that have the apparent effect of changing the duty cycle settings. If an LED output is non-inverted then the Maximum Duty Cycle settings will define the maximum % of time that the LED is **off**. Conversely the Minimum Duty Cycle settings will define the minimum % of time that the LED is **off**. As well, when there is no touch detected or the LED Output Control register bit is at a logic '0' then the LED output will be driven at the minimum duty cycle setting. The relative brightness will then ramp from maximum to minimum and back.

If an LED output is inverted, then the Maximum Duty Cycle settings will define the maximum % of time that the LED is **off** and the Minimum Duty Cycle settings will determine the minimum % of time that the LED is **on**. As well, when there is no touch detected, or the LED Output Control register bit is at a logic '0', then the LED output will be driven at the minimum duty cycle setting. The relative brightness will then ramp from minimum to maximum and back.

Table 5.56, "LED Polarity Behavior" shows the interaction between the polarity controls, output controls and relative brightness.

Table 5.56 LED Polarity Behavior

| LED OUTPUT CONTROL REGISTER | POLARITY | MAX DUTY | MIN DUTY | LED BEHAVIORS | BRIGHTNESS | LED APPEARANCE |
|-----------------------------|--------------|---|---|---------------|--|---------------------------------------|
| 0 | inverted | maximum % of time that the LED is on (logic 0) | minimum % of time that the LED is on (logic 0) | off | maximum brightness at minimum duty cycle | on at minimum duty cycle |
| 1 | inverted | maximum % of time that the LED is on (logic 0) | minimum % of time that the LED is on (logic 0) | on | maximum brightness at max duty cycle. Brightness ramps from min to max | according to LED behavior |
| 0 | non-inverted | maximum % of time that the LED is off (logic 1) | minimum % of time that the LED is off (logic 1) | off | maximum brightness at 100 - min duty cycle | on at 100 - min duty cycle (Note 5.4) |
| 1 | non-inverted | maximum % of time that the LED is off (logic 1) | minimum % of time that the LED is off (logic 1) | on | maximum brightness at 100 - min duty cycle. Brightness ramps from max to min | according to LED behavior |

Note 5.4 For example when polarity is non-inverted, if min duty cycle is 0, then the LED would be at logic 1 (off) 0% of the time. It will be at logic 0 (on), 100% of the time (100 - min duty cycle).

5.38.1 LED Polarity 1

Bit 7 - LED8_POL - Determines the polarity of the LED8 output.

- '0' - The LED8 output is inverted. A setting of '1' in the LED 8 Output register will cause the output to be driven to a logic '0' as determined by the LED behavior. Similarly, the duty cycles corresponding to Pulse 1, Pulse 2, and Breathe operations will indicate the amount of time that the LED is driven to a logic '0' state (corresponding to "active").

- '1' - The LED8 output is direct. A setting of '1' in the LED 8 Output register will cause the output to be driven to a logic '1' or left in the high-z state as determined by its output type and LED behavior. Similarly, the duty cycles corresponding to Pulse 1, Pulse 2, and Breathe operations will indicate to the amount of time that the LED is driven to a logic '1' state (corresponding to "inactive").

Bit 6 - LED7_POL - Determines the polarity of the LED7 output.

Bit 5 - LED6_POL - Determines the polarity of the LED6 output.

Bit 4 - LED5_POL - Determines the polarity of the LED5 output.

Bit 3 - LED4_POL - Determines the polarity of the LED4 output.

Bit 2 - LED3_POL - Determines the polarity of the LED3 output.

Bit 1 - LED2_POL - Determines the polarity of the LED2 output.

Bit 0 - LED1_POL - Determines the polarity of the LED1 output.

5.38.2 LED Polarity 2

Bit 2 - LED11_POL - Determines the polarity of the LED11 output.

- '0' (default) - The LED11 output is inverted. A setting of '1' in the LED 11 Output register will cause the output to be driven to a logic '0' as determined by the LED behavior. Similarly, the duty cycles corresponding to Pulse 1, Pulse 2, and Breathe operations will indicate the amount of time that the LED is driven to a logic '0' state (corresponding to "active").
- '1' - The LED11 output is direct. A setting of '1' in the LED 11 Output register will cause the output to be driven to a logic '1' or left in the high-z state as determined by its output type and LED behavior. Similarly, the duty cycles corresponding to Pulse 1, Pulse 2, and Breathe operations will indicate to the amount of time that the LED is driven to a logic '1' state (corresponding to "inactive").

Bit 1 - LED10_POL - Determines the polarity of the LED10 output.

Bit 0 - LED9_POL - Determines the polarity of the LED9 output.

5.39 Sensor LED Linking Registers

Table 5.57 Sensor LED Linking Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|--------------------|--------------|----------|----------|----------|----------|----------|----------|----------|---------|
| 80h | R/W | Sensor LED Linking | UP_DOWN_LINK | CS7_LED7 | CS6_LED6 | CS5_LED5 | CS4_LED4 | CS3_LED3 | CS2_LED2 | CS1_LED1 | 00h |

The Sensor LED Linking registers control whether a Capacitive Touch Sensor is linked to an LED output or not. If the corresponding bit is set, then the appropriate LED output will change states defined by the LED Behavior controls (see [Section 5.40](#)) in response to the Capacitive Touch sensor.

If the LED channel is configured as an input, then the corresponding Sensor LED Linking bit is ignored.

Bit 7 - UP_DOWN_LINK - Links the LED10 output to a detected UP condition on the group including a slide in the "up" direction, a tap on the "up" side of the group or a press and hold condition on the "up" side of the group. The LED10 driver will be actuated and will behave as determined by the LED10_CTL bits. This bit also links the LED9 output to a detected DOWN condition on the group including a slide in the "down" direction, a tap on the "down" side of the group or a press and hold condition on the "down" side of the group. The LED9 driver will be actuated and will behave as determined by the LED9_CTL bits.

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LED9 and LED10 will not be active simultaneously. If LED9 is actuated by detecting a slide, tap, or press and hold event, LED10 will be inactive. Likewise, if LED10 is actuated by detecting a slide, tap, or press and hold event, LED9 will be inactive.

Bit 6 - CS7_LED7 - Links the LED7 output to a detected touch on the CS7 sensor. When a touch is detected, the LED is actuated and will behave as determined by the LED Behavior controls.

- '0' - The LED7 output is not associated with a the CS7 input. If a touch is detected on the CS7 input, then the LED will not automatically be actuated. The LED is enabled and controlled via the LED Output Configuration register (see [Section 5.37](#)) and the LED Behavior registers (see [Section 5.40](#)).
- '1' - The LED 7 output is associated with the CS7 in put. If a touch is detected on the CS7 input then the LED will be actuated and behave as defined in [Table 5.59](#). Furthermore, the LED will automatically be enabled.

Bit 5 - CS6_LED6 - Links the LED6 output to a detected touch on the CS6 sensor. When a touch is detected, the LED is actuated and will behave as determined by the LED Behavior controls.

Bit 4 - CS5_LED5 - Links the LED5 output to a detected touch on the CS5 sensor. When a touch is detected, the LED is actuated and will behave as determined by the LED Behavior controls.

Bit 4 - CS4_LED4 - Links the LED4 output to a detected touch on the CS4 sensor. When a touch is detected, the LED is actuated and will behave as determined by the LED Behavior controls.

Bit 2 - CS3_LED3 - Links the LED3 output to a detected touch on the CS3 sensor. When a touch is detected, the LED is actuated and will behave as determined by the LED Behavior controls.

Bit 1 - CS2_LED2 - Links the LED2 output to a detected touch on the CS2 sensor. When a touch is detected, the LED is actuated and will behave as determined by the LED Behavior controls.

Bit 0 - CS1_LED1 - Links the LED1 output to a detected touch on the CS1 sensor. When a touch is detected, the LED is actuated and will behave as determined by the LED Behavior controls.

5.40 LED Behavior Registers

Table 5.58 LED Behavior Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------------|-----------------|-----------------|-----------------|---------------|----|----|----|----|---------|
| 81h | R/W | LED Behavior 1 | LED4_CTL[1:0] | LED3_CTL[1:0] | LED2_CTL[1:0] | LED1_CTL[1:0] | | | | | 00h |
| 82h | R/W | LED Behavior 2 | LED8_CTL[1:0] | LED7_CTL[1:0] | LED6_CTL[1:0] | LED5_CTL[1:0] | | | | | 00h |
| 83h | R/W | LED Behavior 3 | LED11_ALT [1:0] | LED11_CTL [1:0] | LED10_CTL [1:0] | LED9_CTL[1:0] | | | | | 00h |

The LED Behavior registers control the operation of LEDs. Each LEDx / GPIOx pin is controlled by a 2-bit field. If the LEDx / GPIOx pin is configured as an input, then these bits are ignored.

If the corresponding LED output is linked to a Capacitive Touch Sensor than the Start and Stop triggers are used. The defined behavior will activate when the Start Trigger is met and will stop when the Stop Trigger is met. See [Table 5.59](#) and note the behavior of the Breathe Hold and Pulse Release option.

If the LED output is not associated with a Capacitive Touch Sensor, then two available options are Direct and Breathe. In this case, the Start and Stop triggers are ignored and the output of the LED is activated exclusively by the bit state of the control signals.

APPLICATION NOTE: The LED Polarity Control register will determine the non actuated state of the LED outputs. If the LED Polarity Control register is set to be inverted (default), then an non actuated LED pin will be driven to a logic '1' state and the LED will be off. If the LED Polarity Control register is set to be non-inverted, then the non actuated LED pin will be driven to the logic '0' state and the LED will be on.

5.40.1 LED Behavior 1 - 81h

Bits 7 - 6 - LED4_CTL[1:0] - Determines the behavior of LED4 / GPIO4 when configured to operate as an LED output

Bits 5 - 4 - LED3_CTL[1:0] - Determines the behavior of LED3 / GPIO3 when configured to operate as an LED output

Bits 3 - 2 - LED2_CTL[1:0] - Determines the behavior of LED2 / GPIO2 when configured to operate as an LED output

Bits 1 - 0 - LED1_CTL[1:0] - Determines the behavior of LED1 / GPIO1 when configured to operate as an LED output

5.40.2 LED Behavior 2 - 82h

Bits 7 - 6 - LED8_CTL[1:0] - Determines the behavior of LED8 / GPIO8 when configured to operate as an LED output

Bits 5 - 4 - LED7_CTL[1:0] - Determines the behavior of LED7 / GPIO7 when configured to operate as an LED output

Bits 3 - 2 - LED6_CTL[1:0] - Determines the behavior of LED6 / GPIO6 when configured to operate as an LED output

Bits 1 - 0 - LED5_CTL[1:0] - Determines the behavior of LED5 / GPIO5 when configured to operate as an LED output

5.40.3 LED Behavior 3 - 83h

Bits 7 - 6 - LED11_ALT[1:0] - Determines the behavior of LED 11 when the PWR_LED bit is set and either the SLEEP or DSLEEP bits are set (see [Section 5.1](#)).

Bits 5 - 4 - LED11_CTL[1:0] - Determines the behavior of LED11 when the PWR_LED bit is set and both the SLEEP and DSLEEP bits are not set (see [Section 5.1](#)).

Bits 3 - 2 - LED10_CTL[1:0] - Determines the behavior of LED10.

Bits 1 - 0 - LED9_CTL[1:0] - Determines the behavior of LED9.

APPLICATION NOTE: When driving the LED / GPIOx output as a GPO, the LEDx_CTL[1:0] bits should be set to 00b.

Table 5.59 LEDx_CTL Bit Decode

| LEDX_CTL [1:0] | | OPERATION - LINKED WITH SENSOR | OPERATION - NOT LINKED WITH SENSOR | DESCRIPTION | START TRIGGER | STOP TRIGGER |
|----------------|---|--------------------------------|------------------------------------|--|----------------|------------------|
| 1 | 0 | | | | | |
| 0 | 0 | Direct | Direct | The LED is driven to the programmed state (active or inactive). | Press Detected | Release Detected |
| 0 | 1 | Pulse Press (Pulse 1) | Direct | The LED will breathe 5 times starting based on the Start Trigger). The total period of each "breath" is determined by the LED Pulse 1 Period controls - see Section 5.41 | Press Detected | n/a |

Table 5.59 LEDx_CTL Bit Decode (continued)

| LEDX_CTL [1:0] | | OPERATION - LINKED WITH SENSOR | OPERATION - NOT LINKED WITH SENSOR | DESCRIPTION | START TRIGGER | STOP TRIGGER |
|----------------|---|--|------------------------------------|---|----------------|------------------|
| 1 | 0 | | | | | |
| 1 | 0 | Breathe Hold + Pulse Release (Pulse 2) | Breathe | The LED will breathe continuously while the corresponding sensor detects a press. When the sensor detects a release, it will breathe 5 additional times and then stop. The total period of each "breath" is determined by the LED Pulse 2 Period controls - see Section 5.42 . | Press Detected | Release Detected |
| 1 | 1 | Breathe | Breathe | The LED will breathe. It will be driven with a duty cycle that ramps up from the programmed minimum duty cycle (default 0%) to the programmed maximum duty cycle and then back down. Each ramp takes up 50% of the programmed period. The total period of each "breath" is determined by the LED Breathe Period controls - see Section 5.43 . | Press Detected | Release Detected |

APPLICATION NOTE: The PWM frequency is determined based on the selected LED behavior, the programmed breathe period, and the programmed min and max duty cycles. For the Direct Mode, the PWM frequency is calculated based on the programmed Rise and Fall times. If these area set at 0, then the maximum PWM frequency will be used based on the programmed duty cycle settings.

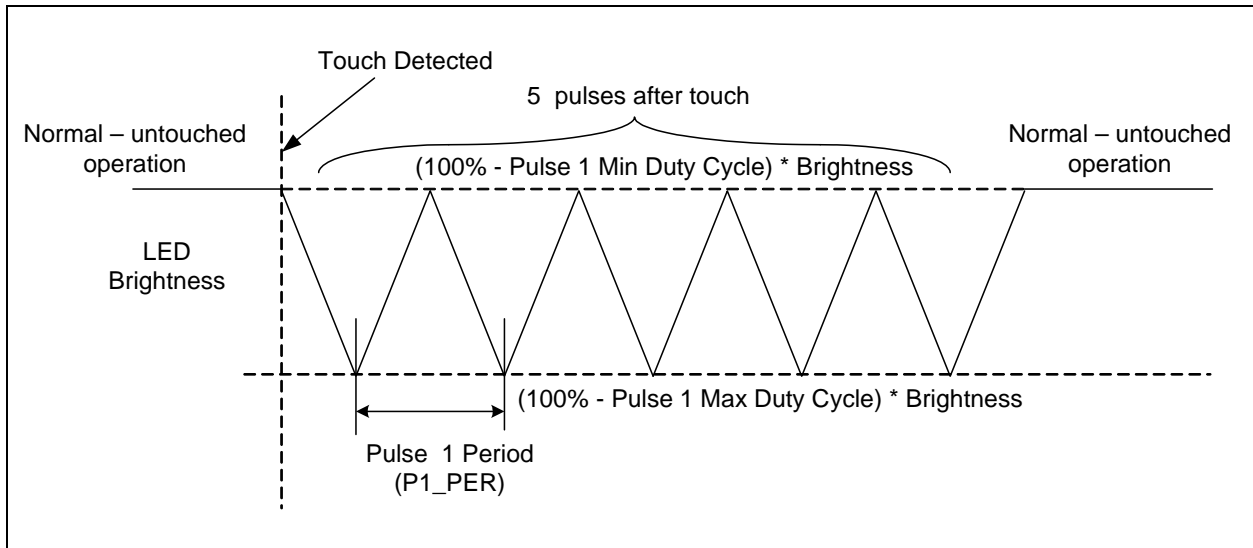
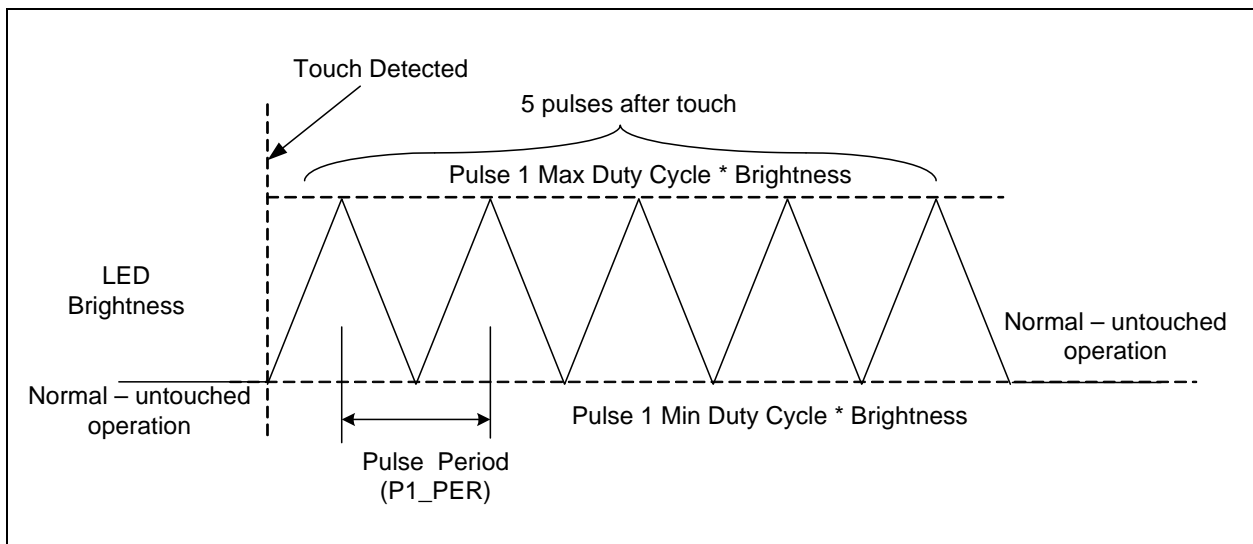
5.41 LED Pulse 1 Period Register

Table 5.60 LED Behavior Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|--------------------|----|----------|----------|----------|----------|----------|----------|----------|---------|
| 84h | R/W | LED Pulse 1 Period | - | P1_ PER6 | P1_ PER5 | P1_ PER4 | P1_ PER3 | P1_ PER2 | P1_ PER1 | P1_ PER0 | 20h |

The LED Pulse 1 Period register determines the overall period of a pulse operation as determined by the LED_CTL registers (see [Table 5.59](#) - setting 01b). Each LSB represents 32ms so that a setting of 14h (20d) would represent a period of 640ms. The total range is from 32ms to 4.06 seconds as shown in [Table 5.61](#).

The Pulse 1 operation is shown in [Figure 5.1](#) (non-inverted polarity) and [Figure 5.2](#) (inverted polarity).


Figure 5.1 Pulse 1 Behavior with Non-Inverted Polarity

Figure 5.2 Pulse 1 Behavior with Inverted Polarity
Table 5.61 LED Pulse / Breathe Period Example

| SETTING (HEX) | SETTING (DECIMAL) | TOTAL BREATHE / PULSE PERIOD (MS) |
|---------------|-------------------|-----------------------------------|
| 00h | 0 | 32 |
| 01h | 1 | 32 |
| 02h | 2 | 64 |
| 03h | 3 | 96 |

Table 5.61 LED Pulse / Breathe Period Example (continued)

| SETTING (HEX) | SETTING (DECIMAL) | TOTAL BREATHE / PULSE PERIOD (MS) |
|---------------|-------------------|-----------------------------------|
| 04h | 4 | 128 |
| ... | ... | ... |
| 7Ch | 124 | 3,968 |
| 7Dh | 125 | 4,000 |
| 7Eh | 126 | 4,032 |
| 7Fh | 127 | 4.064 |

5.42 LED Pulse 2 Period Register

Table 5.62 LED Behavior Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|--------------------|----|---------|---------|---------|---------|---------|---------|---------|---------|
| 85h | R/W | LED Pulse 2 Period | - | P2_PER6 | P2_PER5 | P2_PER4 | P2_PER3 | P2_PER2 | P2_PER1 | P2_PER0 | 14h |

The LED Pulse 2 Period register determines the overall period of a pulse operation as determined by the LED_CTL registers (see [Table 5.59](#) - setting 10b). Each LSB represents 32ms so that a setting of 14h (20d) would represent a period of 640ms. The total range is from 32ms to 4.06 seconds (see [Table 5.61](#)).

The Pulse 2 Behavior is shown in [Figure 5.3](#) (non-inverted polarity) and [Figure 5.4](#) (inverted polarity).

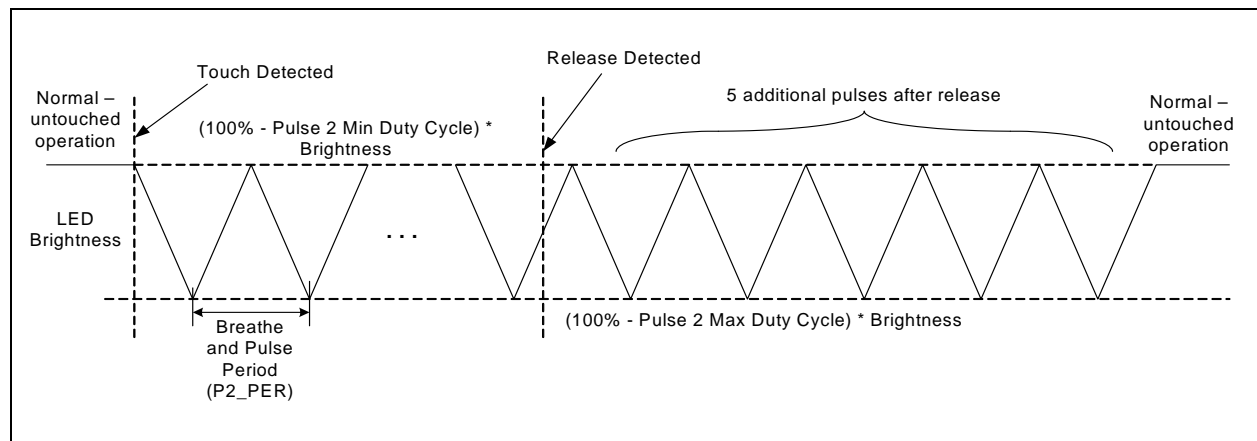


Figure 5.3 Pulse 2 Behavior with Non-Inverted Polarity

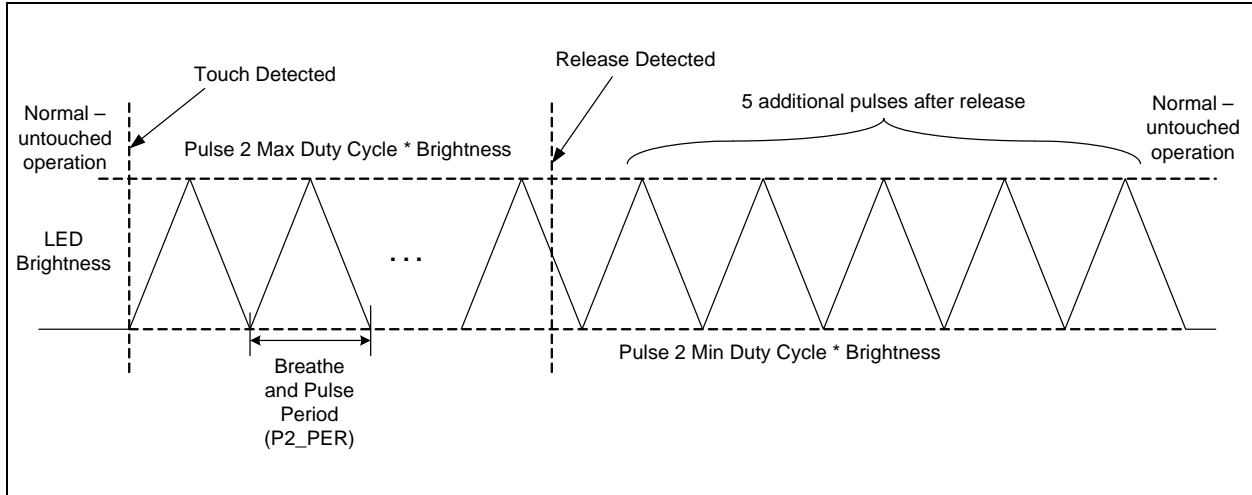


Figure 5.4 Pulse 2 Behavior with Inverted Polarity

5.43 LED Breathe Period Register

Table 5.63 LED Behavior Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|--------------------|----|---------|---------|---------|---------|---------|---------|---------|---------|
| 86h | R/W | LED Breathe Period | - | BR_PER6 | BR_PER5 | BR_PER4 | BR_PER3 | BR_PER2 | BR_PER1 | BR_PER0 | 5Dh |

The LED Breathe Period register determines the overall period of a breathe operation as determined by the LED_CTL registers (see [Table 5.59](#) - setting 11b). Each LSB represents 32ms so that a setting of 14h (20d) would represent a period of 640ms. The total range is from 32ms to 4.06 seconds (see [Table 5.61](#)).

5.44 LED Pulse Configuration Register

Table 5.64 LED Configuration Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|------------------|----|----|-----------------|----|----|-----------------|----|----|---------|
| 88h | R/W | LED Pulse Config | - | - | PULSE2_CNT[2:0] | | | PULSE1_CNT[2:0] | | | 24h |

The LED Pulse Configuration register controls the number of pulses that are sent for the Pulse 1 and Pulse 2 LED output behaviors.

Bits 5 - 3 - PULSE2_CNT[2:0] - Determines the number of pulses used for the Pulse 2 behavior as shown in [Table 5.65](#). The default is 100b.

Bits 2 - 0 - PULSE1_CNT[2:0] - Determines the number of pulses used for the Pulse 1 behavior as shown in [Table 5.65](#).

Table 5.65 PULSE_CNT Decode

| PULSEX_CNT[2:0] | | | NUMBER OF BREATHS |
|-----------------|---|---|-------------------|
| 2 | 1 | 0 | |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 (default) |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 7 |
| 1 | 1 | 1 | 8 |

5.45 LED Pulse and Breathe Duty Cycle Registers

Table 5.66 LED Period and Duty Cycle Registers

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|------------------------|----------------------|----|----|----|----------------------|----|----|----|---------|
| 90h | R/W | LED Pulse 1 Duty Cycle | LED_P1_MAX_DUTY[3:0] | | | | LED_P1_MIN_DUTY[3:0] | | | | F0h |
| 91h | R/W | LED Pulse 2 Duty cycle | LED_P2_MAX_DUTY[3:0] | | | | LED_P2_MIN_DUTY[3:0] | | | | F0h |
| 92h | R/W | LED Pulse 3 Duty Cycle | LED_BR_MAX_DUTY[3:0] | | | | LED_BR_MIN_DUTY[3:0] | | | | F0h |
| 93h | R/W | Direct Duty Cycle | LED_DR_MAX_DUTY[3:0] | | | | LED_DR_MIN_DUTY[3:0] | | | | F0h |

The LED Pulse and Breathe Duty Cycle registers determine the minimum and maximum duty cycle settings used for the LED for each LED behavior. These settings affect the brightness of the LED when it is fully off and fully on.

The LED driver duty cycle will ramp up from the minimum duty cycle (see [Section 5.45](#)) to the maximum duty cycle and back down again.

APPLICATION NOTE: Changes to the Duty Cycle settings will be applied immediately. When the respective register is written, the LED output will be reset to the minimum (or maximum) setting and restarted at the updated settings.

APPLICATION NOTE: Upon power on reset (or upon release of the RESET pin), the first breath will breathe from 100% (or 0% duty cycle as determined by the polarity registers) to the programmed minimum (or maximum as determined by the polarity registers) and then proceed normally.

Bits 7 - 4 - LED_X_MAX_DUTY[3:0] - Determines the maximum PWM duty cycle for the LED drivers as shown in [Table 5.67](#).

Bits 3 - 0 - LED_X_MIN_DUTY[3:0] - Determines the minimum PWM duty cycle for the LED drivers as shown in [Table 5.67](#).

Table 5.67 LED Duty Cycle Decode

| LED_X_MAX/MIN_DUTY [3:0] | | | | DUTY CYCLE |
|--------------------------|---|---|---|------------|
| 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | 0% |
| 0 | 0 | 0 | 1 | 12.5% |
| 0 | 0 | 1 | 0 | 18.75% |
| 0 | 1 | 1 | 1 | 25.0% |
| 0 | 1 | 0 | 0 | 31.25% |
| 0 | 1 | 0 | 1 | 37.5% |
| 0 | 1 | 1 | 0 | 43.75% |
| 0 | 1 | 1 | 1 | 50.0% |
| 1 | 0 | 0 | 0 | 56.25% |
| 1 | 0 | 0 | 1 | 62.5% |
| 1 | 0 | 1 | 0 | 68.75% |
| 1 | 0 | 1 | 1 | 75.0% |
| 1 | 1 | 0 | 0 | 81.25% |
| 1 | 1 | 0 | 1 | 87.5% |
| 1 | 1 | 1 | 0 | 93.75% |
| 1 | 1 | 1 | 1 | 100% |

5.46 LED Direct Ramp Rates Register

Table 5.68 LED Direct Ramp Rates Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|-----------------------|----|----|----------------|----|----|----------------|----|----|---------|
| 94h | R/W | LED Direct Ramp Rates | - | - | RISE_RATE[2:0] | | | FALL_RATE[2:0] | | | 00h |

The LED Direct Ramp Rates register control the rising and falling edge time of an LED that is configured to operate in Direct mode and is linked to a Capacitive Touch sensor. The rising edge time corresponds to the amount of time the LED takes to transition from its minimum duty cycle to its maximum duty cycle. Conversely, the falling edge time corresponds to the amount of time that the LED takes to transition from its maximum duty cycle to its minimum duty cycle.

Bits 5 - 3 - RISE_RATE[2:0] - Determines the rising edge time of an LED when it transitions from its minimum drive state to its maximum drive state as shown in [Table 5.69](#).

Datasheet

Bits 2 - 0 - FALL_RATE[2:0] - Determines the falling edge time of an LED when it transitions from its maximum drive state to its minimum drive state as shown in [Table 5.69](#).

Table 5.69 Rise / Fall Rate Cycle Decode

| RISE/FALL_RATE [2:0] | | | RISE / FALL TIME (T_{RISE} / T_{FALL}) |
|----------------------|---|---|--|
| 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 250ms |
| 0 | 1 | 0 | 500ms |
| 1 | 1 | 1 | 750ms |
| 1 | 0 | 0 | 1s |
| 1 | 0 | 1 | 1.25s |
| 1 | 1 | 0 | 1.5s |
| 1 | 1 | 1 | 2s |

5.47 LED Off Delay Register

Table 5.70 LED Off Delay Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|------------------------|----|----|----|----|----|-------------------|----|----|---------|
| 95h | R/W | LED Off Delay Register | - | - | | - | - | DIR_OFF_DLY [2:0] | | | 00h |

The LED Off Delay register determines the amount of time an LED in direct mode remains active after it is no longer actuated (such as after a release has been detected or the drive state has been changed). This register is only used if the LED is linked to a Capacitive Touch sensor.

Bits 2 - 0 - DIR_OFF_DLY[2:0] - Determines the turn-off delay for all LEDs that are configured to operate in Direct Mode as shown in [Table 5.71](#).

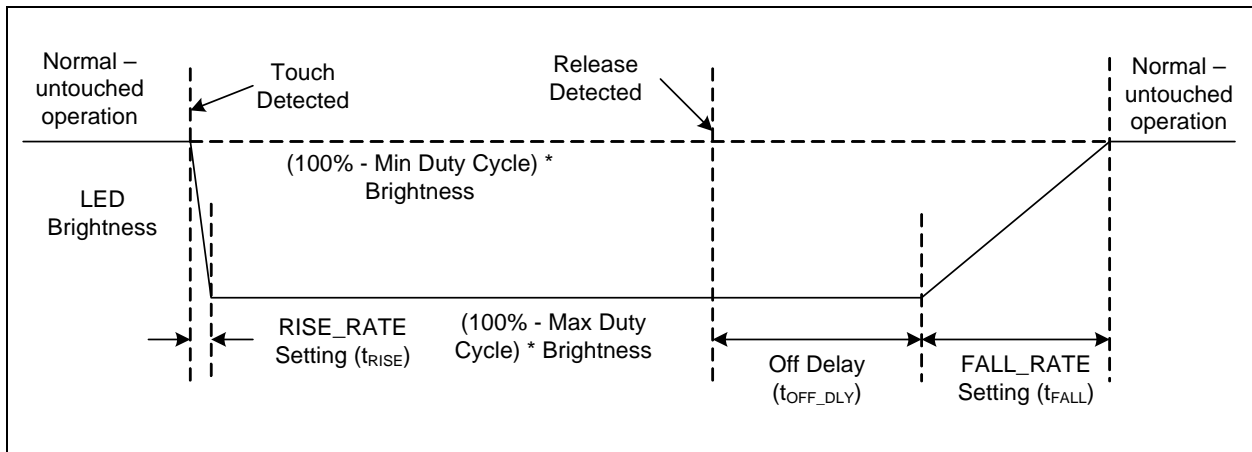
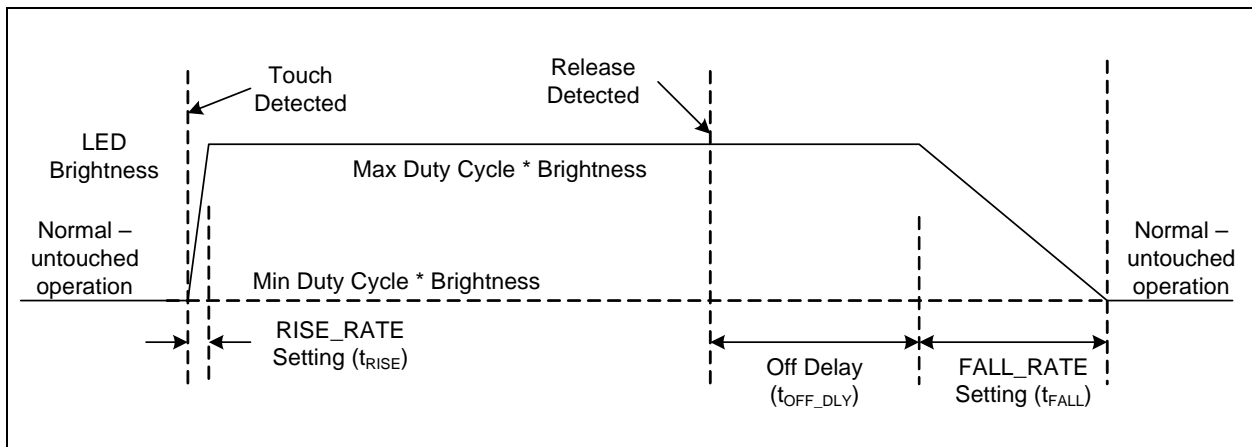
Table 5.71 Off Delay Settings

| DIR_OFF_DLY [2:0] | | | OFF DELAY T_{OFF_DLY} |
|-------------------|---|---|-----------------------------|
| 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0.5s |
| 0 | 1 | 0 | 1.0s |
| 0 | 1 | 1 | 1.5s |
| 1 | 0 | 0 | 2.0s |
| 1 | 0 | 1 | 3.0s |

Table 5.71 Off Delay Settings (continued)

| DIR_OFF_DLY [2:0] | | | OFF DELAY T_{OFF_DLY} |
|-------------------|---|---|-----------------------------|
| 2 | 1 | 0 | |
| 1 | 1 | 0 | 4.0s |
| 1 | 1 | 1 | 5.0s |

The Direct Mode operation is shown determined by the combination of programmed Rise Time, Fall Time, and Off Delay as shown in [Figure 5.5](#) (non-inverted polarity) and [Figure 5.6](#) (inverted polarity).


Figure 5.5 Direct Mode Behavior for Non-Inverted Polarity

Figure 5.6 Direct Mode Behavior for Inverted Polarity

These OTP bits are incremented any time the OTP bits are changed once devices are shipped to HP.

5.48 Product ID Register

Table 5.72 Product ID Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|------------|----|----|----|----|----|----|----|----|---------|
| FDh | R | Product ID | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2Dh |

The Product ID register stores a unique 8-bit value that identifies the device.

5.49 Revision Register

Table 5.73 Revision Register

| ADDR | R/W | REGISTER | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | DEFAULT |
|------|-----|----------|----|----|----|----|----|----|----|----|---------|
| FFh | R | Revision | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 81h |

The Revision register stores an 8-bit value that represents the part revision.

Note: Rev 00h was an engineering build and not released. Revision 81h is the first released version of the device, Functional Revision A.

Chapter 6 Package Information

6.1 Package Drawings

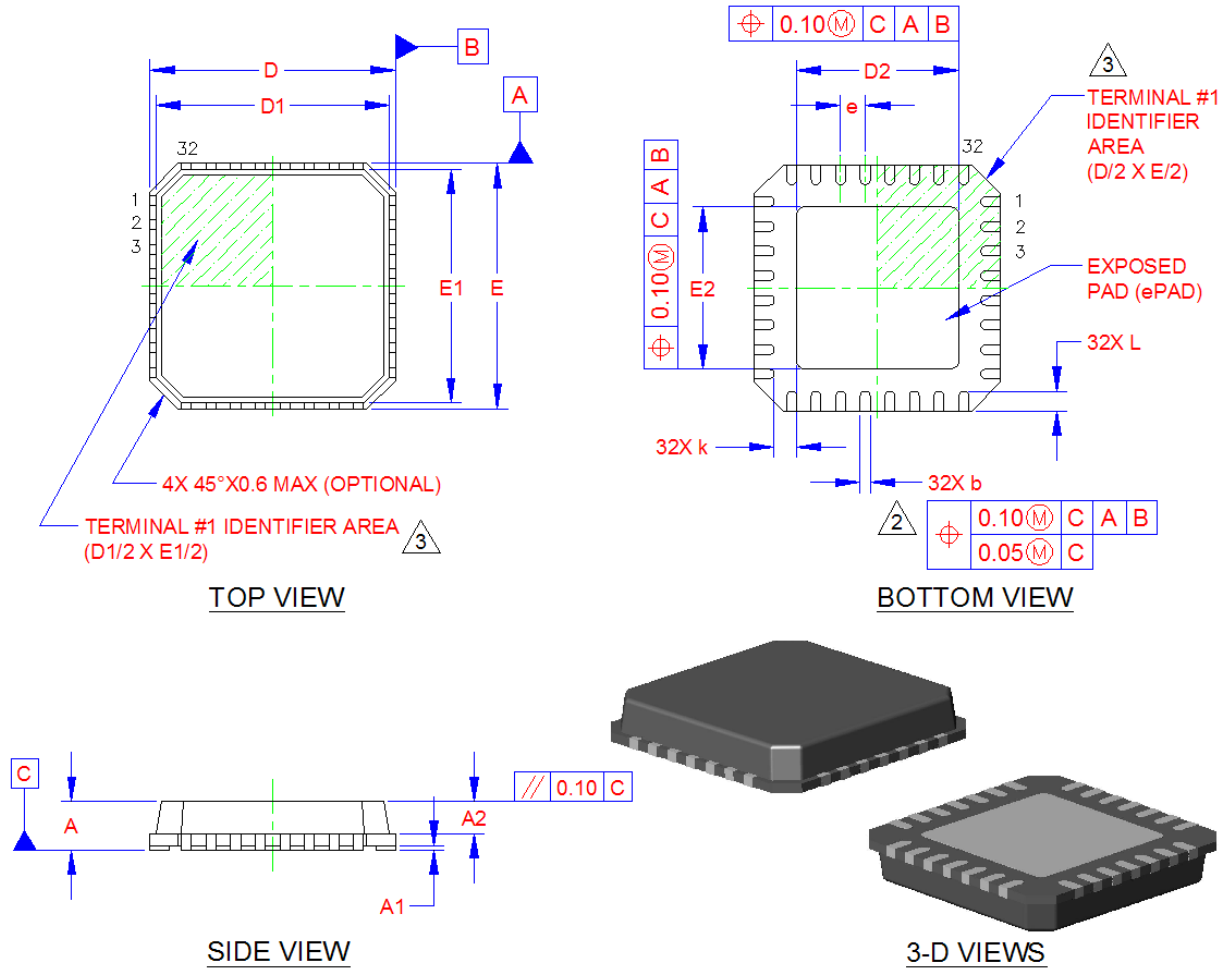


Figure 6.1 Package Diagram - 32-Pin QFN

| COMMON DIMENSIONS | | | | | |
|-------------------|----------|------|------|------|----------------------------|
| SYMBOL | MIN | NOM | MAX | NOTE | REMARK |
| A | 0.70 | 0.85 | 1.00 | - | OVERALL PACKAGE HEIGHT |
| A1 | 0 | 0.02 | 0.05 | - | STANDOFF |
| A2 | - | - | 0.90 | - | MOLD CAP THICKNESS |
| D/E | 4.90 | 5.00 | 5.10 | - | X/Y BODY SIZE |
| D1/E1 | 4.55 | 4.75 | 4.95 | - | X/Y MOLD CAP SIZE |
| D2/E2 | 3.10 | 3.30 | 3.40 | - | X/Y EXPOSED PAD SIZE |
| L | 0.30 | 0.40 | 0.50 | - | TERMINAL LENGTH |
| b | 0.18 | 0.25 | 0.30 | 2 | TERMINAL WIDTH |
| k | 0.35 | - | - | - | TERMINAL TO ePAD CLEARANCE |
| e | 0.50 BSC | | | - | TERMINAL PITCH |

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

Figure 6.1 Package Dimensions - 32-Pin QFN

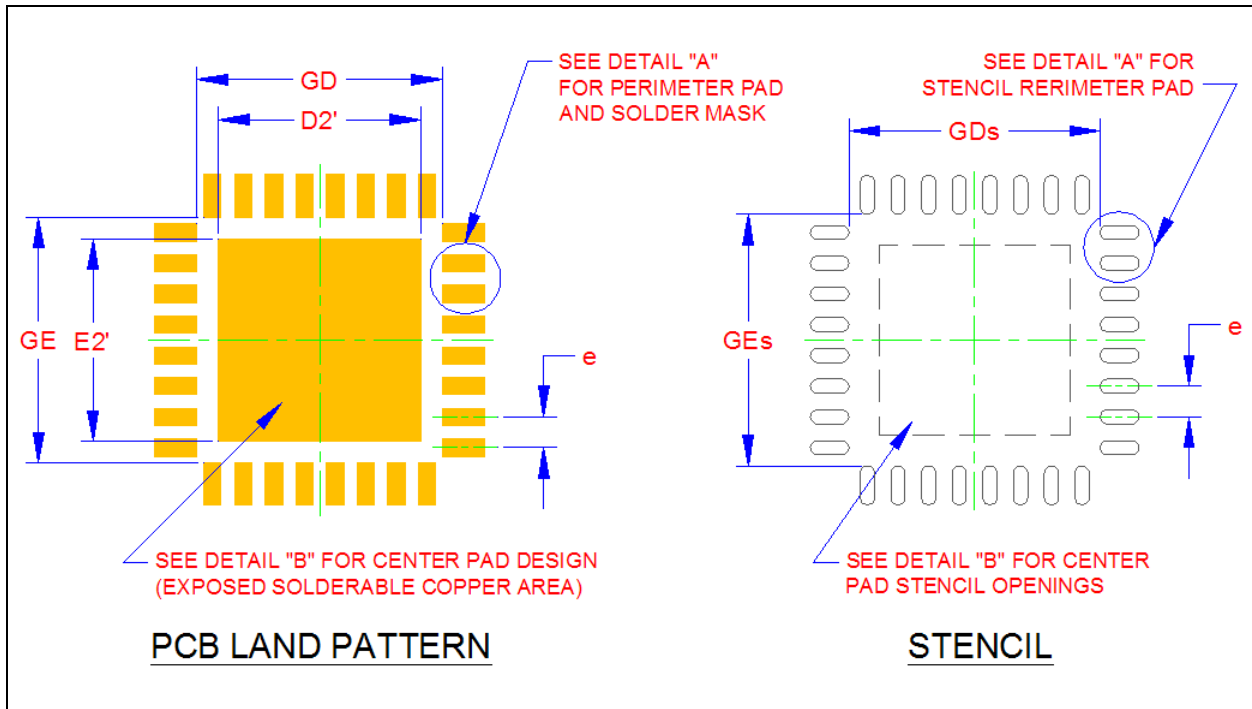


Figure 6.2 Package PCB Land Pattern and Stencil

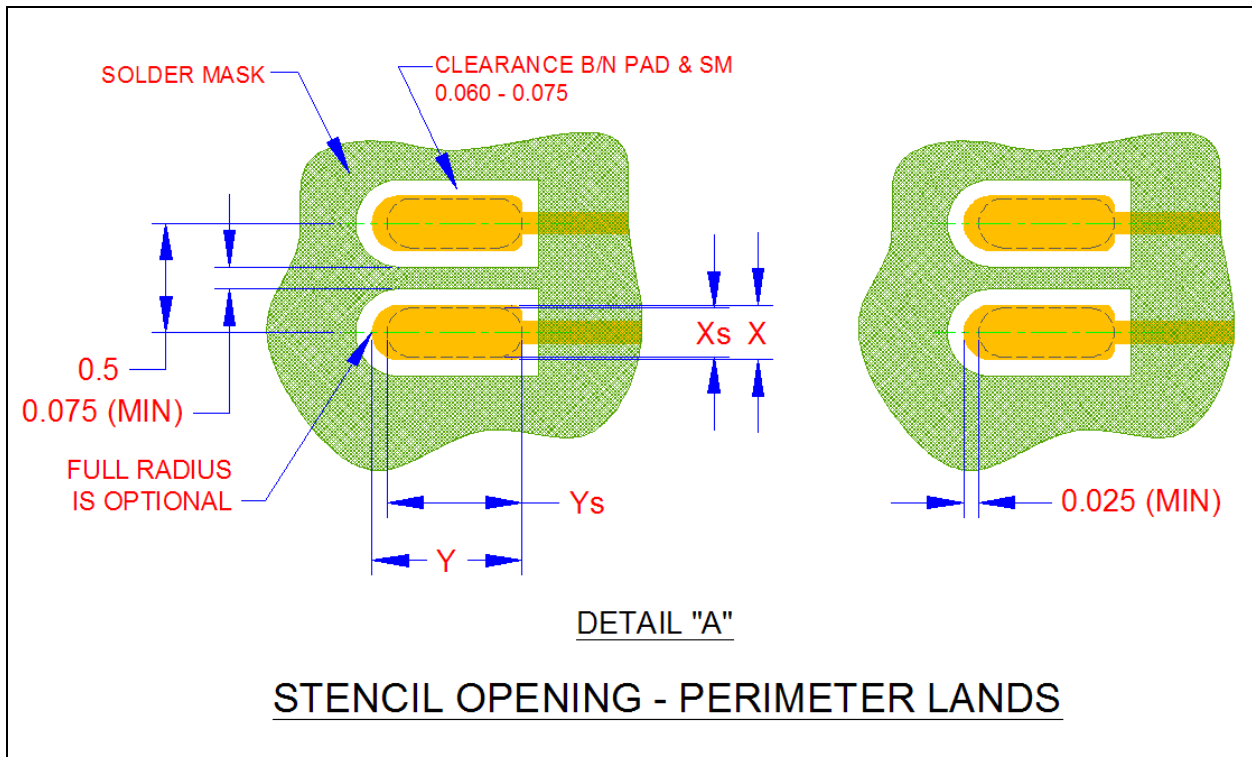


Figure 6.3 Package Detail A - Stencil Opening and Perimeter Lands

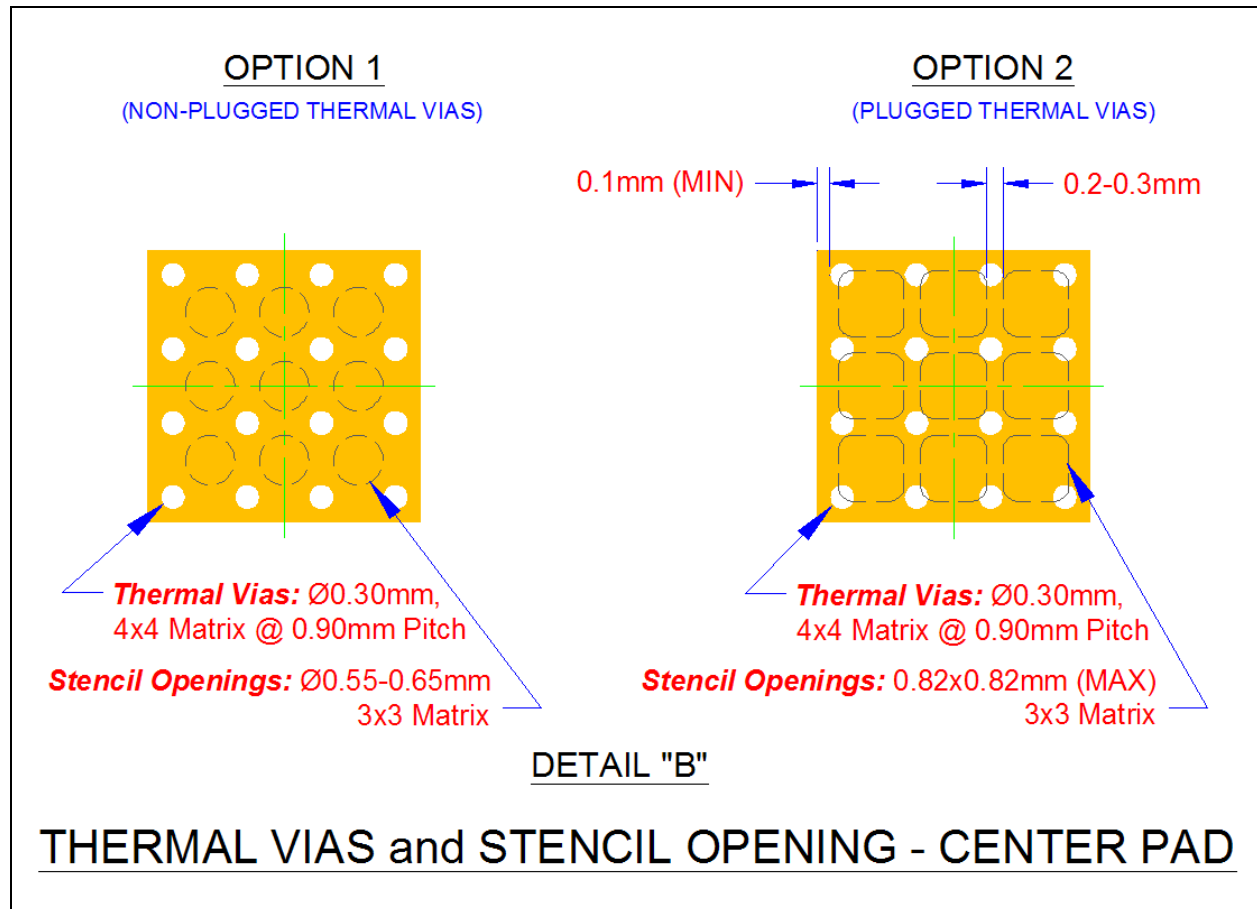


Figure 6.4 Package Detail B - Thermal Via and Stencil Opening

| LAND PATTERN DIMENSIONS | | | |
|-------------------------|------|------|------|
| SYMBOL | MIN | NOM | MAX |
| GD/GE | 4.00 | - | 5.10 |
| GDs/GEs | 4.05 | - | - |
| D2'/E2' | - | 3.30 | 3.30 |
| Pad: X | - | 0.28 | 0.28 |
| Stencil: Xs | - | 0.23 | 0.25 |
| Pad: Y | - | 0.69 | 0.69 |
| Stencil: Ys | - | 0.62 | 0.64 |
| e | 0.50 | | |

Figure 6.5 Package Land Pattern Dimensions

6.2 Package Marking

All packages will be marked as shown in [Figure 6.1](#).

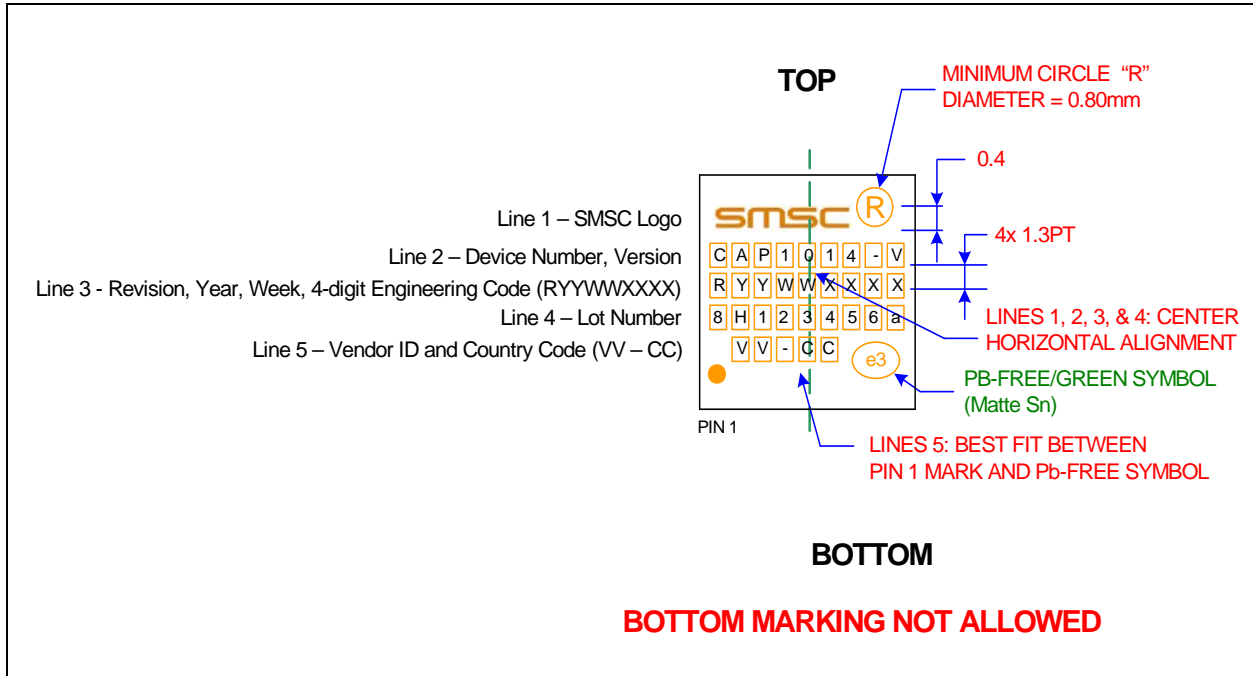


Figure 6.1 Package Markings

Chapter 7 Revision History

Table 7.1 Customer Revision History

| REVISION LEVEL & DATE | SECTION/FIGURE/ENTRY | CORRECTION |
|--------------------------|---|--|
| Revision 1.65 (08-11-09) | Features | Low Power operation bullet; "1 or more buttons" changed to "2" |
| | Ordering Information | Added CAP1014-2 order number. Added "features" column to ordering table. |
| | Table 1.1, "Pin Description for CAP1014" | Added note below table: For all 5V tolerant pins that require a pull-up resistor, the voltage difference between VDD and the pull-up voltage must never exceed 3.6V. |
| | Table 2.1, "Absolute Maximum Ratings" | <p>Added voltage limits for 5V tolerant pins with pull-up resistors: Voltage on 5V tolerant pins ($V_{5VT_pin} - V_{DD}$) 0 to 3.6V.</p> <p>Added note below table: For the 5V tolerant pins that have a pull-up resistor, the pull-up voltage must not exceed 3.6V when the device is unpowered.</p> <p>Updated thetaJA for the device from 40 to 48 and for the package from 52 to 60.</p> <p>Updated via recommendations from 4 to a 4x4 array.</p> |
| | Table 2.2, "Electrical Specifications" | <p>Added typical values for DC Power - Supply Current.</p> <p>I_{SLEEP} MAX value changed from "250" to "300" and</p> <p>I_{DSLEEP} MAX value changed from "100" to "200"</p> <p>Added pull-up voltage $\leq 3.6V$ condition to leakage current.</p> <p>I_{DD} TYP changed from "420" to "0.42"</p> |
| | Section 4.1, "Power States" | Default for Sleep state modified from "2" to "0" |
| | Section 4.4.2, "Lid Closure" | Added. |
| | Section 5.7, "Noise Flag Status Registers" | Added application note regarding lid closure. |
| | Section 5.8, "Lid Closure Status Registers" | Added. |
| | Section 5.10, "Group Status Register" | Added bit 7 for lid closure. |
| | Section 5.23, "Multiple Touch Configuration Register" | Renamed MULT_EN to MULT_BLK_EN. |
| | Section 5.24, "Lid Closure Configuration Register" | Added. |
| | Section 5.25, "Lid Closure Queue Control Register" | Added. |

Table 7.1 Customer Revision History (continued)

| REVISION LEVEL & DATE | SECTION/FIGURE/ENTRY | CORRECTION |
|--------------------------|---|---|
| | Section 5.26, "Lid Closure Pattern Registers" | Added. |
| | Section 5.30, "Lid Closure Threshold Registers" | Added. |
| | Section 5.32, "Sampling Configuration Register" | Added. |
| | Section 5.38, "LED Polarity Registers" | Added application notes and Table 5.56, "LED Polarity Behavior" . |
| | Section 5.40, "LED Behavior Registers" | Added application note regarding polarity controlling non-actuated state of LEDs. |
| | Section 5.41, "LED Pulse 1 Period Register" | Updated figures to show behavior with inverted and normal polarity. |
| | Section 5.42, "LED Pulse 2 Period Register" | Updated figures to show behavior with inverted and normal polarity. |
| | Section 5.47, "LED Off Delay Register" | Updated figures to show behavior with inverted and normal polarity. |
| | Section 5.3, "Build Revision Register" | Updated BUILD register bit settings |
| | Table 5.5, "Build History" | Added table for Build History |
| | Section 6.1, "Package Drawings" | Replaced single composite figure with individual figures to improve readability. |
| Revision 1.64 (01-15-09) | Initial Release | |