

H5N2005DL, H5N2005DS

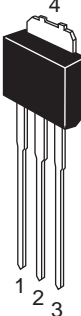

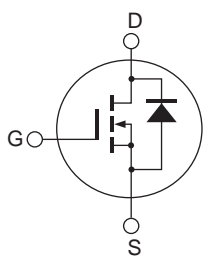
200V - 6A - MOS FET
High Speed Power Switching

R07DS0796EJ0400
(Previous: REJ03G1104-0300)
Rev.4.00
Jun 07, 2012

Features

- Low on-resistance
 $R_{DS(on)} = 0.52 \Omega$ typ. (at $I_D = 3 A$, $V_{GS} = 10 V$, $T_a = 25^\circ C$)
- Low drive power
- High speed switching

Outline

RENESAS Package code: PRSS0004ZD-B (Package name: DPAK(L)-(2))	RENESAS Package code: PRSS0004ZD-C (Package name: DPAK(S))
	
	
1. Gate 2. Drain 3. Source 4. Drain	

Absolute Maximum Ratings

($T_a = 25^\circ C$)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	200	V
Gate to source voltage	V_{GSS}	± 30	V
Drain current	I_D	6	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	24	A
Body-drain diode reverse drain current	I_{DR}	6	A
Body-drain diode reverse drain peak current	$I_{DR(pulse)}$ ^{Note 1}	24	A
Avalanche current	I_{AP} ^{Note 3}	6	A
Channel dissipation	P_{ch} ^{Note 2}	25	W
Channel to case thermal Impedance	θ_{ch-c}	5	$^\circ C/W$
Channel temperature	T_{ch}	150	$^\circ C$
Storage temperature	T_{stg}	-55 to +150	$^\circ C$

- Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
 2. Value at $T_c = 25^\circ C$
 3. $STch = 25^\circ C$, $T_{ch} \leq 150^\circ C$

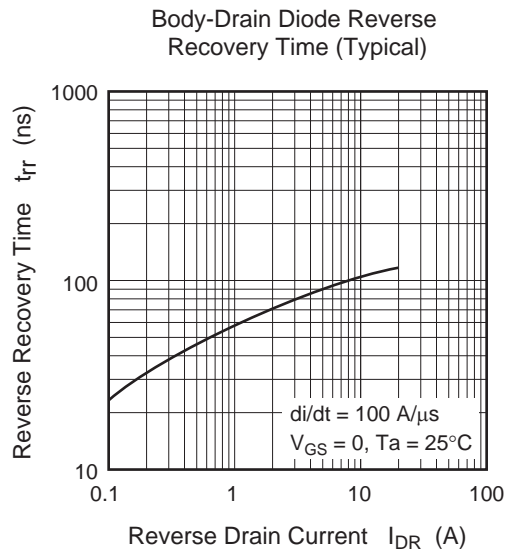
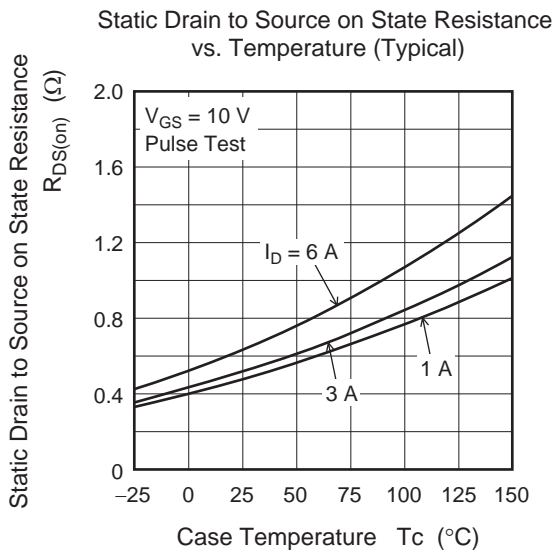
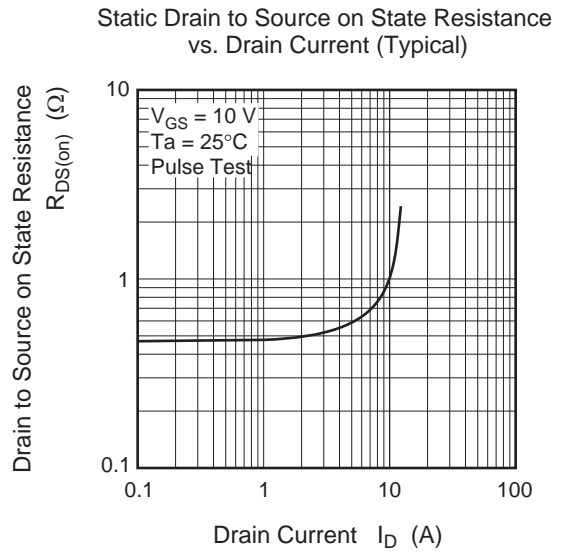
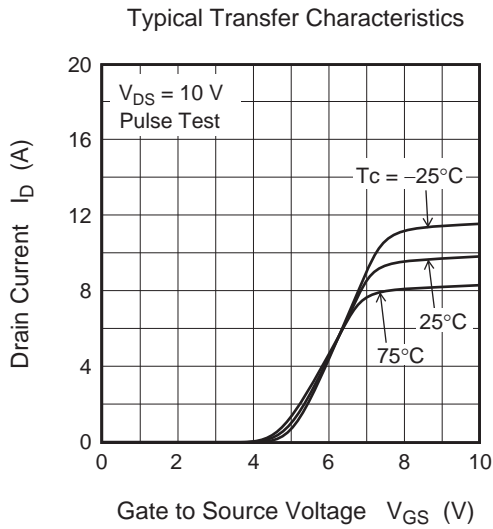
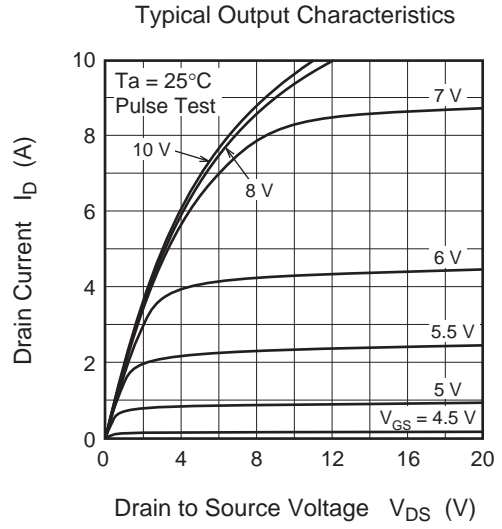
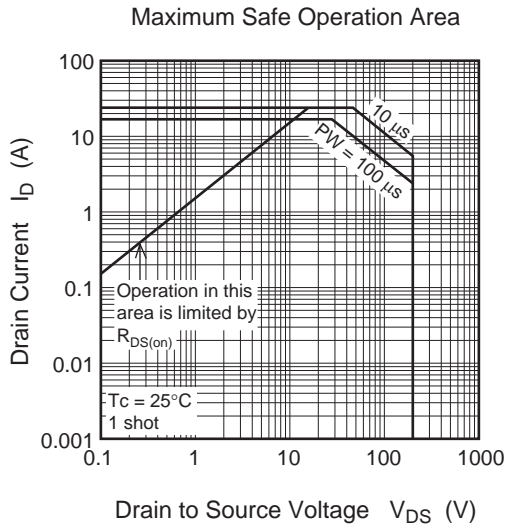
Electrical Characteristics

(Ta = 25°C)

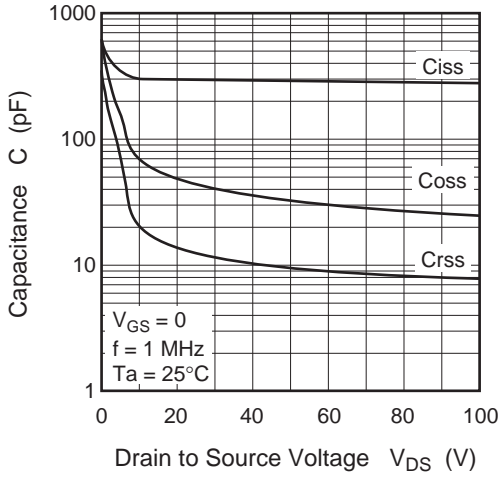
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 200 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.52	0.65	Ω	$I_D = 3 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 4}
Forward transfer admittance	$ y_{fs} $	2.0	3.4	—	S	$I_D = 3 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note 4}
Input capacitance	C_{iss}	—	300	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	C_{oss}	—	44	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	12.5	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	9.8	—	nC	$V_{DD} = 160 \text{ V}$
Gate to source charge	Q_{gs}	—	2.0	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	5.2	—	nC	$I_D = 6 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	23	—	ns	$I_D = 3 \text{ A}$
Rise time	t_r	—	24	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	43.5	—	ns	$R_L = 33.3 \Omega$
Fall time	t_f	—	11	—	ns	$R_g = 10 \Omega$
Body-drain diode forward voltage	V_{DF}	—	1.0	1.5	V	$I_F = 6 \text{ A}$, $V_{GS} = 0$ ^{Note 4}
Body-drain diode reverse recovery time	t_{rr}	—	90	—	ns	$I_F = 6 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery charge	Q_{rr}	—	300	—	nC	$di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

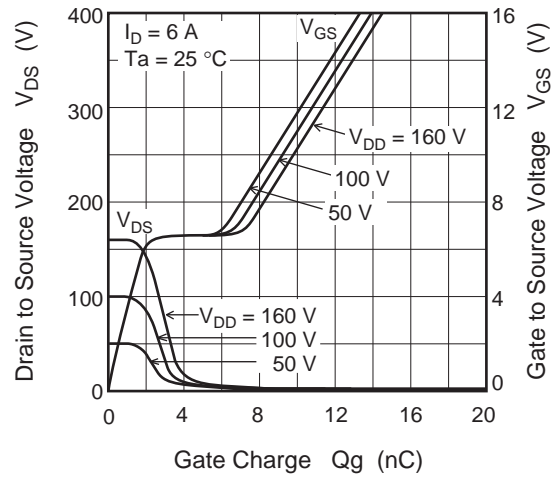
Main Characteristics



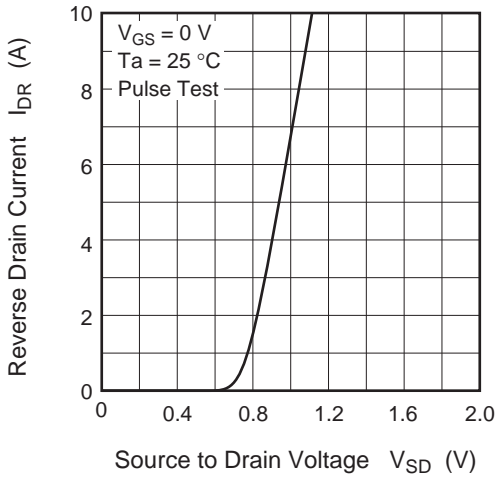
Typical Capacitance vs. Drain to Source Voltage (Typical)



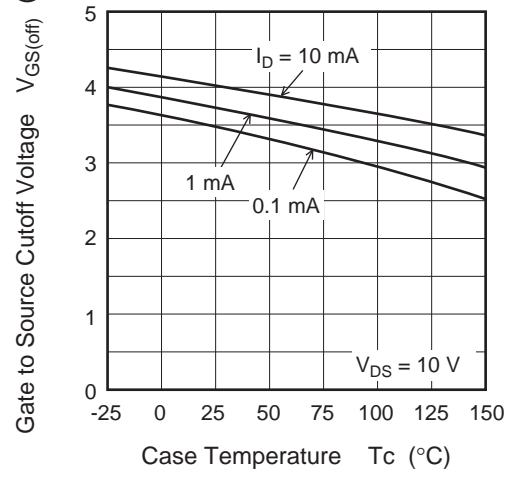
Dynamic Input Characteristics (Typical)



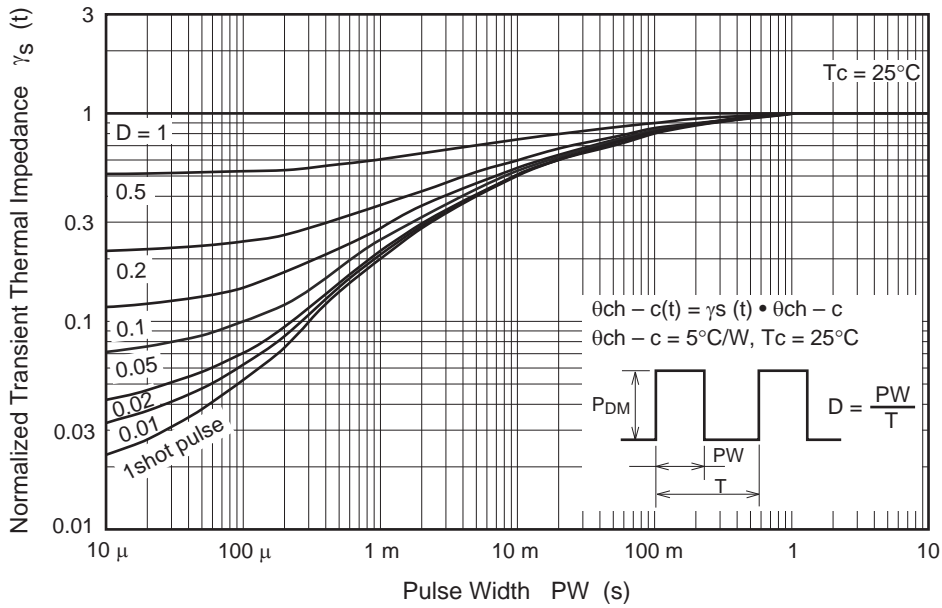
Reverse Drain Current vs. Source to Drain Voltage (Typical)



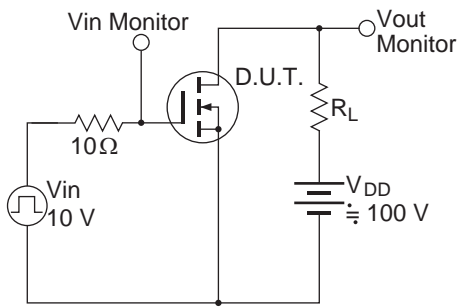
Gate to Source Cutoff Voltage vs. Case Temperature (Typical)



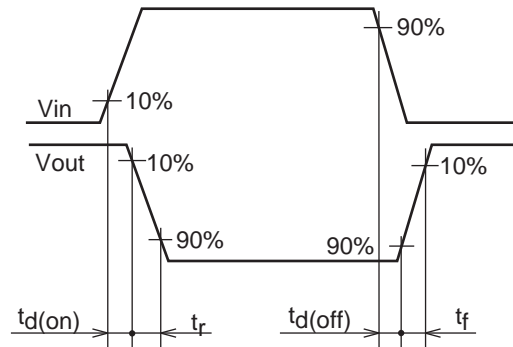
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

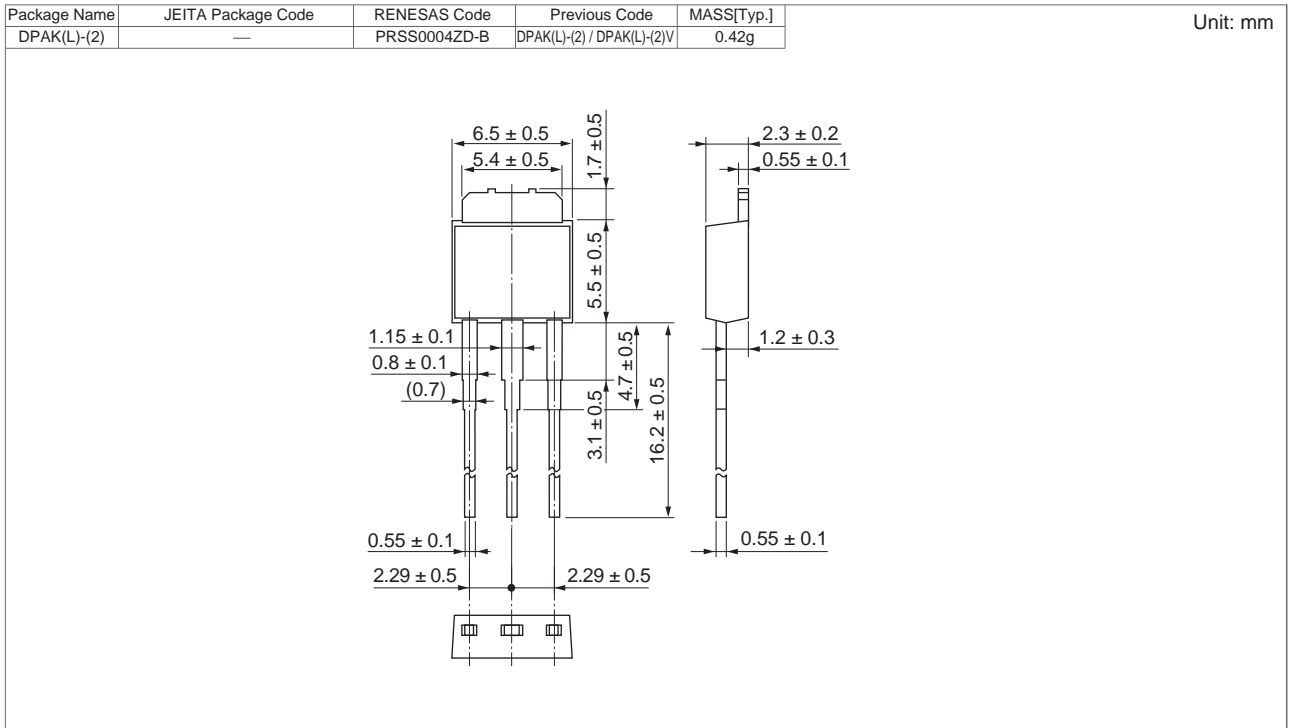


Waveform

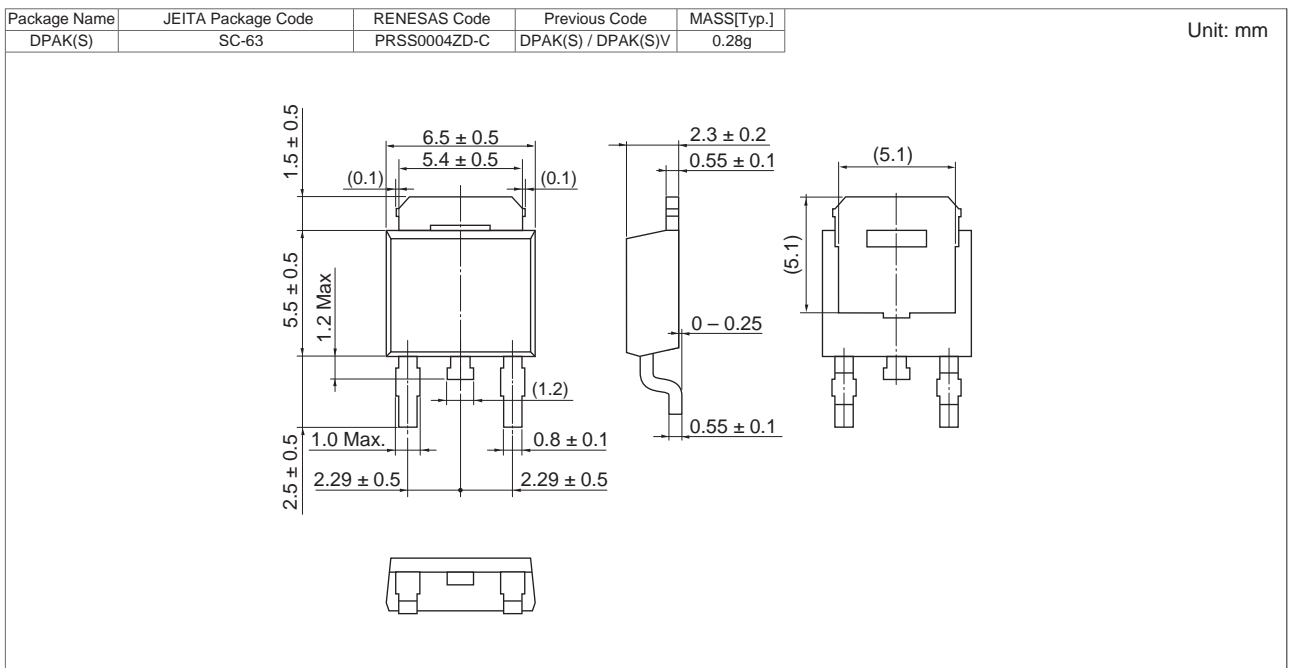


Package Dimensions

• H5N2005DL



• H5N2005DS



Ordering Information

Orderable Part Number	Quantity	Shipping Container
H5N2005DL-E	2160 pcs	Box (Tube)
H5N2005DSTL-E	3000 pcs	Taping

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