PICOR
Semiconductor Power Solutions

Cool-Power®
PI33xx-x0

RoHS

8 V to 36 Vin Cool-Power ZVS Buck Regulator Family

Product Description

The PI33xx-x0 is a family of high efficiency, wide input range DC-DC ZVS-Buck regulators integrating controller, power switches, and support components all within a high density System-in-Package (SiP). The integration of a high performance Zero-Voltage Switching (ZVS) topology, within the PI33xx-x0 series, increases point of load performance providing best in class power efficiency. The PI33xx-x0 requires only an external inductor and minimal capacitors to form a complete DC-DC switching mode Buck Regulator.

Device	Output Voltage		I_{OUT} Max
	Set	Range	
PI3311-x0	1.0 V	1.0 to 1.4 V	10 A
PI3318-x0	1.8 V	1.4 to 2.0 V	10 A
PI3312-x0	2.5 V	2.0 to 3.1 V	10 A
PI3301-x0	3.3 V	2.3 to 4.1 V	10 A
PI3302-x0	5.0 V	3.3 to 6.5 V	10 A
PI3303-x0	12 V	6.5 to 13.0 V	8 A
PI3305-x0	15 V	10.0 to 16.0 V	8 A

The ZVS architecture also enables high frequency operation while minimizing switching losses and maximizing efficiency. The high switching frequency operation reduces the size of the external filtering components, improves power density, and enables very fast dynamic response to line and load transients. The PI33xx-x0 series sustains high switching frequency all the way up to the rated input voltage without sacrificing efficiency and, with its 20 ns minimum on-time, supports large step down conversions up to 36 Vin.

*I²C is a trademark of NXP Semiconductors

Features & Benefits

- High Efficiency ZVS-Buck Topology
- Wide input voltage range of 8 V to 36 V
- Very-Fast transient response
- High accuracy pre-trimmed output voltage
- User adjustable soft-start & tracking
- Power-up into pre-biased load (select versions)
- Parallel capable with single wire current sharing
- Input Over/Undervoltage Lockout (OVLO/UVLO)
- Output Overvoltage Protection (OVP)
- Overtemperature Protection (OTP)
- Fast and slow current limits
- -40°C to 125°C operating range (T_J)
- Optional I²C functionality & programmability:
  - V_{OUT} margining
  - Fault reporting
  - Enable and SYNCI pin polarity
  - Phase delay (interleaving multiple regulators)

Applications

- Rugged, defense applications
- High efficiency systems
- High voltage battery operation

Package Information

- 10 mm x 14 mm x 2.6 mm LGA SiP
- 10.5 mm x 14.5 mm x 2.6 mm BGA SiP

Contents

Order Information

Cool-Power	Output Range		I_{OUT} Max	Package	Transport Media
	Set	Range			
PI3311-00-LGIZ	1.0 V	1.0 to 1.4 V	10 A	10 mm x 14 mm 123-pin LGA	TRAY
PI3318-00-LGIZ	1.8 V	1.4 to 2.0 V	10 A	10 mm x 14 mm 123-pin LGA	TRAY
PI3312-00-LGIZ	2.5 V	2.0 to 3.1 V	10 A	10 mm x 14 mm 123-pin LGA	TRAY
PI3301-00-LGIZ	3.3 V	2.3 to 4.1 V	10 A	10 mm x 14 mm 123-pin LGA	TRAY
PI3302-00-LGIZ	5.0 V	3.3 to 6.5 V	10 A	10 mm x 14 mm 123-pin LGA	TRAY
PI3302-00-BGIZ	5.0 V	3.3 to 6.5 V	10 A	10.5 mm x 14.5 mm BGA	TRAY
PI3303-00-LGIZ	12 V	6.5 to 13.0 V	8 A	10 mm x 14 mm 123-pin LGA	TRAY
PI3305-00-LGIZ	15 V	10.0 to 16.0 V	8 A	10 mm x 14 mm 123-pin LGA	TRAY

I^{2}C Functionality & Programmability

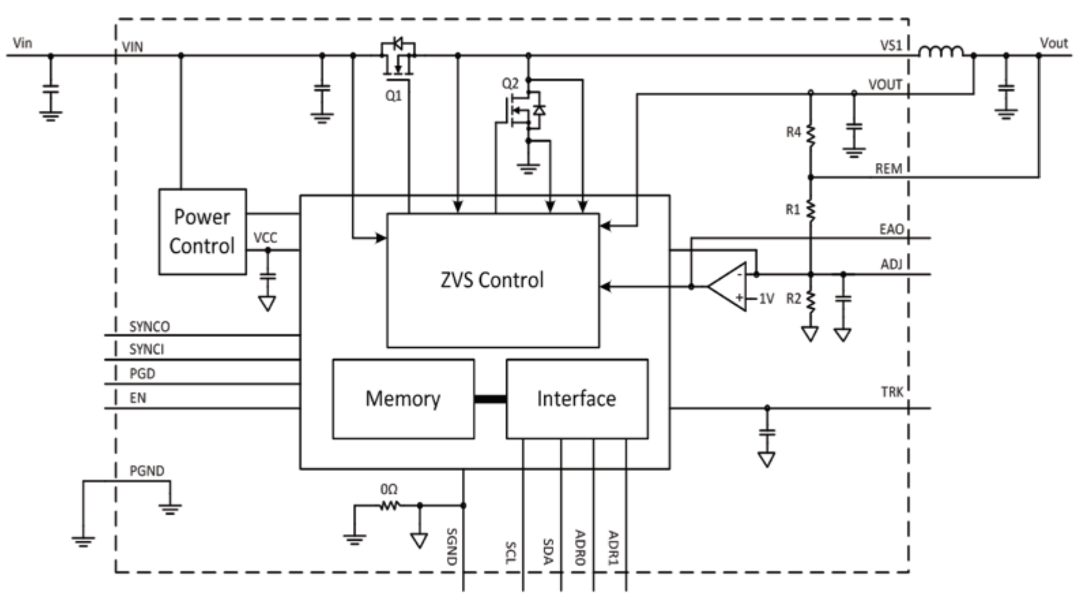
Cool-Power	Output Range		I_{OUT} Max	Package	Transport Media
	Set	Range			
PI3311-20-LGIZ	1.0 V	1.0 to 1.4 V	10 A	10 mm x 14 mm 123-pin LGA	TRAY
PI3318-20-LGIZ	1.8 V	1.4 to 2.0 V	10 A	10 mm x 14 mm 123-pin LGA	TRAY
PI3312-20-LGIZ	2.5 V	2.0 to 3.1 V	10 A	10 mm x 14 mm 123-pin LGA	TRAY
PI3301-20-LGIZ	3.3 V	2.3 to 4.1 V	10 A	10 mm x 14 mm 123-pin LGA	TRAY
PI3302-20-LGIZ	5.0 V	3.3 to 6.5 V	10 A	10 mm x 14 mm 123-pin LGA	TRAY
PI3303-20-LGIZ	12 V	6.5 to 13.0 V	8 A	10 mm x 14 mm 123-pin LGA	TRAY
PI3305-20-LGIZ	15 V	10.0 to 16.0 V	8 A	10 mm x 14 mm 123-pin LGA	TRAY

Absolute Maximum Ratings

Name		Rating
V_{IN}		-0.7 V to 36 V
VS1		-0.7 to 36 V, -4 V for 5 ns
SGND		100 mA
PGD, SYNCO, SYNCI, EN, EAO, ADJ, TRK, ADR1, ADR2, SCL, SDA, REM		-0.3 V to 5.5 V / 5 mA
V_{OUT}	PI3311-x0-LGMZ	-0.3 V to 5.5 V
	PI3318-x0-LGMZ	-0.5 V to 9 V
	PI3312-x0-LGMZ	-0.8 V to 13 V
	PI3301-x0-LGMZ	-1.0 V to 18 V
	PI3302-x0-LGMZ	-1.5 V to 21 V
	PI3303-x0-LGMZ	-3.6 V to 25 V
	PI3305-x0-LGMZ	-4.5 V to 25 V
Storage Temperature		-65°C to 150°C
Operating Junction Temperature		-55°C to 125°C
Soldering Temperature for 20 seconds		245°C
ESD Rating		2 kV HBM

Notes: At 25°C ambient temperature. Stresses beyond these limits may cause permanent damage to the device. Operation at these conditions or conditions beyond those listed in the Electrical Specifications table is not guaranteed. All voltage nodes are referenced to PGND unless otherwise noted. Test conditions are per the specifications within the individual product electrical characteristics.

Functional Block Diagram

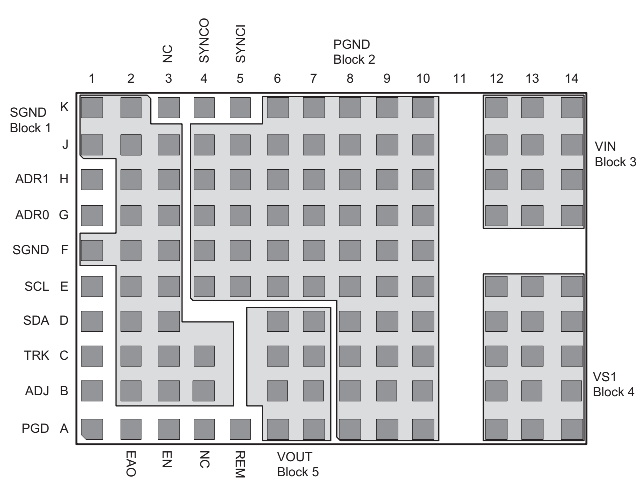


Simpli ed Block Diagram (I^2C pins SCL, SDA, ADR0, and ADR1 only active for PI33xx-20 device versions)

Pin Description

Pin Name	Number	Description
SGND	Block 1	**Signal Ground:** Internal logic ground for EA, TRK, SYNCI, SYNCO, ADJ and I²C (options) communication returns. SGND and PGND are star connected within the regulator package.
PGND	Block 2	**Power Ground:** V_{IN} and V_{OUT} power returns.
V_{IN}	Block 3	**Input Voltage:** and sense for UVLO, OVLO and feed forward ramp.
V_{OUT}	Block 5	**Output Voltage:** and sense for power switches and feed-forward ramp.
VS1	Block 4	**Switching Node**: and ZVS sense for power switches.
PGD	A1	**Parallel Good:** Used for parallel timing management intended for lead regulator.
EAO	A2	**Error Amp Output:** External connection for additional compensation and current sharing.
EN	A3	**Enable Input:** Regulator enable control. Asserted high or left floating – regulator enabled; Asserted low, regulator output disabled. Polarity is programmable via I²C interface.
REM	A5	**Remote Sense:** High side connection. Connect to output regulation point.
ADJ	B1	**Adjust Input:** An external resistor may be connected between ADJ pin and SGND or V_{OUT} to trim the output voltage up or down.
TRK	C1	**Soft-start and Track Input:** An external capacitor may be connected between TRK pin and SGND to decrease the rate of rise during soft-start.
NC	K3, A4	**No Connect:** Leave pins floating.
SYNCO	K4	**Synchronization Output:** Outputs a low signal for ½ of the minimum period for synchronization of other converters.
SYNCI	K5	**Synchronization Input:** Synchronize to the falling edge of external clock frequency. SYNCI is a high impedance digital input node and should always be connected to SGND when not in use.
SDA	D1	**Data Line:** Connect to SGND for PI33xx-00. For use with PI33xx-20 only.
SCL	E1	**Clock Line:** Connect to SGND for PI33xx-00. For use with PI33xx-20 only.
ADR1	H1	**Tri-state Address:** No connect for PI33xx-00. For use with PI33xx-20 only.
ADR0	G1	**Tri-state Address:** No connect for PI33xx-00. For use with PI33xx-20 only.

Package Pin-Out



Block 1: B2-4, C2-4, D2-3, E2-3, F1-3, G2-3, H2-3, J1-3, K1-2

Block 2: A8-10, B8-10, C8-10, D8-10, E4-10, F4-10, G4-10, H4-10, J4-10, K6-10

Block 3: G12-14, H12-14, J12-14, K12-14

Block 4: A12-14, B12-14, C12-14, D12-14, E12-14

Block 5: A6-7, B6-7, C6-7, D6-7

PI3311-x0-LGIZ (1.0 V_{OUT}) Electrical Characteristics

Unless otherwise specified: -55°C < T_J < 125°C, V_{IN} =24 V, L1 = 125 nH [1]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}	Minimum 1 mA load required	8	24	36	V
Input Current	I_{IN_DC}	V_{IN} = 24 V, T_C = 25°C, I_{OUT} =10 A		476		mA
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}	[2]			20	mA
Input Quiescent Current	I_{Q_VIN}	Disabled		2.0		mA
		Enabled (no load)		2.5		mA
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Output Specifications						
Output Voltage Total Regulation	V_{OUT_DC}	[2]	0.987	1.0	1.013	V
Output Voltage Trim Range	V_{OUT_DC}	[3]	1.0		1.4	V
Line Regulation	ΔV_{OUT} (ΔV_{IN})	@25°C, 8 V <V_{IN} <36 V		0.10		%
Load Regulation	ΔV_{OUT} (ΔI_{OUT})	@25°C, 0.5 A <I_{OUT} <10 A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 5 A, C_{OUT} = 8 x 100 µF, 20 MHz BW [4]		20		mVp-p
Continuous Output Current Range	I_{OUT_DC}	[5] Min 1 mA load required			10	A
Current Limit	I_{OUT_CL}			12		A
Protection						
V_{IN} UVLO Start Threshold	V_{UVLO_START}		7.10	7.60	8.00	V
V_{IN} UVLO Stop Threshold	V_{UVLO_STOP}		6.80	7.25	7.60	V
V_{IN} UVLO Hysteresis	V_{UVLO_HYS}			0.33		V
V_{IN} OVLO Start Threshold	V_{OVLO_START}		37.0	38.4		V
V_{IN} OVLO Stop Threshold	V_{OVLO_STOP}		36.1			V
V_{IN} OVLO Hysteresis	V_{OVLO_HYS}			0.77		V
V_{IN} UVLO/OVLO Fault Delay Time	t_{f_DLY}	Number of the switching freq cycles		128		Cycles
V_{IN} UVLO/OVLO Response Time	t_f			500		ns
Output Overvoltage Protection	V_{OVP}	Above V_{OUT}		20		%
Overtemperature Fault Threshold	T_{OTP}		130	135	140	°C
Overtemperature Restart Hysteresis	T_{OTP_HYS}			30		°C

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx-x0 evaluation board with 3x4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

[3] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

[4] Refer to Output Ripple plots.

[5] Refer to Load Current vs. Ambient Temperature curves.

[6] Refer to Switching Frequency vs. Load current curves.

PI3311-x0-LGIZ (1.0 V_{OUT}) Electrical Characteristics

Unless otherwise specified: -55°C < T_J < 125°C, V_{IN} =24 V, L1 = 125 nH [1]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timing						
Switching Frequency	f_S	[6]		500		kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	Relative to set switching frequency [3]	50		110	%
SYNCI Threshold	V_{SYNCI}			2.5		V
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1 mA	4.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1 mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20 pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20 pF load		10		ns
Soft Start And Tracking						
TRK Active Input Range	V_{TRK}	Internal reference tracking range	0		1.04	V
TRK Max Output Voltage				1.2		V
TRK Disable Threshold	V_{TRK_OV}		20	40	60	mV
Charge Current (Soft – Start)	I_{TRK}		-70	-50	-30	µA
Discharge Current (Fault)	I_{TRK_DIS}			6.8		mA
Soft-Start Time	t_{SS}	C_{TRK} = 0 µF		2.2		ms
Enable						
High Threshold	V_{EN_HI}		0.9	1	1.1	V
Low Threshold	V_{EN_LO}		0.7	0.8	0.9	V
Threshold Hysteresis	V_{EN_HYS}		100	200	300	mV
Enable Pull-Up Voltage (floating, unfaulted)	V_{EN_PU}	With positive logic EN polarity		2		V
Enable Pull-Down Voltage (floating, faulted)	V_{EN_PD}	With negative logic EN polarity		0		V
Source Current	I_{EN_SO}	With positive logic EN polarity		-50		µA
Sink Current	I_{EN_SK}	With negative logic EN polarity		50		µA

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx-x0 evaluation board with 3x4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

[3] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

[4] Refer to Output Ripple plots.

[5] Refer to Load Current vs. Ambient Temperature curves.

[6] Refer to Switching Frequency vs. Load current curves.

PI3318-x0-LGIZ (1.8 V_{OUT}) Electrical Characteristics

Unless otherwise specified: -55°C < T_J < 125°C, V_{IN} =24 V, L1 = 155 nH [1]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}	Minimum 1 mA load required	8	24	36	V
Input Current	I_{IN_DC}	V_{IN} = 24 V, T_C = 25°C, I_{OUT} =10 A		835		mA
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}	[2]			20	mA
Input Quiescent Current	I_{Q_VIN}	Disabled		2.0		mA
		Enabled (no load)		2.5		mA
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Output Specifications						
Output Voltage Total Regulation	V_{OUT_DC}	[2]	1.773	1.8	1.827	V
Output Voltage Trim Range	V_{OUT_DC}	[3]	1.4		2.0	V
Line Regulation	ΔV_{OUT} (ΔV_{IN})	@25°C, 8 V <V_{IN} <36 V		0.10		%
Load Regulation	ΔV_{OUT} (ΔI_{OUT})	@25°C, 0.5 A <I_{OUT} <10 A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 5 A, C_{OUT} = 6 x 100 µF, 20 MHz BW [4]		25		mVp-p
Continuous Output Current Range	I_{OUT_DC}	[5]			10	A
Current Limit	I_{OUT_CL}			12		A
Protection						
V_{IN} UVLO Start Threshold	V_{UVLO_START}		7.10	7.60	8.00	V
V_{IN} UVLO Stop Threshold	V_{UVLO_STOP}		6.80	7.25	7.60	V
V_{IN} UVLO Hysteresis	V_{UVLO_HYS}			0.33		V
V_{IN} OVLO Start Threshold	V_{OVLO_START}		37.0	38.4		V
V_{IN} OVLO Stop Threshold	V_{OVLO_STOP}		36.1			V
V_{IN} OVLO Hysteresis	V_{OVLO_HYS}			0.77		V
V_{IN} UVLO/OVLO Fault Delay Time	t_{f_DLY}	Number of the switching freq cycles		128		Cycles
V_{IN} UVLO/OVLO Response Time	t_f			500		ns
Output Overvoltage Protection	V_{OVP}	Above V_{OUT}		20		%
Overtemperature Fault Threshold	T_{OTP}		130	135	140	°C
Overtemperature Restart Hysteresis	T_{OTP_HYS}			30		°C

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx-x0 evaluation board with 3x4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

[3] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

[4] Refer to Output Ripple plots.

[5] Refer to Load Current vs. Ambient Temperature curves.

[6] Refer to Switching Frequency vs. Load current curves.

PI3318-x0-LGIZ (1.8 V_{OUT}) Electrical Characteristics

Unless otherwise specified: -55°C < T_J < 125°C, V_{IN} =24 V, L1 = 155 nH [1]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timing						
Switching Frequency	f_S	[6]		600		kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	Relative to set switching frequency [3]	50		110	%
SYNCI Threshold	V_{SYNCI}			2.5		V
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1 mA	4.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1 mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20 pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20 pF load		10		ns
Soft Start And Tracking						
TRK Active Input Range	V_{TRK}	Internal reference tracking range	0		1.04	V
TRK Max Output Voltage				1.2		V
TRK Disable Threshold	V_{TRK_OV}		20	40	60	mV
Charge Current (Soft – Start)	I_{TRK}		-70	-50	-30	µA
Discharge Current (Fault)	I_{TRK_DIS}			6.8		mA
Soft-Start Time	t_{SS}	C_{TRK} = 0 µF		2.2		ms
Enable						
High Threshold	V_{EN_HI}		0.9	1	1.1	V
Low Threshold	V_{EN_LO}		0.7	0.8	0.9	V
Threshold Hysteresis	V_{EN_HYS}		100	200	300	mV
Enable Pull-Up Voltage (floating, unfaulted)	V_{EN_PU}	With positive logic EN polarity		2		V
Enable Pull-Down Voltage (floating, faulted)	V_{EN_PD}	With negative logic EN polarity		0		V
Source Current	I_{EN_SO}	With positive logic EN polarity		-50		µA
Sink Current	I_{EN_SK}	With negative logic EN polarity		50		µA

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx-x0 evaluation board with 3x4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

[3] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

[4] Refer to Output Ripple plots.

[5] Refer to Load Current vs. Ambient Temperature curves.

[6] Refer to Switching Frequency vs. Load current curves.

PI3318-x0-LGIZ (1.8 V_{OUT}) Electrical Characteristics

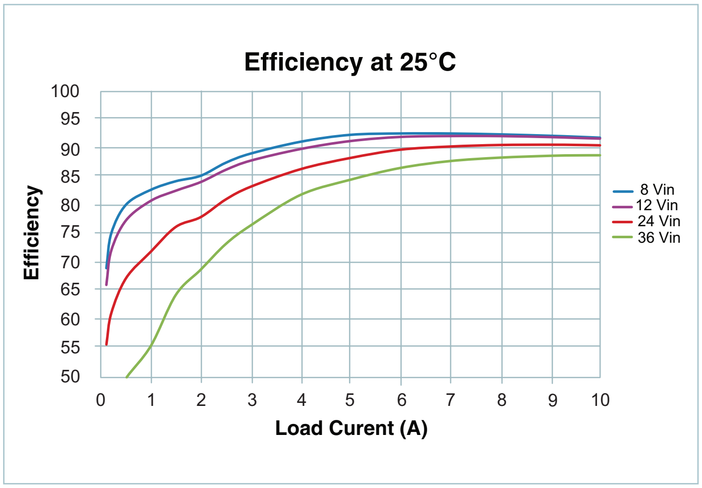


Figure 7 Ef ciency at 25°C

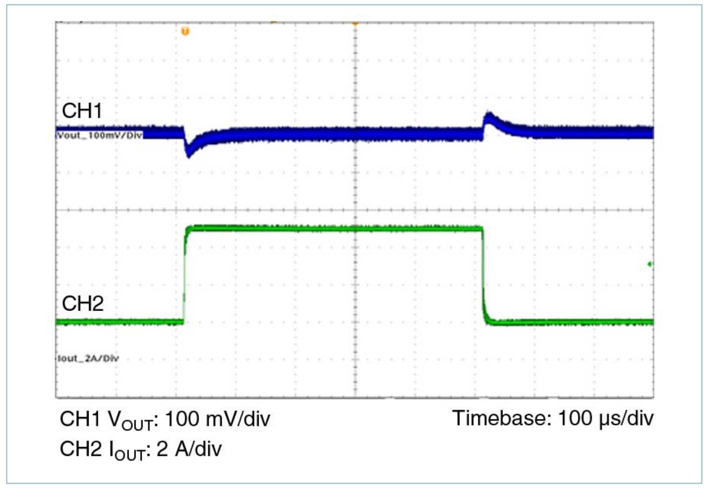


Figure 10 Transient Response 2 A to 7 A, at 5 A/µs

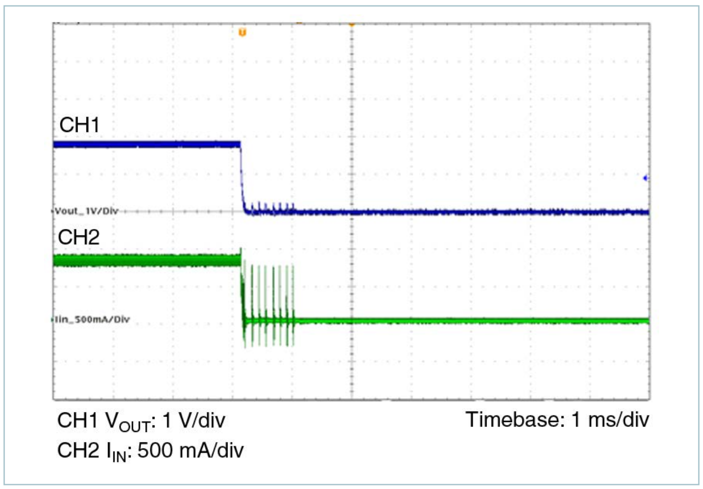


Figure 8 Short Circuit Test

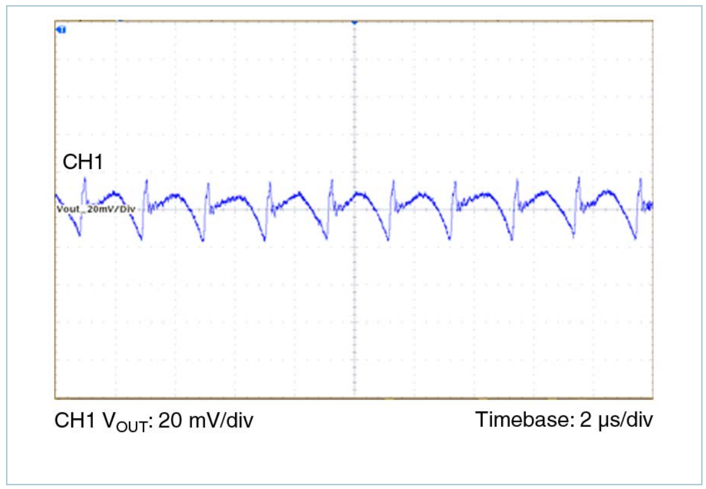


Figure 11 Output Ripple 24 V_{IN}, 1.8 V_{OUT} at 10 A

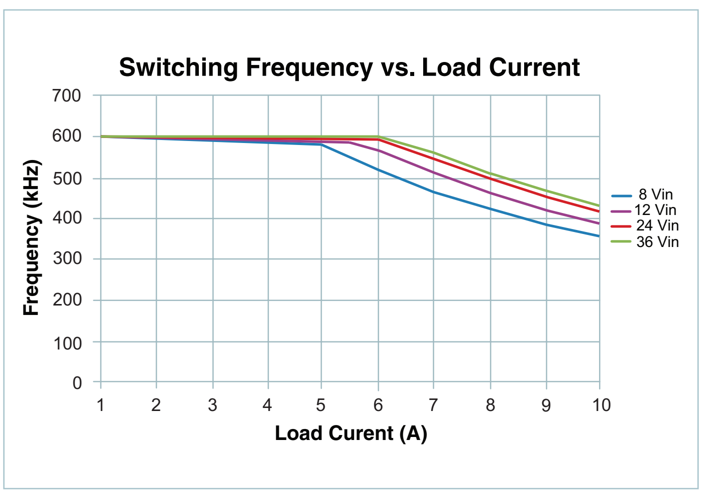


Figure 9 Switching Frequency vs. Load Current

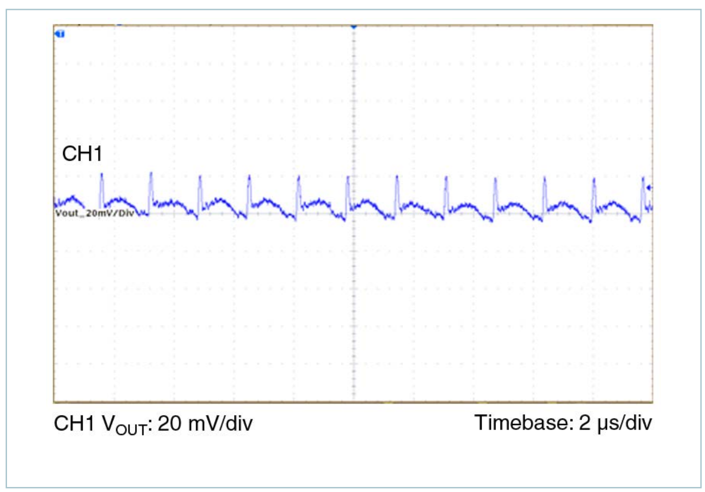


Figure 12 Output Ripple 24 V_{IN}, 1.8 V_{OUT} at 5 A

PI3312-x0-LGIZ (2.5 V_{OUT}) Electrical Characteristics

Unless otherwise specified: -55°C < T_J < 125°C, V_{IN} =24 V, L1 = 200 nH [1]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timing						
Switching Frequency	f_S	[6]		500		kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	Relative to set switching frequency [3]	50		110	%
SYNCI Threshold	V_{SYNCI}			2.5		V
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1 mA	4.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1 mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20 pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20 pF load		10		ns
Soft Start And Tracking						
TRK Active Input Range	V_{TRK}	Internal reference tracking range	0		1.04	V
TRK Max Output Voltage				1.2		V
TRK Disable Threshold	V_{TRK_OV}		20	40	60	mV
Charge Current (Soft – Start)	I_{TRK}		-70	-50	-30	µA
Discharge Current (Fault)	I_{TRK_DIS}			6.8		mA
Soft-Start Time	t_{SS}	C_{TRK} = 0 µF		2.2		ms
Enable						
High Threshold	V_{EN_HI}		0.9	1	1.1	V
Low Threshold	V_{EN_LO}		0.7	0.8	0.9	V
Threshold Hysteresis	V_{EN_HYS}		100	200	300	mV
Enable Pull-Up Voltage (floating, unfaulted)	V_{EN_PU}	With positive logic EN polarity		2		V
Enable Pull-Down Voltage (floating, faulted)	V_{EN_PD}	With negative logic EN polarity		0		V
Source Current	I_{EN_SO}	With positive logic EN polarity		-50		µA
Sink Current	I_{EN_SK}	With negative logic EN polarity		50		µA

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx-x0 evaluation board with 3x4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

[3] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

[4] Refer to Output Ripple plots.

[5] Refer to Load Current vs. Ambient Temperature curves.

[6] Refer to Switching Frequency vs. Load current curves.

[7] Minimum 5 V between V_{IN}-V_{OUT} must be maintained or a minimum load of 1mA required.

PI3312-x0-LGIZ (2.5 V_{OUT}) Electrical Characteristics

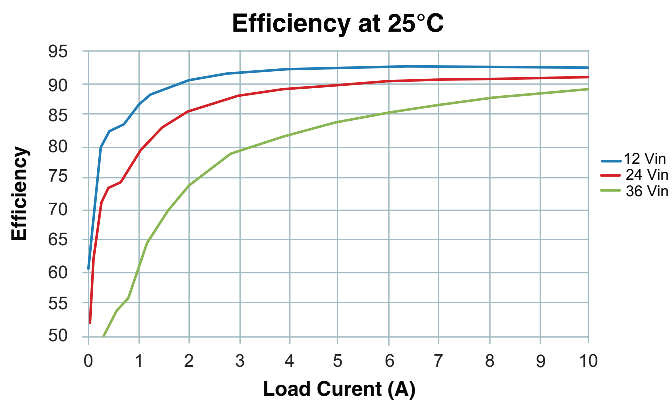
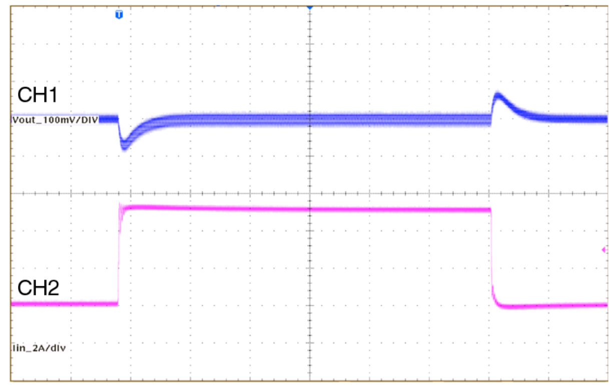
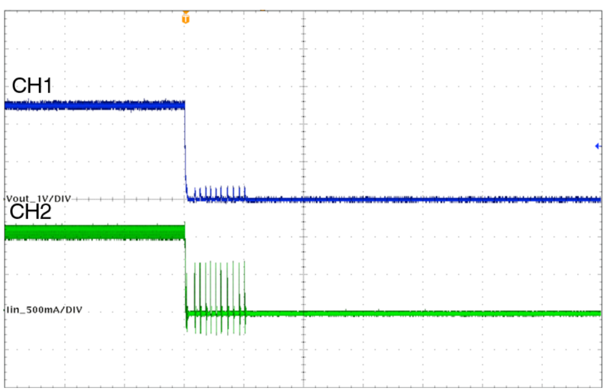


Figure 13 Ef ciency at 25°C



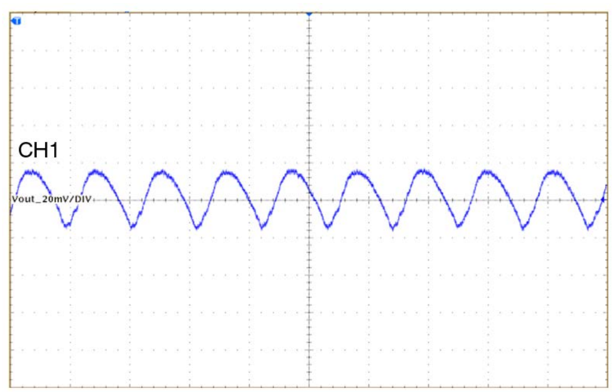
CH1 V_{OUT}: 100 mV/div Timebase: 80 µs/div
CH2 I_{IN}: 2 A/div

Figure 16 Transient Response 5 A to 10 A, at 5 A/µs



CH1 V_{OUT}: 1 V/div Timebase: 1 ms/div
CH2 I_{IN}: 500 mA/div

Figure 14 Short Circuit Test



CH1 V_{OUT}: 20 mV/div Timebase: 2 µs/div

Figure 17 Output Ripple 24 V_{IN}, 2.5 V_{OUT} at 10 A

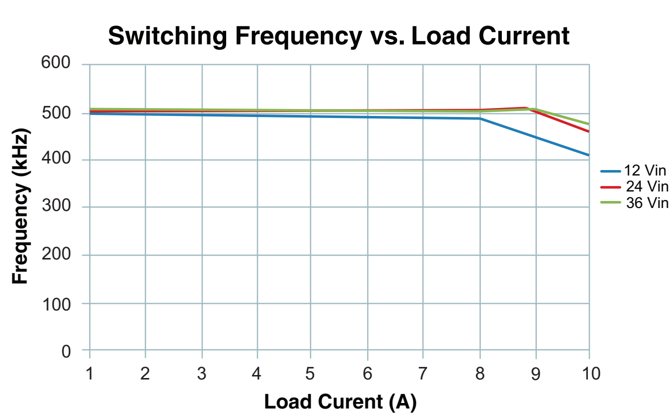
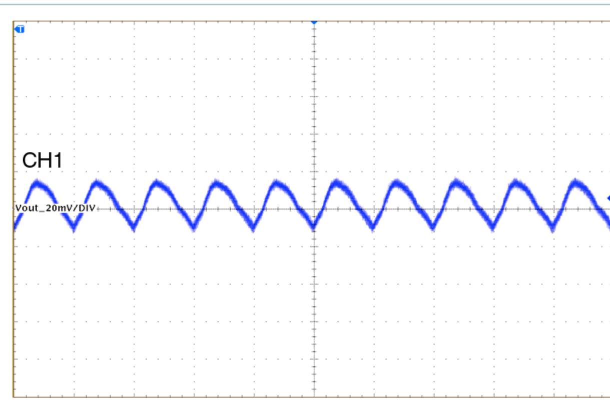


Figure 15 Switching Frequency vs. Load Current



CH1 V_{OUT}: 20 mV/div Timebase: 2 µs/div

Figure 18 Output Ripple 24 V_{IN}, 2.5 V_{OUT} at 5 A

PI3312-x0-LGIZ (2.5 V_{OUT}) Electrical Characteristics

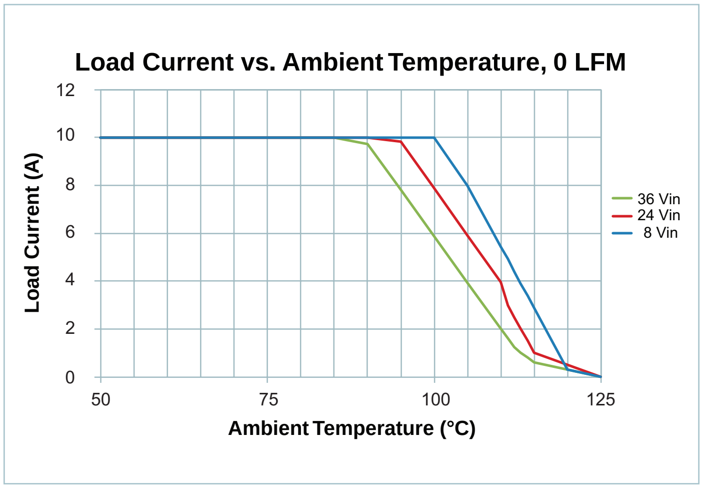


Figure 19 Load Current vs. Ambient Temperature, 0 LFM

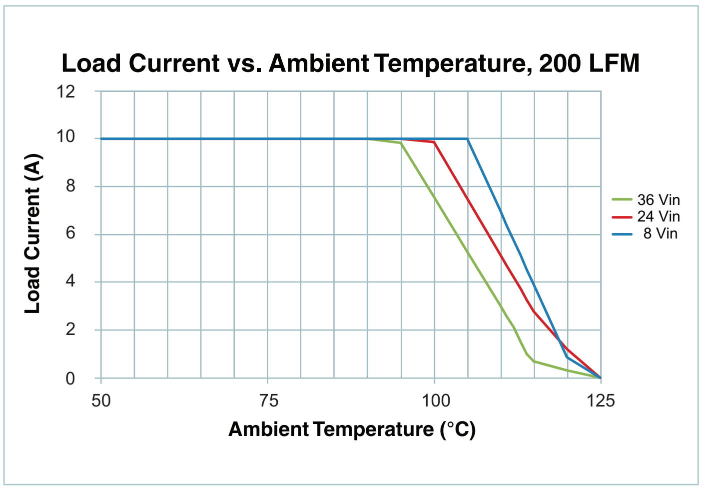


Figure 20 Load Current vs. Ambient Temperature, 400 LFM

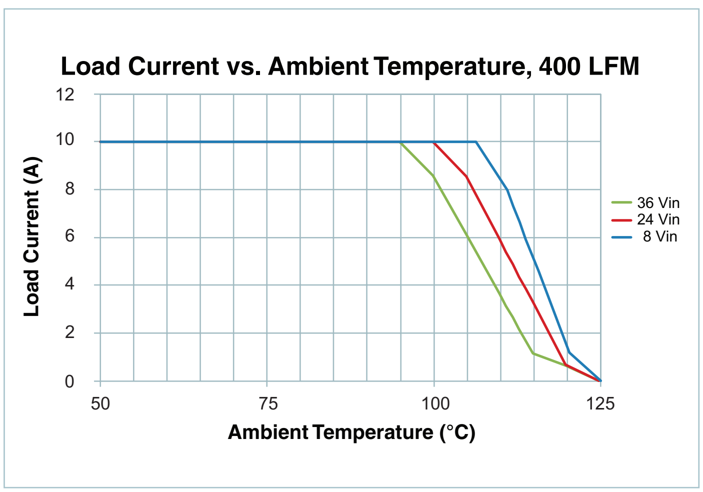


Figure 21 Load Current vs. Ambient Temperature, 200 LFM

PI3301-x0-LGIZ (3.3 V_{OUT}) Electrical Characteristics

Unless otherwise specified: -55°C < T_J < 125°C, V_{IN} =24 V, L1 = 200 nH [1]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}	[7]	8	24	36	V
Input Current	I_{IN_DC}	V_{IN} = 24 V, T_C = 25°C, I_{OUT} =10 A		1.49		A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}	[2]			20	mA
Input Quiescent Current	I_{Q_VIN}	Disabled		2.0		mA
		Enabled (no load)		2.5		mA
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Output Specifications						
Output Voltage Total Regulation	V_{OUT_DC}	[2]	3.25	3.30	3.36	V
Output Voltage Trim Range	V_{OUT_DC}	[3] [7]	2.3	3.3	4.1	V
Line Regulation	ΔV_{OUT} (ΔV_{IN})	@25°C, 8 V <V_{IN} <36 V		0.10		%
Load Regulation	ΔV_{OUT} (ΔI_{OUT})	@25°C, 0.5 A <I_{OUT} <10 A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 5 A, C_{OUT} = 4 x 100 µF, 20 MHz BW [4]		37.5		mVp-p
Continuous Output Current Range	I_{OUT_DC}				10	A
Current Limit	I_{OUT_CL}			12		A
Protection						
V_{IN} UVLO Start Threshold	V_{UVLO_START}		7.10	7.60	8.00	V
V_{IN} UVLO Stop Threshold	V_{UVLO_STOP}		6.80	7.25	7.60	V
V_{IN} UVLO Hysteresis	V_{UVLO_HYS}			0.33		V
V_{IN} OVLO Start Threshold	V_{OVLO_START}		37.0	38.4		V
V_{IN} OVLO Stop Threshold	V_{OVLO_STOP}		36.1			V
V_{IN} OVLO Hysteresis	V_{OVLO_HYS}			0.77		V
V_{IN} UVLO/OVLO Fault Delay Time	t_{f_DLY}	Number of the switching freq cycles		128		Cycles
V_{IN} UVLO/OVLO Response Time	t_f			500		ns
Output Overvoltage Protection	V_{OVP}	Above V_{OUT}		20		%
Overtemperature Fault Threshold	T_{OTP}		130	135	140	°C
Overtemperature Restart Hysteresis	T_{OTP_HYS}			30		°C

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx-x0 evaluation board with 3x4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

[3] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

[4] Refer to Output Ripple plots.

[5] Refer to Load Current vs. Ambient Temperature curves.

[6] Refer to Switching Frequency vs. Load current curves.

[7] Minimum 5 V between V_{IN}-V_{OUT} must be maintained or a minimum load of 1mA required.

PI3301-x0-LGIZ (3.3 V_{OUT}) Electrical Characteristics

Unless otherwise specified: -55°C < T_J < 125°C, V_{IN} =24 V, L1 = 200 nH [1]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timing						
Switching Frequency	f_S	[6]		650		kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	Relative to set switching frequency [3]	50		110	%
SYNCI Threshold	V_{SYNCI}			2.5		V
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1 mA	4.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1 mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20 pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20 pF load		10		ns
Soft Start And Tracking						
TRK Active Input Range	V_{TRK}	Internal reference tracking range	0		1.04	V
TRK Max Output Voltage				1.2		V
TRK Disable Threshold	V_{TRK_OV}		20	40	60	mV
Charge Current (Soft – Start)	I_{TRK}		-70	-50	-30	µA
Discharge Current (Fault)	I_{TRK_DIS}			6.8		mA
Soft-Start Time	t_{SS}	C_{TRK} = 0 µF		2.2		ms
Enable						
High Threshold	V_{EN_HI}		0.9	1	1.1	V
Low Threshold	V_{EN_LO}		0.7	0.8	0.9	V
Threshold Hysteresis	V_{EN_HYS}		100	200	300	mV
Enable Pull-Up Voltage (floating, unfaulted)	V_{EN_PU}	With positive logic EN polarity		2		V
Enable Pull-Down Voltage (floating, faulted)	V_{EN_PD}	With negative logic EN polarity		0		V
Source Current	I_{EN_SO}	With positive logic EN polarity		-50		µA
Sink Current	I_{EN_SK}	With negative logic EN polarity		50		µA

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx-x0 evaluation board with 3x4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

[3] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

[4] Refer to Output Ripple plots.

[5] Refer to Load Current vs. Ambient Temperature curves.

[6] Refer to Switching Frequency vs. Load current curves.

[7] Minimum 5 V between V_{IN}-V_{OUT} must be maintained or a minimum load of 1mA required.

PI3301-x0-LGIZ (3.3 V_{OUT}) Electrical Characteristics

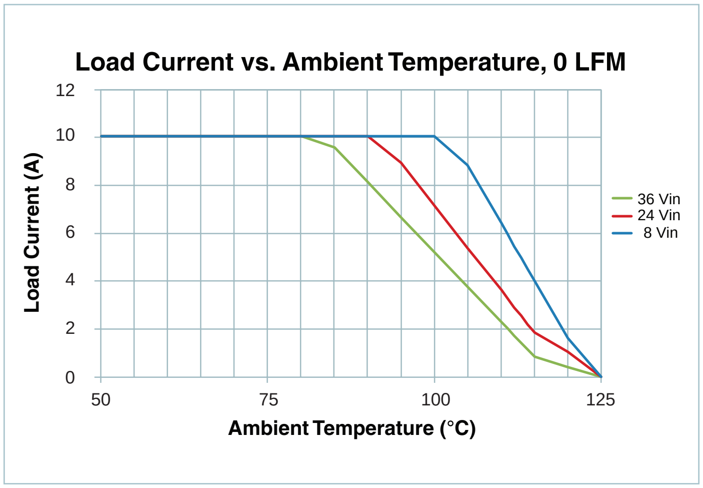


Figure 28 Load Current vs. Ambient Temperature, 0 LFM

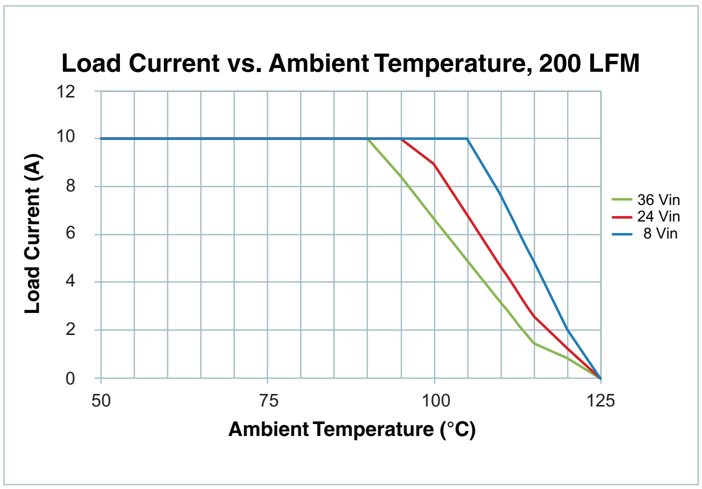


Figure 29 Load Current vs. Ambient Temperature, 400 LFM

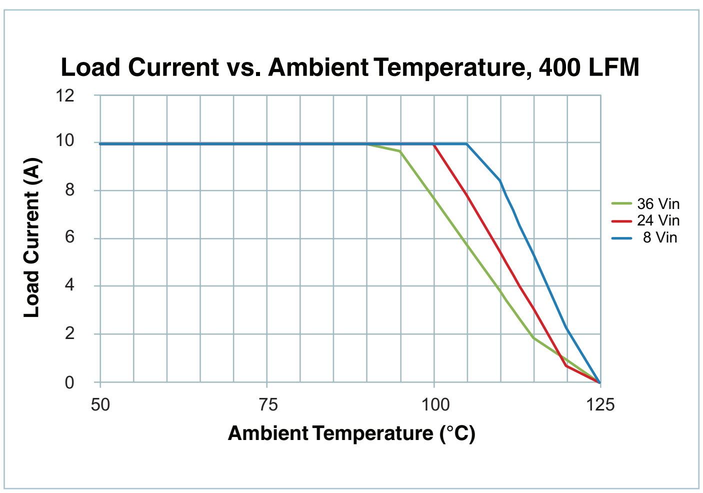


Figure 30 Load Current vs. Ambient Temperature, 200 LFM

PI3302-x0-LGIZ, PI3302-00-BGIZ (5.0 V_{OUT}) Electrical Characteristics

Unless otherwise specified: -55°C < T_J < 125°C, V_{IN} =24 V, L1 = 200 nH [1]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}	[7]	8	24	36	V
Input Current	I_{IN_DC}	V_{IN} = 24 V, T_C = 25°C, I_{OUT} =10 A		2.23		A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}	[2]			20	mA
Input Quiescent Current	I_{Q_VIN}	Disabled		2.0		mA
		Enabled (no load)		2.5		mA
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Output Specifications						
Output Voltage Total Regulation	V_{OUT_DC}	[2]	4.93	5.00	5.07	V
Output Voltage Trim Range	V_{OUT_DC}	[3] [7]	3.3		6.5	V
Line Regulation	ΔV_{OUT} (ΔV_{IN})	@25°C, 8 V <V_{IN} <36 V		0.10		%
Load Regulation	ΔV_{OUT} (ΔI_{OUT})	@25°C, 0.5 A <I_{OUT} <10 A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 5 A, C_{OUT} = 4 x 47 µF, 20 MHz BW [4]		30		mVp-p
Continuous Output Current Range	I_{OUT_DC}	[5] [7]			10	A
Current Limit	I_{OUT_CL}			12		A
Protection						
V_{IN} UVLO Start Threshold	V_{UVLO_START}		7.10	7.60	8.00	V
V_{IN} UVLO Stop Threshold	V_{UVLO_STOP}		6.80	7.25	7.60	V
V_{IN} UVLO Hysteresis	V_{UVLO_HYS}			0.33		V
V_{IN} OVLO Start Threshold	V_{OVLO_START}		37.0	38.4		V
V_{IN} OVLO Stop Threshold	V_{OVLO_STOP}		36.1			V
V_{IN} OVLO Hysteresis	V_{OVLO_HYS}			0.77		V
V_{IN} UVLO/OVLO Fault Delay Time	t_{f_DLY}	Number of the switching freq cycles		128		Cycles
V_{IN} UVLO/OVLO Response Time	t_f			500		ns
Output Overvoltage Protection	V_{OVP}	Above V_{OUT}		20		%
Overtemperature Fault Threshold	T_{OTP}		130	135	140	°C
Overtemperature Restart Hysteresis	T_{OTP_HYS}			30		°C

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx-x0 evaluation board with 3x4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

[3] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

[4] Refer to Output Ripple plots.

[5] Refer to Load Current vs. Ambient Temperature curves.

[6] Refer to Switching Frequency vs. Load current curves.

[7] Minimum 5 V between V_{IN}-V_{OUT} must be maintained or a minimum load of 1mA required.

PI3302-x0-LGIZ, PI3302-00-BGIZ (5.0 V_{OUT}) Electrical Characteristics

Unless otherwise specified: -55°C < T_J < 125°C, V_{IN} =24 V, L1 = 200 nH [1]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timing						
Switching Frequency	f_S	[6]		1.0		kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	Relative to set switching frequency [3]	50		110	%
SYNCI Threshold	V_{SYNCI}			2.5		V
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1 mA	4.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1 mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20 pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20 pF load		10		ns
Soft Start And Tracking						
TRK Active Input Range	V_{TRK}		0		1.04	V
TRK Max Output Voltage				1.2		V
TRK Disable Threshold	V_{TRK_OV}		20	40	60	mV
Charge Current (Soft – Start)	I_{TRK}		-70	-50	-30	µA
Discharge Current (Fault)	I_{TRK_DIS}			6.8		mA
Soft-Start Time	t_{SS}	C_{TRK} = 0 µF		2.2		ms
Enable						
High Threshold	V_{EN_HI}		0.9	1	1.1	V
Low Threshold	V_{EN_LO}		0.7	0.8	0.9	V
Threshold Hysteresis	V_{EN_HYS}		100	200	300	mV
Enable Pull-Up Voltage (floating, unfaulted)	V_{EN_PU}	With positive logic EN polarity		2		V
Enable Pull-Down Voltage (floating, faulted)	V_{EN_PD}	With negative logic EN polarity		0		V
Source Current	I_{EN_SO}	With positive logic EN polarity		-50		µA
Sink Current	I_{EN_SK}	With negative logic EN polarity		50		µA

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI33xx-x0 evaluation board with 3x4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.

[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control.

[3] Output current capability may be limited and other performance may vary from electrical characteristics when switching frequency or V_{OUT} is modified.

[4] Refer to Output Ripple plots.

[5] Refer to Load Current vs. Ambient Temperature curves.

[6] Refer to Switching Frequency vs. Load current curves.

[7] Minimum 5 V between V_{IN}-V_{OUT} must be maintained or a minimum load of 1mA required.

PI3302-x0-LGIZ, PI3302-00-BGIZ (5.0 V_{OUT}) Electrical Characteristics

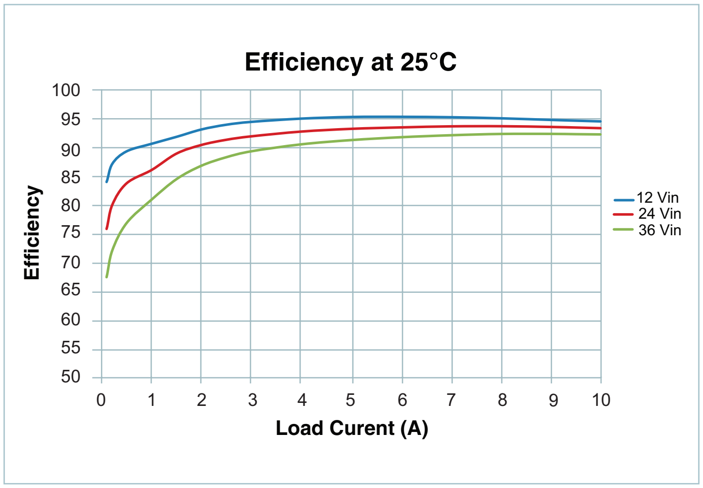


Figure 31 Ef ciency at 25°C

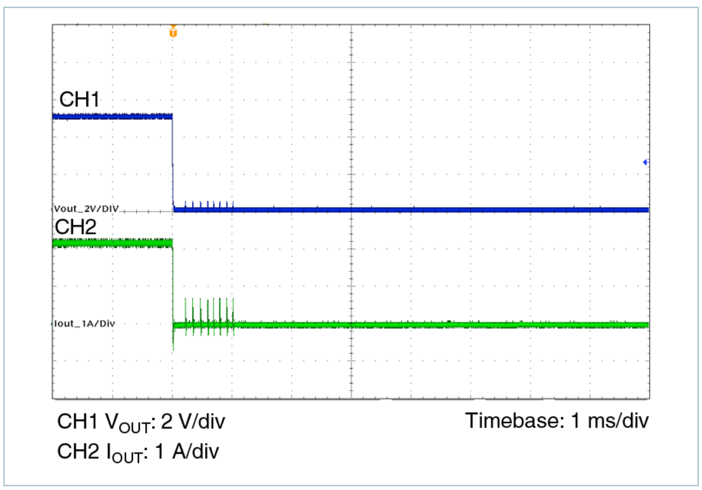


Figure 32 Short Circuit Test

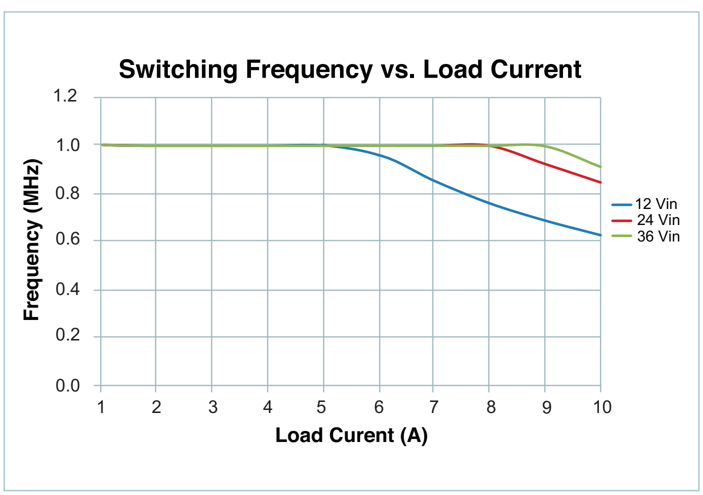


Figure 33 Switching Frequency vs. Load Current

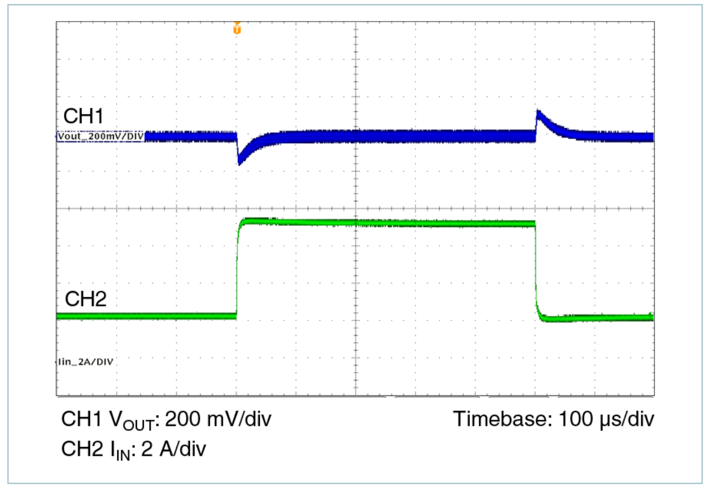


Figure 34 Transient Response 5 A to 10 A, at 5 A/µs

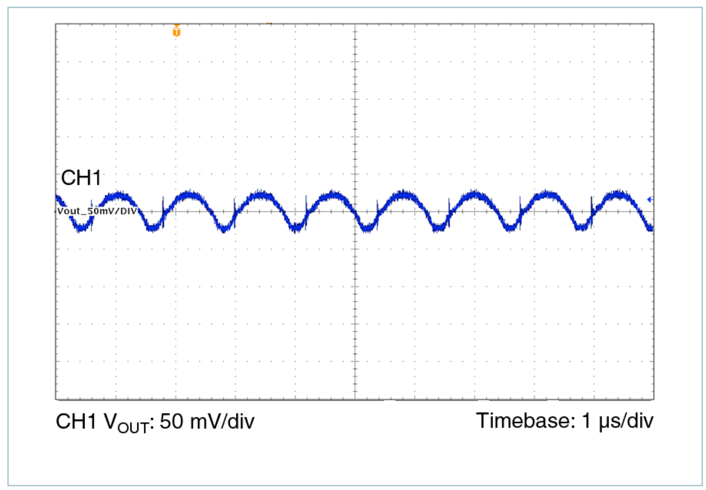


Figure 35 Output Ripple 24 V_{IN}, 5.0 V_{OUT} at 10 A

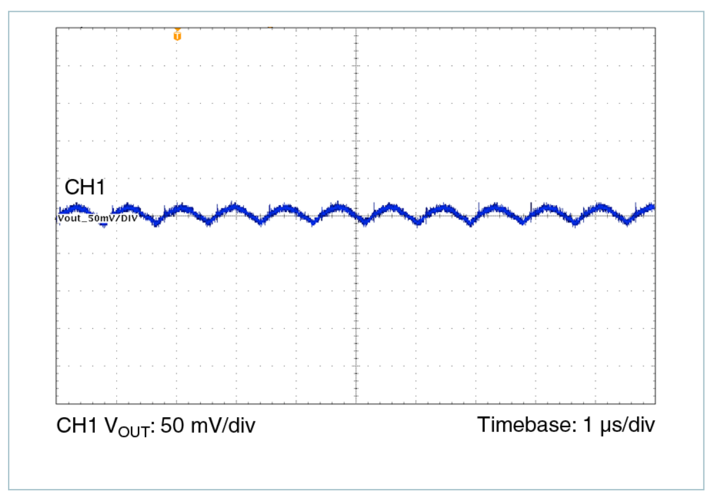


Figure 36 Output Ripple 24 V_{IN}, 5.0 V_{OUT} at 5 A

PI3305-x0-LGIZ (15.0 V_{OUT}) Electrical Characteristics

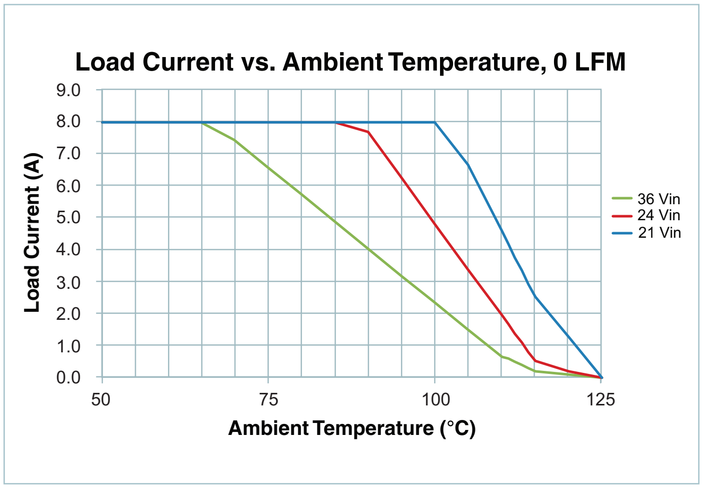


Figure 55 Load Current vs. Ambient Temperature, 0 LFM

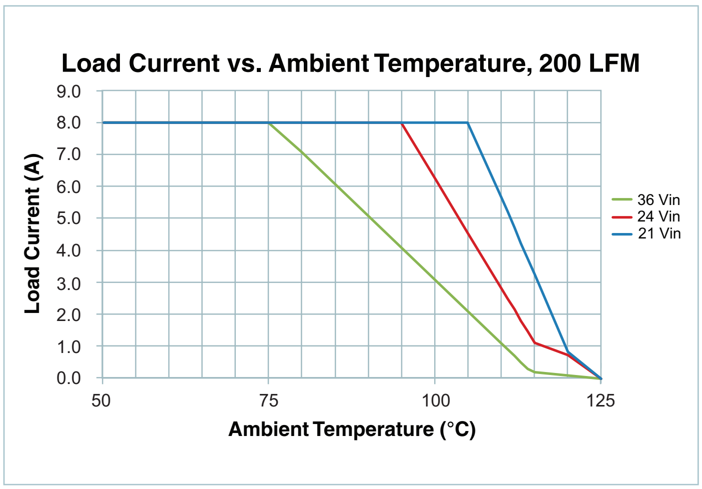


Figure 56 Load Current vs. Ambient Temperature, 400 LFM

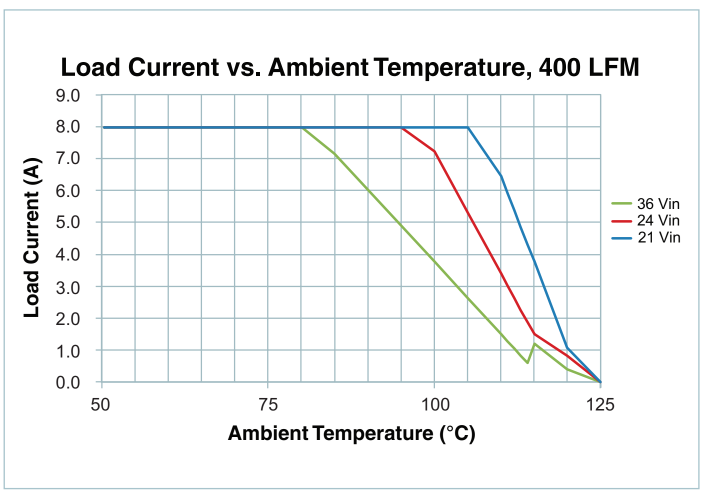


Figure 57 Load Current vs. Ambient Temperature, 200 LFM

Functional Description

The PI33xx-x0 is a family of highly integrated ZVS-Buck regulators. The PI33xx-x0 has a set output voltage that is trimmable within a prescribed range shown in Table 1. Performance and maximum output current are characterized with a specific external power inductor (see Table 4).

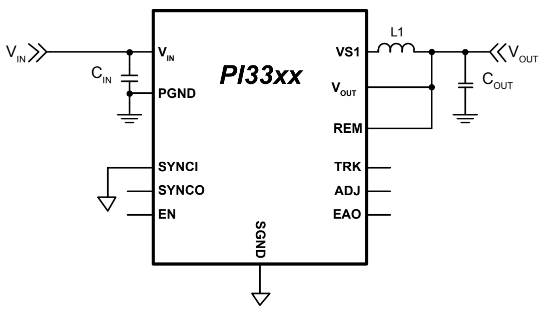


Figure 58 ZVS-Buck with required components

For basic operation, Figure 58 shows the connections and components required. No additional design or settings are required.

ENABLE (EN)

EN is the enable pin of the converter. The EN Pin is referenced to SGND and permits the user to turn the regulator on or off. The EN default polarity is a positive logic assertion. If the EN pin is left floating or asserted high, the converter output is enabled. Pulling EN pin below 0.8 Vdc with respect to SGND will disable the regulator output.

The EN input polarity can be programmed (PI33xx-20 device versions only) via the I^2C data bus. When the EN pin polarity is programmed for negative logic assertion; and if the EN pin is left floating, the regulator output is enabled. Pulling the EN pin above 1.0 Vdc with respect to SGND, will disable the regulator output.

Remote Sensing

An internal 100 Ω resistor is connected between REM pin and V_{OUT} pin to provide regulation when the REM connection is broken. Referring to Figure 58, it is important to note that L1 and C_{OUT} are the output filter and the local sense point for the power supply output. As such, the REM pin should be connected at C_{OUT} as the default local sense connection unless remote sensing to compensate additional distribution losses in the system. The REM pin should not be left floating.

Switching Frequency Synchronization

The SYNCI input allows the user to synchronize the controller switching frequency by an external clock referenced to SGND. The external clock can synchronize the unit between 50% and 110% of the preset switching frequency (fS). For PI33xx-20 device versions only, the phase delay can be programmed via I^2C bus with respect to the clock applied at SYNCI pin. Phase delay allows PI33xx-20 regulators to be paralleled and operate in an interleaving mode.

The PI33xx-x0 default for SYNCI is to sync with respect to the falling edge of the applied clock providing 180° phase shift from SYNCO. This allows for the paralleling of two PI33xx-x0 devices without the need for further user programming or external sync clock circuitry. The user can change the SYNCI polarity to sync with the external clock rising edge via the I^2C data bus (PI33xx-20 device versions only).

When using the internal oscillator, the SYNCO pin provides a 5 V clock that can be used to sync other regulators. Therefore, one PI33xx-x0 can act as the lead regulator and have additional PI33xx-x0s running in parallel and interleaved.

Soft-Start

The PI33xx-x0 includes an internal soft-start capacitor to ramp the output voltage in 2 ms from 0 V to full output voltage. Connecting an external capacitor from the TRK pin to SGND will increase the start-up ramp period. See, "Soft Start Adjustment and Track," in the Applications Description section for more details.

Output Voltage Trim

The PI33xx-x0 output voltage can be trimmed up from the preset output by connecting a resistor from ADJ pin to SGND and can be trimmed down by connecting a resistor from ADJ pin to V_{OUT}. The Table 1 defines the voltage ranges for the PI33xx-x0 family.

Device	Output Voltage	
	Set	Range
PI3311-x0-LGIZ	1.0 V	1.0 to 1.4 V
PI3318-x0-LGIZ	1.8 V	1.4 to 2.0 V
PI3312-x0-LGIZ	2.5 V	2.0 to 3.1 V
PI3301-x0-LGIZ	3.3 V	2.3 to 4.1 V
PI3302-x0-LGIZ	5.0 V	3.3 to 6.5 V
PI3303-x0-LGIZ	12 V	6.5 to 13.0 V
PI3305-x0-LGIZ	15 V	10.0 to 16.0 V

Table 1 PI33xx-x0 family output voltage range

Output Current Limit Protection

PI33xx-x0 has two methods implemented to protect from output short or over current condition.

Slow Current Limit protection: prevents the output load from sourcing current higher than the regulator's maximum rated current. If the output current exceeds the Current Limit (I_{OUT_CL}) for 1024 us, a slow current limit fault is initiated and the regulator is shutdown which eliminates output current flow. After Fault Restart Delay (t_{FR_DLY}), a soft-start cycle is initiated. This restart cycle will be repeated indefinitely until the excessive load is removed.

Fast Current Limit protection: PI33xx-x0 monitors the regulator inductor current pulse-by-pulse to prevent the output from supplying very high current due to sudden low impedance short (50 A Typical). If the regulator senses a high inductor current pulse, it will initiate a fault and stop switching until Fault Restart Delay ends and then initiate a soft-start cycle.

Both the Fast and Slow current limit faults are stored in a Fault Register and can be read and cleared (PI33xx-20 device versions only) via I^2C data bus.

Input Undervoltage Lockout

If V_{IN} falls below the input Undervoltage Lockout (UVLO) threshold, but remains high enough to power the internal bias supply, the PI33xx-x0 will complete the current cycle and stop switching. If V_{IN} recovers within 128 switching cycles, the PI33xx-x0 will resume normal operation. If this time limit is exceeded, the system will enter a low power state and initiate a fault.The system will restart once the input voltage is reestablished and after the Fault Restart Delay. A UVLO fault is stored in a Fault Register and can be read and cleared (PI33xx-20 device versions only) via I^2C data bus.

Input Overvoltage Lockout

If V_{IN} exceeds the input Overvoltage Lockout (OVLO) threshold (VOVLO), while the controller is running, the PI33xx-x0 will complete the current cycle and stop switching. If V_{IN} recovers within 128 switching cycles, the PI33xx-x0 will resume normal operation. Otherwise, the system will enter a low power state and sets an OVLO fault. The system will resume operation when the input voltage falls below 98% of the OVLO threshold and after the Fault Restart Delay. The OVLO fault is stored in a Fault Register and can be read and cleared (PI33xx-20 device versions only) via I^2C data bus.

Output Overvoltage Protection

The PI33xx-x0 family is equipped with output Overvoltage Protection (OVP) to prevent damage to input voltage sensitive devices. If the output voltage exceeds 20% of its set regulated value, the regulator will complete the current cycle, stop switching and issue an OVP fault. The system will resume operation once the output voltage falls below the OVP threshold and after Fault Restart Delay. The OVP fault is stored in a Fault Register and can be read and cleared (PI33xx-20 device versions only) via I^2C data bus.

Overtemperature Protection

The internal package temperature is monitored to prevent internal components from reaching their thermal maximum. If the Over Temperature Protection Threshold (OTP) is exceeded (T_{OTP}), the regulator will complete the current switching cycle, enter a low power mode, set a fault flag, and will soft-start when the internal temperature falls below Overtemperature Restart Hysteresis (T_{OTP_HYS}). The OTP fault is stored in a Fault Register and can be read and cleared (PI33xx-20 device versions only) via I^2C data bus.

Pulse Skip Mode (PSM)

PI33xx-x0 features a PSM to achieve high efficiency at light loads. The regulators are setup to skip pulses if EAO falls below a PSM threshold. Depending on conditions and component values, this may result in single pulses or several consecutive pulses followed by skipped pulses. Skipping cycles significantly reduces gate drive power and improves light load efficiency. The regulator will leave PSM once the EAO rises above the Skip Mode threshold.

Variable Frequency Operation

Each PI33xx-x0 is preprogrammed to a base operating frequency, with respect to the power stage inductor (see Table 4), to operate at peak efficiency across line and load variations. At low line and high load applications, the base frequency will decrease to accommodate these extreme operating ranges. By stretching the frequency, the ZVS operation is preserved throughout the total input line voltage range therefore maintaining optimum efficiency.

Parallel Operation

Paralleling modules can be used to increase the output current capability of a single power rail and reduce output voltage ripple.

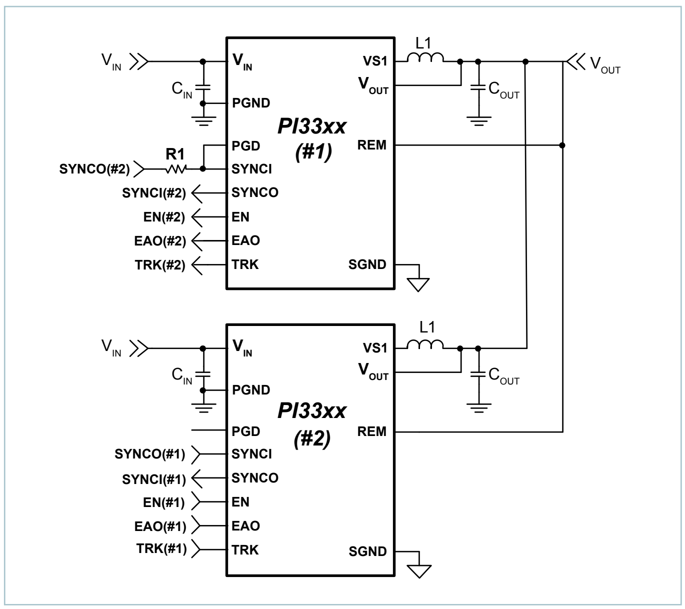


Figure 59 PI33xx-x0 parallel operation

The PI33xx-x0 default for SYNCI is to sync with respect to the falling edge of the applied clock providing 180° phase shift from SYNCO. This allows for the paralleling of two PI33xx-x0 devices without the need for further user programming or external sync clock circuitry. The user can change the SYNCI polarity to sync with the external clock rising edge via the I²C data bus (PI33xx-20 device versions only).

By connecting the EAO pins and SGND pins of each module together the units will share the current equally. When the TRK pins of each unit are connected together, the units will track each other during soft-start and all unit EN pins have to be released to allow the units to start (See Figure 59). Also, any fault event in any regulator will disable the other regulators. The two regulators will be out of phase with each other reducing output ripple (refer to Switching Frequency Synchronization).

To provide synchronization between regulators over the entire operational frequency range, the Parallel Good (PGD) pin must be connected to the lead regulator's (#1) SYNCI pin and a 2.5 kΩ Resistor, R1, must be placed between SYNCO (#2) return and the lead regulator's SYNCI (#1) pin, as shown in Figure 59. In this configuration, at system soft-start, the PGD pin pulls SYNCI low forcing the lead regulator to initialize the open-loop startup synchronization. Once the regulators reach regulation, SYNCI is released and the system is now synchronized in a closed-loop configuration which allows the system to adjust, on the fly, when any of the individual regulators begin to enter variable frequency mode in the loop.

Multi-phasing three regulators is possible (PI33xx-20 only) with no change to the basic single-phase design. For more information about how to program phase delays within the regulator, please refer to Picor application note PI33xx-2x Multi-Phase Design Guide.

I²C Interface Operation

PI33xx-20 devices provide an I²C digital interface that enables the user to program the EN pin polarity (from high to low assertion) and switching frequency synchronization phase/delay. These are one time programmable options to the device.

Also, the PI33xx-20 devices allow for dynamic V_{OUT} margining via I²C that is useful during development (settings stored in volatile memory only and not retained by the device). The PI33xx-20 also have the option for fault telemetry including:

- Fast/Slow current limit
- Output voltage high
- Input overvoltage
- Input undervoltage
- Over temperature protection

For more information about how to utilize the I²C interface please refer to Picor application note PI33xx-2x I²C Digital Interface Guide.

Application Description

Output Voltage Trim

The PI33xx-x0 family of Buck Regulators provides seven common output voltages: 1.0 V, 1.8 V, 2.5 V, 3.3 V, 5.0 V, 12 V and 15 V. A post-package trim step is implemented to offset any resistor divider network errors ensuring maximum output accuracy. With a single resistor connected from the ADJ pin to SGND or REM, each device's output can be varied above or below the nominal set voltage (with the exception of the PI3311-X0 which can only be above the set voltage of 1 V).

Device	Output Voltage	
	Set	Range
PI3311-x0	1.0 V	1.0 to 1.4 V
PI3318-x0	1.8 V	1.4 to 2.0 V
PI3312-x0	2.5 V	2.0 to 3.1 V
PI3301-x0	3.3 V	2.3 to 4.1 V
PI3302-x0	5.0 V	3.3 to 6.5 V
PI3303-x0	12 V	6.5 to 13.0 V
PI3305-x0	15 V	10.0 to 16.0 V

Table 2 PI33xx-x0 family output voltage range

The remote pin (REM) should always be connected to the V_{OUT} pin, if not used, to prevent an output voltage offset. Figure 60 shows the internal feedback voltage divider network.

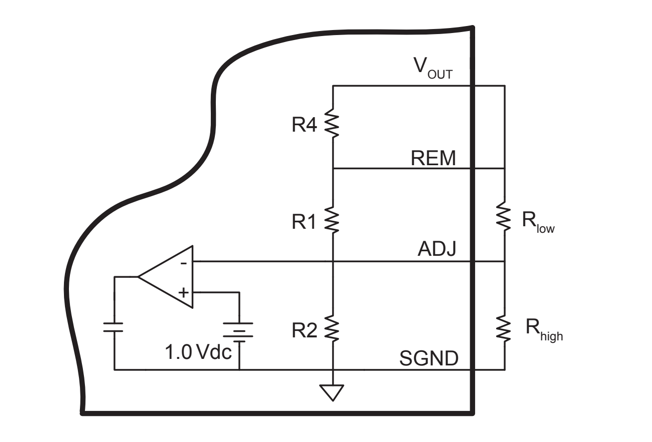


Figure 60 Internal resistor divider network

R1, R2, and R4 are all internal 1.0 % resistors and R_{low} and R_{high} are external resistors for which the designer can add to modify V_{OUT} to a desired output. The internal resistor value for each regulator is listed below in Table 3.

Device	R1	R2	R4
PI3311-x0-LGIZ	1 k	Open	100
PI3318-x0-LGIZ	0.806 k	1.0 k	100
PI3312-x0-LGIZ	1.5 k	1.0 k	100
PI3301-x0-LGIZ	2.61 k	1.13 k	100
PI3302-x0-LGIZ	4.53 k	1.13 k	100
PI3303-x0-LGIZ	11.0 k	1.0 k	100
PI3305-x0-LGIZ	14.0 k	1.0 k	100

Table 3 PI33xx-x0 Internal divider values

By choosing an output voltage value within the ranges stated in Table 2, V_{OUT} can simply be adjusted up or down by selecting the proper R_{high} or R_{low} value, respectively. The following equations can be used to calculate R_{high} and R_{low} values:

$$R_{high} = \frac{1}{\frac{(Vout - 1)}{R1} - \left(\frac{1}{R2}\right)} \qquad (1)$$

$$R_{low} = \frac{1}{\frac{1}{R2(Vout - 1)} - \left(\frac{1}{R1}\right)} \qquad (2)$$

If, for example, a 4.0 V output is needed, the user should choose the regulator with a trim range covering 4.0 V from Table 2. For this example, the PI3301 is selected (3.3 V set voltage). First step would be to use Equation (1) to calculate Rhigh since the required output voltage is higher than the regulator set voltage. The resistor-divider network values for the PI3301 are can be found in Table 3 and are R1 = 2.61 kΩ and R2 = 1.13 kΩ. Inserting these values in to Equation (1), R_{high} is calculated as follows:

$$3.78k = \frac{1}{\frac{(4.0 - 1)}{2.61k} - \left(\frac{1}{1.13k}\right)}$$

Resistor R_high should be connected as shown in Figure 60 to achieve the desired 4.0 V regulator output. No external R_low resistor is need in this design example since the trim is above the regulator set voltage.

The PI3420 output voltage can only be trimmed higher than the factory 1 V setting. The following Equation (3) can be used calculate Rhigh values for the PI3420 regulators.

$$!_{!\ !\ !'}(1V) = \frac{1}{\frac{(Vout - 1)}{11}}\ 111 \qquad (3)$$

Soft-Start Adjust and Tracking

The TRK pin offers a means to increase the regulator's soft-start time or to track with additional regulators. The soft-start slope is controlled by an internal 100 nF and a fixed charge current to provide a minimum startup time of 2 ms (typical) for all PI33xx-x0 regulators. By adding an additional external capacitor to the TRK pin, the soft-start time can be increased further. The following equation can be used to calculate the proper capacitor for a desired soft-start times:

$$C_{TRK} = (t_{TRK}\ x\ I_{TRK}) - 100\ x\ 10^{-9},$$

Where, t_{TRK} is the soft-start time and I_{TRK} is a 50 μA internal charge current (see Electrical Characteristics for limits).

There is typically either proportional or direct tracking implemented within a design. For proportional tracking between several regulators at startup, simply connect all devices TRK pins together. This type of tracking will force all connected regulators to startup and reach regulation at the same time (see Figure 61(a).

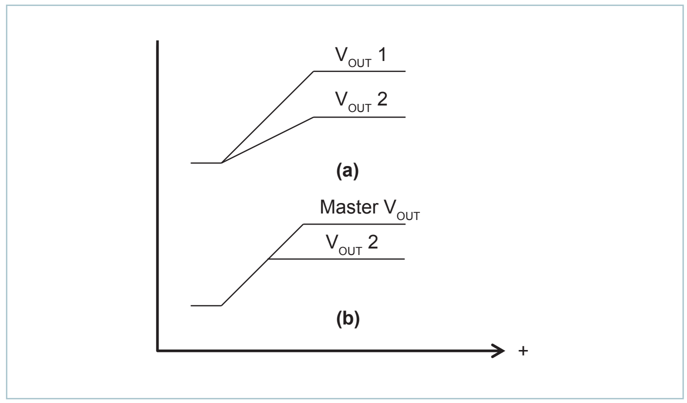


Figure 61 PI33xx-x0 tracking methods

For Direct Tracking, choose the regulator with the highest output voltage as the master and connect the master to the TRK pin of the other regulators through a divider (Figure 62) with the same ratio as the slave's feedback divider (see Table 3 for values).

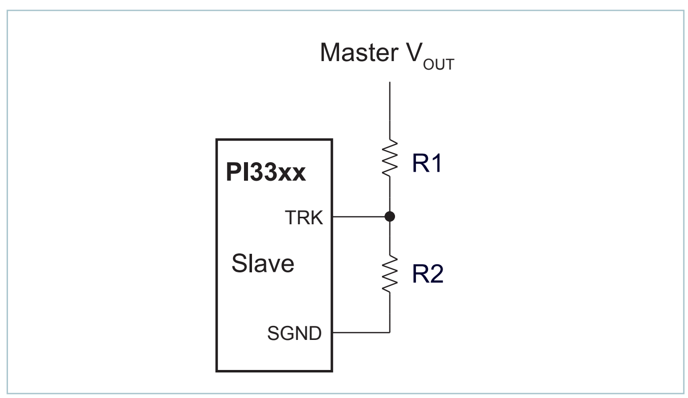


Figure 62 Voltage divider connections for direct tracking

All connected regulators' soft-start slopes will track with this method. Direct tracking timing is demonstrated in Figure 61(b). All tracking regulators should have their Enable (EN) pins connected together to work properly.

Inductor Pairing

The PI33xx-x0 utilizes an external inductor. This inductor has been optimized for maximum efficiency performance. Table 4 details the specific inductor value and part number utilized for each PI33xx-x0 device which are available from Coiltronics and Eaton. Data sheets are available at:

http://www.cooperindustries.com

Device	Inductor [nH]	Inductor Part Number	Manufacturer
PI3311-x0	125	FPV1006-125-R	Eaton
PI3318-x0	150	FPV1006-150-R	Eaton
PI3312-x0	200	FPT705-200-R	Coiltronics
PI3301-x0	200	FPT705-200-R	Coiltronics
PI3302-x0	200	FPT705-200-R	Coiltronics
PI3303-x0	230	FPT705-230-R	Coiltronics
PI3305-x0	230	FPT705-230-R	Coiltronics

Table 4 PI33xx-x0 Inductor pairing

Thermal Derating

Thermal de-rating curves are provided that are based on component temperature changes versus load current, input voltage and air flow. It is recommended to use these curves as a guideline for proper thermal de-rating. These curves represent the entire system and are inclusive to both the Picor regulator and the external inductor. Maximum thermal operation is limited by either the MOSFETs or inductor depending upon line and load conditions.

Thermal measurements were made using a standard PI33xx-x0 Evaluation board which is 3 x 4 inches in area and uses 4-layer, 2 oz copper. Thermal measurements were made on the three main power devices, the two internal MOSFETs and the external inductor, with air flows of 0, 200, and 400 LFM.

Filter Considerations

The PI33xx-x0 requires input bulk storage capacitance as well as low impedance ceramic X5R input capacitors to ensure proper start up and high frequency decoupling for the power stage. The PI33xx-x0 will draw nearly all of the high frequency current from the low impedance ceramic capacitors when the main high side MOSFET is conducting. During the time the high side MOSFET is off, they are replenished from the bulk capacitor. If the input impedance is high at the switching frequency of the converter, the bulk capacitor must supply all of the average current into the converter, including replenishing the ceramic capacitors. This value has been chosen to be 100 µF so that the PI33xx-x0 can start up into a full resistive load and supply the output capacitive load with the default minimum soft start capacitor when the input source impedance is 50 Ohms at 1 MHz. The ESR for this capacitor should be approximately 20 mΩ. The RMS ripple current in this capacitor is small, so it should not be a concern if the input recommended ceramic capacitors are used. Table 5 shows the recommended input and output capacitors to be used for the various models as well as expected transient response, RMS ripple currents per capacitor, and input and output ripple voltages. Table 6 includes the recommended input and output ceramic capacitors.

Device	V_{IN} (V)	I_{LOAD} (A)	C_{INPUT} Ceramic X5R	C_{INPUT} Bulk Elec.	C_{OUTPUT} Ceramic X5R	C_{INPUT} Ripple Current (I_{RMS})	C_{OUTPUT} Ripple Current (I_{RMS})	Input Ripple (mVpp)	Output Ripple (mVpp)	Output Ripple (mVpp)	Recovery Time (µs)	Load Step (A) (Slew/µs)
PI3311	24	10	4 x 4.7 µF 50 V	100 µF 50 V	8 X 100 µF 2 X 1 µF 1 X 0.1 µF	0.5	0.8	120	20	-/+40	40	5 (5 A/µs)
		5						100	15			
PI3318	24	10	4 x 4.7 µF 50 V	100 µF 50 V	6 X 100 µF 2 X 1 µF 1 X 0.1 µF	0.5	0.8	120	20	-/+40	40	5 (5 A/µs)
		5						100	15			
PI3312	24	10	4 x 4.7 µF	100 µF 50 V	4 X 100 µF 2 X 1 µF 1 X 0.1 µF	1	1.75	150	50	-/+80	25	5 (10 A/µs)
		5						100	24			
PI3301	24	10	4 x 4.7 µF	100 µF 50 V	4 X 100 µF 2 X 1 µF 1 X 0.1 µF	1.05	1.625	200	40	-/+100	20	5 (1 0A/µs)
		5						125	33			
PI3302	24	10	4 x 4.7 µF	100 µF 50 V	4 X 47 µF 2 X 1 µF 1 X 0.1 µF	1.2	1.5	220	50	-/+170	30	5 (5 A/µs)
		5						140	30			
PI3303	24	8	4 x 4.7 µF	100 µF 50 V	4 X 22 µF 2 X 1 µF 1 X 0.1 µF	1.3	1.36	275	100	-/+300	30	4 (10 A/µs)
		4						150	60			
PI3305	24	8	4 x 4.7 µF	100 µF 50 V	4 X 22 µF 2 X 1 µF 1 X 0.1 µF	1.38	1.2	280	150	-/+400	30	4 (10 A/µs)
		4						160	75			

Table 5 Recommended input and output capacitance

Murata Part Number	Description
GRM188R71C105KA12D	1µF 16 V 0603 X7R
GRM319R71H104KA01D	0.1µF 50 V 1206 X7R
GRM31CR60J107ME39L	100 µF 6.3 V 1206 X5R
GRM31CR71H475KA12K	4.7 µF 50 V 1206 X7R
GRM31CR61A476ME15L	47 µF 10 V 1206 X5R
GRM31CR61E226KE15L	22 µF 25 V 1206 X5R

Table 6 Capacitor manufacturer part numbers

Layout Guidelines

To optimize maximum efficiency and low noise performance from a PI33xx-x0 design, layout considerations are necessary. Reducing trace resistance and minimizing high current loop returns along with proper component placement will contribute to optimized performance.

A typical buck converter circuit is shown in Figure 63. The potential areas of high parasitic inductance and resistance are the circuit return paths, shown as LR below.

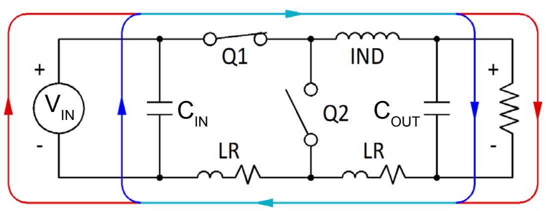


Figure 63 Typical Buck Converter

The path between the C_{OUT} and C_{IN} capacitors is of particular importance since the AC currents are flowing through both of them when Q1 is turned on.

Figure 64, schematically, shows the reduced trace length between input and output capacitors. The shorter path lessens the effects that copper trace parasitics can have on the PI33xx-x0 performance.

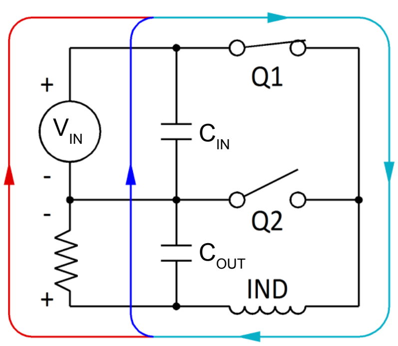


Figure 64 Current ow: Q1 closed

When Q1 is on and Q2 is off, the majority of $C_{IN's}$ current is used to satisfy the output load and to recharge the C_{OUT} capacitors. When Q1 is off and Q2 is on, the load current is supplied by the inductor and the C_{OUT} capacitor as shown in Figure 65. During this period C_{IN} is also being recharged by the V_{IN}. Minimizing C_{IN} loop inductance is important to reduce peak voltage excursions when Q1 turns off. Also, the difference in area between the C_{IN} loop and C_{OUT} loop is vital to minimize switching and GND noise.

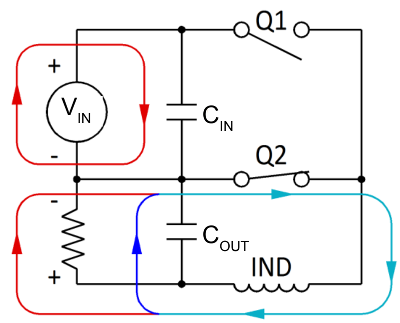


Figure 65 Current ow: Q2 closed

The recommended component placement, shown in Figure 66, illustrates the tight path between C_{IN} and C_{OUT} (and V_{IN} and V_{OUT}) for the high AC return current. This optimized layout is used on the PI33xx-x0 evaluation board.

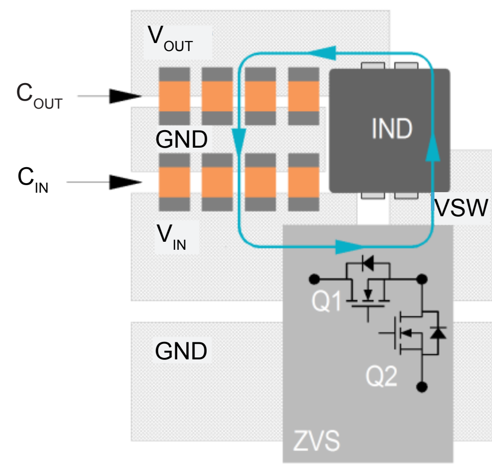


Figure 66 Recommended component placement and metal routing

Figure 67 details the recommended receiving footprint for PI33xx-x0 10 mm x 14 mm package. All pads should have a final copper size of 0.55 mm x 0.55 mm, whether they are solder-mask defined or copper defined, on a 1 mm x 1 mm grid. All stencil openings are 0.45mm when using either a 5 mil or 6 mil stencil.

Recommended PCB Footprint and Stencil

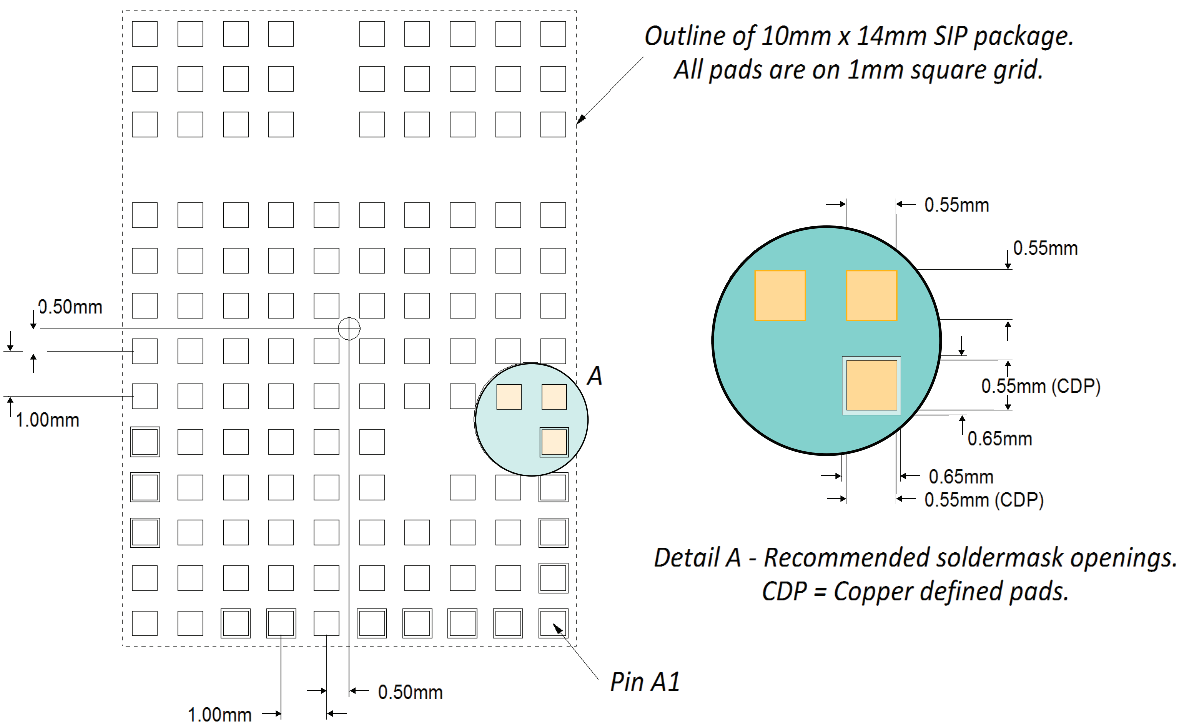
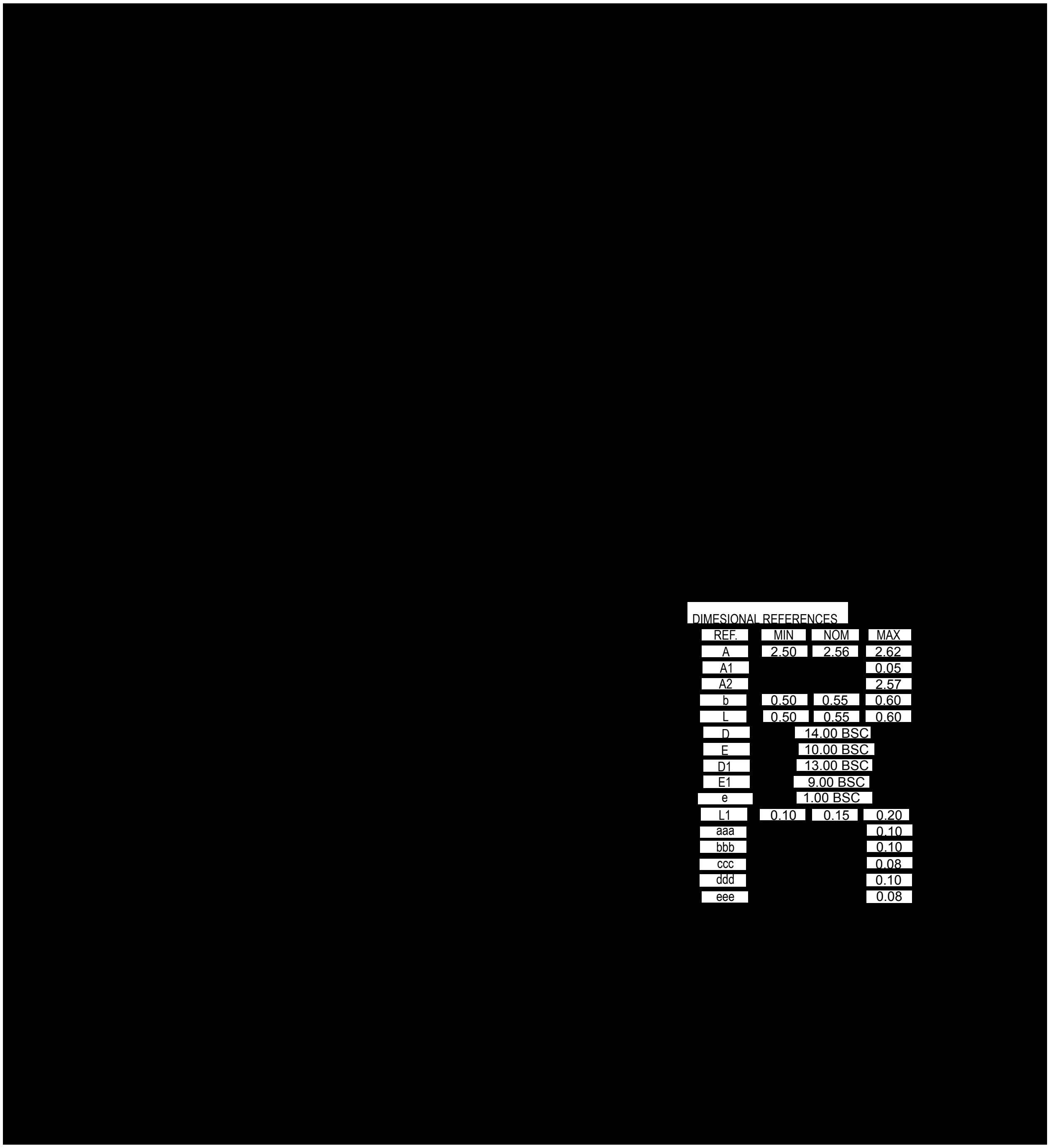


Figure 67 Recommended Receiving PCB footprint

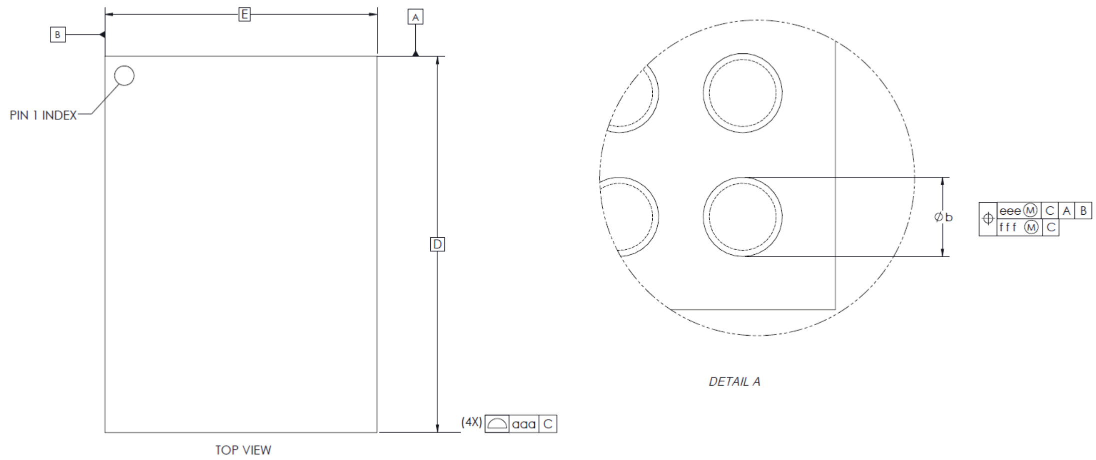
LGIZ Package Drawing

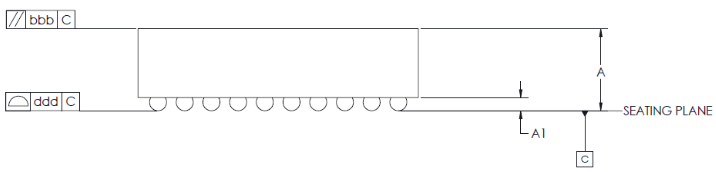


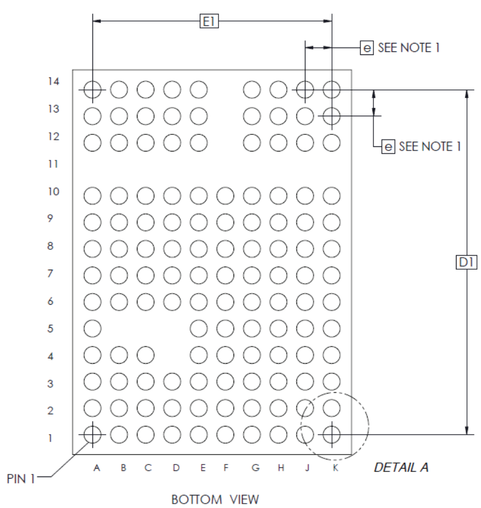
DIMESIONAL REFERENCES

REF.	MIN	NOM	MAX
A	2.50	2.56	2.62
A1			0.05
A2			2.57
b	0.50	0.55	0.60
L	0.50	0.55	0.60
D		14.00 BSC	
E		10.00 BSC	
D1		13.00 BSC	
E1		9.00 BSC	
e		1.00 BSC	
L1	0.10	0.15	0.20
aaa			0.10
bbb			0.10
ccc			0.08
ddd			0.10
eee			0.08

BGIZ Package Drawing







DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	2.96	3.05	3.14
A1	0.44	0.49	0.54
b	0.59	0.64	0.69
D	14.40	14.50	14.60
E	10.40	10.50	10.60
D1	13.00 BSC		
E1	9.00 BSC		
e	1.00 BSC		

DIMENSIONAL REFERENCES	
REF.	TOLERANCE OF FORM AND POSITION
aaa	0.20
bbb	0.25
ddd	0.15
eee	0.25
fff	0.10

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. 'b' IS MEASURABLE AT THE MAXIMUM SOLDER BALL DIAMETER AFTER REFLOW PARALLEL TO PRIMARY DATUM C.
4. DIMENSION 'ddd' IS MEASURED PARALLEL TO THE PRIMARY DATUM C.
5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. THE OVERALL PACKAGE THICKNESS 'A' ALREADY CONSIDERS COLLAPSED BALLS.
7. DIMENSIONAING AND TOLERANCING PER ASME Y14.5M 1994.
8. REFERENCE TO JEDEC MO-234B.
9. RoHS COMPLIANT PER CST-0001 LATEST REVISION.

Revision History

Revision	Date	Description	Page Number(s)
1.5	06/13	Last release in old format	n/a
1.6	08/03/15	Reformatted in new template	n/a
1.7	08/21/15	Formatting edits	6, 21, 22, 25, 26, 29, 30 & 36
1.8	09/18/15	Formatting edits	all
1.9	01/06/16	Clarifications made in Enable Pin Conditions BGA package added	7, 18, 22, 26 & 30 1, 3, 20–23, 34 & 40
2.0	02/22/16	Corrected Input Current spec unit of measure from mA to A	12, 16, 20, 24 & 28

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