

DESCRIPTION

The RH1056A JFET input operational amplifiers combine precision specifications with high speed performance.

For the first time, 16V/ μ s slew rate and 6.5MHz gain-bandwidth product are simultaneously achieved with offset voltage of typically 50 μ V, 1.2 μ V/ $^{\circ}$ C drift, bias currents of 40pA at 70 $^{\circ}$ C.

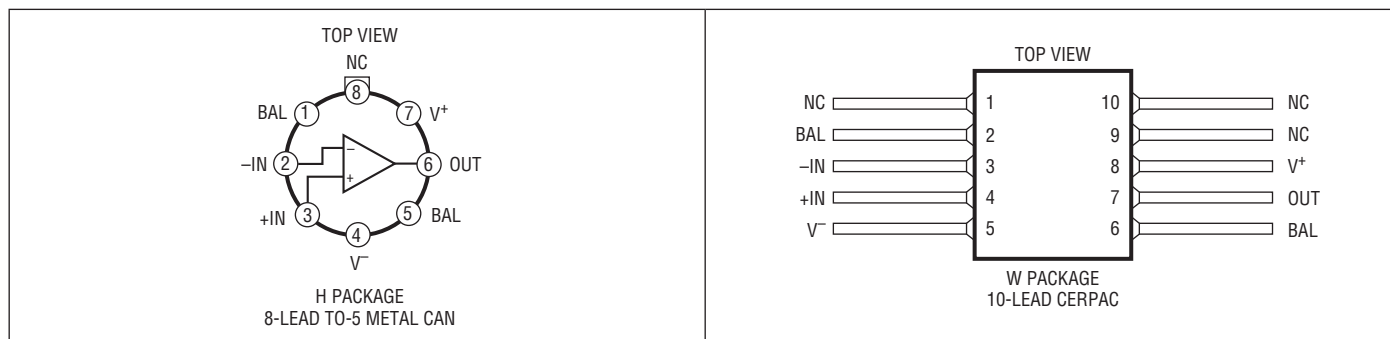
The wafer lots are processed to LTC's in-house Class S flow to yield circuits usable in stringent military applications.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage	± 20 V
Differential Input Voltage.....	± 40 V
Input Voltage.....	± 20 V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range.....	-55° C to 125° C
Storage Temperature Range.....	-65° C to 150° C
Lead Temperature (Soldering, 10 sec)	300° C

PACKAGE INFORMATION



BURN-IN CIRCUIT

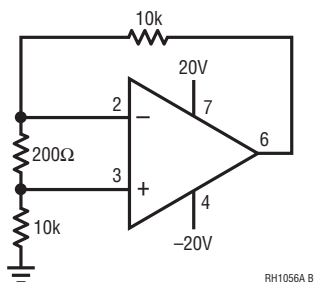


TABLE 1: ELECTRICAL CHARACTERISTICS (Preirradiation) (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	T _A = 25°C			SUB-GROUP	-55°C ≤ T _A ≤ 125°C			SUB-GROUP	UNITS
				MIN	TYP	MAX		MIN	TYP	MAX		
V _{OS}	Input Offset Voltage	RH1056AMW RH1056AMH	2			300 300	4 4			900 1100	2, 3 2, 3	μV μV
I _{OS}	Input Offset Current	Fully Warmed Up T _A = 125°C	4 4			10	1			1.5	2	pA nA
I _B	Input Bias Current	Fully Warmed Up T _A = 125°C	4			50	1			3.0	2	pA nA
R _{IN}	Input Resistance					10 ¹²						Ω
A _{VOL}	Large-Signal Voltage Gain	V _S = ±15V, V _O = ±10V, R _L = 2k V _S = ±15V, V _O = ±10V, R _L = 1k		150 130			4 4	40			5,6	V/mV V/mV
V _O	Output Voltage Swing	V _S = ±15V, R _L = 2k		±12			4	±12			5,6	V
V _{CM}	Input Common Mode Voltage Range	V _S = ±15V		±11			1	±11			2,3	V
CMRR	Common Mode Rejection Ratio	V _{CM} = ±11V V _{CM} = ±10.5V		86			1	85			2,3	dB dB
PSRR	Power Supply Rejection Ratio	V _S = ±10V to ±18V V _S = ±10V to ±17V		90			1	88			2,3	dB dB
I _S	Supply Current	V _S = ±15V				6.5	1					mA
SR	Slew Rate	A _V = 1, V _S = ±15V		10			7					V/μs
GBW	Gain-Bandwidth Product	V _S = ±15V				6.5						MHz
e _n	Input Noise Voltage Density	V _S = ±15V, f = 10Hz V _S = ±15V, f = 1kHz				28 14						fA/√Hz fA/√Hz
i _n	Input Noise Current Density	V _S = ±15V, f = 10Hz V _S = ±15V, f = 1kHz				1.8 1.8						fA/√Hz fA/√Hz
C _{IN}	Input Capacitance					4		4				pF

TABLE 1A: ELECTRICAL CHARACTERISTICS (Postirradiation) (Note 5)

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRAD (Si)		20KRAD (Si)		50KRAD (Si)		100KRAD (Si)		200KRAD (Si)		UNITS
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{OS}	Input Offset Voltage		2		300		300		370		570		870	μV
I _{OS}	Input Offset Current		4		±10		±50		±150		±250		±350	pA
I _B	Input Bias Current		4		±50		±250		±500		±1000		±2000	pA
A _{VOL}	Large-Signal Voltage Gain	V _O = ±10V, R _L ≥ 2k V _O = ±10V, R _L ≥ 1k		150 130		150 130		150 130		100 87		75 65		V/mV V/mV
V _O	Output Voltage Swing	R _L ≥ 2k		±12		±12		±12		±12		±12		V
V _{CM}	Input Common Mode Voltage Range	V _S = ±15V		±11		±11		±11		±11		±11		V
CMRR	Common Mode Rejection Ratio	V _{CM} = ±11V		86		86		86		86		86		dB
PSRR	Power Supply Rejection Ratio	V _S = ±10V to ±18V		90		90		90		90		90		dB
I _S	Supply Current				7		7		7		7		7	mA
SR	Slew Rate	A _V = 1, V _S = ±15V		10		10		9		9		9		V/μs
C _{IN}	Input Capacitance				3(Typ)		3(Typ)		3(Typ)		3(Typ)		3(Typ)	pF

TABLE 1A: ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage. Offset voltage is measured under two different conditions: (a) approximately 0.5 seconds after application of power, (b) at $T_A = 25^\circ\text{C}$ only, with the chip heated to approximately 45°C to account for chip temperature rise when the device is fully warmed up.

Note 3: Unless otherwise stated, $V_S = \pm 15\text{V}$; and V_{OS} , I_B and I_{OS} are measured at $V_{CM} = 0\text{V}$.

Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_J = T_A + (\theta_{JA} \cdot P_D)$ where θ_{JA} is the thermal resistance from junction to ambient.

Note 5: Unless otherwise stated, $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$ and $T_A = 25^\circ\text{C}$.

TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*, 2, 3, 4, 5, 6, 7
Group A Test Requirements (Method 5005)	1, 2, 3, 4, 5, 6, 7
Group B and D for Class S, and Class C and D for Class B** End Point Electrical Parameters (Method 5005)	1

*PDA applies to subgroup 1. See PDA Test Notes.

**For D3, D4, B5 and B6 V_{OS} Limit as follows

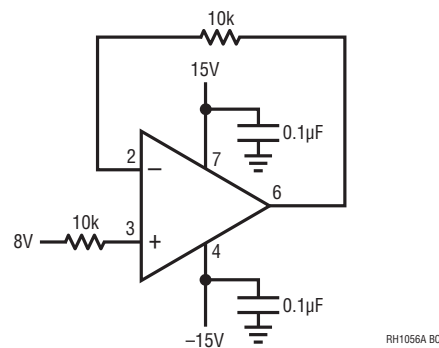
W Package	H Package
500 μV	700 μV

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

Linear Technology Corporation reserves the right to test to tighter limits than those given.

TOTAL DOSE BIAS CIRCUIT



TYPICAL PERFORMANCE CHARACTERISTICS

