

Features

- 4.2A, 400V, $R_{DS(on)} = 1.15\Omega @ V_{GS} = 10\text{ V}$
- Low gate charge (typical 13 nC)
- Low Crss (typical 9.5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

TO-252

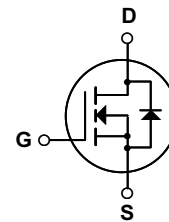


TO-251


General Description

These N-Channel enhancement mode power field effect transistors are produced using Kersemi proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, electronic lamp ballast based on half bridge.


Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	KSMD6N40 / KSMU6N40	Units
V_{DSS}	Drain-Source Voltage	400	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	4.2	A
	- Continuous ($T_C = 100^\circ\text{C}$)	2.66	A
I_{DM}	Drain Current - Pulsed (Note 1)	16.8	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	330	mJ
I_{AR}	Avalanche Current (Note 1)	4.2	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	2.5	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	50	W
	- Derate above 25°C	0.4	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	$^\circ\text{C}/\text{W}$

* When mounted on the minimum pad size recommended (PCB Mount)



Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	400	--	--	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	--	0.42	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 400 V, V _{GS} = 0 V	--	--	1	μA
		V _{DS} = 320 V, T _C = 125°C	--	--	10	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V	--	--	-100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	3.0	--	5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 2.1 A	--	0.92	1.15	Ω
g _{FS}	Forward Transconductance	V _{DS} = 50 V, I _D = 2.1 A (Note 4)	--	3.8	--	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	480	620	pF
C _{oss}	Output Capacitance		--	80	100	pF
C _{rss}	Reverse Transfer Capacitance		--	9.5	13	pF

Switching Characteristics

t _{d(on)}	Turn-On Delay Time	V _{DD} = 200 V, I _D = 5.5 A, R _G = 25 Ω (Note 4, 5)	--	13	35	ns
t _r	Turn-On Rise Time		--	65	140	ns
t _{d(off)}	Turn-Off Delay Time		--	20	50	ns
t _f	Turn-Off Fall Time		--	35	80	ns
Q _g	Total Gate Charge	V _{DS} = 320 V, I _D = 5.5 A, V _{GS} = 10 V (Note 4, 5)	--	13	17	nC
Q _{gs}	Gate-Source Charge		--	3.5	--	nC
Q _{gd}	Gate-Drain Charge		--	6.0	--	nC

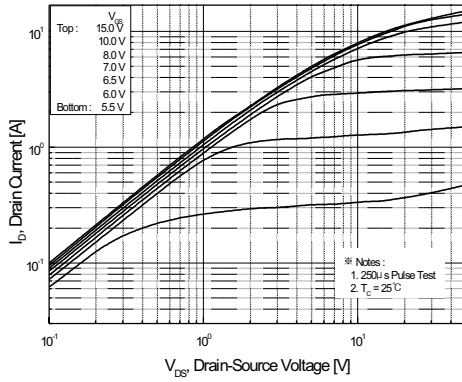
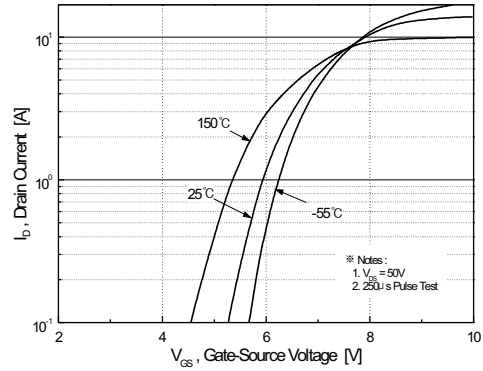
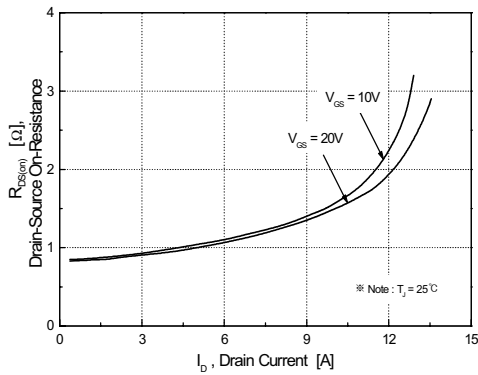
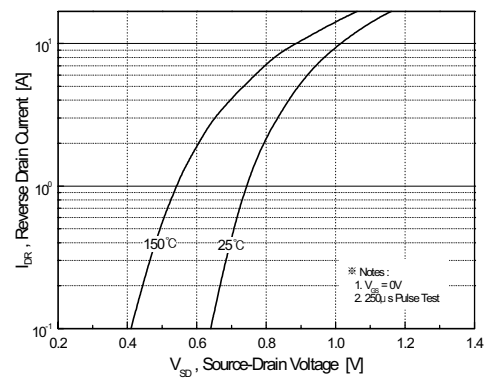
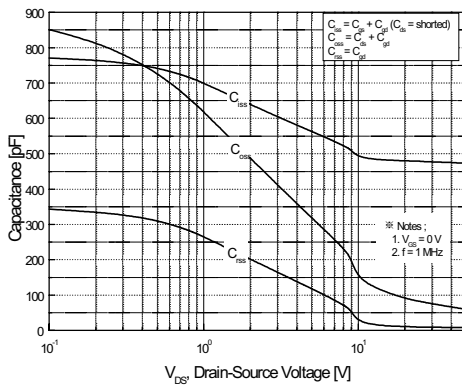
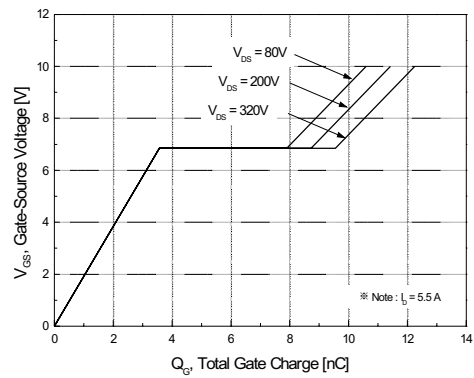
Drain-Source Diode Characteristics and Maximum Ratings

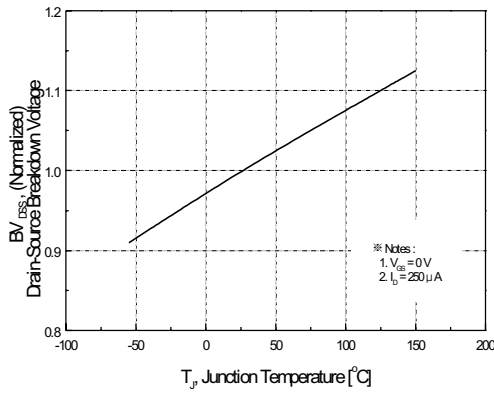
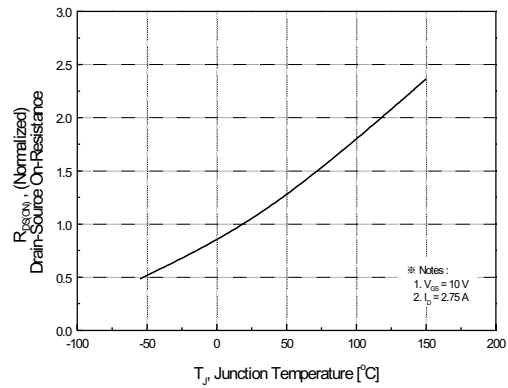
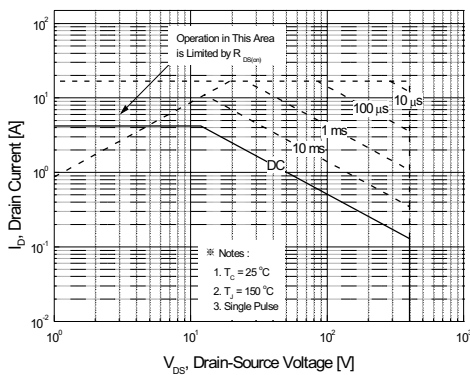
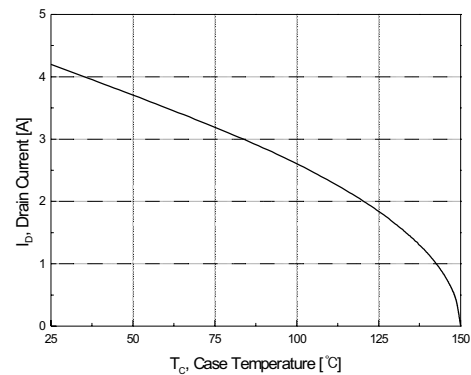
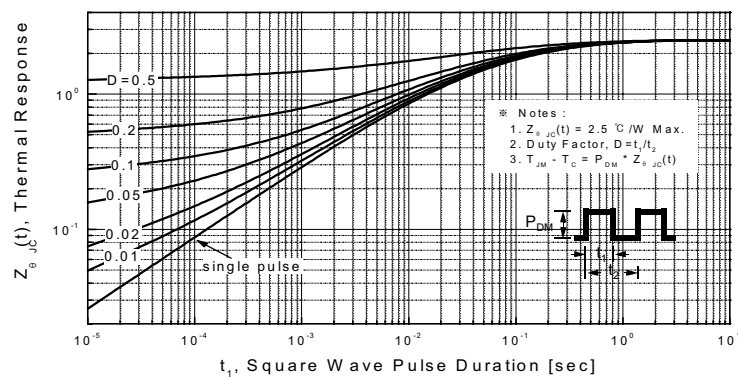
I _S	Maximum Continuous Drain-Source Diode Forward Current	--	--	4.2	A	
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	16.8	A	
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 4.2 A	--	--	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 5.5 A, di _F / dt = 100 A/μs (Note 4)	--	190	--	ns
Q _{rr}	Reverse Recovery Charge		--	1.15	--	μC

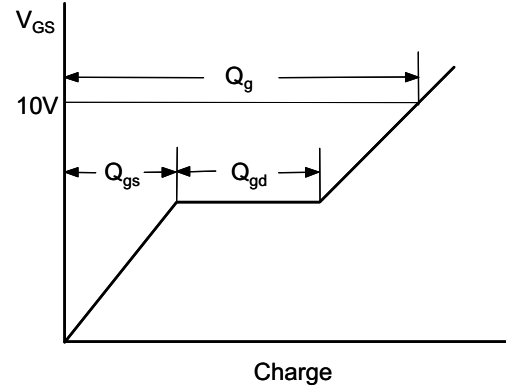
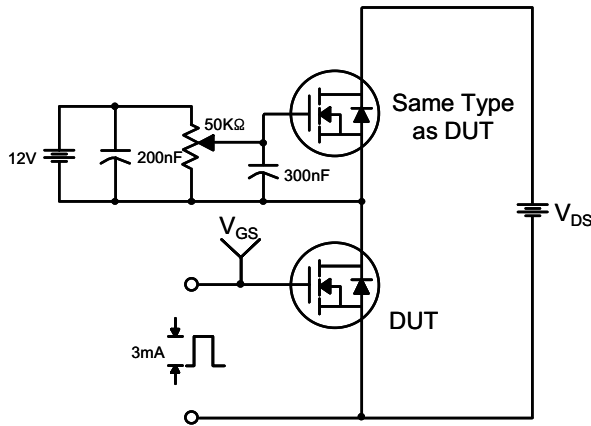
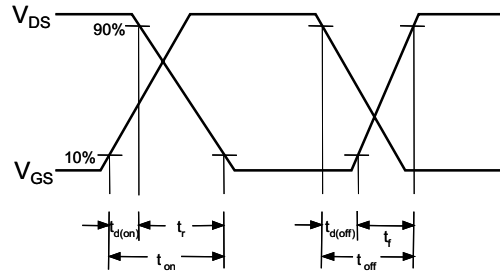
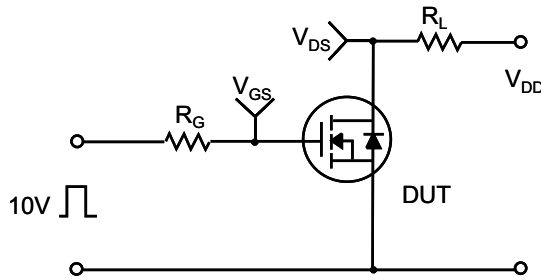
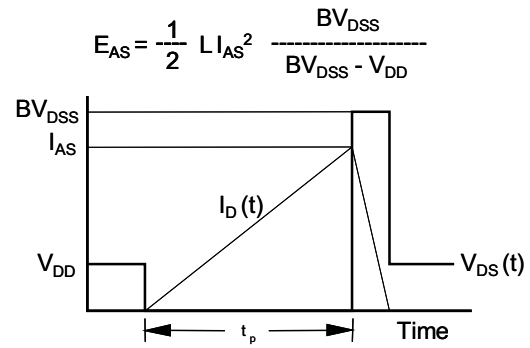
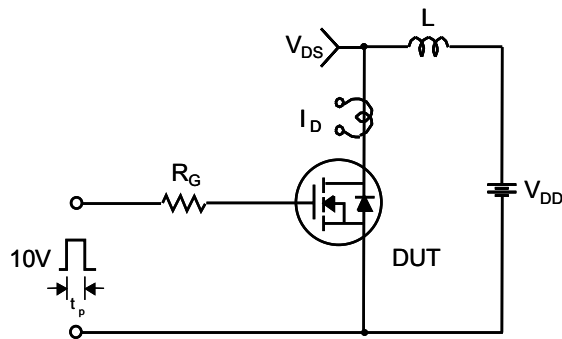
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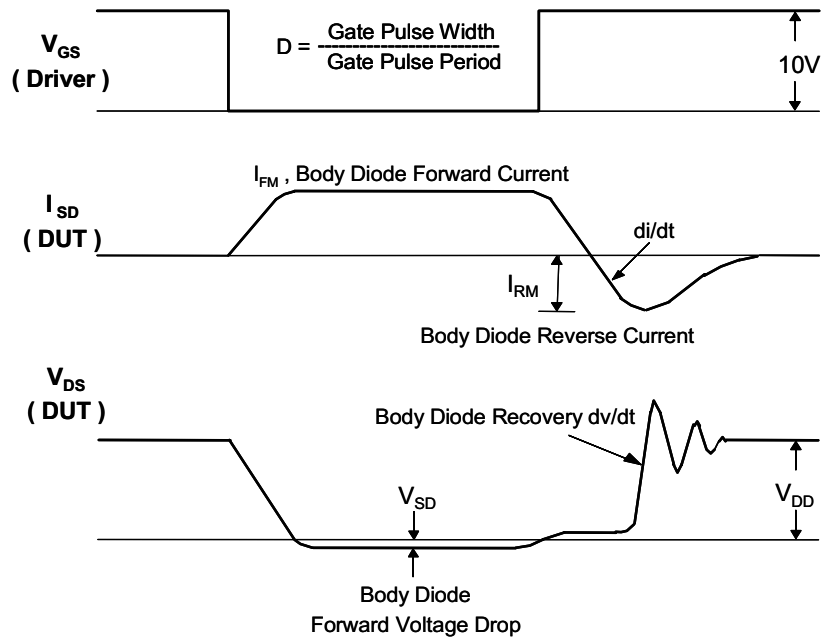
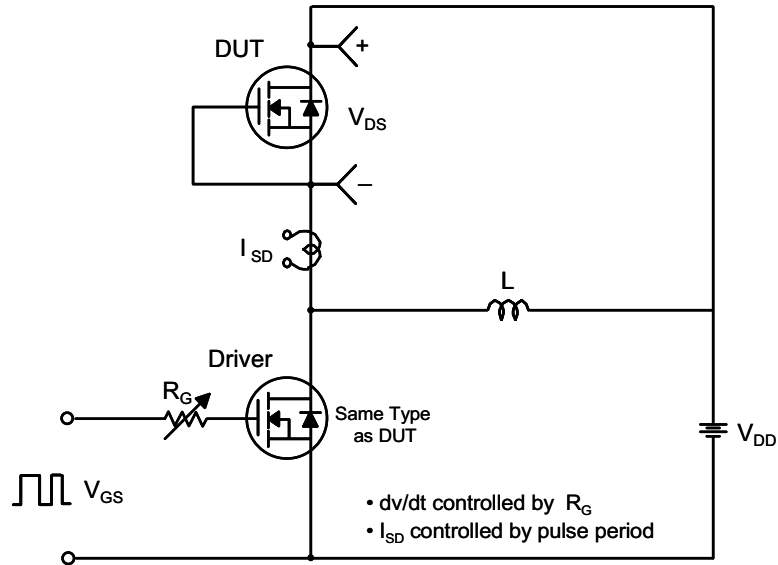
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 32.7mH, I_{AS} = 4.2A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 5.5A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics


Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics

Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

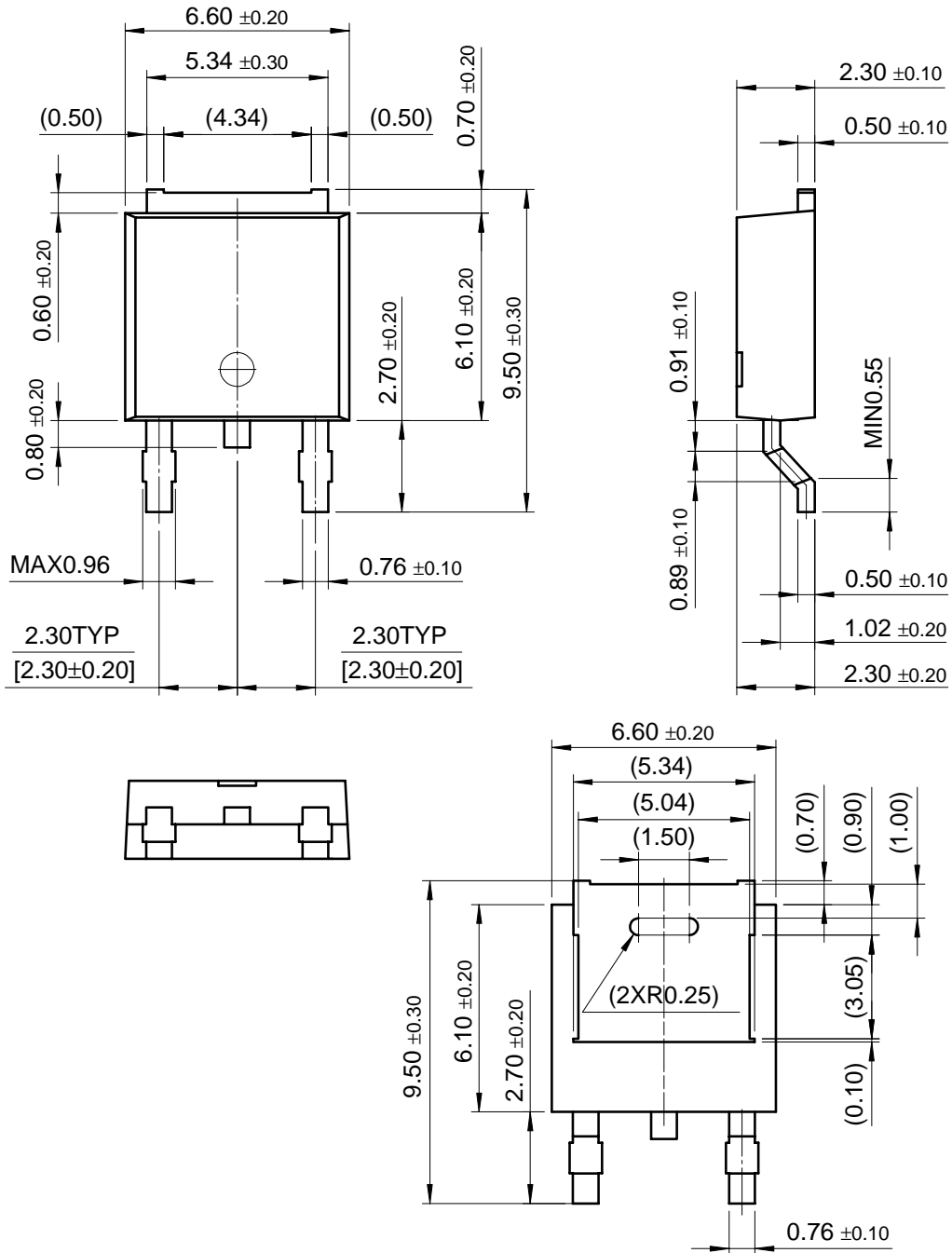
Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

Figure 8. On-Resistance Variation vs. Temperature

Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform

Resistive Switching Test Circuit & Waveforms

Unclamped Inductive Switching Test Circuit & Waveforms


Peak Diode Recovery dv/dt Test Circuit & Waveforms


Package Dimensions

DPAK



Package Dimensions (Continued)

IPAK

