

Ultra LDO 2A Linear Regulator With Adjustable & Bypass Pin

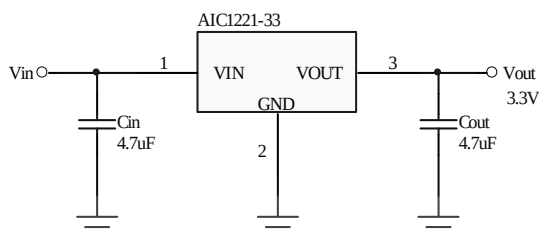
FEATURES

- Guaranteed 2A Output Current.
- Fast Response in Line/Load Transient.
- Wide Operating Voltage Ranges: 1.8V to 6V.
- 0.01 μ A Shutdown Standby Current.
- Low Quiescent Current: 30 μ A.
- Fixed: 1.8V, 2.5V, 3.3V, 5V Output Voltage.
- Adjustable Output Voltage are available from 0.8~5.5V.
- Low Dropout : 550mV at 2A and 3.3V output voltage, 480mV at 2A and 5V output voltage.
- High PSRR : 70dB at 1kHz.
- Active Low or High Shutdown Control. Current Limit and Thermal Protection.
- Available in $\pm 2\%$ Output Tolerance.
- Available in SOT-223 & TO-252 (3 & 5 pin) and SOP-8 Package.

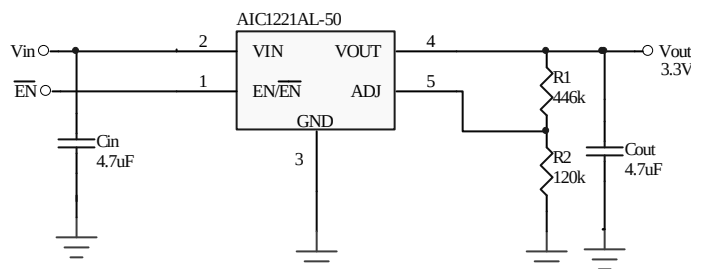
APPLICATIONS

- LCD TV, LCD Monitor, DPF
- Networking
- STB
- DVD, HDD Driver
- Portable AV Equipment
- PC Peripherals

TYPICAL APPLICATION CIRCUIT

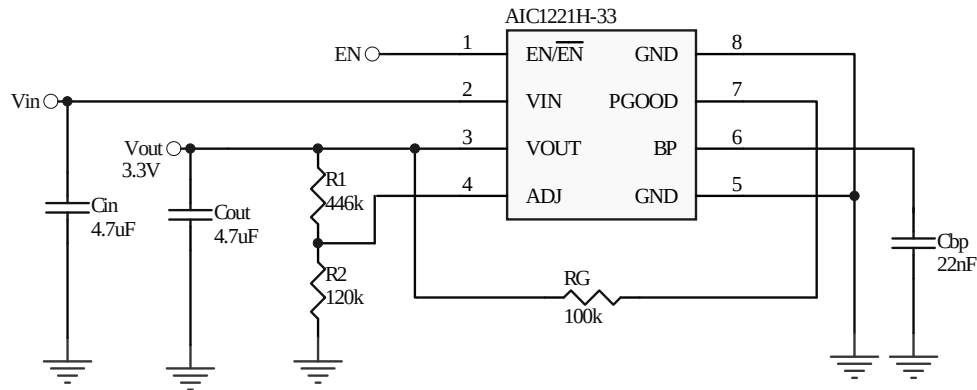


Fixed Linear Regulator



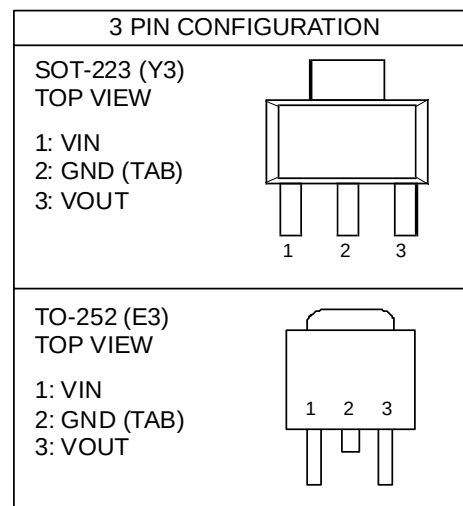
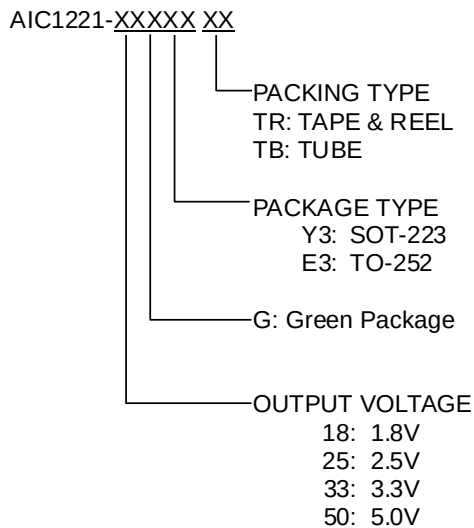
Adjustable Linear Regulator

■ TYPICAL APPLICATION CIRCUIT (Continued)



Adjustable Linear Regulator in SOP-8 Package

■ ORDERING INFORMATION



(Of a unit of 0.1V within
0.8~5.5V, additional voltage
versions are available on
demand)

Example: AIC1221-18GY3TR
→ 1.8V Version, in SOT-223 Green
Package & Tape & Reel Packing Type

Example: AIC1221-18GE3TR
→ 1.8V Version, in TO-252 Green Package
& Tape & Reel Packing Type

ORDERING INFORMATION (Continued)

AIC1221XX-XXXXXXXX

PACKING TYPE
TR: TAPE & REEL
TB: TUBE

PACKAGE TYPE
E5: TO-252-5
E5T: TO-252-5

G: Green Package

OUTPUT VOLTAGE
18: 1.8V
25: 2.5V
33: 3.3V
50: 5.0V

(Of a unit of 0.1V within
0.8~5.5V, additional voltage
versions are available on
demand)

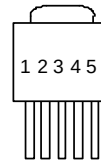
ENABLE TYPE
L: Chip Enable Low
H: Chip Enable High

B: Bypass
A: ADJ
(For E5 package only)

5 PIN CONFIGURATION

TO-252-5 (E5)
TOP VIEW

1: EN / $\overline{\text{EN}}$
2: VIN
3: GND (TAB)
4: VOUT
5: BP/ADJ



TO-252-5 (E5T)
TOP VIEW

1: EN / $\overline{\text{EN}}$
2: VIN
3: GND (TAB)
4: VOUT
5: NC



Example: AIC1221BH-18GE5TR

→ With Bypass Pin, Chip Enable High, 1.8V
Version, in TO-252-5 Green Package &
Tape & Reel Packing Type

Example: AIC1221H-18GE5TTR

→ Chip Enable High, 1.8V Version, in
TO-252-5 Green Package & Tape & Reel
Packing Type

ORDERING INFORMATION (Continued)

AIC1221X-XXXXXXXX

PACKING TYPE
TR: TAPE & REEL
TB: TUBE

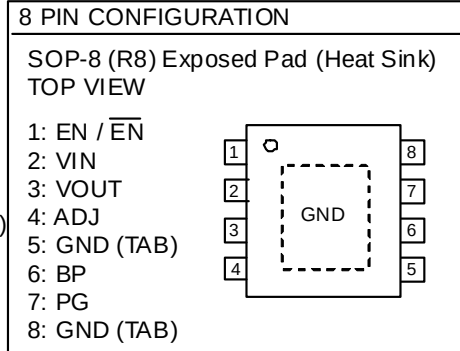
PACKAGE TYPE
R8: SOP-8 Exposed Pad (Heat Sink)

G: Green Package

OUTPUT VOLTAGE
18: 1.8V
25: 2.5V
33: 3.3V
50: 5.0V

(Of a unit of 0.1V within 0.8~5.5V,
additional voltage versions are
available on demand)

ENABLE TYPE
L: Chip Enable Low
H: Chip Enable High



Example: AIC1221H-18GR8TR

→ Chip Enable High, 1.8V Version, in SOP-8
Exposed Pad (Heat Sink) Green Package &
Tape & Reel Packing Type

Input Voltage	7V
EN Pin Voltage	7V
Noise Bypass Terminal Voltage	7V
Operating Temperature Range	-40°C~85°C
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C~150°C
Lead Temperature (Soldering, 10 sec)	260°C
Thermal Resistance (Junction to Case)	
SOT-223.....	15°C /W
TO-252.....	8°C /W
SOP-8 (Exposed Pad)*	15°C /W
Thermal Resistance (Junction to Ambient)	
(Assume no ambient airflow, no heat sink) SOT-223	130°C /W
TO-252.....	100°C /W
(Assume no ambient airflow) SOP-8 (Exposed Pad)*	60°C /W

Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

* The package is placed on a two layers PCB with 2 ounces copper and 2 square inch, connected by 8 vias.

■ ELECTRICAL CHARACTERISTICS

($C_{IN} = C_{OUT} = 4.7\mu F$ (Note 1), $C_{BP} = 22nF$, $V_{IN} = V_{OUT} + 1V$, $T_J = 25^\circ C$, unless otherwise specified)
(Note 2)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Voltage (Note 3)		V_{IN}	1.8		6	V
Output Voltage Tolerance	$I_{OUT} = 1mA$	V_{OUT}	-2		2	%
Continuous Output Current	$V_{IN} \geq 2.3V$	I_{OUT}	2			A
Quiescent Current	Chip Enable Low, $V_{EN} \leq 0.4V$, $I_{OUT} = 0mA$ Chip Enable High, $V_{EN} \geq 1.6V$, $I_{OUT} = 0mA$	I_Q		30	50	μA
GND Pin Current	Chip Enable Low, $V_{EN} \leq 0.4V$, $I_{OUT} = 2A$ Chip Enable High, $V_{EN} \geq 1.6V$, $I_{OUT} = 2A$	I_{GND}		30	50	μA
Standby Current	Chip Enable Low, $V_{EN} = V_{IN}$ Chip Enable High, $V_{EN} = 0$	I_{STBY}		0.01	0.5	μA
Output Current Limit	$R_{LOAD} = 0.1\Omega$	I_{IL}	2.2	3.0	3.9	A
Current Fold Back	$R_{LOAD} = 0.1\Omega$	I_{CFB}		1.0		A
Dropout Voltage	$I_{OUT} = 2A$, $V_{OUT} = 1.8V$	V_{DROP}		700	900	mV
	$I_{OUT} = 2A$, $V_{OUT} = 3.3V$			550	700	
	$I_{OUT} = 2A$, $V_{OUT} = 5.0V$			480	600	
Line Regulation	$V_{IN} = V_{OUT} + 1V$ to 6V, $I_{OUT} = 1mA$	ΔV_{LIR}		3	15	mV
Load Regulation	$I_{OUT} = 1mA$ to 2A	ΔV_{LOR}		5	15	mV
Ripple Rejection	$f = 1KHz$, Ripple = 0.5Vp-p,	PSRR		70		dB
Temperature Coefficient		TC		50		ppm/ $^\circ C$
Thermal Shutdown Temperature	$V_{IN} = V_{OUT} + 1V$	T_{SD}		150		$^\circ C$
Thermal Shutdown Hysteresis		ΔT_{SD}		20		$^\circ C$
ADJ Pin Specifications						
ADJ Pin Current	$V_{ADJ} = V_{REF}$	I_{ADJ}		10	100	nA
ADJ Pin Threshold		$V_{TH(ADJ)}$	0.05	0.1	0.2	V
Reference Voltage Tolerance		V_{REF}	0.686	0.7	0.714	V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Shutdown Pin Specifications						
Shutdown Pin Current	V _{EN} = V _{IN} or GND	I _{EN}	0	0.5		μA
Shutdown Exit Delay Time	I _{OUT} = 30mA	Δt	100			μS
Max Output Discharge Resistance to GND during Shutdown		R _{DS(on)_CLMP}	20	100		Ω
Shutdown Input Threshold	Chip Enable Low, Output OFF, V _{IN} = 1.6V to 6V Chip Enable High, Output ON, V _{IN} = 1.6V to 6V	V _{ENH}	1.6			V
	Chip Enable Low, Output ON, V _{IN} = 1.6V to 6V Chip Enable High, Output OFF, V _{IN} = 1.6V to 6V	V _{ENL}			0.4	
Power Good Specifications						
PGOOD Rise Threshold			90	93		%
PGOOD Hysteresis			3	10		%
PGOOD Sink Capability	I _{PGOOD} =10mA		0.2	0.4		V
PGOOD Delay			0.5		5	ms

Note 1: In the case of $V_{out} < 1.8V$, $10\mu F$ C_{out} is recommended.

Note 2: Specifications are production tested at $T_A = 25^\circ C$. Specifications over the $-40^\circ C$ to $85^\circ C$ operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).

Note 3: $V_{in(min)}$ is the higher value of $V_{out} + \text{Dropout Voltage}$ or $1.8V$.

TYPICAL PERFORMANCE CHARACTERISTICS

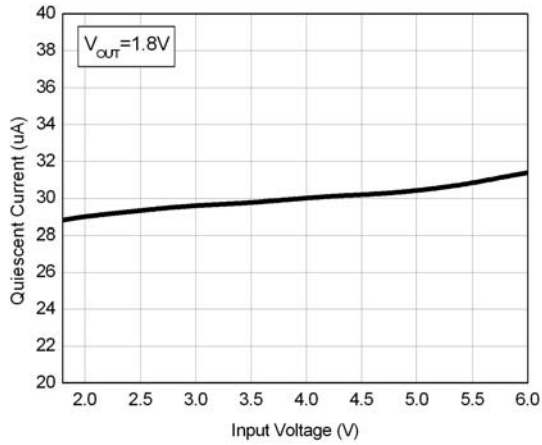


Fig. 1 Quiescent Current vs. Input Voltage at $V_{OUT}=1.8V$

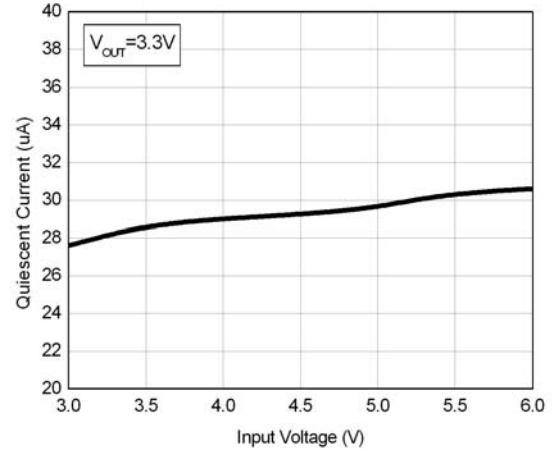


Fig. 2 Quiescent Current vs. Input Voltage at $V_{OUT}=3.3V$

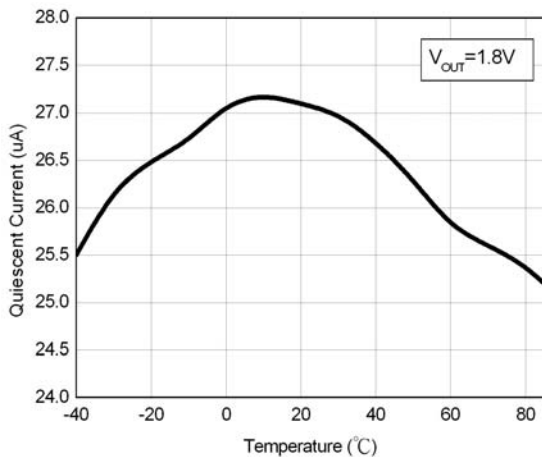


Fig. 3 Quiescent Current vs. Temperature at $V_{OUT}=1.8V$

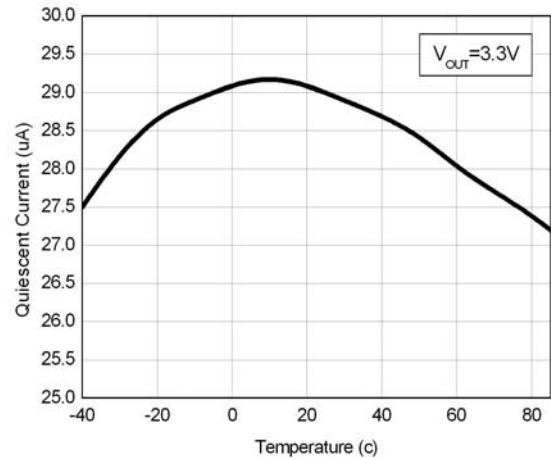


Fig. 4 Quiescent Current vs. Temperature at $V_{OUT}=3.3V$

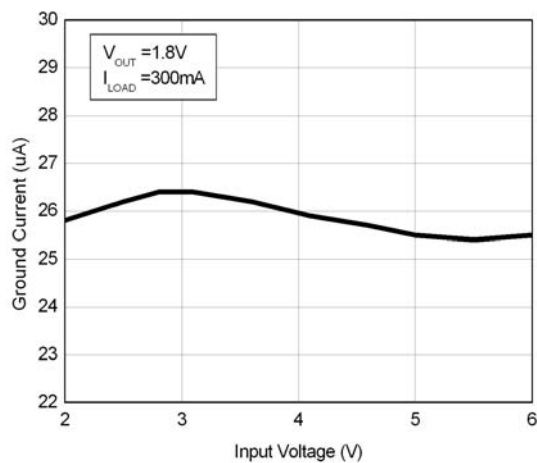


Fig. 5 Ground Current vs. Input Voltage at $V_{OUT}=1.8V$

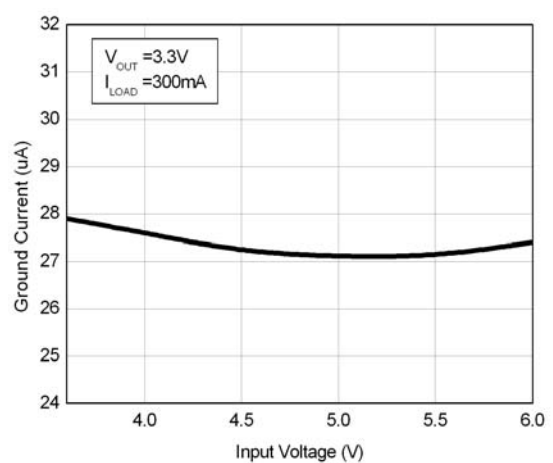
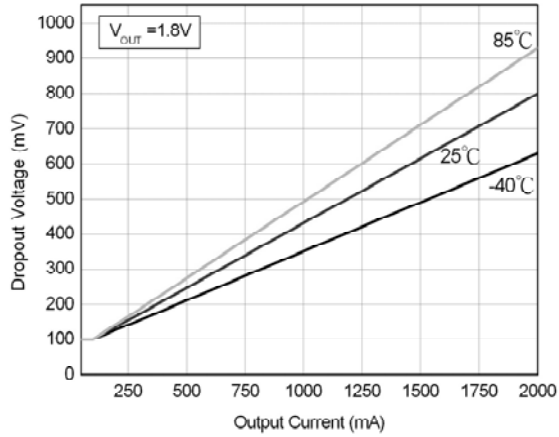
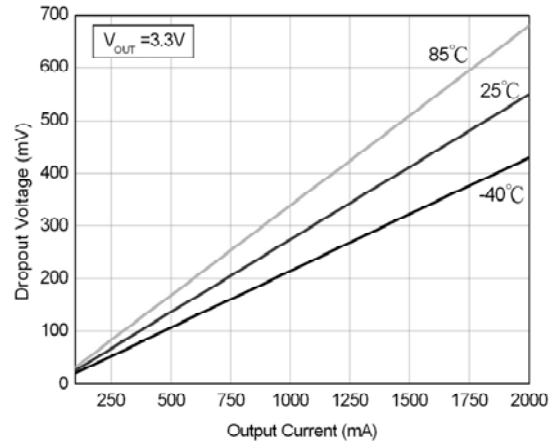
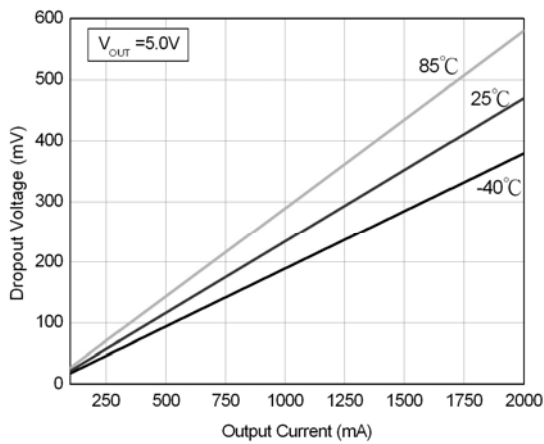
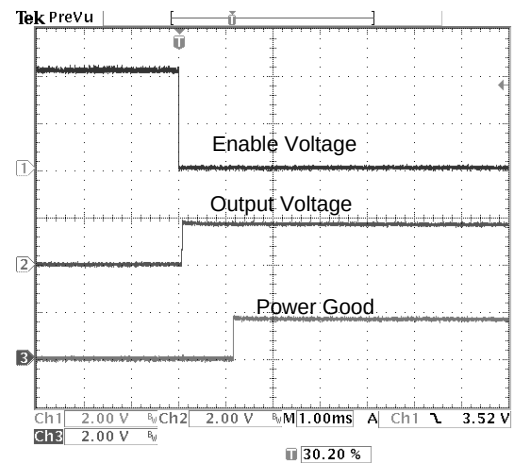
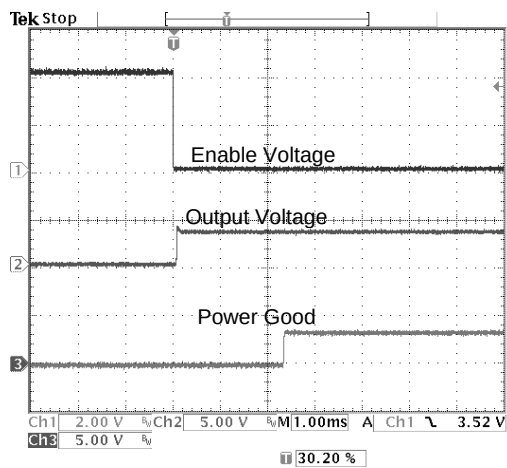
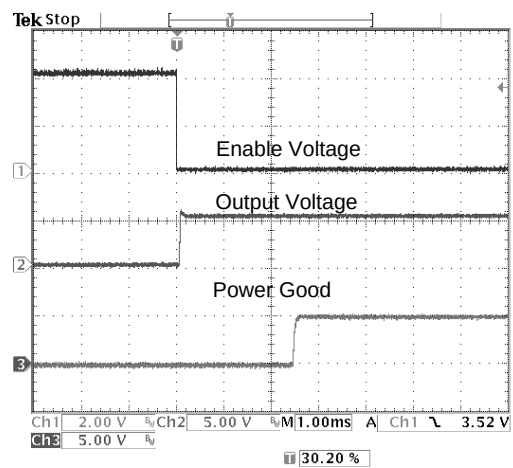
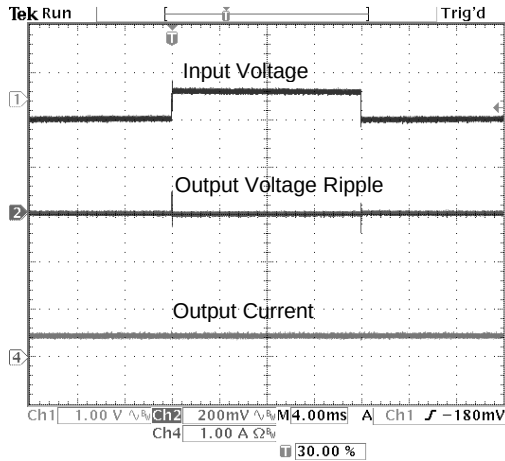
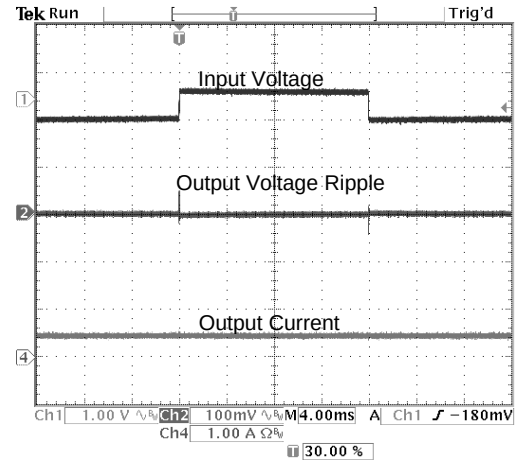
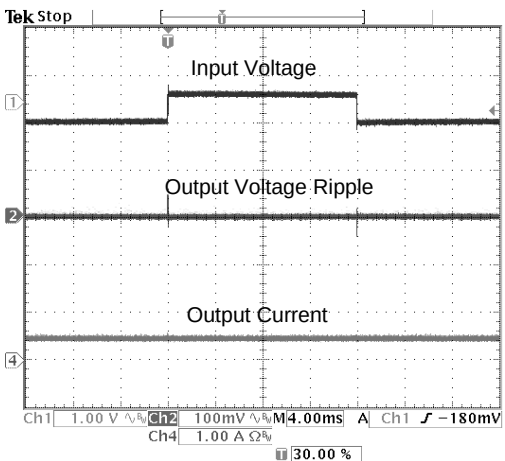
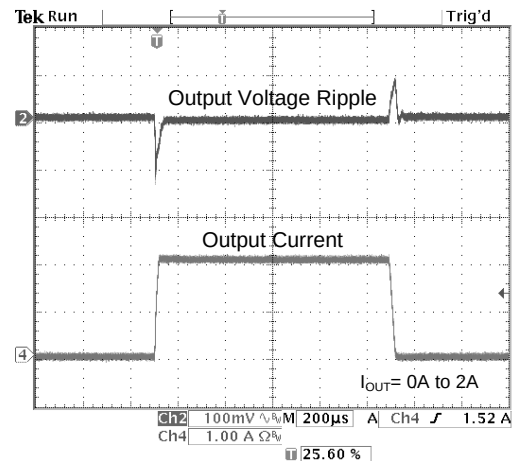
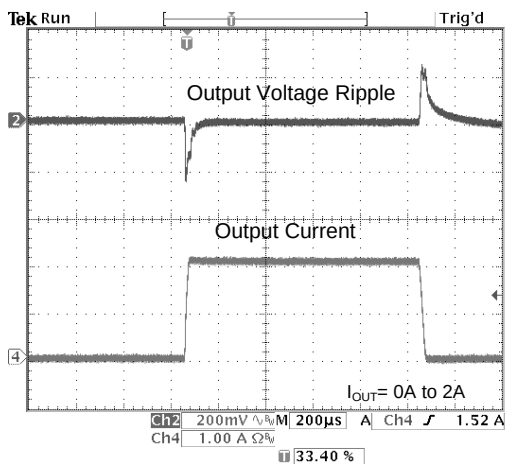
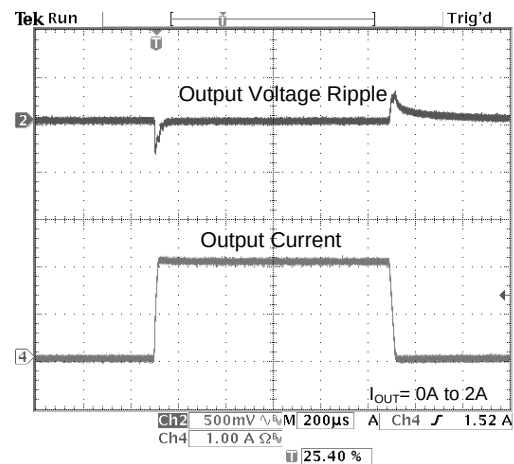


Fig. 6 Ground Current vs. Input Voltage at $V_{OUT}=3.3V$

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)


Fig. 7 Dropout Voltage at $V_{OUT}=1.8V$

Fig. 8 Dropout Voltage at $V_{OUT}=3.3V$

Fig. 9 Dropout Voltage at $V_{OUT}=5.0V$

Fig. 10 Enable Startup at $V_{OUT}=1.8V$

Fig. 11 Enable Startup at $V_{OUT}=3.3V$

Fig. 12 Enable Startup at $V_{OUT}=5.0V$

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)


Fig.13 Line Transient Response at $V_{OUT}=1.8V$

Fig. 14 Line Transient Response at $V_{OUT}=3.3V$

Fig. 15 Line Transient Response at $V_{OUT}=5.0V$

Fig.16 Load Transient Response at $V_{OUT}=1.8V$

Fig.17 Load Transient Response at $V_{OUT}=3.3V$

Fig.18 Load Transient Response at $V_{OUT}=5.0V$

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

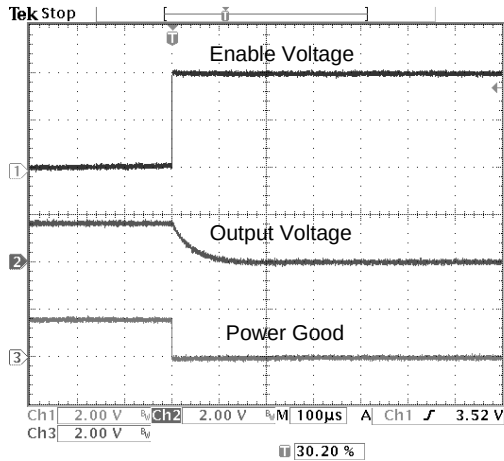
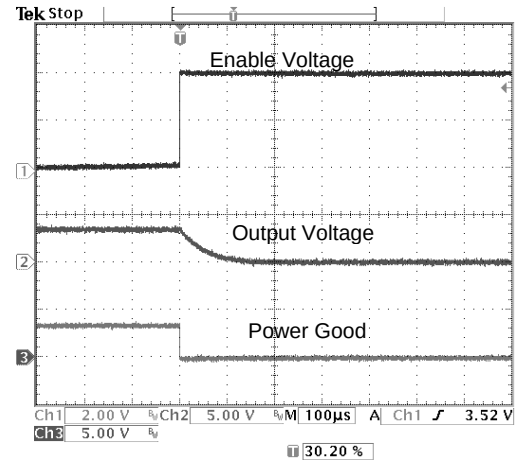
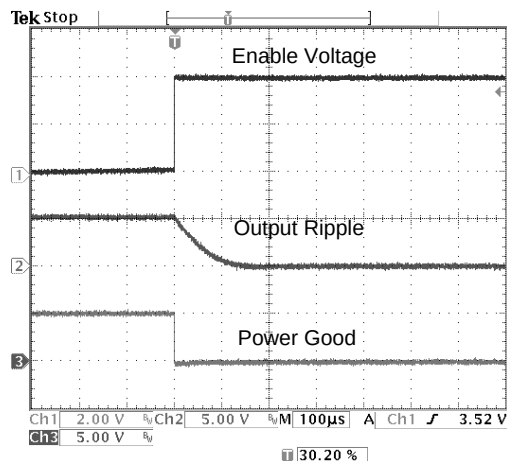
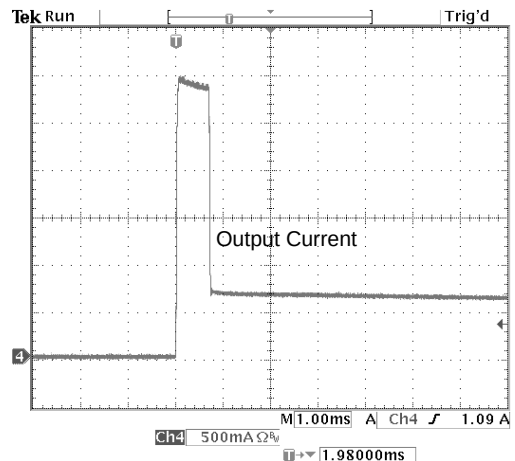
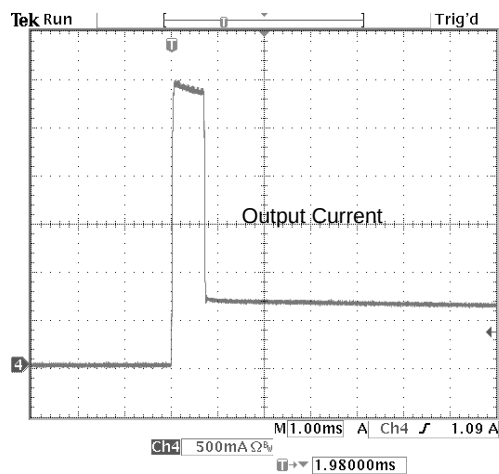
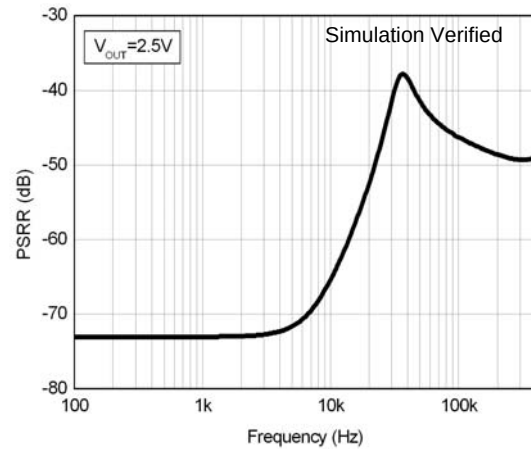
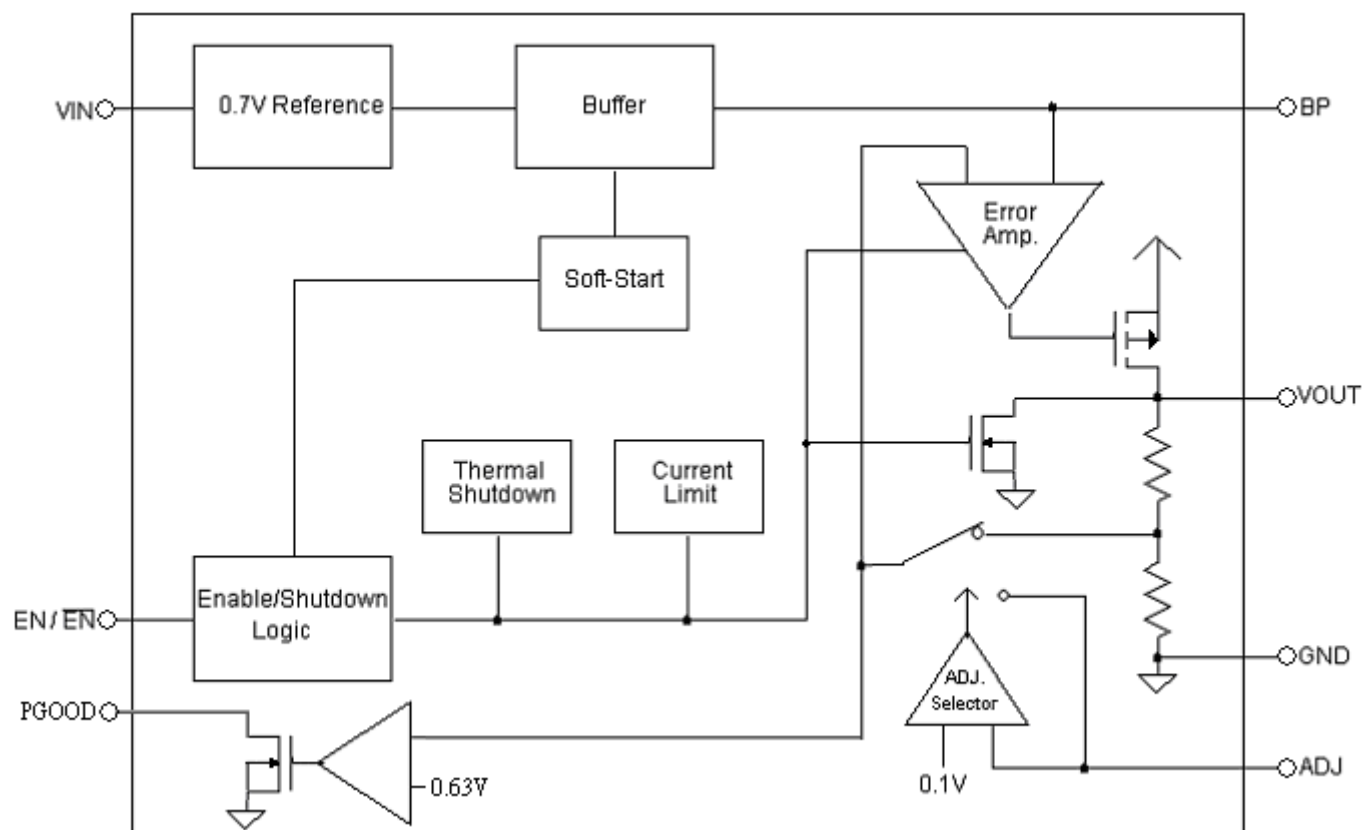

Fig.19 Shutdown Transient at $V_{OUT}=1.8V$

Fig.20 Shutdown Transient at $V_{OUT}=3.3V$

Fig. 21 Shutdown Transient at $V_{OUT}=5.0V$

Fig.22 Current Fold Back at $V_{OUT}=1.8V$

Fig. 23 Current Fold Back at $V_{OUT}=3.3V$


Fig.24 PSRR Curve

■ BLOCK DIAGRAM



■ PIN DESCRIPTION

VIN	– Power supply input pin. Bypass with a 4.7μF capacitor to GND.
GND	– Ground.
VOUT	– Regulator Output pin. Sources up to 2A.
$\overline{\text{EN}}$ (5 Pin and 8 Pin)	– Chip Enable (Active Low). This pin isn't allowed to float.
EN (5 Pin and 8 Pin)	– Chip Enable (Active High). This pin isn't allowed to float.
BP (5 Pin and 8 Pin)	– Bypass pin. It should be connected to external 22nF capacitor to GND to reduce output noise. The bypass pin could be floating if it's unnecessary.
PGOOD (8 Pin)	– Power Good open Drain output.
ADJ (5 Pin and 8 Pin)	– The output voltage can either be set by the internal feedback resistors when this pin is grounded, or be set by the external feedback resistors when using a resistive divider.

■ APPLICATION INFORMATION

The AIC1221 is a high performance linear regulator that provides low-dropout voltage and low quiescent-current. The device is available in an adjustable version and fixed output voltages ranging from 0.8V to 5.5V, and the device can supply loads up to 2A.

SHUTDOWN

By connecting $\overline{\text{EN}}$ (EN) pin to V_{IN} (ground), the AIC1221 can be shutdown to reduce the supply current to 0.01 μ A(typ.). At this operation mode, the output voltage of AIC1221 is equal to 0V.

CURRENT LIMIT

The AIC1221 includes a current limiter, which monitors and controls the maximum output current. If the output is overloaded or shorted to ground, this can protect the device from being damaged.

THERMAL PROTECTION

The AIC1221 includes a thermal-limiting circuit, which is designed to protect the device against overload condition. When the junction temperature exceeds $T_J=150^\circ\text{C}$, the thermal-limiting circuit turns off the pass transistor and allows the IC to cool. For continuous load condition, maximum rating of junction temperature must not be exceeded.

INPUT-OUTPUT CAPACITORS

Linear regulators require input and output capacitors to maintain stability. Input capacitor with a 4.7 μ F, Output capacitor with a 4.7 μ F or 10 μ F ($V_{\text{out}} < 1.8\text{V}$, 10 μ F C_{out} is recommended) ceramic output capacitor is recommended. When choosing the input and output ceramic capacitors, X5R and X7R types are recommended because they retain their capacitance over wider ranges of voltage and temperature than other types.

NOISE BYPASS CAPACITOR

A 22nF bypass capacitor at BP pin can reduce output voltage noise. The bypass pin can be floating if it's unnecessary.

OUTPUT VOLTAGE PROGRAMMING

Its internal feedback resistors can set the output voltage of AIC1221 linear regulator when the ADJ pin is grounded. In addition, the external feedback resistors when connecting a resistive divider R1 and R2 can set the output voltage of AIC1221 linear regulator. While connecting a resistive divider, V_{OUT} can be calculated as:

$$V_{\text{OUT}} = 0.7 \times \left(1 + \frac{R_1}{R_2} \right)$$

The resistive divider should sit as close to ADJ pin as possible.

POWER DISSIPATION

The maximum power dissipation of AIC1221 depends on the thermal resistance of its case and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The rate of temperature rise is greatly affected by the mounting pad configuration on the PCB, the board material, and the ambient temperature. When the IC mounting with good thermal conductivity is used, the junction temperature will be low even when large power dissipation applies.

The power dissipation across the device is

$$P = I_{\text{OUT}} (V_{\text{IN}} - V_{\text{OUT}})$$

The maximum power dissipation is:

$$P_{\text{MAX}} = \frac{(T_{J-\text{max}} - T_A)}{R\theta_{JA}}$$

Where $T_{J-\text{max}}$ is the maximum allowable junction temperature (150°C), and T_A is the ambient temperature suitable in application.

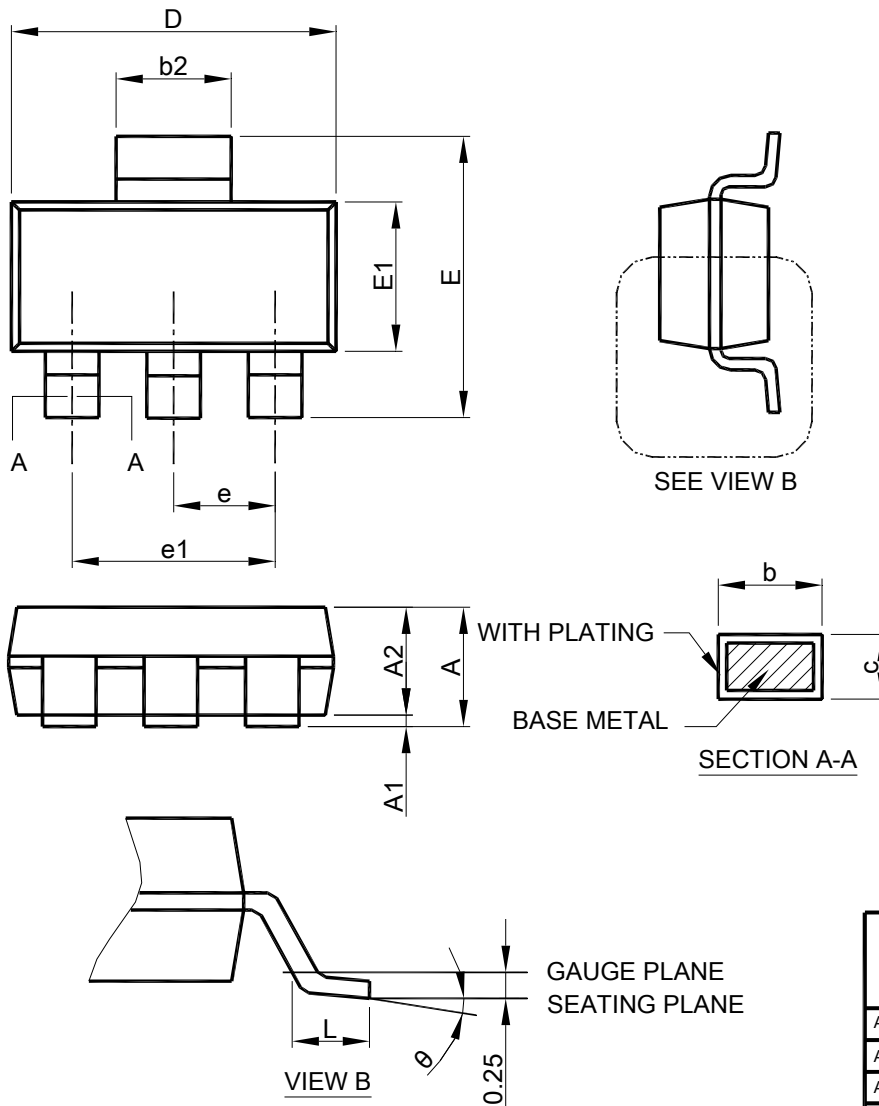
As a general rule, the lower temperature is, the better reliability of the device is. So the PCB mounting pad should provide maximum thermal conductivity to maintain low device temperature.

LAYOUT CONSIDERATION

Connect the bottom-side pad to a large ground plane. Use as much copper as possible to decrease the thermal resistance of the device.

■ PHYSICAL DIMENSIONS

● SOT-223 PACKAGE OUTLINE DRAWING

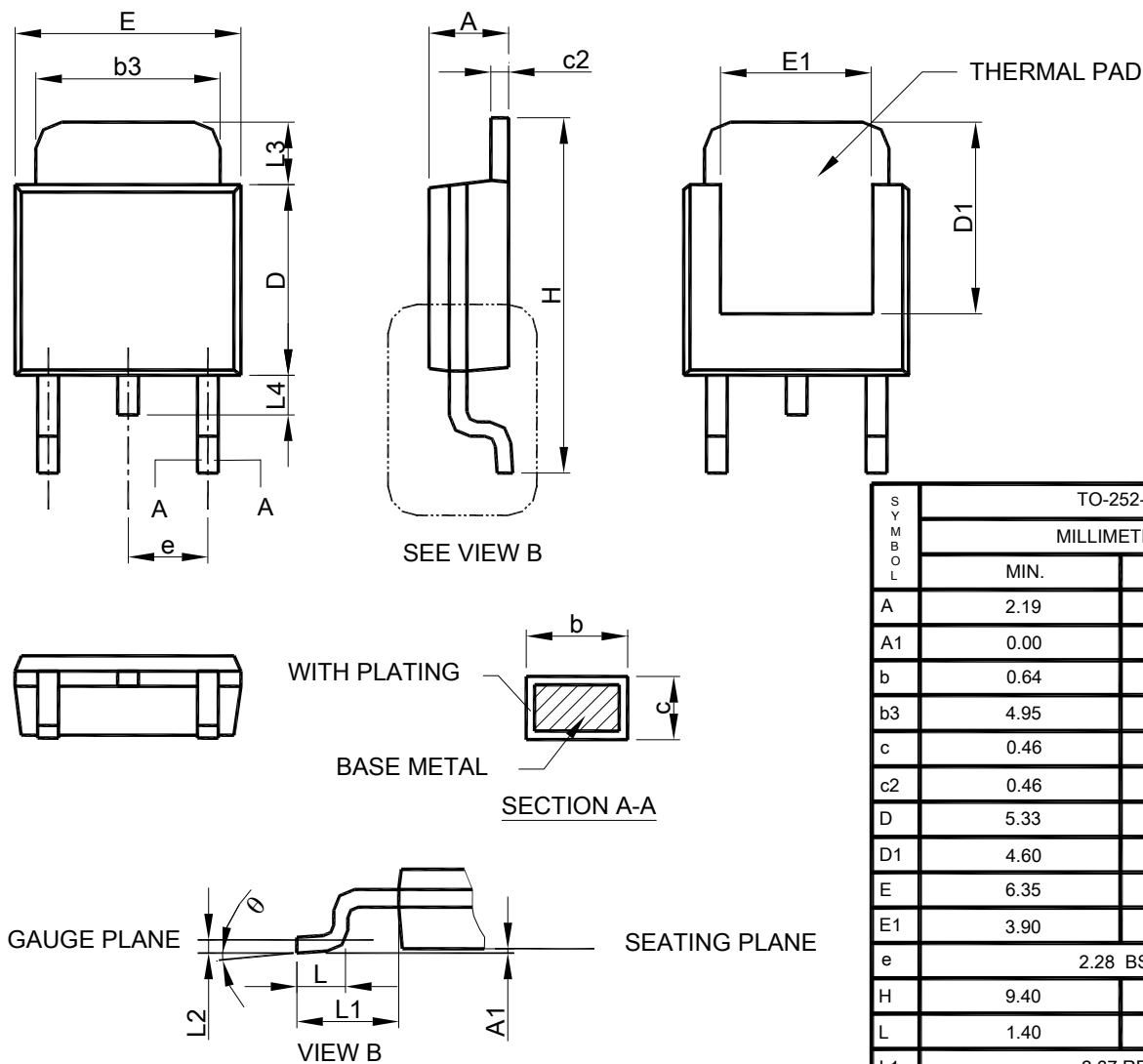


Note: 1. Refer to JEDEC TO-261AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E1" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

SYMBOL	SOT-223	
	MILLIMETERS	
	MIN.	MAX.
A		1.80
A1	0.02	0.10
A2	1.55	1.65
b	0.66	0.84
b2	2.90	3.10
c	0.23	0.33
D	6.30	6.70
E	6.70	7.30
E1	3.30	3.70
e	2.30 BSC	
e1	4.60 BSC	
L	0.90	
θ	0°	8°

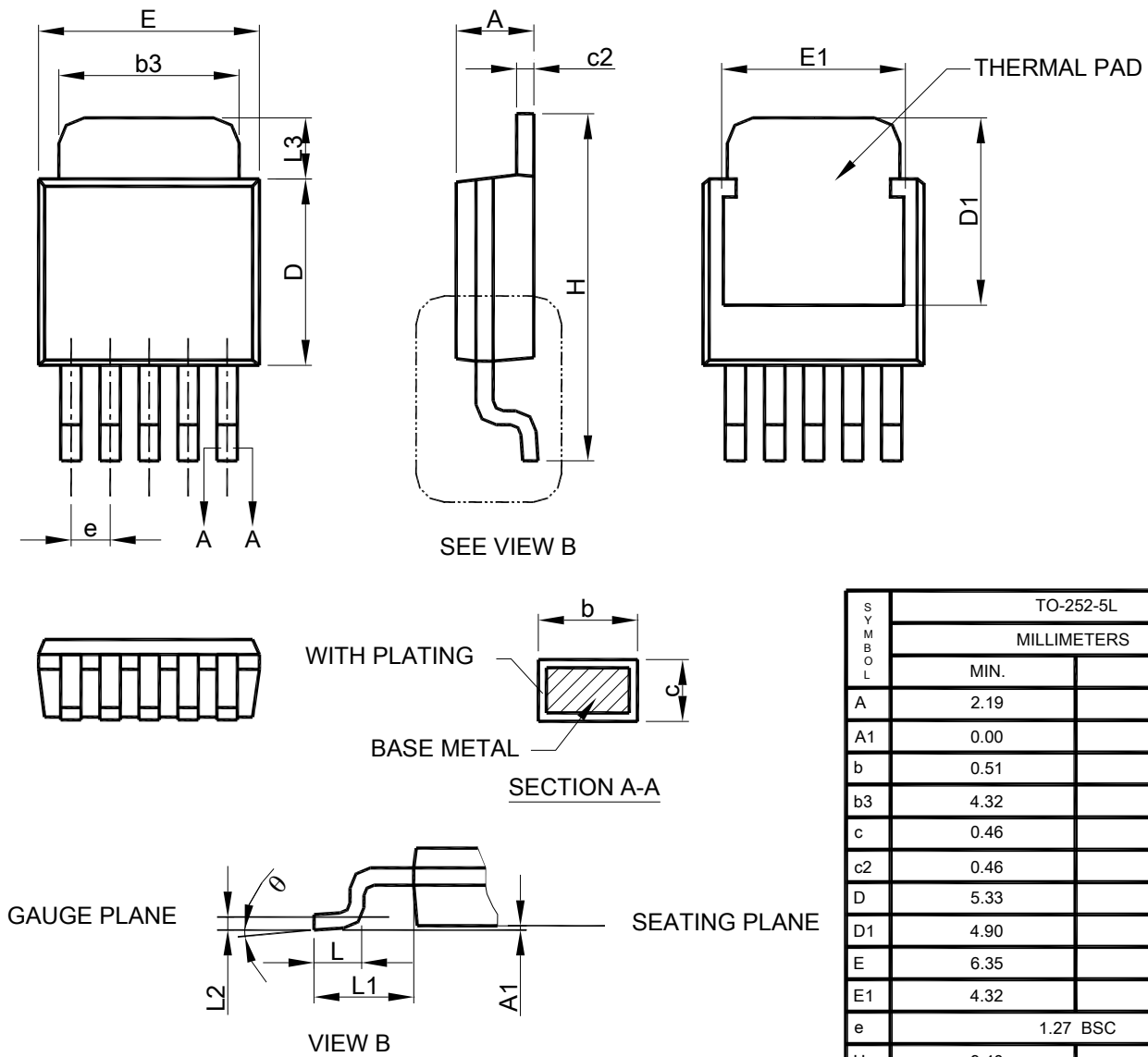
● TO-252-3L PACKAGE OUTLINE DRAWING



SYMBOL	TO-252-3L	
	MILLIMETERS	
	MIN.	MAX.
A	2.19	2.38
A1	0.00	0.13
b	0.64	0.89
b3	4.95	5.46
c	0.46	0.61
c2	0.46	0.89
D	5.33	6.22
D1	4.60	6.00
E	6.35	6.73
E1	3.90	5.46
e	2.28 BSC	
H	9.40	10.41
L	1.40	1.78
L1	2.67 REF	
L2	0.51 BSC	
L3	0.89	2.03
L4	--	1.02
θ	0°	8°

- Note: 1. Refer to JEDEC TO-252AA and AB.
2. Dimension "E" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "D" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

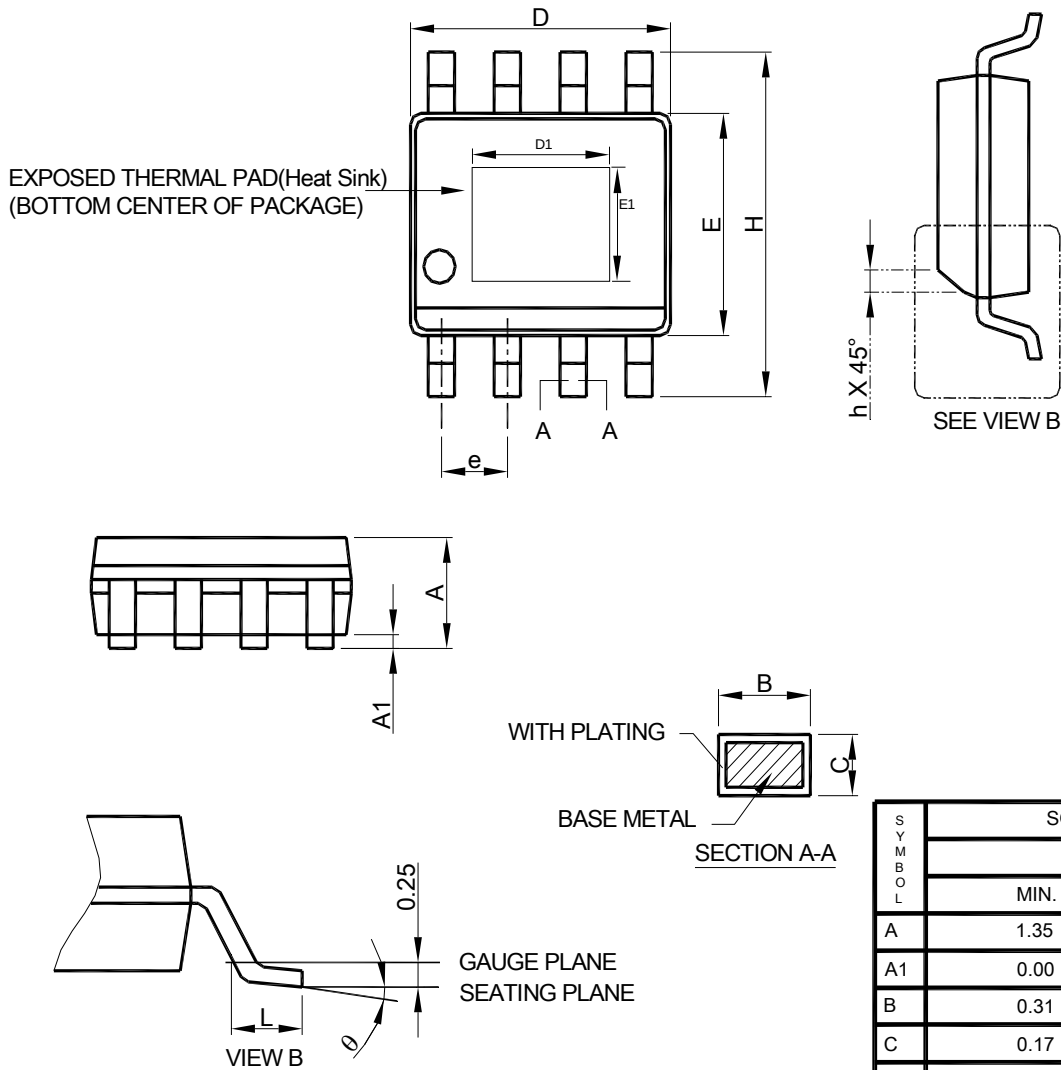
● **TO-252-5L PACKAGE OUTLINE DRAWING**



SYMBOL	TO-252-5L	
	MILLIMETERS	
	MIN.	MAX.
A	2.19	2.38
A1	0.00	0.13
b	0.51	0.71
b3	4.32	5.46
c	0.46	0.61
c2	0.46	0.89
D	5.33	6.22
D1	4.90	6.00
E	6.35	6.73
E1	4.32	5.33
e	1.27 BSC	
H	9.40	10.41
L	1.40	1.78
L1	2.67 REF	
L2	0.51 BSC	
L3	0.89	2.03
θ	0°	8°

- Note: 1. Refer to JEDEC TO-252AD and AB.
 2. Dimension "E" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
 3. Dimension "D" does not include inter-lead flash or protrusions.
 4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

● **SOP-8 Exposed Pad (Heat Sink) PACKAGE OUTLINE DRAWING**



Note : 1. Refer to JEDEC MS-012E.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

SYMBOL	SOP-8 Exposed Pad(Heat Sink)	
	MILLIMETERS	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.15
B	0.31	0.51
C	0.17	0.25
D	4.80	5.00
D1	1.50	3.50
E	3.80	4.00
E1	1.0	2.55
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
θ	0°	8°

Note:

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