

# 128KX32 STATIC RAM CMOS, HIGH SPEED MODULE

## FEATURES

- 128Kx32 bit CMOS Static
- Random Access Memory
  - Access Times: 15, 20, and 25ns
  - Individual Byte Selects
  - Fully Static, No Clocks
  - TTL Compatible I/O
- Single +5V ( $\pm 10\%$ ) Supply Operation
- High Density Package with JEDEC Standard Pinouts
  - 64 Pin ZIP, No. 85
    - Height: 13.97 (0.550")
  - 64 Lead SIMM, No. 333
    - Height: 15.62 (0.615")
  - Common Data Inputs and Outputs

## DESCRIPTION

The EDI8F32128C is a high speed 4Mb Static RAM module organized as 128K words by 32 bits. This module is constructed from four 128Kx8 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

Four chip enables (E0# - E3#) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The EDI8F32128C is offered in 64 pin ZIP/SIMM package which enables eight megabits of memory to be placed in less than 1.4 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

The ZIP and SIMM modules contain two pins, PD1 and PD2, which are used to identify module memory density in applications where alternate modules can be interchanged.

**FIG. 1 – PIN CONFIGURATIONS AND BLOCK DIAGRAM**

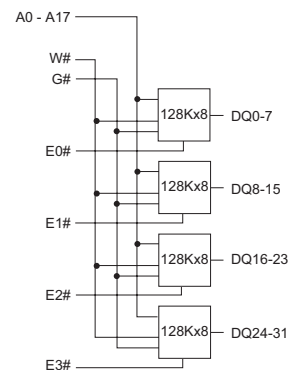
PD0	2	1	V <sub>ss</sub>
DQ0	4	3	PD1
DQ1	6	5	DQ8
DQ2	8	7	DQ9
DQ3	10	9	DQ10
V <sub>cc</sub>	12	11	DQ11
A7	14	13	A0
A8	16	15	A1
A9	18	17	A2
DQ4	20	19	DQ12
DQ5	22	21	DQ13
DQ6	24	23	DQ14
DQ7	26	25	DQ15
W#	28	27	V <sub>ss</sub>
A14	30	29	A15
E0#	32	31	E1#
E2#	34	33	E3#
A16	36	35	NC
V <sub>ss</sub>	38	37	G#
DQ16	40	39	DQ24
DQ17	42	41	DQ25
DQ18	44	43	DQ26
DQ19	46	45	DQ27
A10	48	47	A3
A11	50	49	A4
A12	52	51	A5
A13	54	53	V <sub>cc</sub>
DQ20	56	55	A6
DQ21	58	57	DQ28
DQ22	60	59	DQ29
DQ23	62	61	DQ30
V <sub>ss</sub>	64	63	DQ31

PD0 = OPEN  
PD1 = OPEN

**PIN NAMES**

A0-A16	Address Inputs
E0#-E3#	Chip Enables
W#	Write Enables
G#	Output Enable
DQ0-DQ31	Common Data Input/Output
V <sub>cc</sub>	Power (+5V $\pm 10\%$ )
V <sub>ss</sub>	Ground

**BLOCK DIAGRAM**



White Electronic Designs Corp. reserves the right to change products or specifications without notice.



**ABSOLUTE MAXIMUM RATINGS\***

Voltage on any pin relative to V <sub>SS</sub>	-0.5V to 7.0V
Operating Temperature T <sub>A</sub> (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	8.0 Watt
Output Current	20 mA

\* Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Supply Voltage	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.2	--	V <sub>CC</sub> +0.3V	V
Input Low Voltage	V <sub>IL</sub>	-0.3	--	0.8	V

**AC TEST CONDITIONS**

Input Pulse Levels	V <sub>SS</sub> to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 30pF

(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

**DC ELECTRICAL CHARACTERISTICS**

Parameter	Sym	Conditions	Min	Max	Units
Operating Power Supply Current	I <sub>CC1</sub>	WE# = V <sub>IL</sub> , I/O = 0mA, Min Cycle	—	780	mA
Standby (TTL) Power Supply Current	I <sub>CC2</sub>	E# ≥ V <sub>IH</sub> , V <sub>IN</sub> ≤ V <sub>IL</sub> or V <sub>IN</sub> ≥ V <sub>IH</sub>	—	80	mA
Full Standby Power Supply Current CMOS	I <sub>CC3</sub>	E# ≥ V <sub>CC</sub> -0.2V V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V	—	20	mA
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = 0V to V <sub>CC</sub>	—	±10	µA
Output Leakage Current	I <sub>LO</sub>	V I/O = 0V to V <sub>CC</sub>	—	±10	µA
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA	2.4	—	V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0mA	—	0.4	V

**TRUTH TABLE**

E#	W#	G#	Mode	Output	Power
H	X	X	Standby	HIGH Z	I <sub>CC3</sub>
L	H	L	Read	DOUT	I <sub>CC1</sub>
L	L	X	Write	DIN	I <sub>CC1</sub>
L	H	H	Output Deselect	HIGH Z	I <sub>CC1</sub>

**CAPACITANCE**

(f = 1.0MHz, V<sub>IN</sub>=V<sub>CC</sub> or V<sub>SS</sub>)

Parameter	Sym	Max	Unit
Address Lines	CI	25	pF
Data Lines	CD/Q	35	pF
Chip Enable Line	CC	25	pF
Write Control Line	CN	35	pF

These parameters are sampled, not 100% tested.



AC CHARACTERISTICS READ CYCLE

Parameter	Symbol		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	15		20		25		ns
Address Access Time	TAVQV	TAA		15		20		25	ns
Chip Enable Access	TELQV	TACS		15		20		25	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		8		10		12	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		8		13		15	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Disable to Output in High Z (1)	TGHQZ	TOHZ		5		8		10	ns

Note 1: Parameter guaranteed, but not tested.

FIG. 2 READ CYCLE 1 - W# HIGH, G#, E# LOW

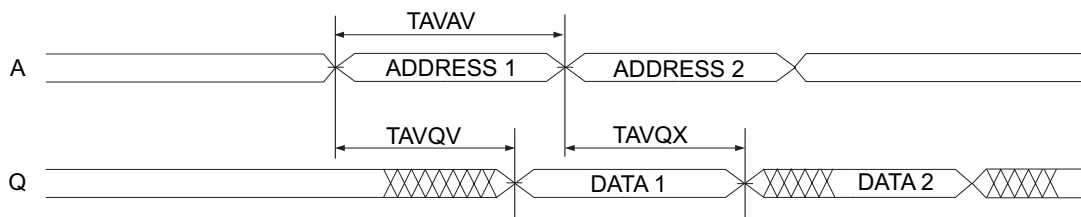
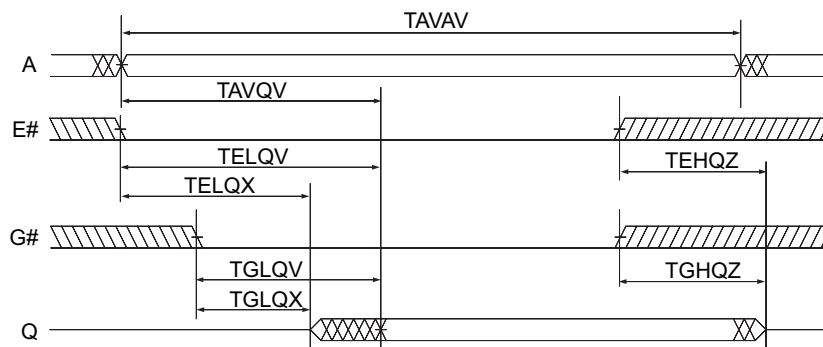


FIG. 3 READ CYCLE 2 - W# HIGH





## AC CHARACTERISTICS WRITE CYCLE

Parameter	Symbol		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	15		20		25		ns
Chip Enable to End of Write	TELWH	TCW	12		15		15		ns
	TWLEH	TCW	12		15		15		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	12		15		15		ns
	TAVEH	TAW	12		15		15		ns
Write Pulse Width	TWLWH	TWP	12		15		15		ns
	TELEH	TWP	12		15		15		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time	TWHDX	TDH	3		3		3		ns
	TEHDX	TDH	3		3		3		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	9	0	9	0	9	ns
Data to Write Time	TDVWH	TDW	7		8		8		ns
	TDVEH	TDW	7		8		8		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

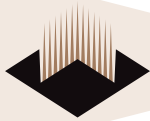


FIG. 4 WRITE CYCLE 1 - W# CONTROLLED

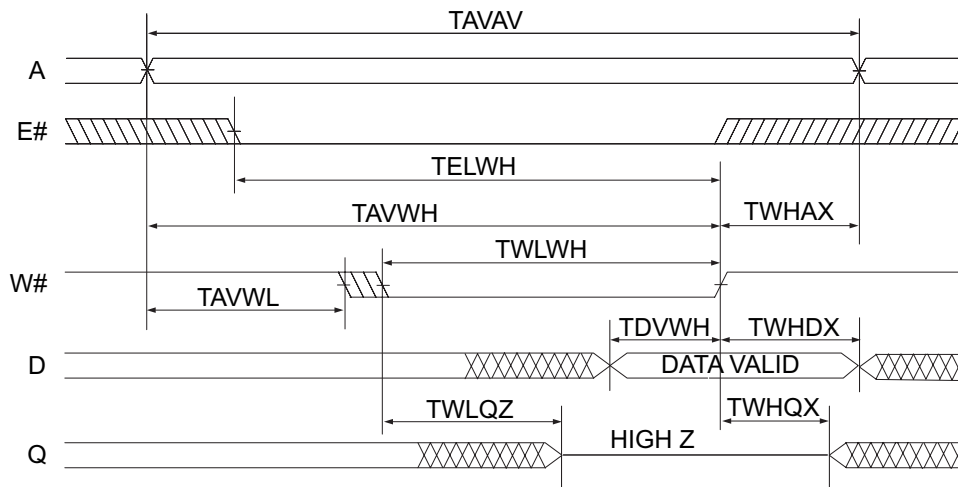
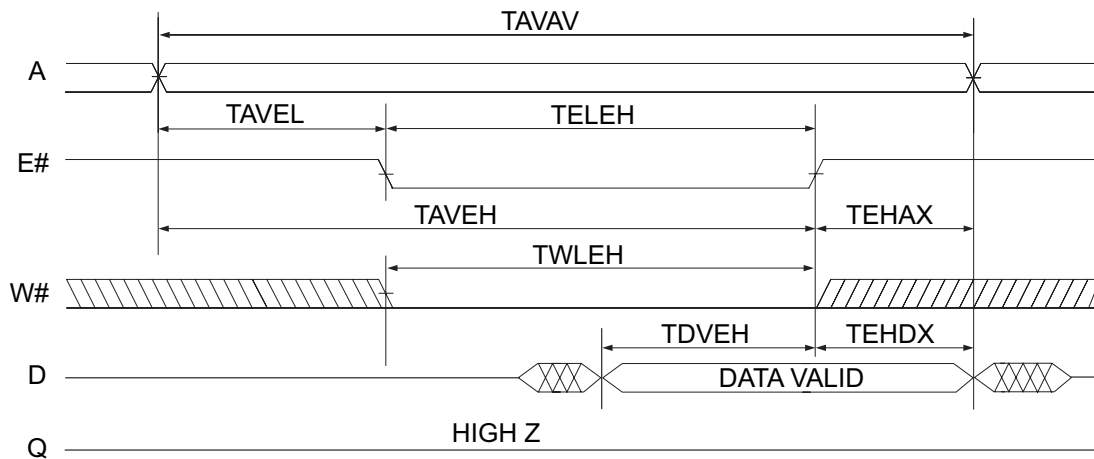


FIG. 5 WRITE CYCLE 2 - E# CONTROLLED



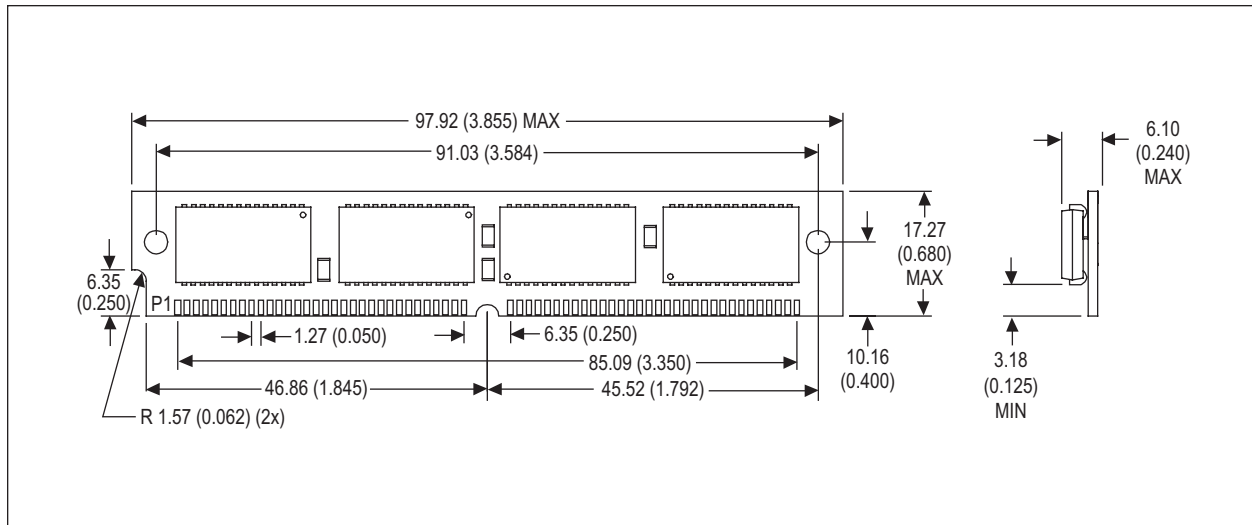


ORDERING INFORMATION PACKAGE NO. 32: 64 LEAD ANGLED SIMM

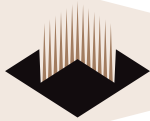
Part Number	Speed (ns)	Package No.	Package Height*
EDI8F32128C15MNC	15	32	17.27 (0.680")
EDI8F32128C20MNC	20	32	17.27 (0.680")
EDI8F32128C25MNC	25	32	17.27 (0.680")

NOTE: 1. For Gold SIMM change form EDI8F to EDI8G.

PACKAGE NO. 32: 64 LEAD ANGLED SIMM



\* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

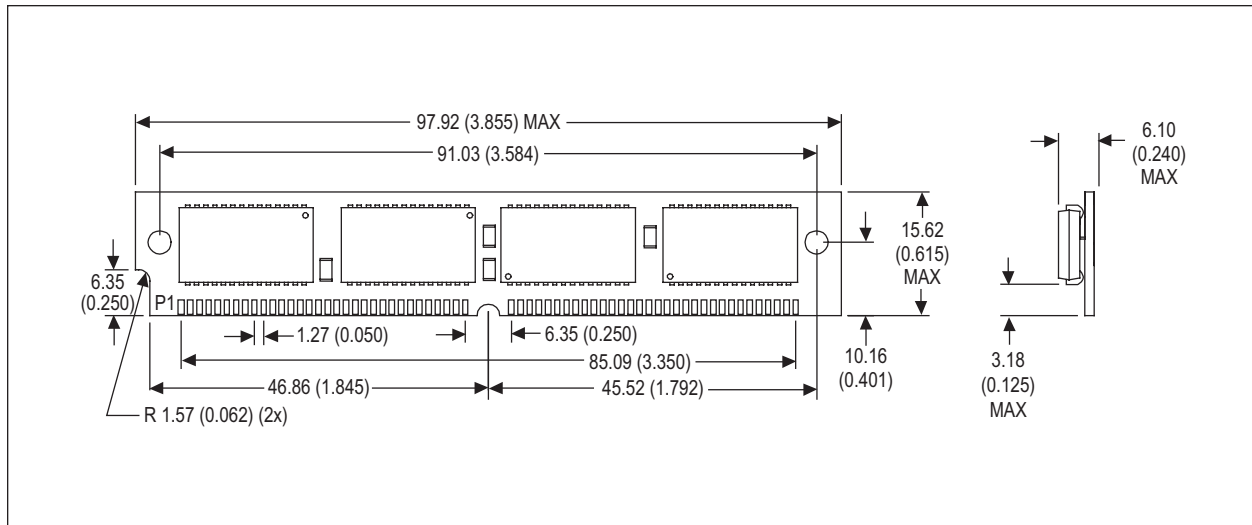


ORDERING INFORMATION FOR PACKAGE NO. 333: 64 LEAD SIMM

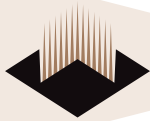
Part Number	Speed (ns)	Package No.	Package Height*
EDI8F32128C15MMC	15	333	15.62 (0.615")
EDI8F32128C20MMC	20	333	15.62 (0.615")
EDI8F32128C25MMC	25	333	15.62 (0.615")

NOTE: 1. For Gold SIMM change form EDI8F to EDI8G.

PACKAGE NO. 333: 64 LEAD SIMM



\* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

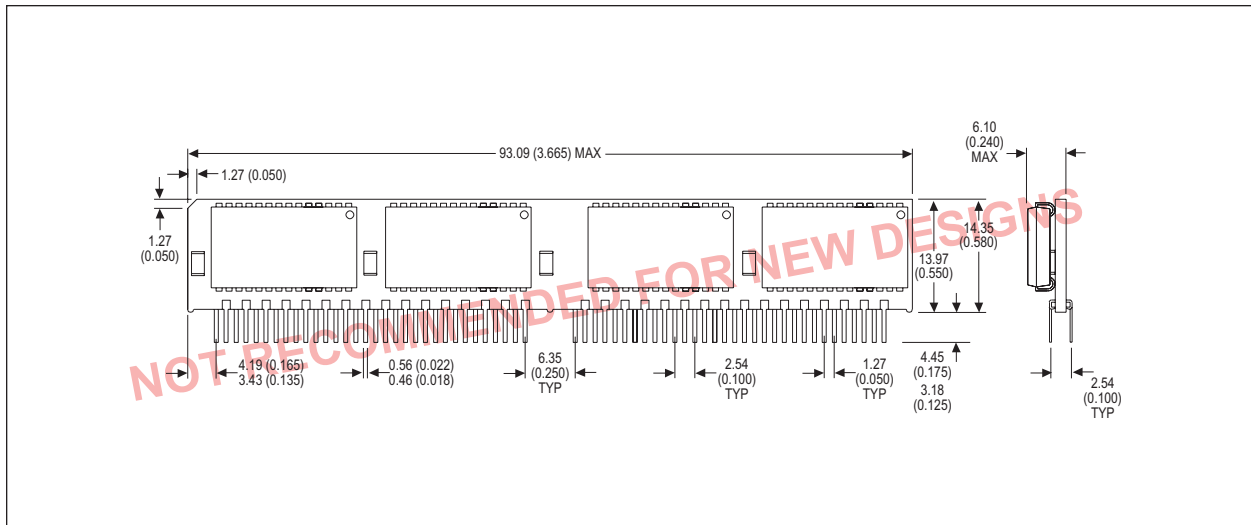


**ORDERING INFORMATION FOR PACKAGE NO. 85: 64 PIN ZIP**

Part Number	Speed (ns)	Package No.	Package Height*
EDI8F32128C15MZC	15	85	13.97 (0.550")
EDI8F32128C20MZC	20	85	13.97 (0.550")
EDI8F32128C25MZC	25	85	13.97 (0.550")

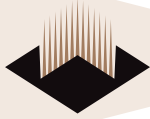
NOTE: 1. For Gold SIMM change form EDI8F to EDI8G.

**PACKAGE NO. 85: 64 PIN ZIP**



\* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)





**Document Title**

**128M x 32 Static RAM CMOS, High Speed Mode**

**Revision History**

<b>Rev #</b>	<b>History</b>	<b>Release Date</b>	<b>Status</b>
Rev 0	Created	June 2003	Advanced
Rev 1	Update on Operating Power Supply Current $I_{CC1}$ from 150mA to 780mA	May 2006	Final