

General Description

The CS5519 is a low-cost high-resolution single chip solution for APA capacitive touch screen. It is an 8-bit single cycle 8051 microcontroller with I²C Interface. The chip includes 8-bit successive approximation analog-to-digital converters with an I²C interface and multiplexer-switcher circuits for flexible measurement of analog signal from APA panel. An accurate switched-capacitor integrator is built-in and it can auto calibrate the pixel parameters for a wide range of capacitance on the touch screen (0.1pF to 4pF). On-chip capacitor can replace external component. This touch screen controller (TSC) with CMOS integration circuit provides an ideal choice for APA touch panel. The CS5519 is specified over the temperature range of -40°C to 95°C.

The CS5519 is available in QFN-7×7-56 and QFN-8×8-68 packages.

Features

- Mutual Capacitive Touch Sensing
- Dual Power Supply: 2.8V to 3.6V Operation Voltage; 1.6V to 2.0V Operation Voltage
- Up to 38/30 Drive Lines and 22/17 Sense Lines
- Dedicated Internal Two-wire Serial Control Bus I²C and UART between CS5519 and Host
- Single-end Integrator with Programmable Gain Control and Offset Control
- Multiplexed Analog Digitization with Two 8-bit Resolution Odd/Even Scan SAR ADCs and Its Dedicated 2X to 8X Accumulator XSRAM Buffers

Features (Continued)

- Single Cycle 8051 CPU Core, Maximum Operating Clock up to 24MHz from IOSC (Zero Wait State); 48MHz from IOSC(With Wait State) 4MHz to 48MHz Internal Oscillator (IOSC) 64K-byte Flash ROM 256-byte Internal SRAM and 12032-byte XSRAM
- Extra XSRAMs for AFE:
 - ◆ 896×12-bit×2 XSRAM for 8-bit SAR ADC
 - ◆ 896×8-bit XSRAM for 8-bit Parasitital Capacitor Compensator
- Two 16-bit Timers T0/T1 and One 16-bit ECT Timer T2
- One I²C Slave Controller and One I²C Master Controller Shared with the Same Port
 - ◆ With Asynchronous I²C Slave Address Detection Logic Design
- 4 General Purpose GPIO Pins
- One External Interrupt Pin
- One UART Data Transfer Output Pin
- ISP/IAP via I²C Port
- Operation Temperature Range: -40°C to 95°C
- Package Types: QFN-7×7-56 and QFN-8×8-68
- RoHS Compliance
- Operating Mode:

| Mode | Description |
|------------|--|
| Power-down | No scan with power-down mode |
| Standard | Higher scan rate when fingers are on panel, IOSC can up to 4MHz to 48MHz |

Applications

- Mobile Phones
- Personal Digital Assistants
- Smart Hand-held or Gaming Devices

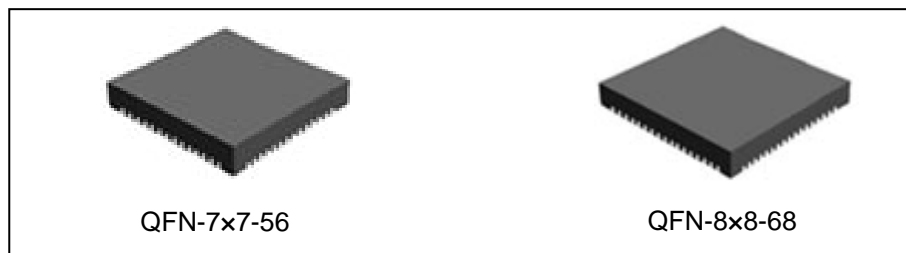


Figure 1. Package Types of CS5519

Pin Configuration

FN Package
(QFN-7x7-56)

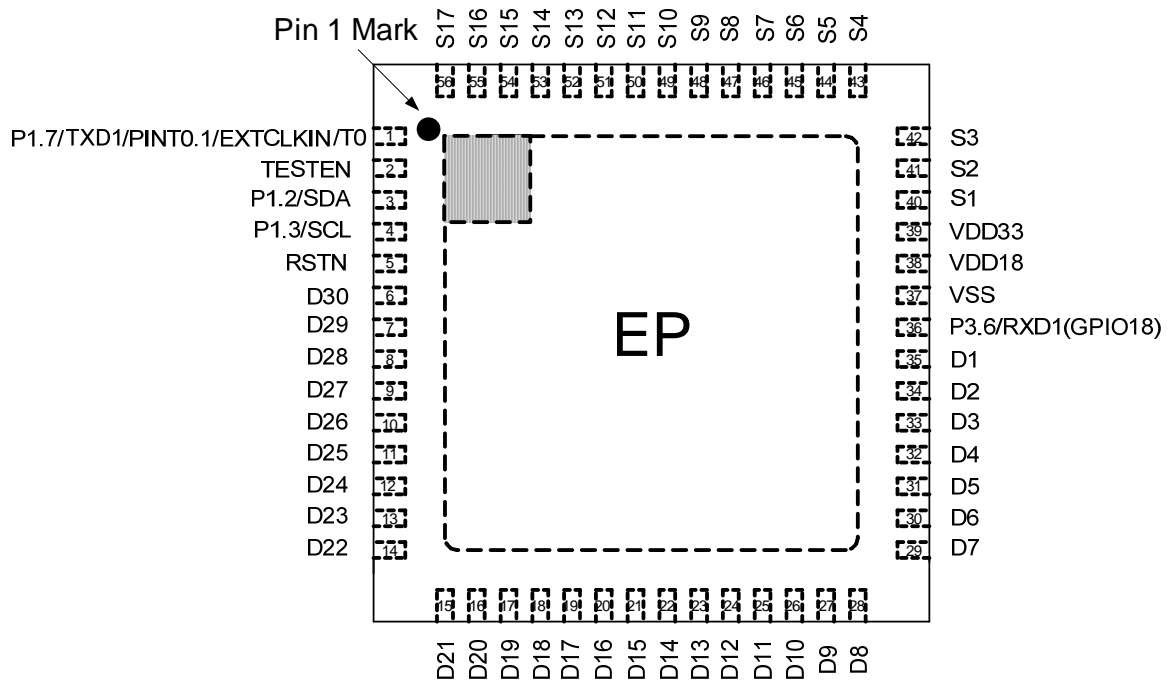


Figure 2. Pin Configuration of CS5519 (56-pin) (Top View)

Pin Configuration (Continued)

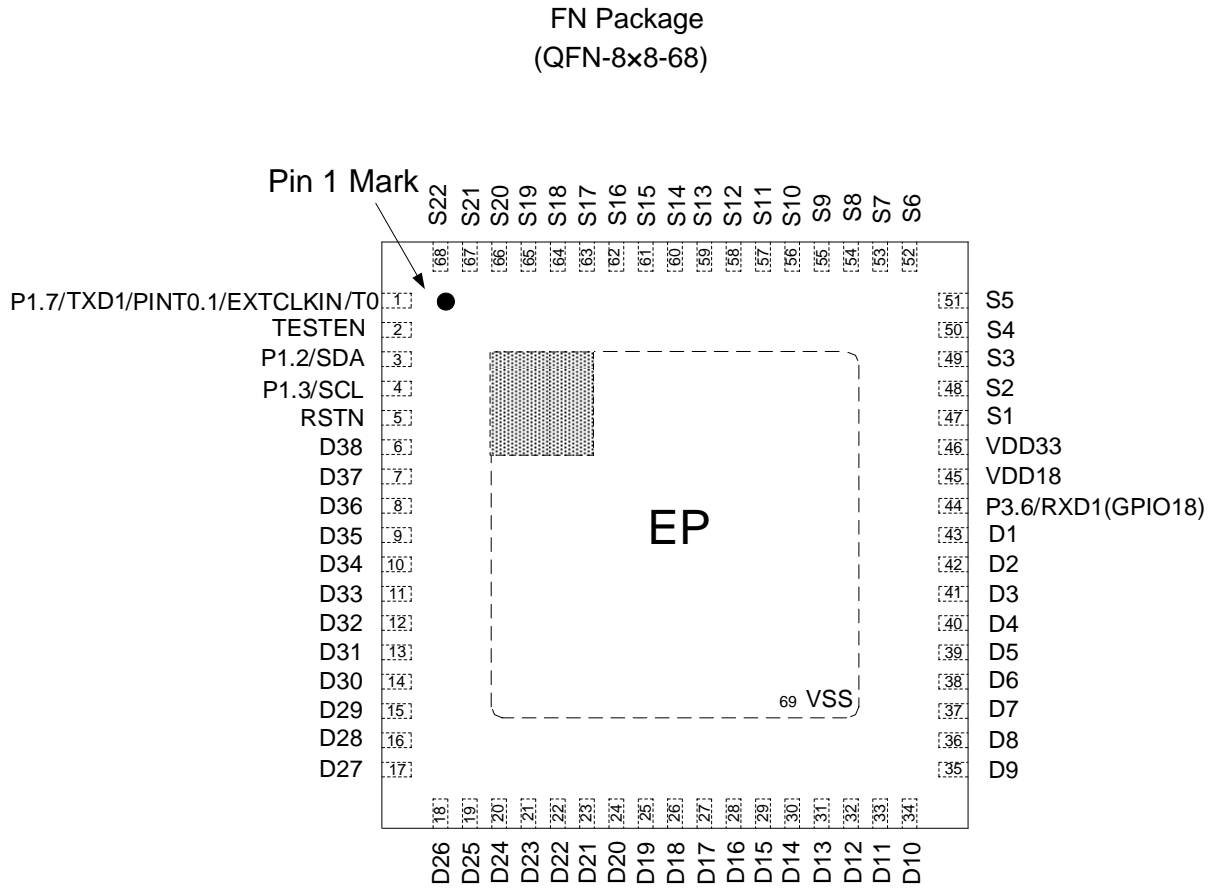


Figure 3. Pin Configuration of CS5519 (68-pin) (Top View)

Pin Description

| Pin Number | | Pin Name | Pin Type | Pin Function |
|----------------|----------------|---|----------|---|
| QFN-7×7 -56 | QFN-8×8 -68 | | | |
| 1 | 1 | P1.7/ TXD1/ PINT0.1/ EXTCLKIN/ T0 | I/O | Port 1.7 GPIO 8051 P1.7 GPIO TXD1 This pin also can be configured as TXD of UART 1 PINT0.1 This pin also can be configured as the expanded INTO interrupt External Clock Input External clock input source. T0 Timer 0 Input This pin also can be configured as Timer 0 input |
| 2 | 2 | TESTEN | I | Test Mode Enable High Active This pin has an internal weakly pull low resistor connected. If it is connected high, the chip enters into Test Mode condition |
| 3 | 3 | P1.2/SDA (open-drain) | I/O | Port 1.2 GPIO 8051 P1.2 GPIO SDA This pin also can be configured as the SDA signal of the I2C master or I2C slave controller. In this operation mode, this pin should also be configured as bi-directional I/O with open-drain output |
| 4 | 4 | P1.3/SCL (open-drain) | I/O | Port 1.3 GPIO 8051 P1.3 GPIO SCL This pin also can be configured as the SCL signal of the I ² C master or I ² C slave controller. In I ² C master mode, this pin should be configured as open-drain output. In I ² C slave, this pin should be configured as input only |
| 5 | 5 | RSTN | I | Reset Low Active Typically connect a resistor to VDD18 and a capacitor to VSS Low asserted and threshold at $0.5 \times V_{DD18}$. When forced low, the chip enters into reset condition This pin should not be connected to any level above V_{DD18} |



Pin Description (Continued)

| Pin Number | | Pin Name | Pin Type | Pin Function |
|----------------|----------------|-------------------------------|----------|---|
| QFN-7×7 -56 | QFN-8×8 -68 | | | |
| - | 6 to 13 | D38 to D31 | O, A | D38, D37, D36, D35, D34, D33, D32, D31 Driving line 38 to line 31 |
| 6 to 35 | 14 to 43 | D30 to D1 | O, A | D30, D29, D28, D27, D26, D25, D24, D23, D22, D21, D20, D19, D18, D17, D16, D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1 Driving line 30 to line 1 |
| 36 | 44 | P3.6/ RXD1 (open-drain) | I/O | Port 3.6 GPIO 8051 P3.6 GPIO This pin should be configured as open-drain output and the input range can be 1.8V to 3.3V RXD1 This pin also can be configured as RXD of UART 1 |
| 37 | 69 | VSS | Power | Ground Voltage. 0V |
| 38 | 45 | VDD18 | Power | Internal Regulator Output. 1.6V to 2.0V Typical decoupling capacitors of 0.1μF and 10μF should be connected between VDD18 and VSS |
| 39 | 46 | VDD33 | Power | Supply Voltage. 2.8V to 3.6V A good decoupling capacitor between VDD33 and VSS is critical for good performance |
| 40 to 56 | 47 to 63 | S1 to S17 | I, A | S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12, S13, S14, S15, S16, S17 Sensing line 1 to line 17 |
| - | 64 to 68 | S18 to S22 | I, A | S18, S19, S20, S21, S22 Sensing line 18 to line 22 |

Functional Block Diagram

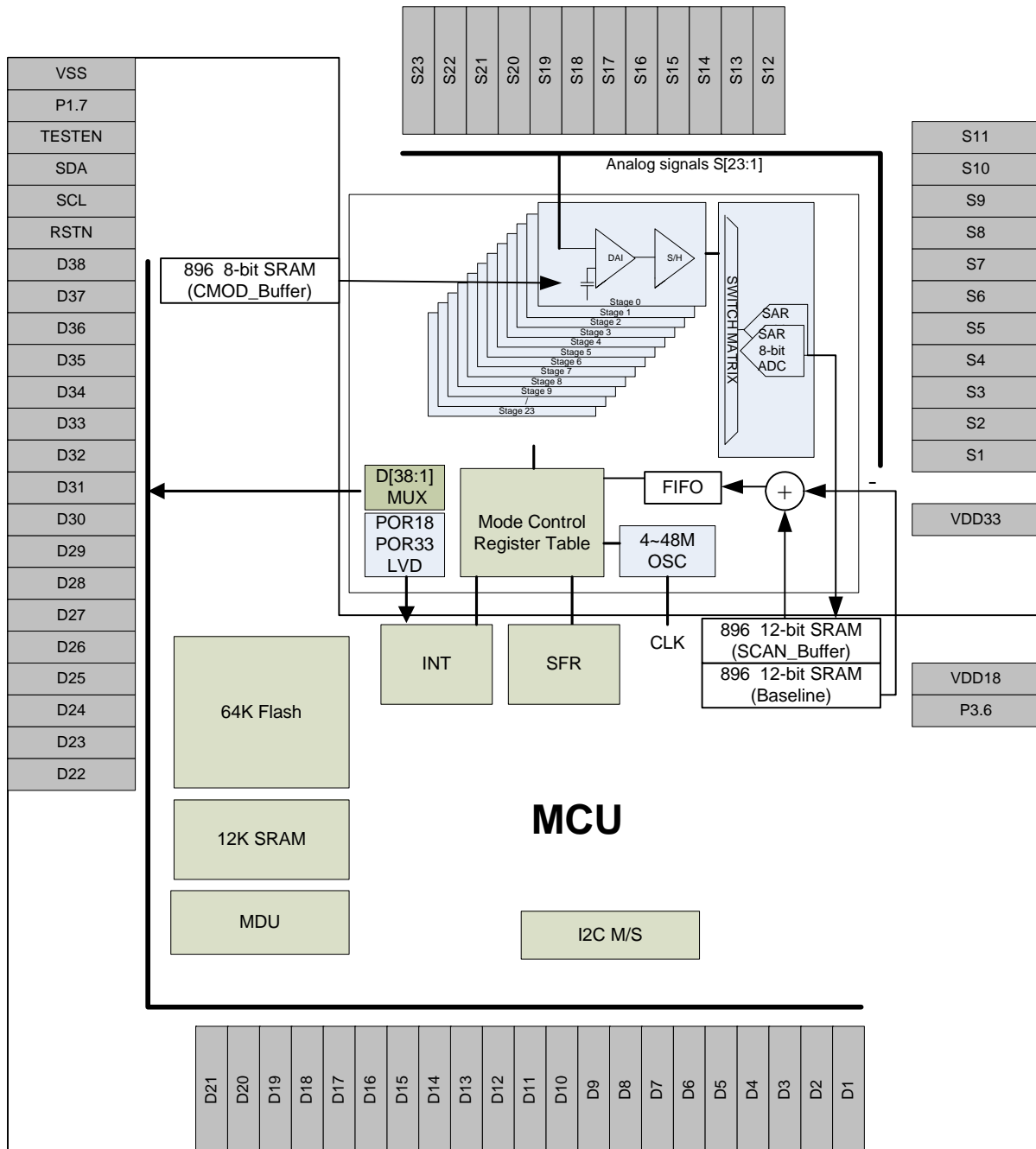
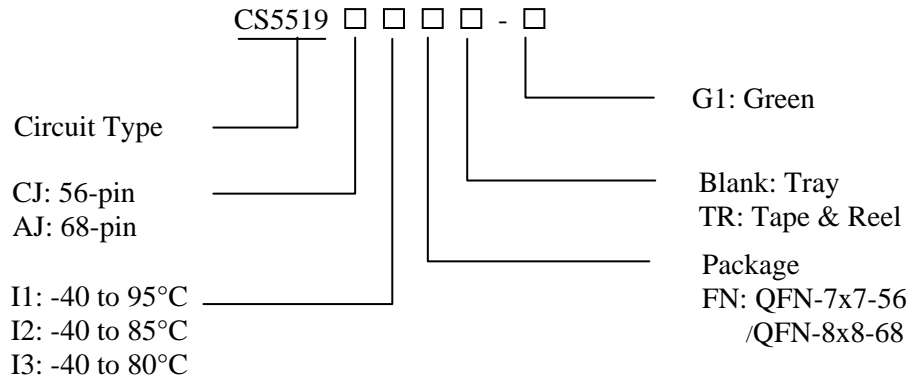


Figure 4. Main AFE I/O Pin Assignment and Whole Chip's Functional Block Diagram

Ordering Information



| Package | Temperature Range | Part Number | Marking ID | Packing Type |
|------------|-------------------|-------------------|-------------|--------------|
| QFN-7x7-56 | -40 to 95°C | CS5519CJI1FN-G1 | CS5519CJ-I1 | Tray |
| | | CS5519CJI1FNTR-G1 | CS5519CJ-I1 | Tape & Reel |
| | -40 to 85°C | CS5519CJI2FN-G1 | CS5519CJ-I2 | Tray |
| | | CS5519CJI2FNTR-G1 | CS5519CJ-I2 | Tape & Reel |
| | -40 to 80°C | CS5519CJI3FN-G1 | CS5519CJ-I3 | Tray |
| | | CS5519CJI3FNTR-G1 | CS5519CJ-I3 | Tape & Reel |
| QFN-8x8-68 | -40 to 95°C | CS5519AJI1FN-G1 | CS5519AJ-I1 | Tray |
| | | CS5519AJI1FNTR-G1 | CS5519AJ-I1 | Tape & Reel |
| | -40 to 85°C | CS5519AJI2FN-G1 | CS5519AJ-I2 | Tray |
| | | CS5519AJI2FNTR-G1 | CS5519AJ-I2 | Tape & Reel |
| | -40 to 80°C | CS5519AJI3FN-G1 | CS5519AJ-I3 | Tray |
| | | CS5519AJI3FNTR-G1 | CS5519AJ-I3 | Tape & Reel |

BCD Semiconductor's Pb-free products, as designated with "G1" in the part number, are RoHS compliant and green.

**Enhanced Multi-touch Capacitive Touch Screen Controller****CS5519****CS5519 Support 7" to 13" Touch Panel, Listed Below:**

| PN | TX/ RX | Multi - Touch | Package | Panel size |
|--------|--------|----------------|------------|------------|
| CS5519 | 30/17 | 10 point 100HZ | QFN-7x7-56 | 7" to 10" |
| | 38/22 | 10 point 100HZ | QFN-8x8-68 | 8" to 13" |

Absolute Maximum Ratings (Note 1)

| Parameter | Symbol | Value | Unit |
|-----------------------------------|------------|----------------------|------|
| Supply Voltage 1 | V_{DD} | 2.8 to 3.6 | V |
| Supply Voltage 2 | V_{DD18} | 1.6 to 2.0 | V |
| Analog Input Voltage (Other pins) | V_{DDA} | -0.3 to $V_{DD}+0.3$ | V |
| Logic Input Voltage | V_{DDD} | -0.3 to $V_{DD}+0.3$ | V |
| Power Dissipation | P_D | 250 | mW |
| Maximum Junction Temperature | T_J | 100 | °C |
| Operating Temperature | T_{OP} | -40 to 95 | °C |
| Storage Temperature | T_{STG} | -65 to 150 | °C |

Note 1: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.



Enhanced Multi-touch Capacitive Touch Screen Controller

CS5519

Electrical Characteristics

DA/AC Characteristics for AFE

T_A=-40°C to 95°C, V_{DD}=3.3V, I²C bus frequency=400kHz, unless otherwise noted.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------------------|-------------------|---|-----------------------|------|------------------------|------|
| ADC DC Accuracy | | | | | | |
| Resolution | | | | | 8 | Bits |
| No Missing Codes | | Standard/Fast | 6 | 8 | | Bits |
| Integral Linearity Error | INL | Standard/Fast | | ±2 | | LSB |
| Differential Linearity Error | DNL | External V _{REF} | | ±1 | | LSB |
| Offset Error | | | | ±2 | | LSB |
| Gain Error | | | | ±1 | | LSB |
| Analog Input | | | | | | |
| Full-scale Input Span | | | 0 | | V _{DD} | V |
| Absolute Input Range | | | -0.2 | | V _{DD} +0.2 | V |
| ADC Sampling Dynamics | | | | | | |
| Throughput Rate | | | | 500 | | ksps |
| Reference Input | | | | | | |
| Input Voltage Range | | | 1.8 | | V _{DD} | V |
| Switched-capacitor Integrator | | | | | | |
| Output Voltage Range | | | 0.3 | | V _{DD} -0.3 | V |
| Integrator Capacitor | C _{INT} | | | 12 | | pF |
| Digital Input/Output | | | | | | |
| Logic Family | | | | CMOS | | |
| Input High Voltage | V _{IH} | | 0.7×V _{DD} | | V _{DD} +0.3 | V |
| Input Low Voltage | V _{IL} | | -0.3 | | 0.3×V _{DD} | V |
| Output High Voltage | V _{OH} | | 0.8×V _{DD} | | | V |
| Output Low Voltage | V _{OL} | | | | 0.4 | V |
| Input High Voltage for P3.6 (GPIO18) | V _{IH18} | | 0.7×V _{DD18} | | V _{DD18} +0.3 | V |
| Input Low Voltage for P3.6 (GPIO18) | V _{IL18} | | -0.3 | | 0.3×V _{DD18} | V |
| Output High Voltage for P3.6 (GPIO18) | V _{OH18} | | 0.8×V _{DD18} | | | V |
| Output Low Voltage for P3.6 (GPIO18) | V _{OL18} | | | | 0.2×V _{DD18} | V |
| Power Supply | | | | | | |
| Supply Voltage | V _{DD} | Operating voltage | 2.8 | | 3.6 | V |
| Quiescent Current | | Standard mode: IOSC=4MHz to 48MHz | | TBD | | mA |
| | | Power-down mode | | 10 | | µA |
| Temperature Range | | | | | | |
| Specified Performance | | | -40 | | 95 | °C |

**Electrical Characteristics (Continued)****DA/AC Characteristics for AFE** $T_A = -40^{\circ}\text{C}$ to 95°C , $V_{DD} = 3.3\text{V}$, I²C bus frequency = 400kHz, unless otherwise noted.

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--------------------------------|----------------------|-----------------------------|-----------|-----|----------|---------------|
| 3.3V-to-1.8V LDO | | | | | | |
| Internal 1.8V Regulator Output | V_{DD18} , 15mA | | 1.6 | 1.8 | 2.0 | V |
| Output Voltage Trimming Level | | | -2/4/6 | 0 | 2/4/6 | % |
| Internal OSC | | | | | | |
| Frequency | | | 4 | | 48 | MHz |
| Operating Current | | Operating frequency = 12MHz | | 50 | | μA |
| Frequency Trimming Level | | | -10/20/30 | 0 | 10/20/30 | % |

**Enhanced Multi-touch Capacitive Touch Screen Controller****CS5519****Electrical Characteristics (Continued)****DA/AC Characteristics for 8051 CPU Core, Digital GPIO pins, Digital Peripherals, and IOSC**T_A=-40°C to 95°C, V_{DD}=2.8V to 3.6V, unless otherwise noted.

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|--------------------------------|------|------|------|------|------|
| Power Supply Current | | | | | | |
| Normal Mode Supply Current Using IOSC up to 48MHz | I _{DD} , normal IOSC1 | | | 25 | mA | 2 |
| Normal Mode Supply Current Using IOSC=4MHz | I _{DD} , normal IOSC2 | | 2.9 | | mA | 2 |
| PMM Mode Supply Current Using IOSC up to 48MHz | I _{DD} , PMM IOSC1 | | 6 | | mA | 2 |
| PMM Mode Supply Current Using IOSC=4MHz | I _{DD} , PMM IOSC2 | | 1.5 | | mA | 2 |
| Idle Mode Supply Current Using IOSC up to 48MHz | I _{DD} , idle IOSC1 | | 3 | | mA | 2 |
| Stop Mode Supply Current Using IOSC Keeps Low | I _{DD} , stop | | 3 | | μA | 2 |
| Digital GPIO Characteristics | | | | | | |
| Input High Voltage | V _{IH} | 2 | | 3.6 | V | 3 |
| Input Low Voltage | V _{IL} | -0.3 | | 0.8 | V | 3 |
| Output High Voltage | V _{OH} | 2.4 | | | V | 3 |
| Output Low Voltage | V _{OL} | | | 0.4 | V | 3 |
| High Level Output Current @V _{OH} (min) | I _{OH} (2mA) | 3.0 | 7.87 | 12.9 | mA | |
| | I _{OH} (4mA) | 7.7 | 15.6 | 25.8 | mA | |
| Low Level Output Current @V _{OL} (max) | I _{OL} (2mA) | 3.4 | 5.4 | 7.4 | mA | |
| | I _{OL} (4mA) | 6.7 | 10.7 | 14.7 | mA | |
| Input Pull Up Resistance | R _{PU} | 34 | | 74 | kΩ | 3 |
| Input Pull Down Resistance | R _{PD} | 29 | | 86 | kΩ | 3 |
| Input Low to High Level, RSTN | V _{IH} , RSTN | 0.85 | | 0.93 | V | 4 |
| Input High to Low Level, RSTN | V _{IL} , RSTN | 0.63 | | 0.71 | V | 4 |
| Output Rise Time | t _{RISE} | | 5 | | ns | 7 |
| Output Fall Time | t _{FALL} | | 5 | | ns | 7 |
| Internal 3.3V-to-1.8V LDO from AFE | | | | | | |
| Internal 1.8V Regulator Output | V _{DD18} , 15mA | 1.6 | 1.8 | 2.0 | V | 5 |
| Power On/Off Reset Level | V _{DD18} , Reset | 80 | 85 | 90 | % | 6 |

Note 2: Does not include load current and tested under NOP loop and all peripheral disabled.

Note 3: For Digital I/O only.

Note 4: For RSTN pin only.

Note 5: Supply to internal digital and analog circuit only.

Note 6: This is measured as the percentage of steady state value of V_{DD18}.

Note 7: This is measured with 20pF load and 20% to 80% output level.

Enhanced Multi-touch Capacitive Touch Screen Controller

CS5519

Typical Application

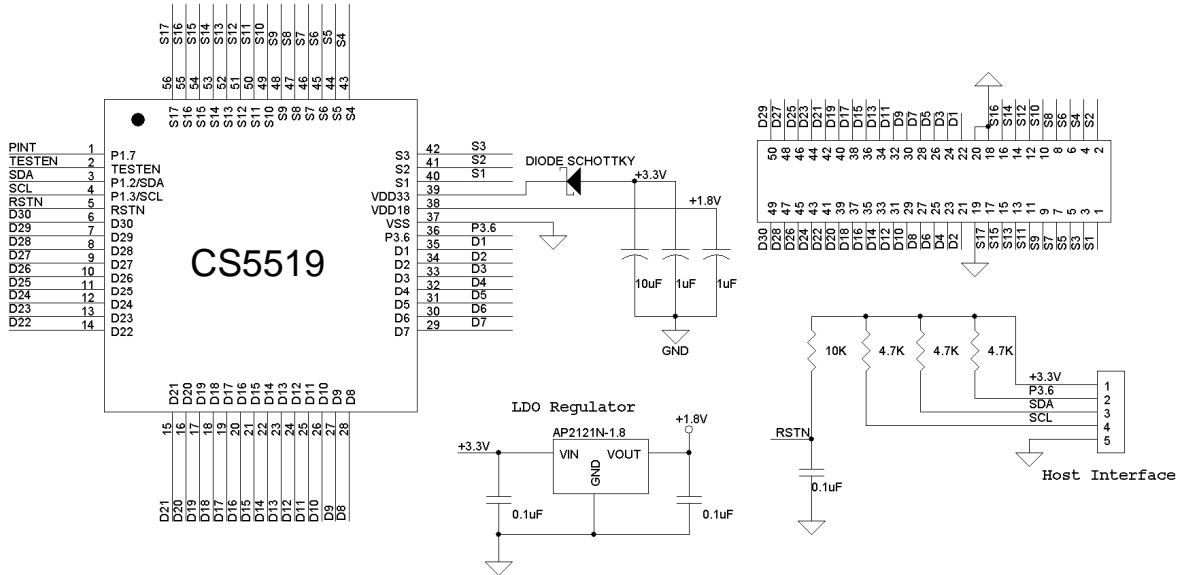


Figure 5. Typical Application Schematic of CS5519 (For QFN-7x7-56 Package)

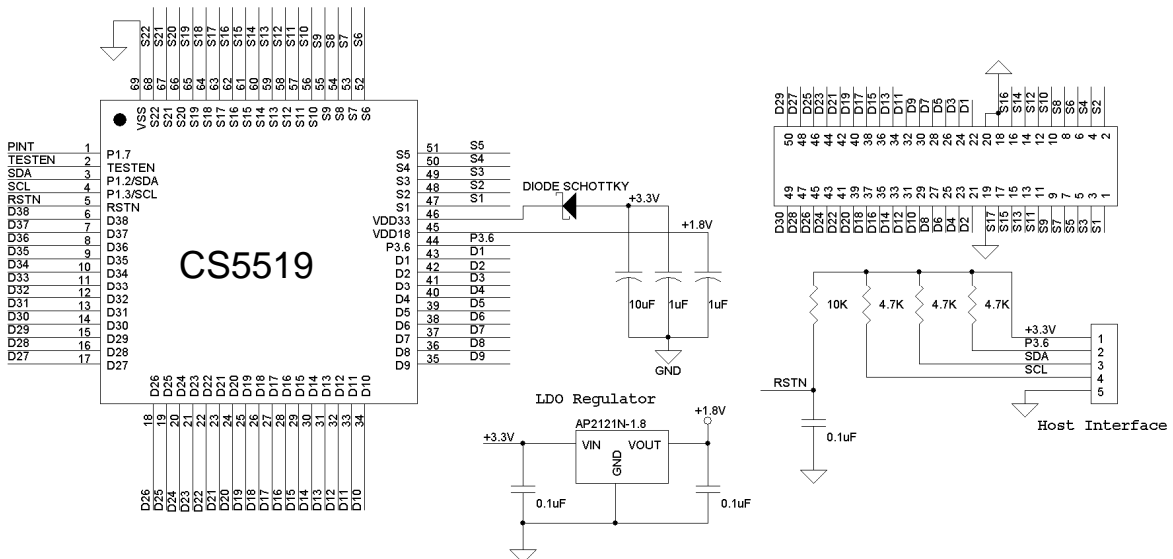
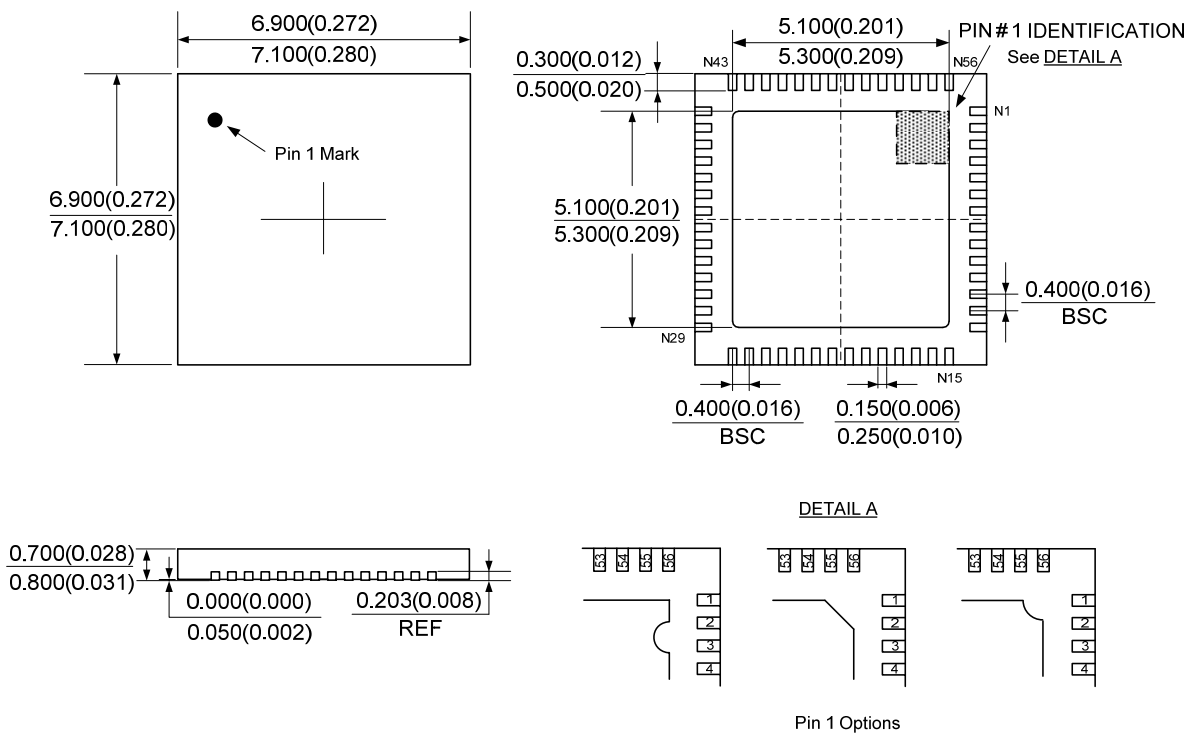


Figure 6. Typical Application Schematic of CS5519 (For QFN-8x8-68 Package)

Mechanical Dimensions

QFN-7x7-56

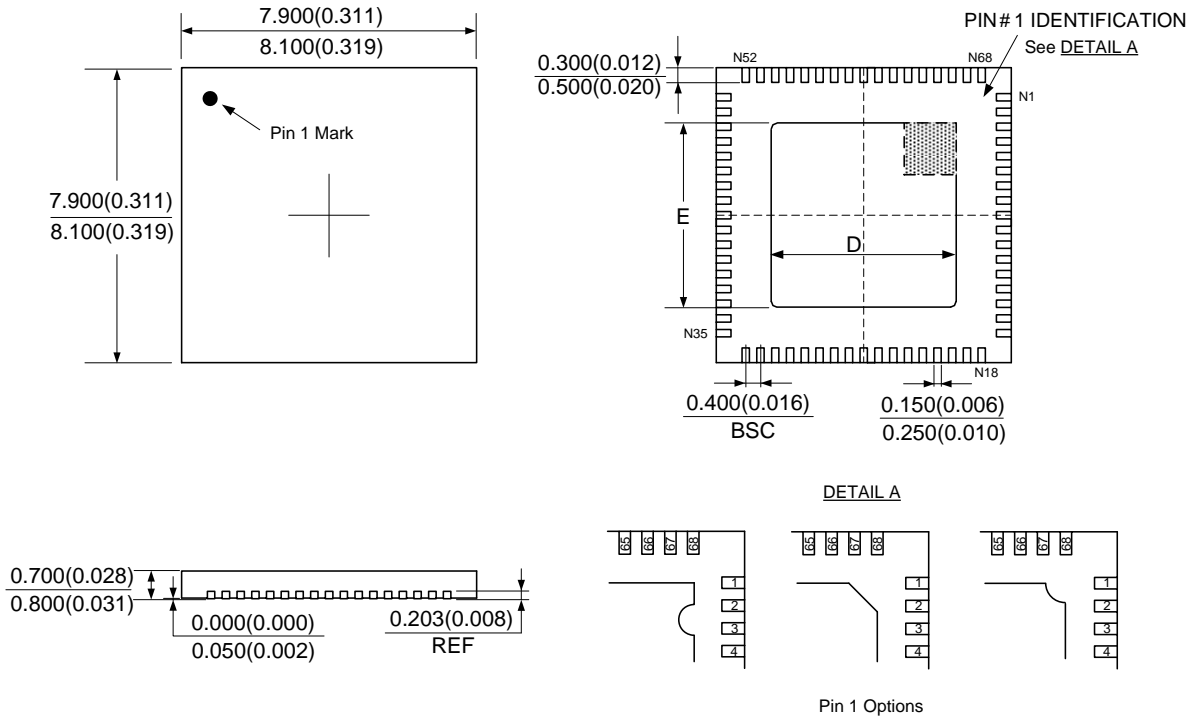
Unit: mm(inch)



Mechanical Dimensions (Continued)

QFN-8x8-68

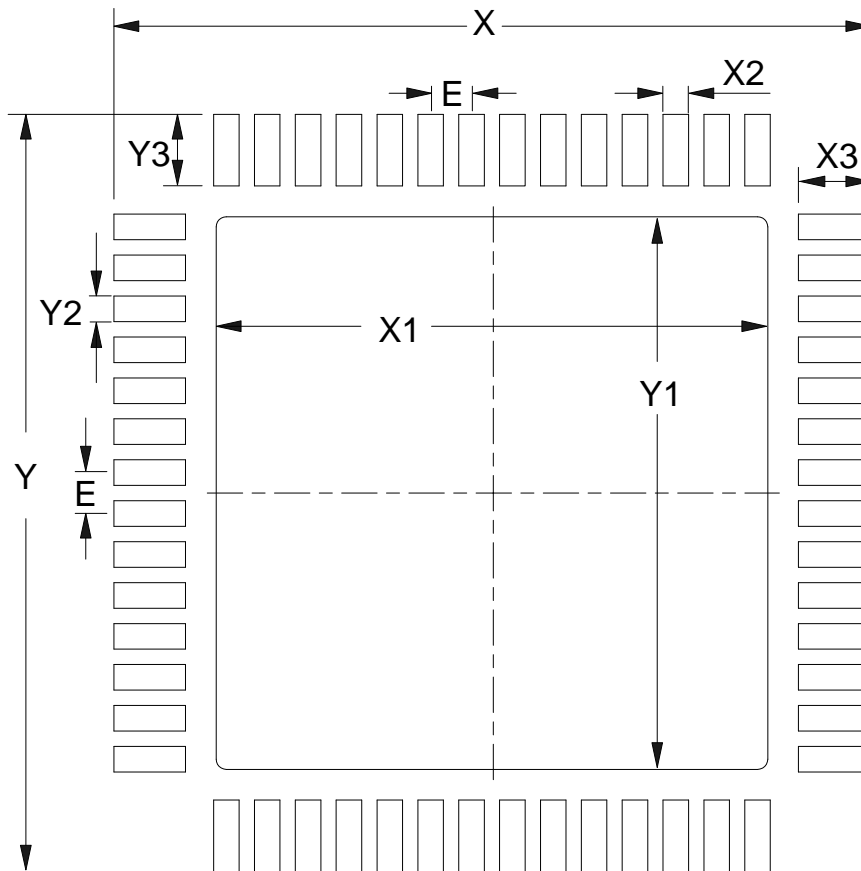
Unit: mm(inch)



| Symbol | D | | | | E | | | |
|---------|---------|---------|-----------|-----------|---------|---------|-----------|-----------|
| | min(mm) | max(mm) | min(inch) | max(inch) | min(mm) | max(mm) | min(inch) | max(inch) |
| Option1 | 4.300 | 4.500 | 0.169 | 0.177 | 4.300 | 4.500 | 0.169 | 0.177 |
| Option2 | 5.400 | 5.600 | 0.213 | 0.220 | 5.400 | 5.600 | 0.213 | 0.220 |
| Option3 | 6.100 | 6.300 | 0.240 | 0.248 | 6.100 | 6.300 | 0.240 | 0.248 |

Mounting Pad Layout

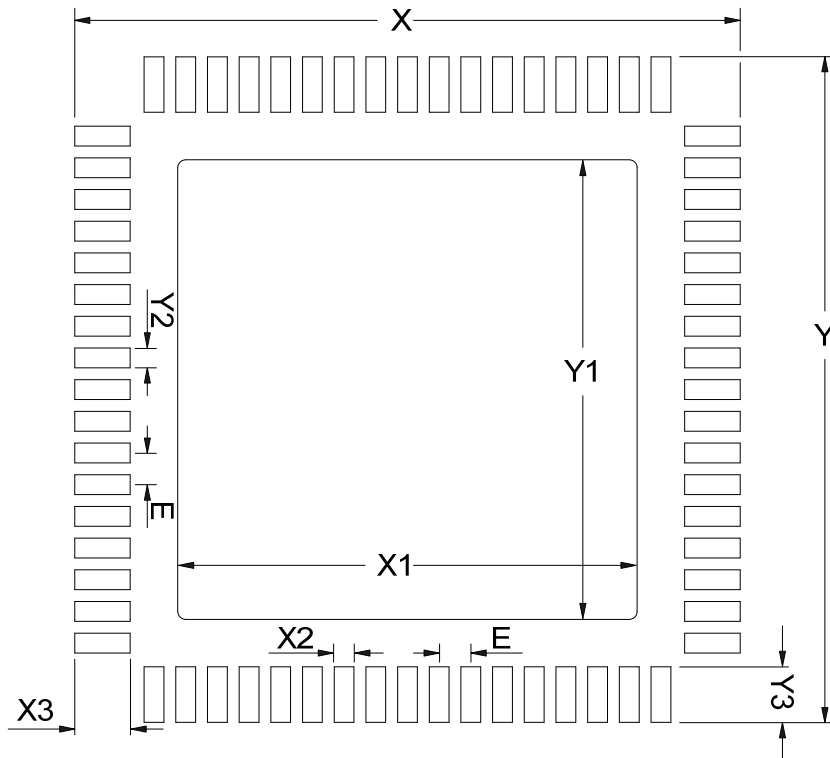
QFN-7x7-56



| Dimensions | X=Y (mm)/(inch) | X1=Y1 (mm)/(inch) | X2=Y2 (mm)/(inch) | X3=Y3 (mm)/(inch) | E (mm)/(inch) |
|------------|--------------------|----------------------|----------------------|----------------------|------------------|
| Value | 7.400/0.291 | 5.400/0.213 | 0.250/0.010 | 0.700/0.028 | 0.400/0.016 |

Mounting Pad Layout (Continued)

QFN-8x8-68



| Dimensions | X=Y (mm)/(inch) | X1=Y1 (mm)/(inch) | X2=Y2 (mm)/(inch) | E (mm)/(inch) | X3=Y3 (mm)/(inch) |
|------------|--------------------|----------------------|----------------------|------------------|----------------------|
| Option1 | 8.400/0.331 | 4.700/0.185 | 0.250/0.010 | 0.400/0.016 | 0.700/0.028 |
| Option2 | 8.400/0.331 | 5.800/0.228 | 0.250/0.010 | 0.400/0.016 | 0.700/0.028 |
| Option3 | 8.400/0.331 | 6.500/0.256 | 0.250/0.010 | 0.400/0.016 | 0.700/0.028 |



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