

SN8000/SN8000UFL

Wi-Fi Module

Datasheet

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Revision History

Revision	Date	Author	Change Description
1.0	11/08/13	R. Willett	Initial version
1.1	11/25/13	R Willett	Removed SyChip logo; revised copyright notice; revised tech support information; deleted Chap 12 "Disclaimer;" deleted one referenced document, 1.4 – Reference, page 6; revised Table 14, page 20;

Table of Contents

1	SYSTEM DESCRIPTIONS	5
1.1	APPLICATIONS	5
1.2	BLOCK DIAGRAM	6
1.3	ACRONYMS.....	6
1.4	REFERENCE	6
2	MECHANICAL SPECIFICATIONS	7
2.1	MODULE DIMENSION (SN8000 / SN8000UFL).....	7
2.2	MODULE TOP AND SIDE VIEW	7
2.3	PCB FOOTPRINT (TOP VIEW).....	8
2.4	MODULE PIN-OUT.....	9
3	DC ELECTRICAL SPECIFICATIONS	11
3.1	TYPICAL POWER CONSUMPTION.....	11
3.2	POWER UP/DOWN SEQUENCE.....	12
3.3	GPIO INTERFACE	12
3.4	SDIO INTERFACE	13
3.4.1	SDIO Timing (Default Mode).....	14
3.4.2	SDIO Timing (High Speed Mode)	15
3.5	GSPI INTERFACE.....	16
4	RF SPECIFICATIONS	17
4.1	DC/RF CHARACTERISTICS FOR IEEE 802.11B	17
4.2	DC/RF CHARACTERISTICS FOR IEEE 802.11G	18
4.3	DC/RF CHARACTERISTICS FOR IEEE 802.11N	19
5	ANTENNA INFORMATION	20
6	ENVIRONMENTAL SPECIFICATIONS	20
6.1	ABSOLUTE MAXIMUM RATINGS	20
6.2	RECOMMENDED OPERATING CONDITIONS.....	20
7	PACKAGING AND MARKING INFORMATION	21
7.1	CARRIER TAPE DIMENSIONS.....	21
7.2	MODULE MARKING INFORMATION	22
8	ORDERING INFORMATION	22
9	ROHS DECLARATION	22
10	REGULATORY INFORMATION	23
11	TECHNICAL SUPPORT CONTACT	24

LIST OF FIGURES

FIGURE 1 SN8000/8000UFL MODULE BLOCK DIAGRAM.....	6
FIGURE 2 SN8000 TOP AND SIDE VIEW	7
FIGURE 3 SN8000UFL TOP AND SIDE VIEW.....	8
FIGURE 4 DETAILED PAD DIMENSIONS (FOR BOTH SN8000 AND SN8000UFL) (TOP VIEW)	8
FIGURE 5 BOOT-UP SEQUENCE	12
FIGURE 6 SDIO CONNECTION.....	13
FIGURE 7 SDIO TIMING (DEFAULT MODE).....	14
FIGURE 8 SDIO TIMING (HIGH SPEED MODE)	15
FIGURE 9 GSPI SIGNAL TIMING	16
FIGURE 10 GSPI INTERFACE	16
FIGURE 11 CARRIER TAPE DIMENSIONS	21
FIGURE 12 SN8000 PIN1 ORIENTATION.....	21
FIGURE 13 MODULE MARKING DETAIL	22

LIST OF TABLES

TABLE 1 MODULE CONNECTOR SIGNAL DESCRIPTION	9
TABLE 2 TYPICAL POWER CONSUMPTION FOR SN8000	11
TABLE 3 TYPICAL POWER CONSUMPTION FOR SN8000UFL.....	11
TABLE 4 DIGITAL I/O REQUIREMENTS.....	12
TABLE 5 SDIO PIN DESCRIPTION	13
TABLE 6 SDIO INTERFACE TIMING DEFAULT.....	14
TABLE 7 SDIO TIMING - HIGH SPEED.....	15
TABLE 8 SDIO PIN DESCRIPTION – GSPI MODE.....	16
TABLE 9 RF CHARACTERISTICS FOR IEEE 802.11B.....	17
TABLE 10 RF CHARACTERISTICS FOR IEEE 802.11G.....	18
TABLE 11 RF CHARACTERISTICS FOR IEEE 802.11N.....	19
TABLE 12 EXTERNAL ANTENNA TO COMPLY WITH REGULATION (ONLY SN8000UFL).....	20
TABLE 13 ABSOLUTE MAXIMUM RATING	20
TABLE 14 RECOMMENDED OPERATING CONDITIONS	20
TABLE 15 ORDERING INFORMATION	22

1 System Descriptions

SN8000/SN8000UFL

Wi-Fi Module



1.1 Applications

The SN8000 is a certified 2.4 GHz IEEE 802.11b/g/n Wi-Fi module based on the Broadcom BCM43362 chipset. It is designed to fit indoor and outdoor sensor and control applications. The SN8000 integrates a Wi-Fi IC, RF front end, temperature compensated crystal (TCXO) and an on-board antenna.

The SN8000 is compatible with Broadcom WICED™ SDK software to support low power, low cost microcontroller platforms from STM32 ARM Cortex M3 and M4 families.

The SN8000 module is an ideal solution for home automation, industrial control, Smart Energy, medical, and healthcare applications with or without cloud services.

A footprint compatible version with U.FL connector, SN8000UFL, is also available for use with an external antenna.

Module Summary

- 2.4GHz IEEE 802.11b/g/n radio technology
- Dimension: 24.0 mm × 11.4 mm × 2.0mm
- Antenna Configuration: On-board chip antenna or U.FL connector
- Transmit power: +18.5 dBm @ 802.11b
- Receive sensitivity: -96dBm
- Host interface: SDIO, SPI
- Operating temperature range: -40°C to 85°C
- RoHS2 compliant
- MSL Level 3
- FCC/IC certified; ETSI compliant
- Compatible with Broadcom WICED™ SDK

1.2 Block Diagram

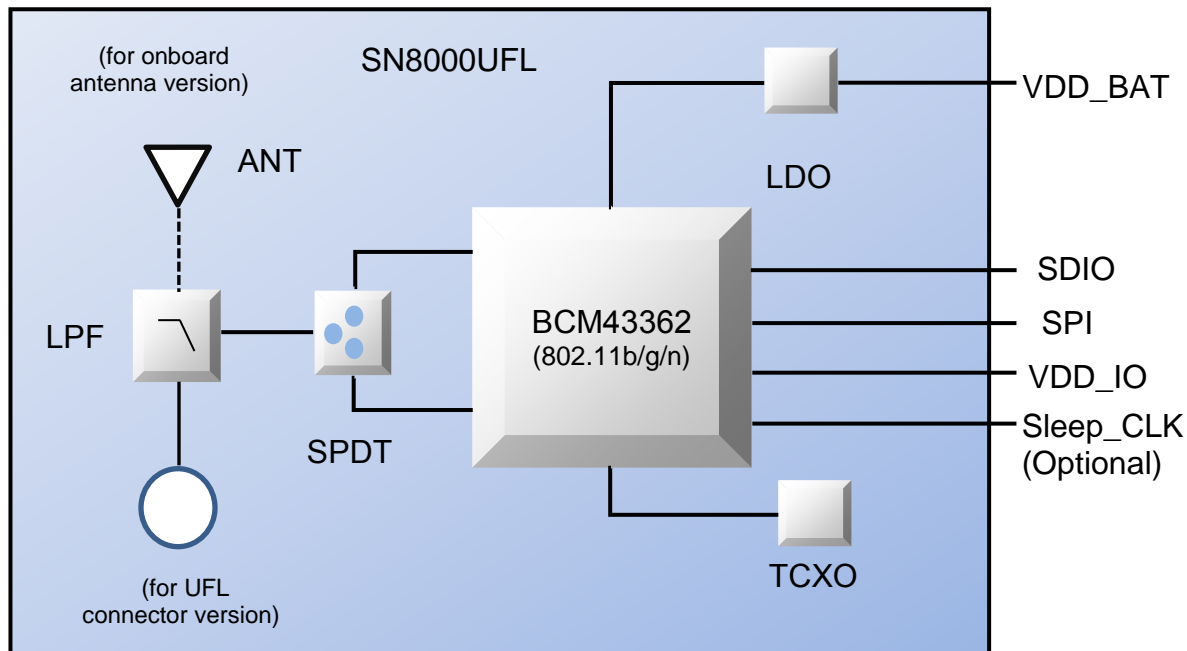


Figure 1 SN8000/8000UFL Module Block Diagram

1.3 Acronyms

ISM	Industrial, Scientific and Medical
MAC	Medium Access Control
MSL	Moisture Sensitivity Level
PER	Packet Error Rate
ROHS	Restriction of Hazardous Substances
SPI	Serial Peripheral Interface
SDIO	Secure Digital Input Output

1.4 Reference

- [1] SN8000/SN8000UFL Wi-Fi Module User Manual, Murata

2 Mechanical Specifications

2.1 Module dimension (SN8000 / SN8000UFL)

Parameter	Typical	Units
Dimension (LxWxH)	24.0 x 11.4 x 2.0	mm
Dimension tolerances (LxWxH)	$\pm 0.2/\pm 0.2/\pm 0.15$	mm

2.2 Module top and side view

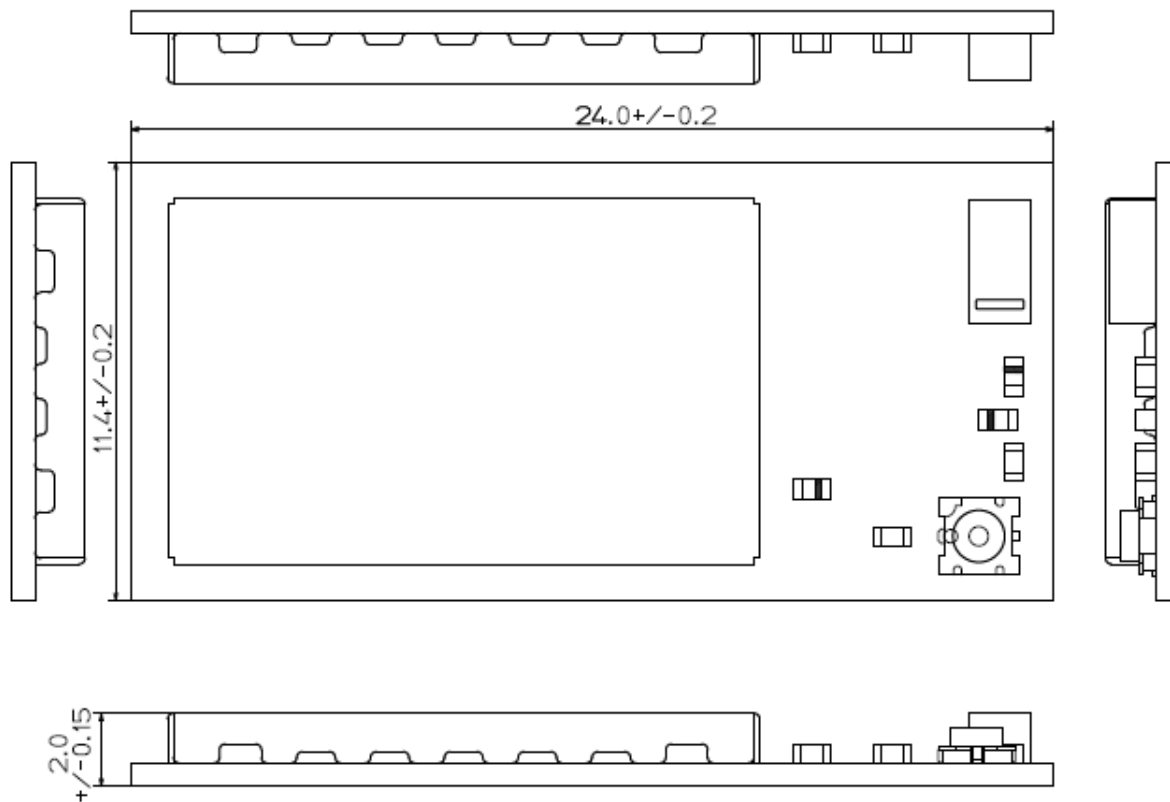


Figure 2 SN8000 Top and Side View

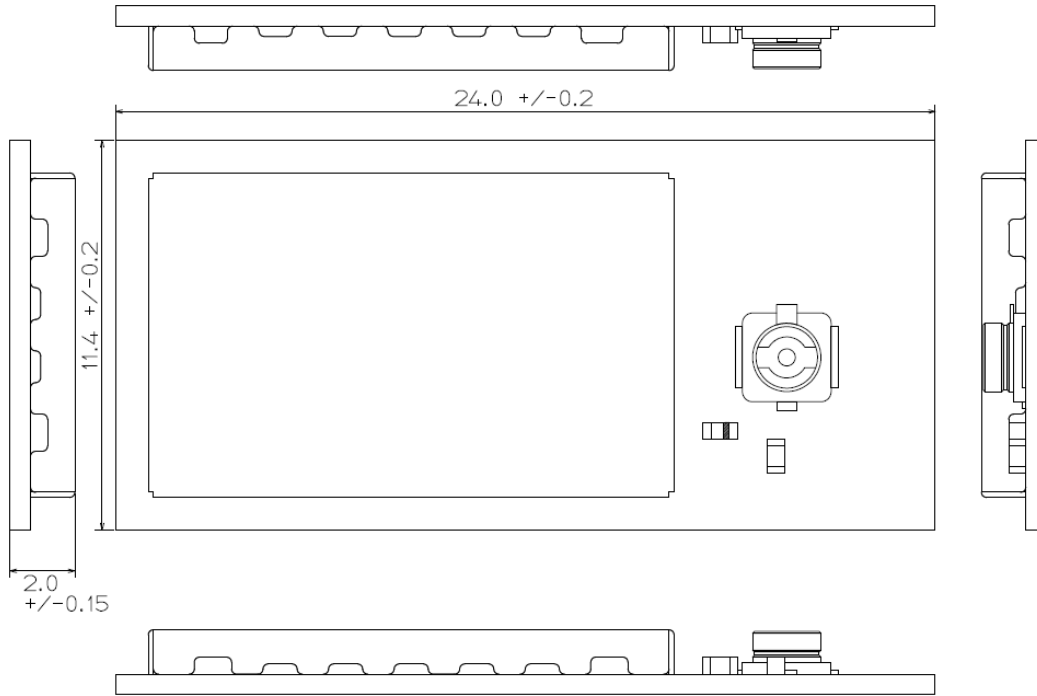


Figure 3 SN8000UFL Top and Side View

2.3 PCB footprint (top view)

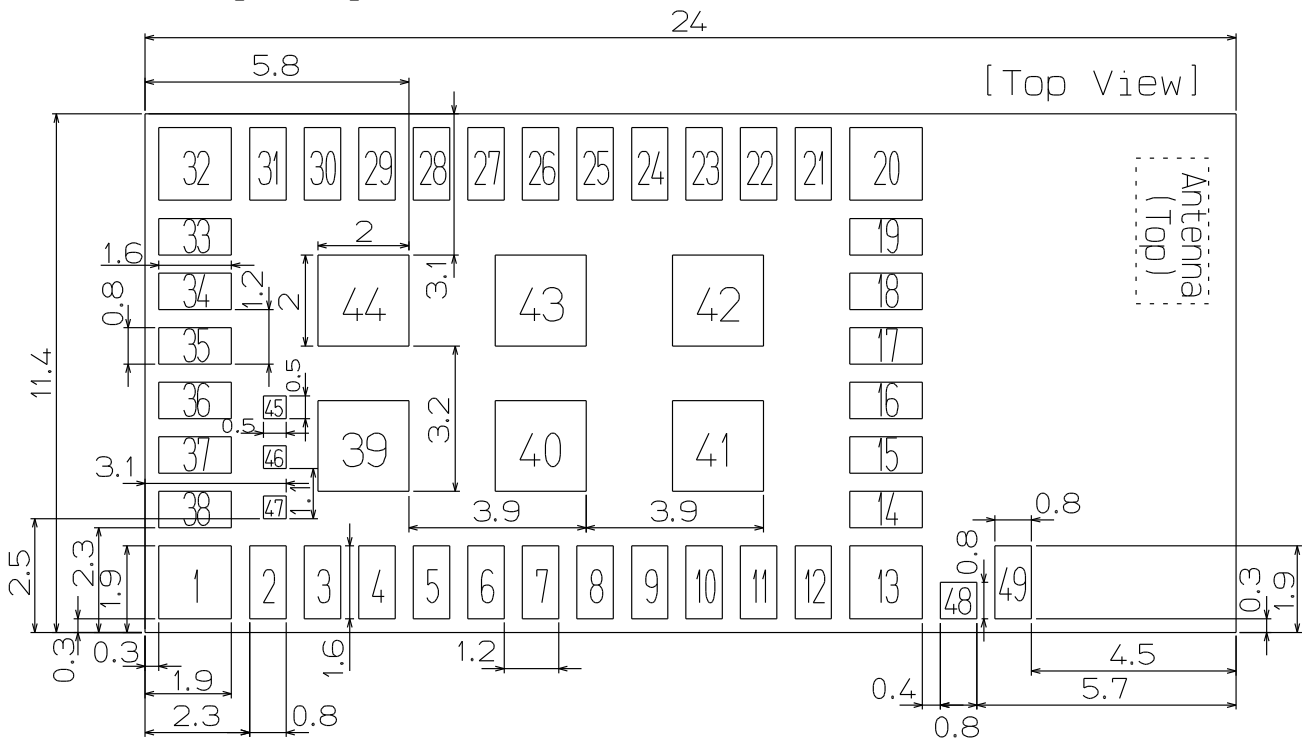


Figure 4 Detailed Pad Dimensions (For both SN8000 and SN8000UFL) (top view)

2.4 Module Pin-out

Table 1 Module Connector Signal Description

Pin #	Pin name	I/O	Description
1	GND	-	Ground
2	SDIO_D2	I/O	SDIO data line 2 with internal weak pull-up that can be disabled.
3	JTAG_TDI	-	JTAG_TDI, N/C otherwise.
4	JTAG_TDO	-	JTAG_TDO, N/C otherwise.
5	BTCX_FREQ/GPIO1	I/O	GPIO/Coexistence output signal indicating Bluetooth transmission in restricted channel. Hi-Z at power-up and reset.
6	GPIO0	I/O	GPIO/Strapping option for SDIO (pull low) or SPI mode (pull high). Has weak internal pull down.
7	ANT_SEL2	O	Auxiliary antenna selection (RFSW_CONTROL3). Default low.
8	ANT_SEL1	O	Main antenna selection (RFSW_CONTROL0). Default high.
9	GND	-	Ground
10	RST_N	I	Active low WLAN reset signal with internal 200K pull-down.
11	VDD_3V3_EN	I	Enables 3.3V LDO
12	VDD_BAT	I	Module power supply
13	GND	-	Ground
14	GND	-	Ground
15	GND	-	Ground
16	GND	-	Ground
17	GND	-	Ground
18	GND	-	Ground
19	GND	-	Ground
20	GND	-	Ground
21	GND	-	Ground
22	GND	-	Ground
23	GND	-	Ground
24	GND	-	Ground
25	GND	-	Ground
26	GND	-	Ground

Pin #	Pin name	I/O	Description
27	GND	-	Ground
28	BTCX_STATUS/GPIO4	I/O	GPIO/Coexistence signal indicating Bluetooth priority status and TX/RX direction. Hi-Z at power-up and reset.
29	BTCX_TXCONF/GPIO3	I/O	GPIO/Coexistence output giving Bluetooth permission to transmit. Hi-Z at power-up and reset.
30	BTCX_RF_ACTIVE/GPIO5	I/O	GPIO/Coexistence signal indicating Bluetooth is active. Hi-Z at power-up and reset.
31	SLEEP_CLK	I	Optional external 32KHz sleep clock. Tie to GND if not used.
32	GND	-	Ground
33	VDD_IO	I	Power for IO and SDIO pads
34	SDIO_D1/SPI_IRQ	I/O	SDIO data line 1 with internal weak pull-up that can be disabled.
35	SDIO_D0/SPI_MISO	I/O	SDIO data line 0 with internal weak pull-up that can be disabled.
36	SDIO_CLK/ SPI_CLK	I	SDIO/SPI clock.
37	SDIO_CMD/ SPI_MOSI	I/O	SDIO command line with internal weak pull-up that can be disabled.
38	SDIO_D3/ SPI_CSX	I/O	SDIO data line 3 with internal weak pull-up that can be disabled.
39	GND	-	Ground
40	GND	-	Ground
41	GND	-	Ground
42	GND	-	Ground
43	GND	-	Ground
44	GND	-	Ground
45	JTAG_TCK	-	JTAG_TCK, N/C otherwise.
46	JTAG_TRSTN	-	JTAG_TRSTN, N/C otherwise.
47	JTAG_TMS	-	JTAG_TMS, N/C otherwise.
48	NC4	-	No connect
49	GND	-	Ground

3 DC Electrical Specifications

3.1 Typical Power Consumption

Condition: 25°C, VDD_BAT=3.6V, VDD_IO= 3.6V

Table 2 Typical Power Consumption for SN8000

Item	Condition	Values			Units
		Min	Typ	Max	
11b	Receive mode		70		mA
	Transmit mode (18.5dBm/100% Duty Cycle)		315		mA
11g	Receive mode		70		mA
	Transmit mode (14.5dBm/100 % Duty Cycle)		235		mA
11n	Receive mode		70		mA
	Transmit mode (13.5dBm/100% Duty Cycle)		225		mA

Table 3 Typical Power Consumption for SN8000UFL

Item	Condition	Values			Units
		Min	Typ	Max	
11b	Receive mode		70		mA
	Transmit mode (16.5dBm/100% Duty Cycle)		285		mA
11g	Receive mode		70		mA
	Transmit mode (14.5dBm/ 100 % Duty Cycle)		235		mA
11n	Receive mode		70		mA
	Transmit mode (13.5dBm/100% Duty Cycle)		225		mA

3.2 Power Up/Down Sequence

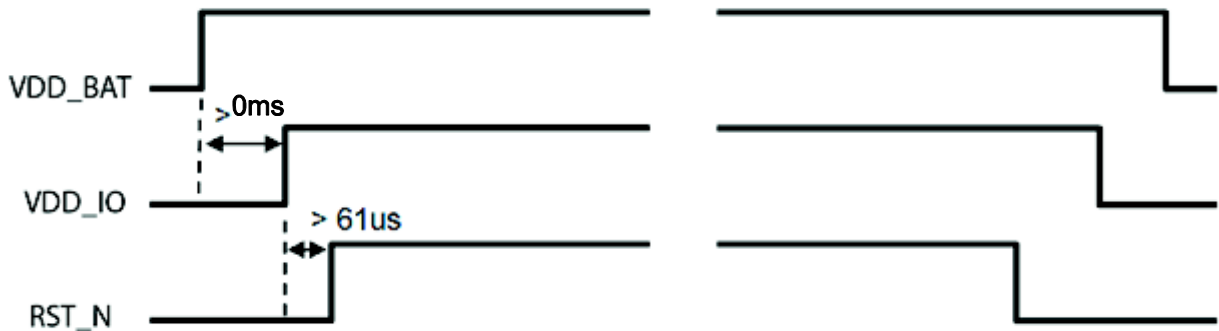


Figure 5 Boot-Up Sequence

3.3 GPIO Interface

Five general purpose I/O (GPIO) pins are available on the SN8000 that can be used to connect to various external devices.

GPIOs are tristated by default. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. They can also be programmed to have internal pull-up or pull-down resistors.

GPIO_0 is initially used as a strapping option to select between SDIO and SPI modes

GPIOs 3, 4, and 5 are multiplexed with the Bluetooth Coexistence Interface. By default, these pins are BT_COEX pins. Software can reprogram these pins to behave as GPIOs.

GPIO_1 is a GPIO by default, but can be programmed to become the BCTX_FREQ signal.

Table 4 Digital I/O Requirements

	SYM	min.	typ.	max.	unit
Input low voltage (VDD_IO = 3.3V)	V _I	-	-	0.8	V
Input high voltage (VDD_IO = 3.3V)	V _{IH}	2.0	-	VDD_IO	V
Input low voltage (VDD_IO = 1.8V) ¹	V _I	-	-	0.7	V
Input high voltage (VDD_IO = 1.8V)	V _{IH}	1.1	-	VDD_IO	V
Input low voltage (RESET pin)	V _{IL}	-	-	0.4	V
Input high voltage (RESET pin)	V _{IH}	1.08	-	3.6	V
Output low voltage	V _{OL}	-	-	0.4	V
Output high voltage	V _{OH}	VDD_IO-0.4	-	-	V
Input low current	I _{IL}	-	0.3	-	uA
Input high current	I _{IH}	-	0.3	-	uA

3.4 SDIO Interface

Table 5 SDIO Pin Description

No.	Pin Name	(i) SD 4-bit Mode		(ii) SD 1-bit Mode	
		DATA	Description	Signal	Description
2	SDIO_D2	DATA2	Data line 2	NC	Not used
34	SDIO_D1	DATA1	Data line 1 /Interrupt	IRQ	Interrupt
35	SDIO_D0	DATA0	Data line 0	DATA	Data line
36	SDIO_CLK	CLK	Clock	CLK	Clock
37	SDIO_CMD	CMD	Command line	CMD	Command line
38	SDIO_D3	DATA3	Data line 3	NC	Not used

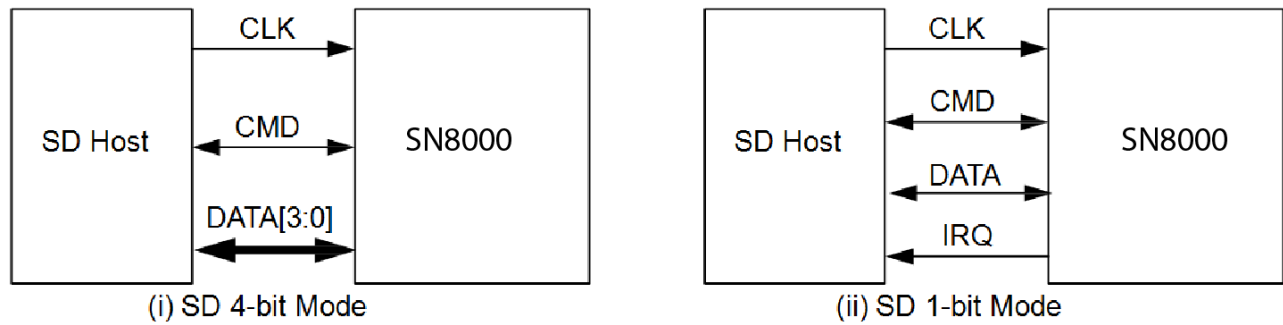


Figure 6 SDIO Connection

3.4.1 SDIO Timing (Default Mode)

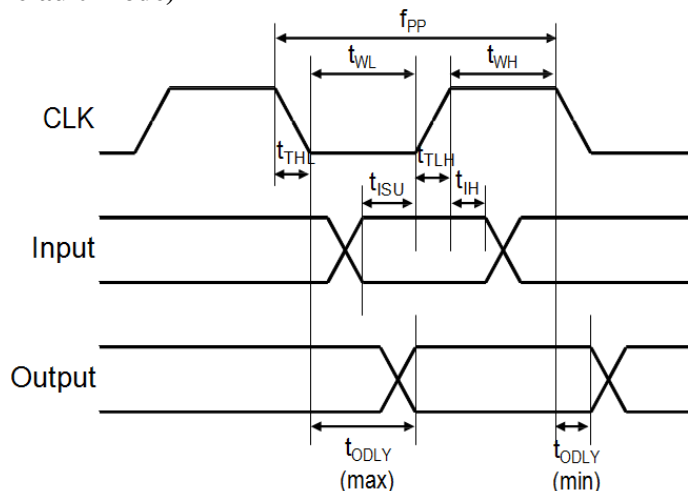


Figure 7 SDIO Timing (Default Mode)

Table 6 SDIO Interface Timing Default

Parameter	Symbol	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
Clock CLK (All values are referred to min. VIH and max. VIL ⁽²⁾)					
Frequency-Data Transfer Mode	fPP	0	-	25	MHz
Frequency-Identification Mode	fOD	0	-	400	kHz
Clock Low Time	tWL	10	-	-	ns
Clock High Time	tWH	10	-	-	ns
Clock Rise Time	tTLH	-	-	10	ns
Clock Falling Time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input Setup Time	tISU	5	-	-	ns
Input Hold Time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output Delay time-Data Transfer Mode	tODLY	0	-	14	ns
Output Delay time-Identification Mode	tODLY	0	-	50	ns

(1). Timing is based on $CL \leq 40pF$ load on CMD and Data.

(2). Min (Vih) = $0.7 \cdot VDDIO$ and max (Vil) = $0.2 \cdot VDDIO$.

3.4.2 SDIO Timing (High Speed Mode)

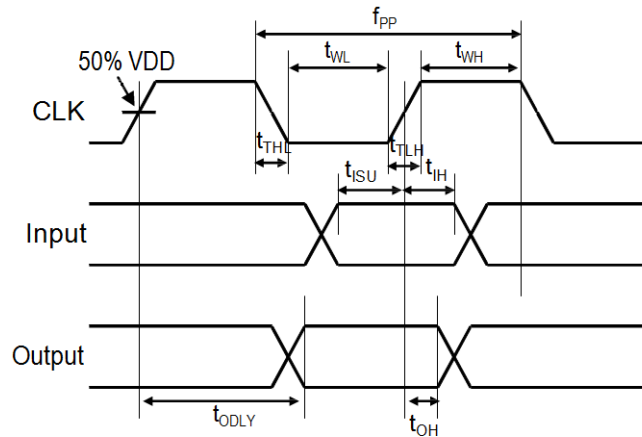


Figure 8 SDIO Timing (High Speed Mode)

Table 7 SDIO Timing - High Speed

Parameter	Symbol	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
Clock CLK (All values are referred to min. VIH and max. VIL ⁽²⁾)					
Frequency-Data Transfer Mode	fPP	0	-	50	MHz
Frequency-Identification Mode	fOD	0	-	400	kHz
Clock Low Time	tWL	7	-	-	ns
Clock High Time	tWH	7	-	-	ns
Clock Rise Time	tTLH	-	-	3	ns
Clock Falling Time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input Setup Time	tISU	6	-	-	ns
Input Hold Time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output Delay time-Data Transfer Mode	tODLY	-	-	14	ns
Output Hold time	tOH	2.5	-	-	ns
Total System Capacitance (each line)	CL	-	-	40	pF

(1). Timing is based on $CL \leq 40\text{pF}$ load on CMD and Data.

(2). Min (Vih) = $0.7 \cdot VDD_IO$ and max (Vil) = $0.2 \cdot VDD_IO$.

3.5 gSPI Interface

The gSPI device always samples data on the rising edge of the clock.

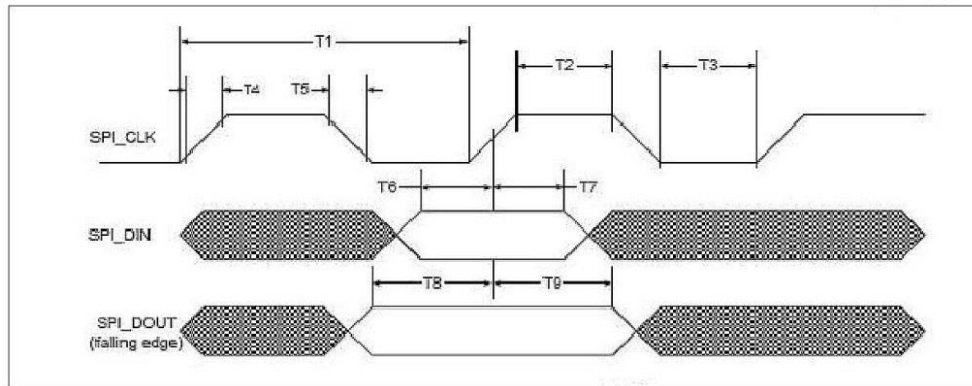


Figure 9 gSPI Signal Timing

Table 8 SDIO Pin Description – gSPI Mode

Pin	gSPI Mode	
2	NC	Not used
34	IRQ	Interrupt
35	DO	Data output
36	SCLK	Clock
37	DI	Data Input
38	CS	Card select

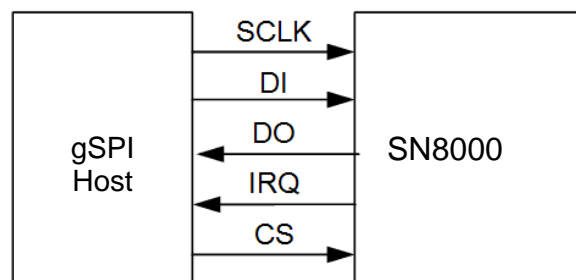


Figure 10 gSPI Interface

4 RF Specifications

4.1 DC/RF Characteristics for IEEE 802.11b

Conditions: 25deg.C, VDD_BAT=3.6V, VDD_IO= 3.3V
(11Mbps mode unless otherwise specified.)

Parameters measured at RF connector except EIRP

Table 9 RF Characteristics for IEEE 802.11b

Parameters		Specification			
Modulation		DSSS/CCK			
Physical layer data rate		1,2,5.5,11Mbps			
RF Characteristics		Min	Typ.	Max.	Unit
Frequency range		2400	--	2483.5	MHz
Carrier frequency error		-20	--	+20	ppm
Transmit output power ¹	SN8000UFL	15.0	17.0	19.0	dBm
Transmit power, EIRP	SN8000		18.5		dBm
Spectrum mask					
1 st side lobes		--	--	-30	dBr
2 nd side lobes		--	--	-50	dBr
Power-on and Power-down ramp		--	--	2	usec
RF Carrier Suppression		15	--	--	dBc
Modulation accuracy (EVM)		--	--	35	%
Outband spurious emissions					
30MHz to 1GHz (BW=100KHz)				-96	dBm
1GHz to 12.75GHz (BW=1MHz)				-41	dBm
1.8GHz to 1.9GHz (BW=1MHz)				-65	dBm
5.15GHz to 5.3GHz (BW=1MHz)				-85	dBm
Receive Sensitivity ¹					
1Mbps (FER≤ 8%)		-94	-96	--	dBm
11Mbps (FER≤ 8%)		-86	-88	--	dBm
Maximum input level (FER≤ 8%)		-9.5	--	--	dBm
Adjacent channel rejection (FER≤ 8%)		35			dB

[Note]

- Derate by 1.5 dB for temperatures less than -10 °C or more than +55 °C in both transmit and receive modes.

4.2 DC/RF Characteristics for IEEE 802.11g

Condition: 25deg.C, VDD_BAT=3.6V, VDD_IO= 3.3V

(54Mbps mode unless otherwise specified.)

Parameters measured at RF connector except EIRP

Table 10 RF Characteristics for IEEE 802.11g

Parameters		Specification			
Standard conformance		IEEE 802.11 g			
Modulation		OFDM			
Data rate		6, 9, 12, 18, 24, 36, 48, 54Mbps			
RF Characteristics		Min	Typ.	Max.	Unit
Frequency range		2400	--	2483.5	MHz
Carrier frequency error		-20	--	+20	ppm
Transmit output power ¹	SN8000UFL	12.5	14.5	16.5	dBm
Transmit power, EIRP	SN8000		14.5		dBm
Spectrum mask					
9MHz to 11MHz (0dB ~ -20dB)		0		-	dB
11MHz to 20MHz (-20dB ~ -28dB)		0		-	dB
20MHz to 30MHz (-28dB ~ -40dB)		0		-	dB
30MHz to 33MHz (-40dB)		0		-	dB
Constellation Error (EVM)		--	--	-25	dB
Outband spurious emissions					
30MHz to 1GHz (BW=100KHz)				-96	dBm
1GHz to 12.75GHz (BW=1MHz)				-41	dBm
1.8GHz to 1.9GHz (BW=1MHz)				-65	dBm
5.15GHz to 5.3GHz (BW=1MHz)				-85	dBm
Receive Sensitivity ¹					
6Mbps (PER ≤ 10%)		-87	-89	--	dBm
54Mbps (PER ≤ 10%)		-72	-74	--	dBm
Maximum input level (PER ≤ 10%)		-13	--	--	dBm
Adjacent channel rejection (PER ≤ 10%)		-1			dB

[Note]

1. Derate by 1.5 dB for temperatures less than -10 °C or more than +55 °C in both transmit and receive modes.

4.3 DC/RF Characteristics for IEEE 802.11n

Condition: 25deg.C, VDD_BAT=3.6V, VDD_IO= 3.3V
(65Mbps mode unless otherwise specified.)

Parameters measured at RF connector except EIRP

Table 11 RF Characteristics for IEEE 802.11n

Parameters		Specification			
Standard conformance		IEEE 802.11 n			
Modulation		OFDM			
Data rate		6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps			
RF Characteristics		Min	Typ.	Max.	Unit
Frequency range		2400	--	2483.5	MHz
Carrier frequency error		-20	--	+20	ppm
Transmit output power ¹	SN8000UFL	11.5	13.5	15.5	dBm
Transmit power, EIRP	SN8000		13.5		dBm
Spectrum mask					
9MHz to 11MHz (0dB ~ -20dB)		0		-	dB
11MHz to 20MHz (-20dB ~ -28dB)		0		-	dB
20MHz to 30MHz (-28dB ~ -45dB)		0		-	dB
30MHz to 33MHz (-45dB)		0		-	dB
Constellation Error (EVM)		--	--	-28	dB
Outband spurious emissions					
30MHz to 1GHz (BW=100KHz)				-96	dBm
1GHz to 12.75GHz (BW=1MHz)				-41	dBm
1.8GHz to 1.9GHz (BW=1MHz)				-65	dBm
5.15GHz to 5.3GHz (BW=1MHz)				-85	dBm
Receive Sensitivity ¹					
65Mbps (PER ≤ 10%)		-69	-71	--	dBm
Maximum input level (PER ≤ 10%)		-13			dBm
Adjacent channel rejection (PER ≤ 10%)		-2			dB

[Note]

1. Derate by 1.5 dB for temperatures less than -10 °C or more than +55 °C in both transmit and receive modes.

5 Antenna Information

The table below shows the information of the reference antennae that are used in FCC, IC and ETSI testing for SN8000UFL.

Table 12 External Antenna to comply with regulation (Only SN8000UFL)

Part Number	Vendor	Gain (dBi)	Antenna Type	Connector	Remarks
TRF-1002	Microchip	5.0	Omnidirectional	U.FL	For FCC/IC compliance
W1049B050	Pulse	2.0	Omnidirectional	U.FL	For FCC/IC and ETSI compliance
W3525B100	Pulse	2.0	Omnidirectional	U.FL	For FCC/IC and ETSI compliance

6 Environmental Specifications

6.1 Absolute maximum ratings

Table 13 Absolute Maximum Rating

Symbol	Description	Min	Max	Unit
T _{sop}	Specification temperature	-30	85	°C
T _{op} *	Operating temperature	-40	85	°C
T _{st}	Storage temperature	-40	85	°C
VDD_IO	IO Power supply	0	3.6	V
VDD_BAT	Power supply	0	5.0	V
RFin	RF input power		0	dBm
MSL	Moisture Sensitivity Level	3		
RoHS2	Restriction of Hazardous Substances	Compliant		

*Note: RF performance may be degraded at extreme temperatures.

6.2 Recommended Operating Conditions

Table 14 Recommended Operating Conditions

	Min (V)	Typ (V)	Max (V)	Description
VDD_IO	1.75	3.3	3.6	Supply to the IO pads
VDD_BAT	3.0	3.6	5.0	Supply to BCM43362 BB/MAC/RF

7 Packaging and Marking Information

7.1 Carrier Tape Dimensions

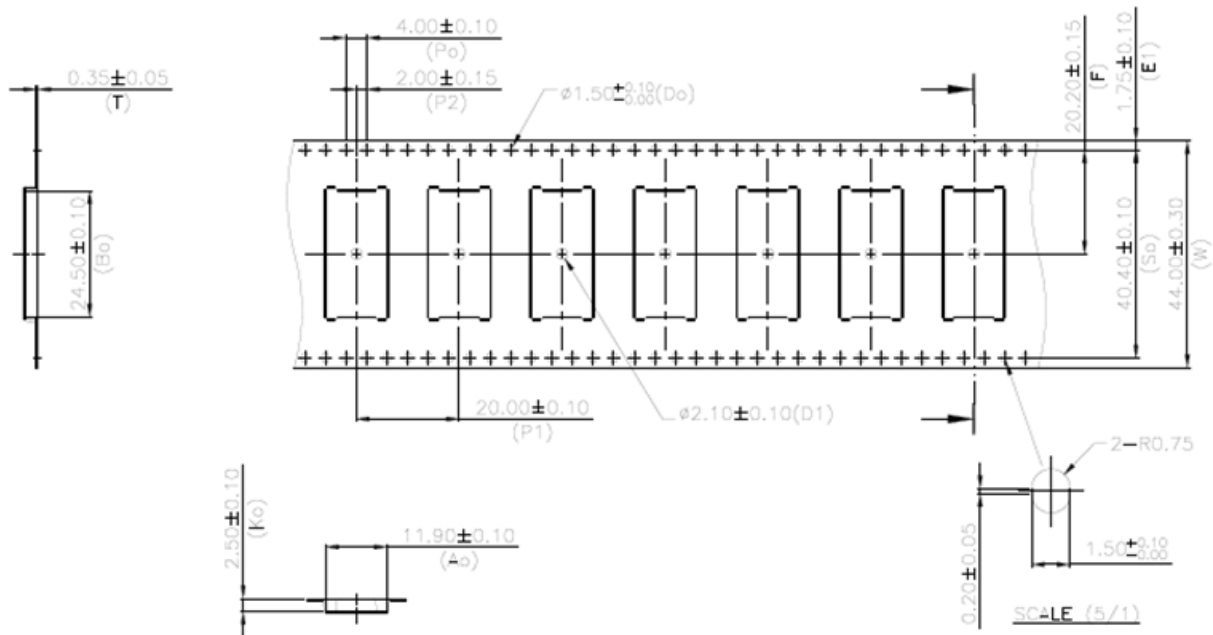
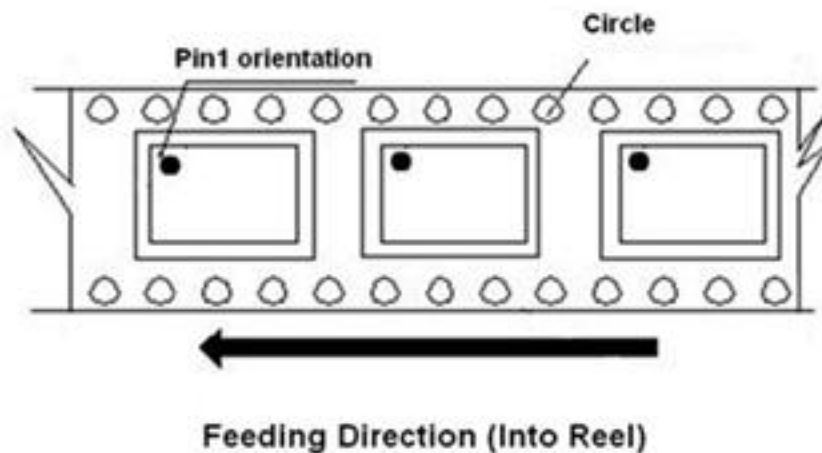


Figure 11 Carrier Tape Dimensions

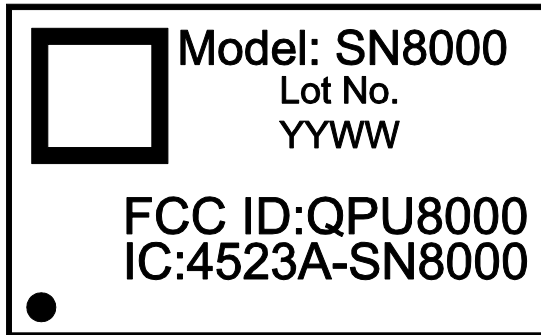


Double Sprocket Holes

Figure 12 SN8000 Pin1 Orientation

7.2 Module Marking Information

Module Marking for SN8000



Module Marking for SN8000UFL

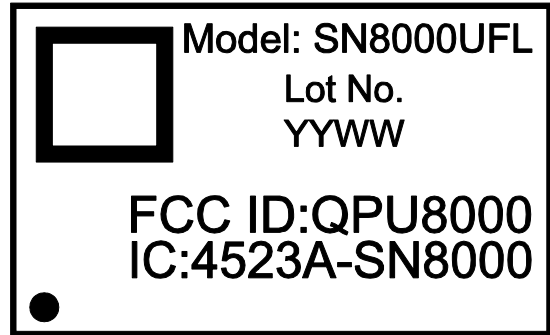


Figure 13 Module Marking Detail

8 Ordering Information

Table 15 Ordering Information

Product	RFM Model Number	RFM Part Number	Standard Order Increment
SN8000 Evaluation Development Kit	SN8000EVK	88-00153-85	1 pc
SN8000 Module in Tape & Reel	SN8000	88-00153-00	400 pcs/reel
SN8000UFL Evaluation Development Kit	SN8000UFL EVK	88-00153-87	1 pc
SN8000UFL Module in Tape & Reel	SN8000UFL	88-00153-02	400 pcs/reel

9 RoHS Declaration

To the best of our present knowledge, given our supplier declarations, this product does not contain substances that are banned by Directive 2011/65/EU or contain a maximum concentration of 0.1% by weight in homogeneous materials for

- Lead and lead compounds
- Mercury and mercury compounds
- Chromium (VI)
- PBB (polybrominated biphenyl)
- PBDE (polybrominated biphenyl ether)

And a maximum concentration of 0.01% by weight in homogeneous materials for

- Cadmium and cadmium compounds
-

10 Regulatory Information

The table below shows the regulatory compliance status of the SN8000/8000UFL module.

Regulatory Body	Standard	Certificate ID
FCC	Part 15	QPU8000
IC	RSS-210	4523A-SN8000
ETSI	EN300 328, Ver. 1.8.1 ETSI EN301.489 - 17	Compliant

For more information, see SN8000/SN8000UFL Wi-Fi Module User Manual [2].



Innovator in Electronics

11 Technical Support Contact

For technical support, please contact us at tech_sup@murata.com.

Murata Electronics N.A., Inc.
4441 Sigma Road
Dallas, TX 75244
USA