

## 5-44GHz Detector

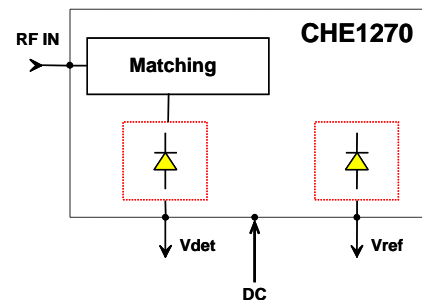
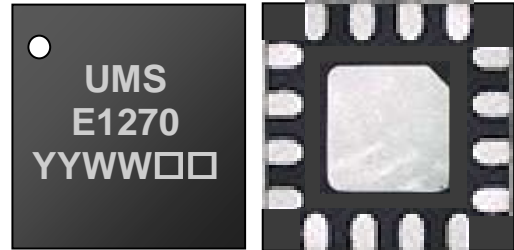
### GaAs Monolithic Microwave IC in SMD leadless package

#### Description

The CHE1270-QAG is a detector that integrates a matched detector diode (Vdet) and a reference diode (Vref).

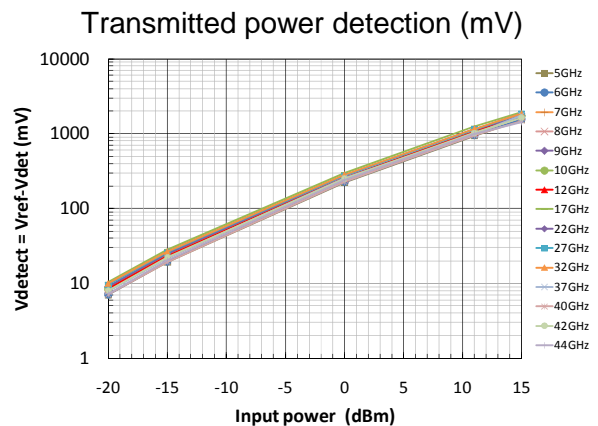
It is designed for a wide range of applications where an accurate transmitted power control is required, typically commercial communication systems.

The circuit is manufactured with a Schottky diode MMIC process, 1 $\mu$ m gate length, via holes through the substrate and air bridges. It is supplied in RoHS compliant SMD package.



#### Main Features

- Broadband performances: 5-44GHz
- 30dB dynamic range
- ESD protected
- 16L-QFN3x3
- MSL1



#### Main Characteristics

Tamb.= +25°C, VDC = +4.5V

| Symbol | Parameter       | Min | Typ | Max | Unit |
|--------|-----------------|-----|-----|-----|------|
| Freq   | Frequency range | 5   |     | 44  | GHz  |
| Dr     | Dynamic range   | 30  |     |     | dB   |
| RL     | Return Loss     |     | -10 |     | dB   |

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| Symbol  | Parameter  | Min | Typ | Max  | Unit |
|---------|--|-----|-----|------|------|
| F       | Frequency range  | 5   |     | 44   | GHz  |
| Dr      | Dynamic range (for Input Power detection)                | 30  |     |      | dB   |
| IPd     | Input Power detection                                    | -15 |     | 15   | dBm  |
| Vdetect | Voltage detection Vref – Vdet<br>from IPd_min to IPd_max | 5   |     | 2200 | mV   |
| RL      | Return Loss (5 – 10GHz)                                  |     | -5  | -4   | dB   |
|         | Return Loss (10 – 12GHz)                                 |     | -8  | -7   | dB   |
|         | Return Loss (12 – 36GHz)                                 |     | -10 | -9   | dB   |
|         | Return Loss (36 – 44GHz)                                 |     | -8  | -7   | dB   |
| VDC     | Bias Voltage   |     | 4.5 |      | V    |
| IDC     | Bias Current   | 50  | 70  | 90   | μA   |

These values are representative of onboard measurements as defined in the paragraph "Evaluation mother board" with 27kΩ resistor in parallel on Vdet and Vref pads.

**Absolute Maximum Ratings** <sup>(1)</sup>T<sub>amb.</sub> = +25°C

| Symbol | Parameter                   | Values      | Unit |
|--------|-----------------------------|-------------|------|
| VDC    | Bias voltage                | 6           | V    |
| P_max  | Maximum Power               | 18          | dBm  |
| Ta     | Operating temperature range | -40 to +85  | °C   |
| Tstg   | Storage temperature range   | -55 to +155 | °C   |

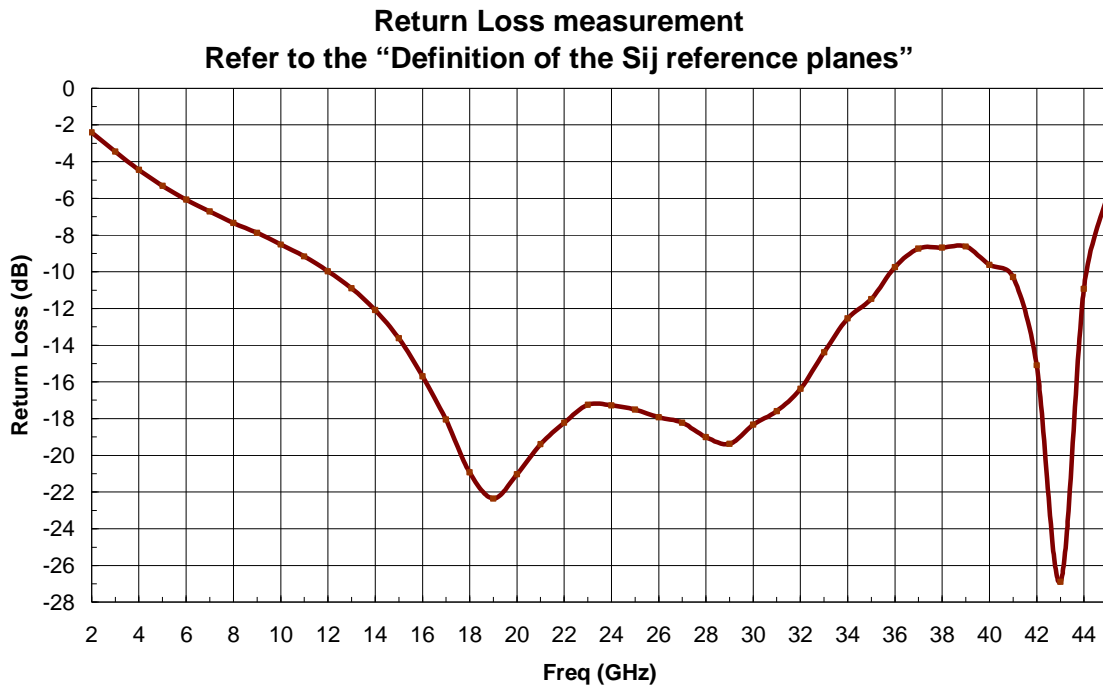
<sup>(1)</sup> Operation of this device above any one of these parameters may cause permanent damage.

## Typical Measured Performances

Tamb.= +25°C, VDC = +4.5V

27kΩ resistor in parallel on Vdet and Vref pads (see Notes).

Board losses de-embedded (result given in the package access plan)



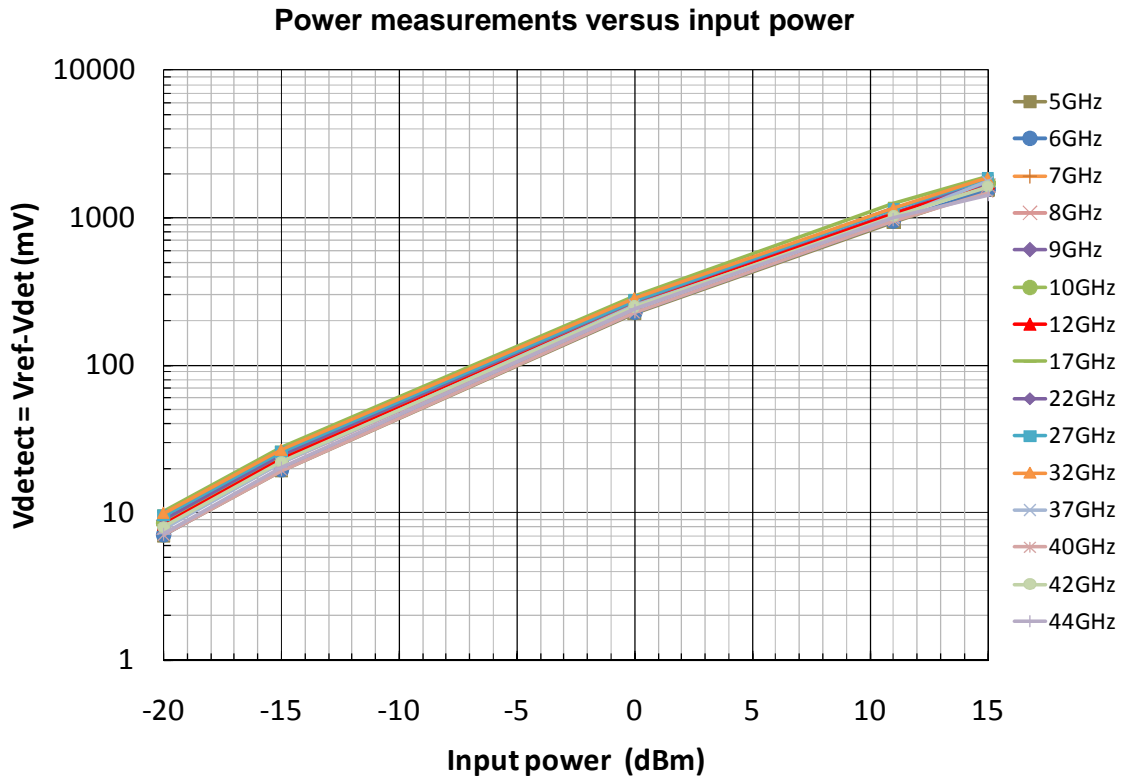
**Typical Measured Performances**

Tamb.= +25°C, VDC = +4.5V

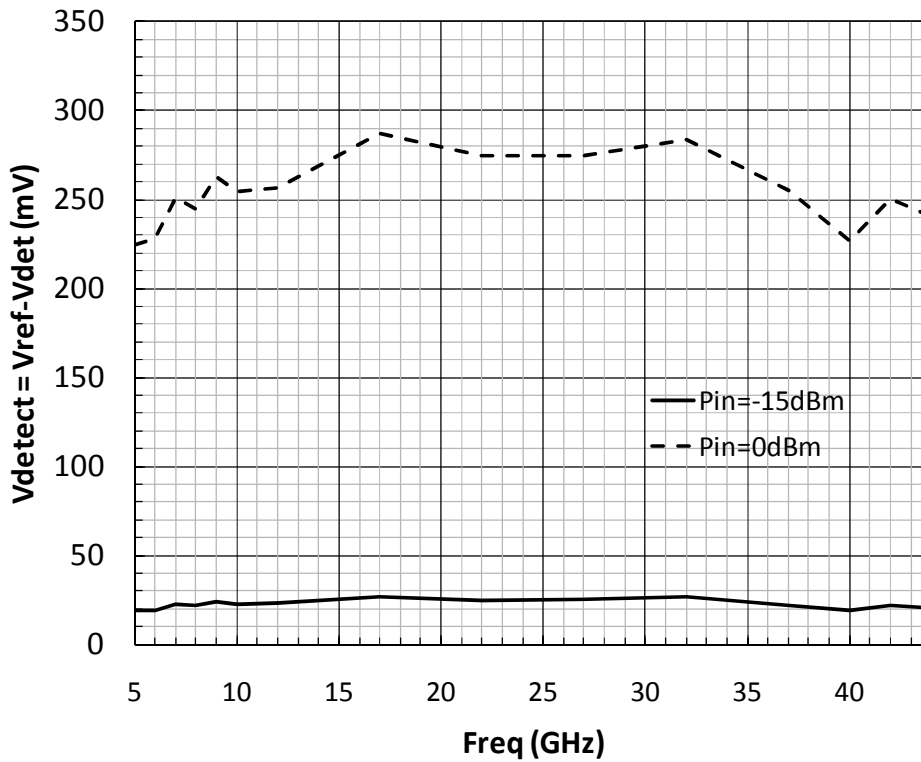
27kΩ resistor in parallel on Vdet and Vref pads (see Notes).

Board losses not de-embedded (result given in the plan of connectors)

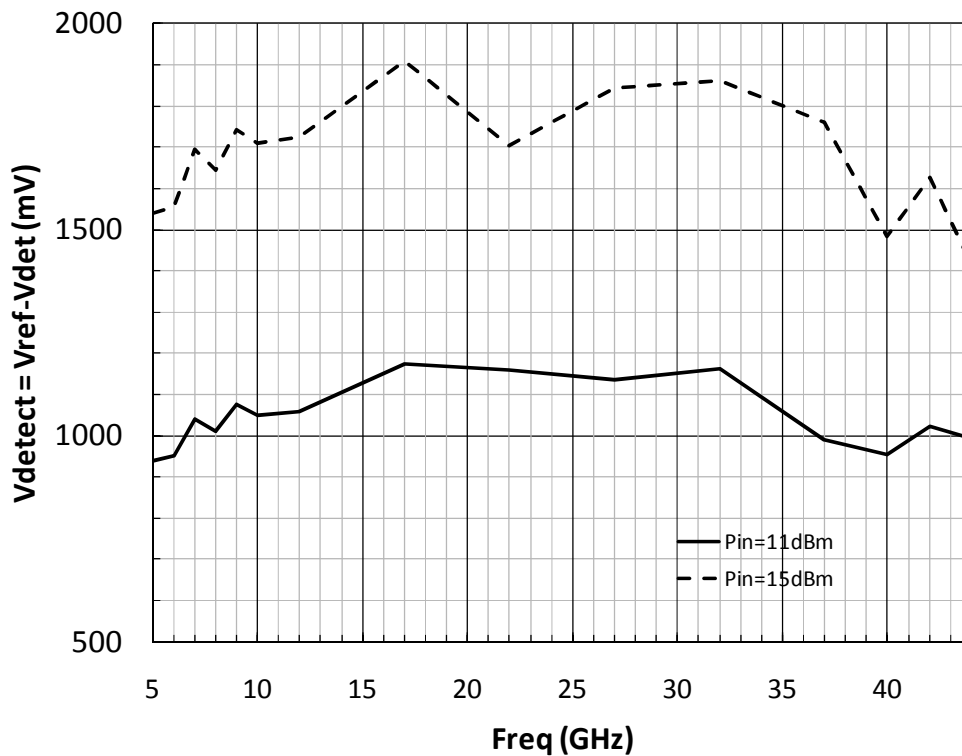
Refer to the proposed land pattern & board 96272-B (see "Evaluation mother board")



Transmitted power detection versus frequency  
@ -15 and 0dBm input power



Transmitted power detection versus frequency  
@ +11 and +15dBm input power

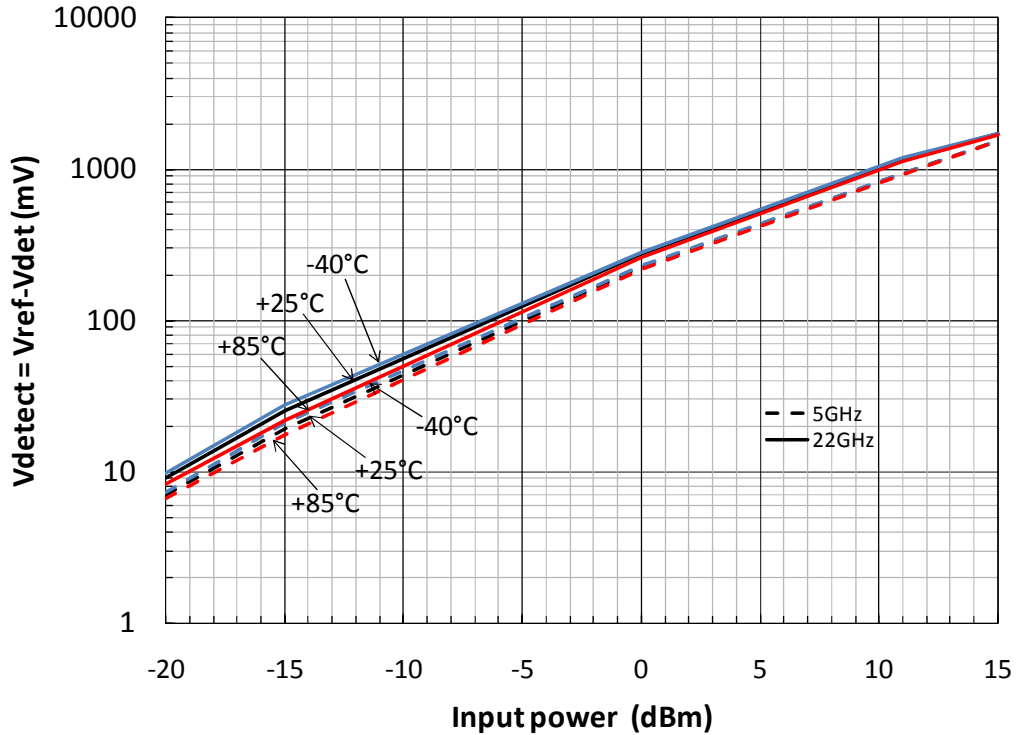


**Typical Measured Performances**

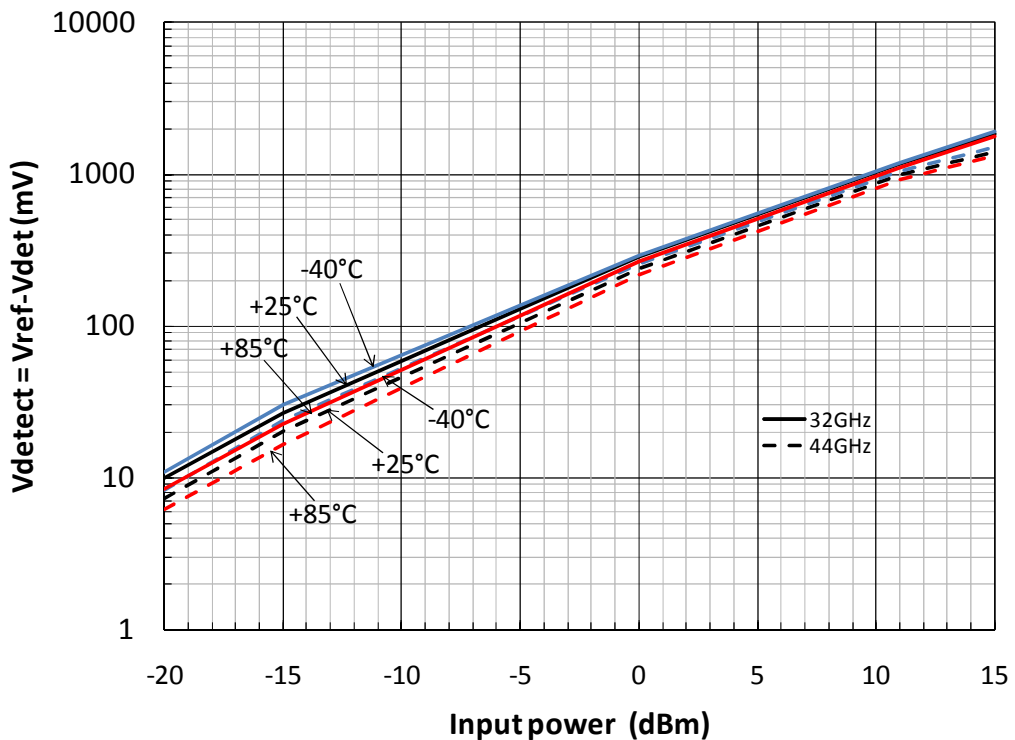
Tamb = +25°C, Tcold = -40°C, Thot = +85°C, VDC = +4 .5V

Board losses not de-embedded (result given in the plan of connectors)

**Transmitted power detection versus frequency and temperature @ 5 and 22GHz**



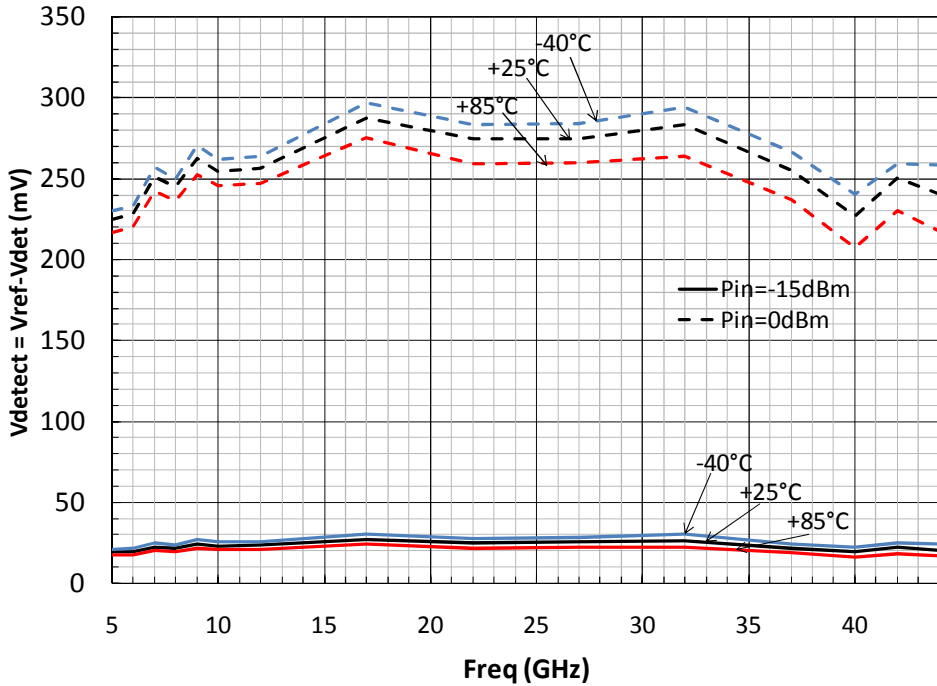
**Transmitted power detection versus frequency and temperature @ 32 and 44GHz**



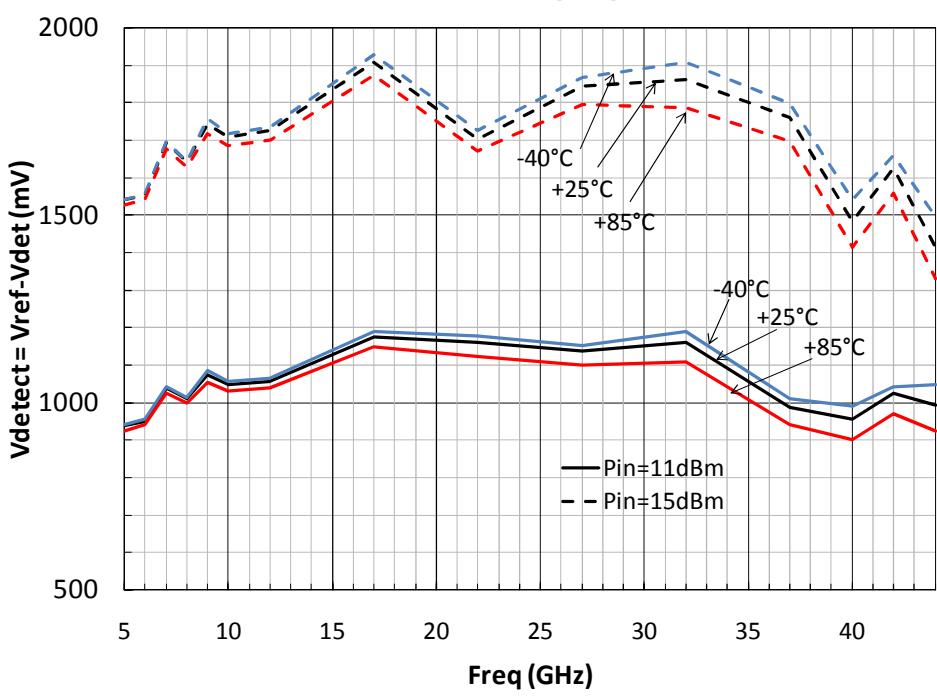
Typical Measured Performances

Tamb = +25°C, Tcold = -40°C, Thot = +85°C, VDC = +4 .5V  
 Board losses not de-embedded (result given in the plan of connectors)

Transmitted power detection versus frequency and temperature @ -15 and 0dBm input power

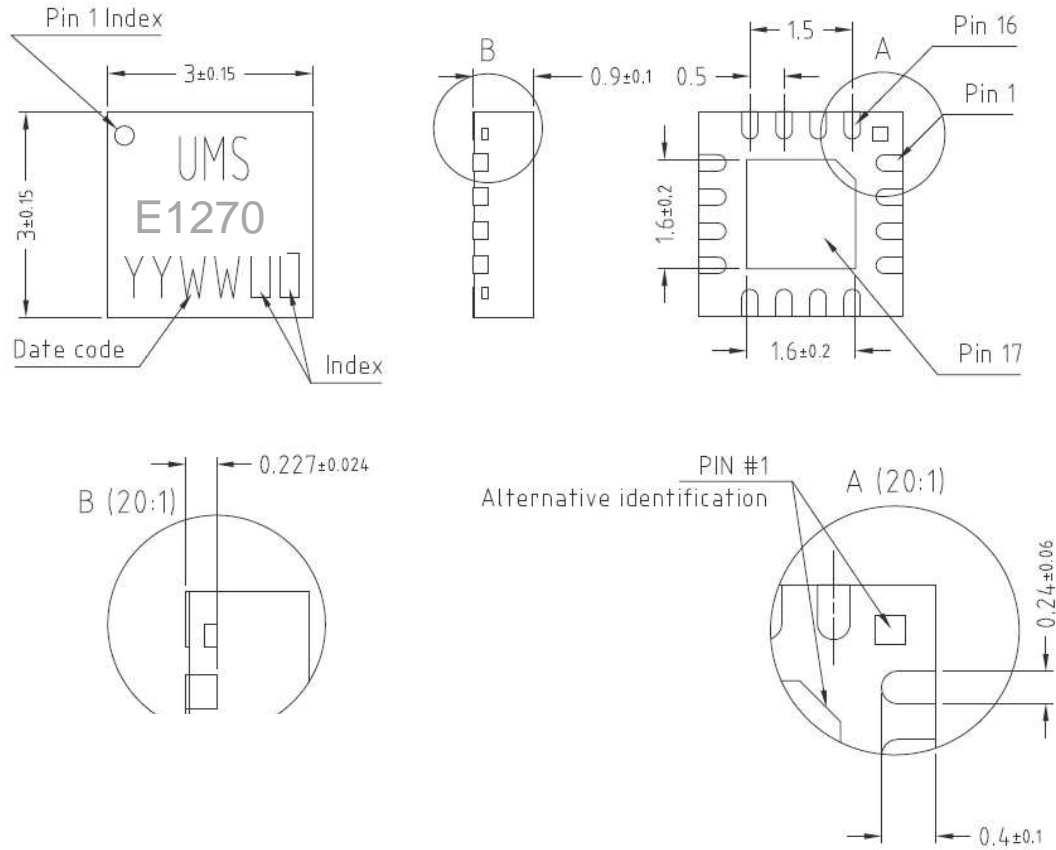


Transmitted power detection versus frequency and temperature @ +11 and +15dBm input power





Package outline <sup>(1)</sup>



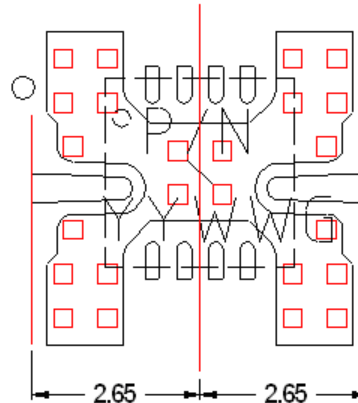
|                     |                        |    |                    |     |                    |     |    |
|---------------------|------------------------|----|--------------------|-----|--------------------|-----|----|
| Matt tin, Lead Free | (Green)                | 1- | Nc                 | 7-  | Vref               | 13- | Nc |
| Units :             | mm                     | 2- | Gnd <sup>(2)</sup> | 8-  | Nc                 | 14- | Nc |
| From the standard : | JEDEC MO-220<br>(VGGD) | 3- | RF in              | 9-  | Gnd <sup>(2)</sup> | 15- | Nc |
|                     |                        | 4- | Gnd <sup>(2)</sup> | 10- | Nc                 | 16- | Nc |
| 17-                 | GND                    | 5- | Vdet               | 11- | Gnd <sup>(2)</sup> |     |    |
|                     |                        | 6- | DC                 | 12- | Nc                 |     |    |

<sup>(1)</sup> The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

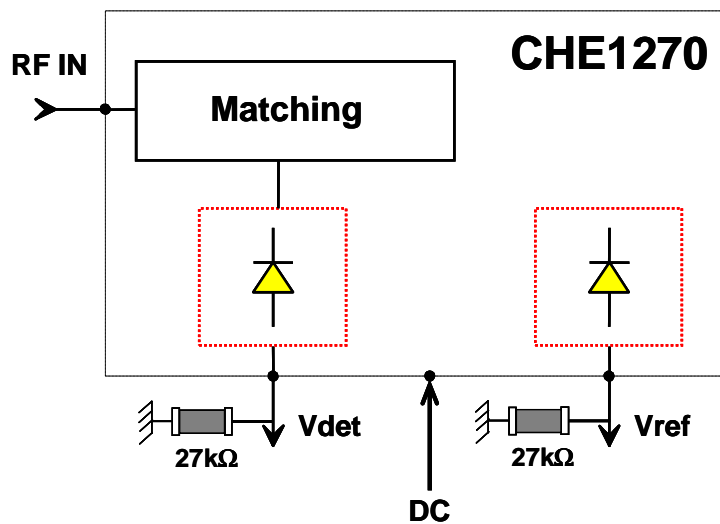
<sup>(2)</sup> It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

## Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 2.65mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation motherboard".



## Notes



### Recommended external resistors assembly

27kΩ resistors in parallel with Vdet and Vref pads are recommended to provide the best behaviour in the whole operating temperature range.

As the voltage detection is the difference between Vref and Vdet, the external resistor value should be identical on these two ports.

For information, a variation of 3% leads around 1mV variation of detected voltage.

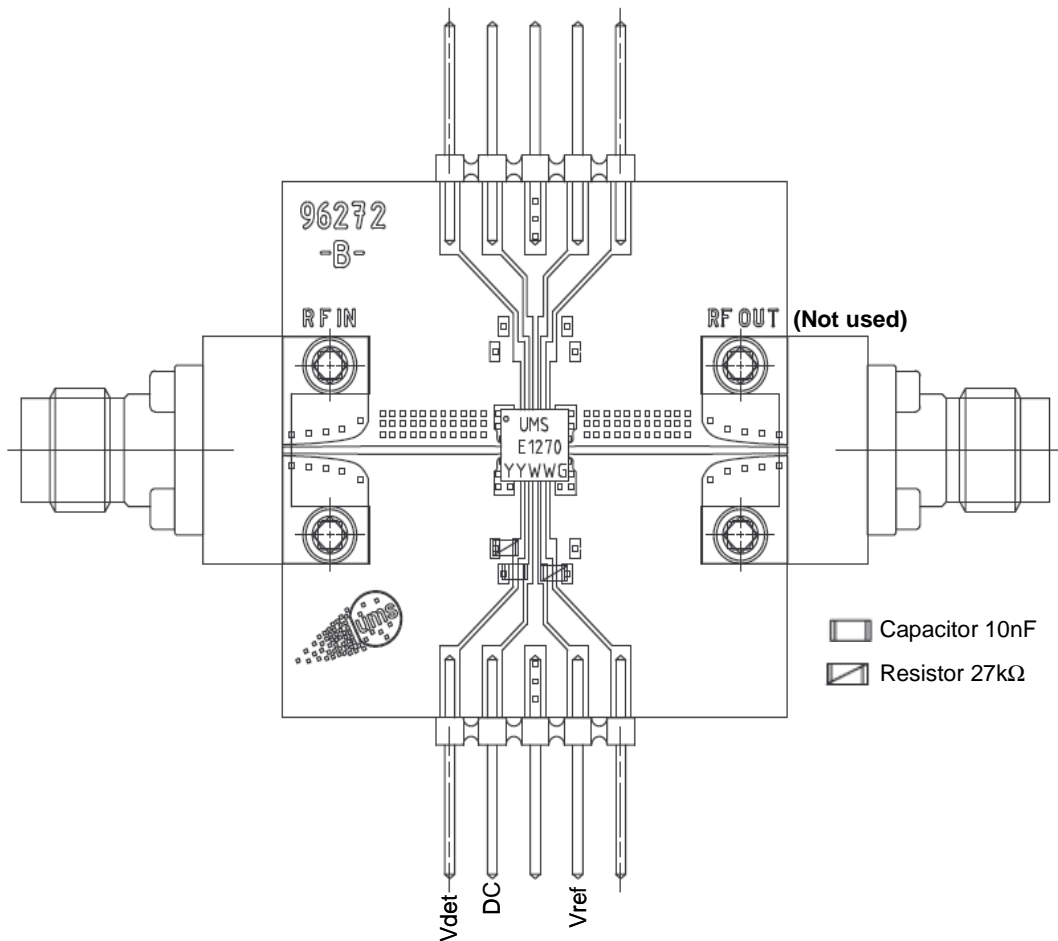
Due to ESD protection circuits on RF input, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF access.

ESD protections are also implemented on Vdet and Vref accesses.

The DC connection (on DC pad) does not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

## Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF  $\pm 10\%$  are recommended for all DC accesses.
- See application note AN0017 for details.



## Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

## SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

## Recommended environmental management

Refer to the application note AN0019 available at <http://www.ums-gaas.com> for environmental data on UMS package products.

## Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

## Ordering Information

QFN 4x4 RoHS compliant package:

CHE1270-QAG/XY

Stick: XY = 20

Tape & reel: XY = 21

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