LinearDimensions
SEMICONDUCTOR

The LND-PLL901

IF QUADRTURE TRANSCEIVER

The LND-PLL901 IF Quadrature Transceiver

What is the LND-PLL901?

The LND-PLL901 is a low power, low voltage phase locked loop (PLL) frequency synthesizer directed towards frequency synthesis applications. Such applications might include wireless LANS, portable communications equipment, transmitting and receiving devices, GSM, PCN, DECT, CT2, CT1, etc.

How Do I get samples?
The LND-PLL901 is available

Features

- Highly integrated 350 MHz IF to baseband quadrature transceiver function
- 47.5 dB Automatic Gain Controln the receiver
- High linearity transmitter with 21 dB programmable gain control
- Integated frequency synthesizer
- Integrated references for A/D and D/A converters
- Low operating current consumption with standby mode
- Covers QAM, PSK and FSK modulation schemes
- 7 different modes of operation

Applications

- Wireless LANS
- Cordless telephones
- Mobile telephones
- GSM, PCN, DECT, CT2,CTI
- Satellite and cable TV decoders

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AGC1	AGC0	Gain/dB
0	0	0
0	1	2.5
1	0	5
1	1	7.5

AGC4	AGC3	AGC2	Gain/dB
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	10.5
1	0	1	20
1	1	0	30
1	1	1	40

ALC1	ALC0	Gain/dB
0	0	0
0	1	3
1	0	6
1	1	9

ALC2	Gain/dB
0	0
1	12

Modes of operation (continued)

Mode table selection for the 5 V CMOS level controlled decoder							
Mode	Mode Name	MSTX	MSRX	MSPLL	MSTE	MSLIM	Description
1	Transmit	0	1	0	0	0	Transmitter = enabled, PLL = enabled Receiver = disabled
2	Receive	1	0	0	0	0	Transmitter = disabled, PLL = enabled Receiver = enabled
3	PLL	1	1	0	0	0	Transmitter = disabled, PLL = enabled Receiver = disabled
4	Standby	1	1	1	0	0	Transmitter = disabled, PLL = disabled Receiver = disabled
5	Loop Back	0	0	0	1	0	Transmitter = enabled, PLL = enabled Receiver = enabled
6	Limiter Enable	1	0	0	0	1	Transmitter = disabled, PLL = enabled Receiver = enabled, Limiter = enabled
7	Full Duplex	1	1	1	1	0	Transmitter = enabled, PLL = enabled Receiver = enabled, Limiter = disabled
Note: Full duplex mode is provided for production test purposes only.							

The table below details the maximum response times switching from one mode to another.

Maximum mode-to-mode response times (? s)							
To -->	Transmit	Receive	PLL	Standby	Loop Back	Limiter Enable	Full Duplex
From							
Transmit	****	1	1	100	****	10	100
Receive	1	****	10	100	10	1	100
PLL	1	1	****	20	10	10	100
Standby (see note)	****	****	20	****	****	****	100
Loop Back	****	100	100	100	****	****	100
Limiter Enable	1	1	10	100	****	****	100
Full Duplex	100	100	100	100	100	100	****
Note: Maximum response times switching the device from standby to any other modes are application dependent (approximately 20 μs).							

Operating Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Vcc (max)	Power Supply Voltage	-0.5		7+	V	relative to Vee (0 V)
Tstg	Storage Temperature	-55		150+	°C	
Tj	Junction Temperature	-55		150+	°C	
Vshort	Voltage on any pin	-0.5		7+	V	

Operating Characteristics (continued)

Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Vcc	Power Supply Voltage	4.75	5	5.25	V	
Top	Operating Temperature Range	0		70+	°C	

D.C. Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Icc1	Supply Current Receive Mode		57	77.5	mA	All, no external ADC connected
Icc2	Supply Current Transmit Mode		52.5	67.5	mA	All, see note 1
Icc3	Supply Current PLL Mode		16.5	20.5	mA	All
Icc4	Supply Current Standby Mode			100	µA	All
Vih	Logic Inputs High Level	2.4		Vcc + 0.5	V	
Vil	Logic Inputs Low Level	Vee - 0.5		0.8	V	
LAVH	Loop Amplifier High o/p Voltage	Vcc -1.1			V	Iout = 10 µA
LAVL	Loop Amplifier Low o/p Voltage			1.1	V	Iout = 10 µA
RLT	ADC Reference - top of ladder	2.35	2.5	2.65	V	
RLB	ADC Reference - bottom of ladder	1.15	1.3	1.45	V	
RDIFF	ADC Ladder Voltage (Voltage difference between top and bottom of ladder)	1.1	1.2	1.3	V	
REFI	TxDAC Reference Current	0.75	1	1.25	V	
RTI	ADC Reference - Source Current (TREFI/TREFQ)	6			mA	
RBI	ADC Reference - Sink Current (BREFI/BREFQ)	0.8			mA	see note 2

Notes:

1 Includes 2 mA (nomial) DAC reference current but excludes any current sourceconnected tt to the TX baseband inputs.

2 To conserve power the on-chip current sink capability s nominally 1 mA (800 µA maximum) while the reference for the top of the ladder has the capability to source up to 6 mA. To use external ADC's that have a ladder resistance requiring a greater current sink capability than this , an external pull down resistor must be placed between BREFI, BREFQ and ground.

Operating Characteristics (continued)

A.C. Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Receiver Section						
FIFRX	IF Input Frequency	200		400	MHz	
BBFRX	Rx Baseband Output 1 dB Bandwidth	2.0	5.0		MHz	
GR1	Receive Gain (AGC(4…0) = 00000)	23	27	29	dB	Rload => 100 ? AC coupled
GR2	Receive Gain (AGC(4…0) = 11111)	70	73	76	dB	Rload => 100 ? AC coupled
RGS	Receive Gain Step Accuracy	0.5-		0.5	dB	see note 1
GF1	Rx Gain Flatness			4	dB	across IF frequency band
NF	Noise Figure (DSB)		19	20.5	dB	RS = 50 ? maximum gain selected see note 2
RCMP1	Receiver 1 dB Compression point	6	7		dBm	AGC (4…0) = 00000; see note 3 Rload => 100 ? AC coupled
RCMP2	Receiver 1 dB Compression point	5.5	6.5		dBm	AGC (4…0) = 11111 see note 3
S11	Input reflection coefficient (single-ended)		11-		dB	referred tp 50 ? see note 4
SBB	Baseband Spurii 100 Hz - 1000 MHz		46-		dBc	baseband signal level 1.2 Vpp see note 5
AGCT	Receive AGC response time			100	ns	without baseband filter present
DCS1	DC settling time at IF2 (70 MHz)			300	ns	see note 6
PBRX	I/Q Receive phase balance			1	deg	
ABRX	I/Q Receive amplitude balance		0.2	0.3	dB	
SOV	Saturated O/P voltage at OPI/OPQ, any AGC setting		1.9		Vpp	10- dBm at RXIN, <1 Mhz in baseband
DCBB	DC offset, baseband output			150	mV	see note 7
LPF1	Internal Baseband low pass filter 3 dB cutoff		10		MHz	
LIM1	Limiter mode, maximum output		1	1.2	Vpp	see note B
RLIM	Limiter, o/p resistance (differential between RXFILP, RXFILN)	340	400	460	?	
GCL	Gain Change Rx Mode to Limiter mode	10.5-	11-	12-	dB	

Notes:

1 Receive gain step accuracy is for a single step in gain of either .5 dB, 5 dB or 10 dB
2 The SSB noise figure will be NF (SSB) ~ NF (DSB) + 3 dB
3 0 dBm≅ 1 mW
4 Usage of a resistor (R = 110 Ohms) placed directly in parallel with the input connector creates an improvement in S11, measured value S11 = -28.5 dB
5 With Dallen-key-filter (f3dB = 600 kHZ) present; fout = 250 kHz
6 DC settling time from change in AGC gain is to within 10% of the final DC value
7 Baseband DC offset is measured relative to the mid point of the ADC reference voltage
8 Measured at the final baseband output with Receive filters in place

Operating Characteristics (continued)

A.C. Characteristics (continued)

Symbol	Parameter	Min.	Typ.	Max.	Uni	Conditions
Transmitter Section						
FIFTX	Tx IF Input Frequency	200	350	400	MHz	
BBFTX	Tx Baseband Output 1 dB Bandwidth	2.0			MHz	
GF2	Tx Gain Flatness			4	dB	across IF frequency band
TXRIN	Tx baseband input resistance @ TxBBIN (differential)	425	500	575	Ω	
TMAX	Tx maximum O/P signal	0.2	0.25		Vpp	External load 100 ? each O/P ALC (2…0) = 111 at 0.2 dB compression - see note
TCG	Tx end-to-end transimpedance		0.12		V/mA	External load 100 ? each O/P ALC (2…0) = 111 - see note
TGS	Tx gain step accuracy	1.0-		1	dB	see note 3
TXROP	IF output resistance (differential)		200		Ω	
LOL1	Tx LO leakage (70 MHz)	66-	61-	57-	dBm	see notes 4, 5, 6
LOL2	Tx LO leakage (280 MHz)	49-	47-	46-	dBm	see notes 4, 5, 6
IRM	Image Rejection	42-	36-	30-	dBc	see note 5
STX	Tx Spurii - PLL reference and harmonics		65-		dBc	o/p signal level 0.25 Vpp - see note 7
MRTX	Tx baseband input resistor match (measured at TxBBIN)			1.0	%	see note 9
PBTX	I/Q Transmit phase balance		0.7	1	deg	
ABTX	I/Q Transmit amplitude balance		0.2	0.5	dB	
LBG1	Loop back Gain		0.6		V/mA	see note 10

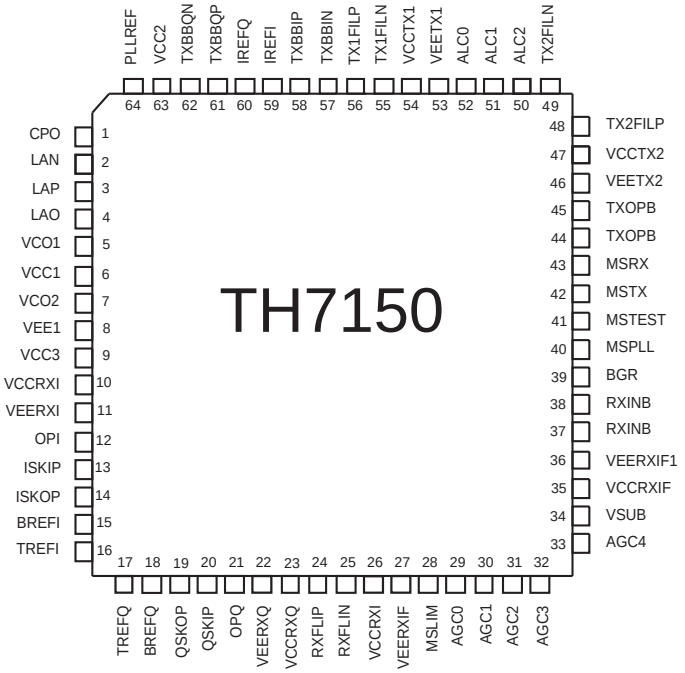
Notes:

1 The transmit output compression is measured with the 70 MHz LC filters present component values shown in the application diagram
2 The transmit end-toend transimpedance is (differential current in)/(differential current out) such that a 2 mA peak-peak input from a DAC will give 250 mVpp at the O/P when correctly terminated. Driving an open crcuit load the transimpedancewill be 6 dB higher.
3 Transmit gain step accuracy is for a single step in gain of either 3 dB, 6 dB or 12 dB
4 In 200 ohms divverential measured at Tx output with ALC (2...0) = 111
5 Measured with Tx LC filters present - components values as shown in the application diagram
6 0 dBm 1 mW
7 Measured with the 70 MHz and 350 MHz LC filters present - component values as shown in the application diagram
8 STX4 excludes legitimate mixed products
9 This is match between all 4 250 ohms input resistors
10 The loop back gain is such that a 2 mA differential pk-pk current input DAC (1 mA full scale current for each input) will give a 1.2 Vpp single ended output at the fnal baseband output

A.C. Characteristics (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Transmitter Section						
LBG2	Loop back Gain variation	-2.0		2.0	dB	see note
TX70	Resistance @ 70 MHz Transmit IF (differential)	340	400	460	Ω	
TX350	Resistance @ 350 MHz Transmit IF (differential)	340	400	460	Ω	
Note	The loop back gain variation is defined for a current input at the Tx baeband inputs referenced (normally by a DAC) to the on-chip Tx DAC reference current i.e. this specification excludes any variation due to the 250 ohms on-chip resistord at the Tx baseband inputs.					

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Frequency Synthesizer Section						
PLLR	PLL reference frequency		2		MH	
PDG	Phase Detector Gain		32		?A ra	
FVCO	VCO Operating Frequency	160	280	320	MHz	
VRL	PLL Input Reference Level	0.7	1	2	Vpp	AC coupled
RSP	Reference Spurii Level		60-		dBc	
FSH	Frequency Shift Per Mode			200	kHz	between modes Rx, Tx and PLL
PN	VCO SSB Phase Noise		86-	85-	dBc /Hz	25 kHz offset, Tank Q = 20
OPNO	PLL Loop amplifier input referred noise		10	15	nV/ Hz	see note
Note: Loop filter not present						



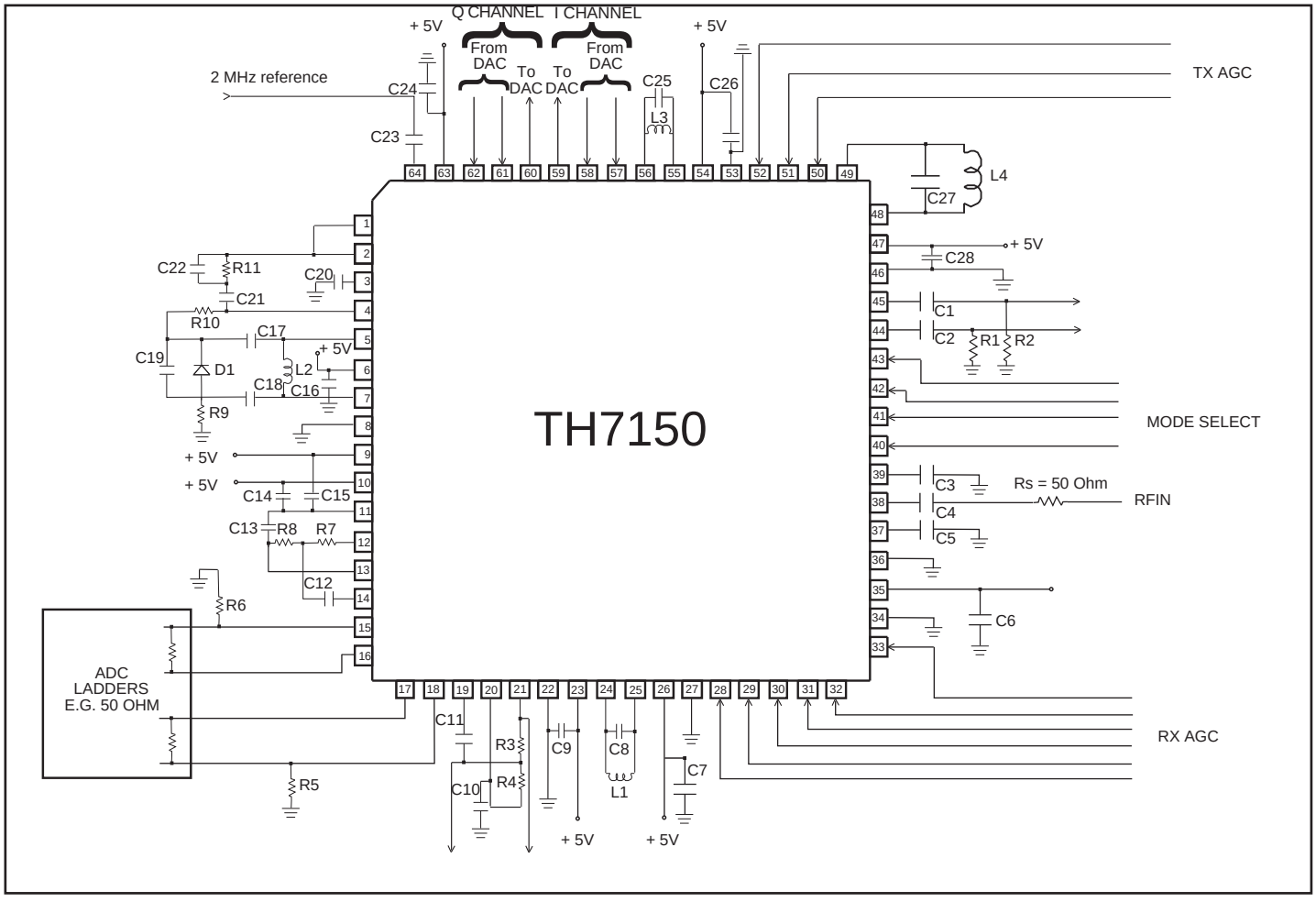
Pinout Information (continued)

Pin No.	Symbol	Function
1	CPO	Charge pump output
2	LAN	Loop filter op amp inveritng input
3	LAP	Loop filter op amp non-inveritng input
4	LAO	Loop filter op amp output
5	VCO1	Tank pin (+ve)
6	VCC1	VCO positive pwer supply
7	VCO2	Tank pin (-ve)
8	VEE1	PLL negative power supply (0 V)
9	VCC3	PLL positive power supply
10	VCCRXI	Receive baseband positive power supply (I channel)
11	VEERXI	Receive baseband negative (0 V) power supply (I channel)
12	OPI	Rx I channel baseband output
13	ISKIP	voltage follower input (I channel)
14	ISKOP	Voltage follower output (I channel)
15	BREFI	ADC reference voltage, bottom (I channel)
16	TREFI	ADC reference voltage, top (I channel)
17	TREFQ	ADC reference voltage, top (Q channel)
18	BREFQ	ADC reference voltage, bottom (Q channel)
19	QSKOP	Voltage follower output (Q channel)
20	QSKIP	voltage follower input (Q channel)
21	OPQ	Rx Q channel baseband output
22	VEERXQ	Receive baseband negative (0 V) power supply (Q channel)
23	VCCRXQ	Receive baseband positive power supply (Q channel)
24	RXFLIP	Limiter Load Resistor (optional external band pass filter)
25	RXFLIN	Limiter Load Resistor (optional external band pass filter)
26	VCCRXI	Receive 2nd IF positive power supply
27	VEERXIF	Receive 2nd IF negative power supply (0 V)
28	MSLIM	Mode select enable Limiter
29	AGC0	Rx AGC control input
30	AGC1	Rx AGC control input
31	AGC2	Rx AGC control input
32	AGC3	Rx AGC control input

Pin	Symbo	Function
33	AGC4	Rx AGC control input
34	VSUB	Substrate power supply (0
35	VCCRXIF	Receive 1st IF positive power supply
36	VEERXIF1	Receive 1st IF negative power supply (0 V)
37	RXINB	Receive input (inverted) - a.c.
38	RXINB	Receive input
39	BGR	Band gap reference
40	MSPLL	Mode select - PLL mode
41	MSTEST	Mode select - test mode
42	MSTX	Mode select - transmit mode
43	MSRX	Mode select - receive mode
44	TXOPB	Transmit path output(complementary)
45	TXOPB	Transmit path output
46	VEETX2	Transmit negative (0 V) power supply
47	VCCTX2	Transmit negative power supply
48	TX2FILP	Image reject mixer (external bandpass filter)
49	TX2FILN	Image reject mixer (external bandpass filter)
50	ALC2	Transmit path gain adjust 3
51	ALC1	
52	ALC0	Transmit path gain adjust 1
53	VEETX1	Transmit negative (0 V) power supply
54	VCCTX1	Transmit positive power supply
55	TX1FILN	I/Q modulator output (optional external bandpass filter)
56	TX1FILP	I/Q modulator output (optional external bandpass filter)
57	TXBBIN	Transmit Baseband Input (I channel) - complementary input
58	TXBBIP	Transmit Baseband Input (I channel)
59	IREFI	External DAC reference current (Q channel)
60	IREFQ	(Q channel) - complementary input
61	TXBBQP	Transmit Baseband input (Q channel)
62	TXBBQN	Transmit Baseband input (Q channel)
63	VCC2	Loop amplifier positive power supply
64	PLLREF	PLL reference clock

Pin Definition List
Application Diagram

The application diagram below is provided to assist the customer in using the IC. The configuration can be changed for other applications.

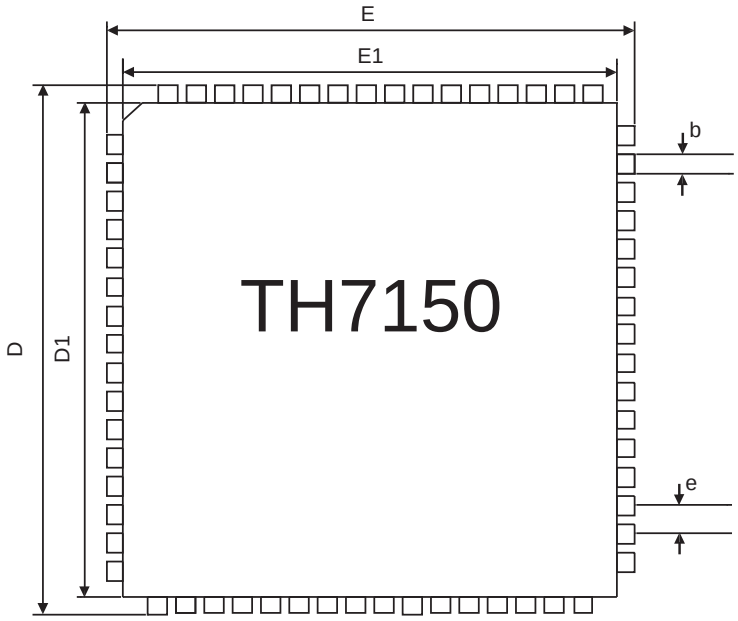


Component List for Application Diagram

Component	Function	Value	Unit
C1, C2	Transmit O/P AC coupling	100	pF
C3	Band gap Reference Decouple	10	nF
C4	LNA input AC coupling	100	pF
C5	LNA input AC decoupling	100	pF
C6, C7, C9, C14, C15, C16, C24, C26, C28	VCC decoupling	10	nF
C8	70 MHz Receive (limiter) filter		
C10, C13	Sallen Key Filter		
C11, C12	Sallen Key Filter		
C17, C18	VCO AC coupling	100	pF
C19	VCO tank capacitor		pF
C20	Loop Filter Decouple	10	nF
C21	Loop Filter		
C22	Loop Filter		
C23	PLL Reference AC Coupling		
C25	70 MHz Transmit Filter	9	pF
C27	350 MHz Transmit Filter	9	pF
R1, R2	Transmit Termination	100	Ω
R3, R4, R7, R8	Sallen Key Filter		Ω
R5, R6	ADC Ladder Pull Down	400	Ω
R9, R10	VCO DC Block	100	k
R11	Loop Filter		
D1	Varacator Diode		
L1	70 MHZ Receive Filter		
L2	VCO Tank		
L3	70 MHz Transmit Filter	575	nH
L4	350 MHz Transmit Filter	23	nH

Note: not specified values are application specific and depend on PCB parasitics

Package Information



Thin Quad Flat Packsge (TQFP)												
Package Type		E1/D1	A	A1	A2	e	b	L	?	E/D	Co-planarity	Package Code
TQFP 64	min	0.547		0.002	0.053	0.031	0.010	0.018		0.620		NK64E
	max	0.555	0.063	0.006	0.057		0.018	0.030	7°	0.640	0.004	
Dimensions in inches, original dimension: millimeters												

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	max	0.555	0.063	0.006	0.057		0.018	0.030	7°	0.640	0.004	
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