DSC400

Configurable Four Output, Low Jitter Crystal-less™ Clock Generator

General Description

The DSC400 is a four output crystal-less™ clock generator. It utilizes Micrel's proven PureSilicon™ MEMS technology to provide excellent jitter and stability while incorporating additional device functionality.

The frequencies of the outputs can be identical or independently derived from common PLLs.

Each output may be configured independently to support a single ended LVCMOS interface or a differential interface. Differential options include LVPECL, LVDS, or HCSL.

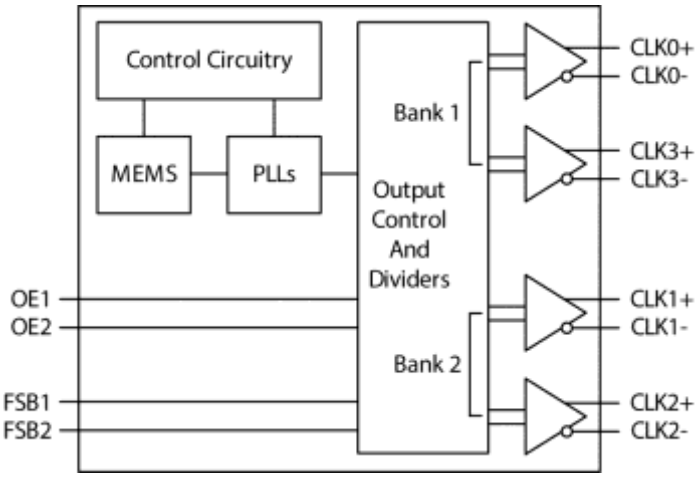
The DSC400 provides two independent select lines for choosing between two sets of pre-configured frequencies per bank. It also has two OE pins to allow for enabling and disabling outputs.

The DSC400 is packaged in a 20-pin QFN (5mm x 3.2mm) and is available in extended commercial and industrial temperature grades.

Features

- **Low RMS Phase Jitter: <1 ps (typ)**
- **High Stability: ±25ppm, ±50ppm**
- **Wide Temperature Range**
  - Ext. commercial: -20°C to 70°C
  - Industrial: -40°C to 85°C
- **High Supply Noise Rejection: -50 dBc**
- **Four format configurable outputs:**
  - LVPECL, LVDS, HCSL, LVCMOS
- **Available Pin-Selectable frequency table**
  - 1 pin per bank for 2 frequency sets
- **Wide Freq. Range:**
  - 2.3 MHz – 460 MHz
- **20 QFN Footprint (5mm x 3.2mm)**
- **Excellent Shock & Vibration Immunity**
  - Qualified to MIL-STD-883
- **High Reliability**
  - 20x better MTF than quartz based devices
- **Wide Supply Range of 2.25 to 3.6 V**
- **Lead Free & RoHS Compliant**
- **AEC-Q100 Automotive Qualified**

Block Diagram



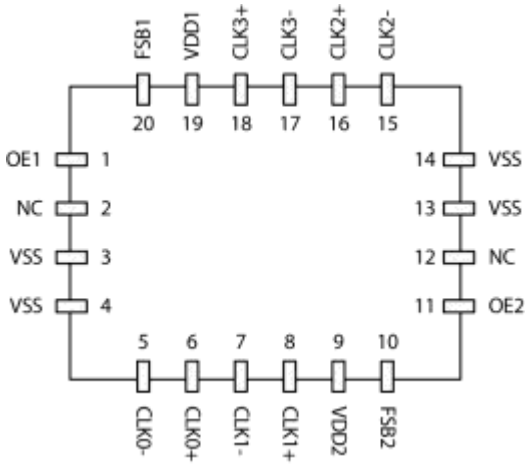
Applications

- **Communications and Networks**
- **Ethernet**
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- **Storage Area Networks**
  - SATA, SAS, Fibre Channel
- **Passive Optical Networks**
  - EPON, 10G-EPON, GPON, 10G-PON
- **HD/SD/SDI Video & Surveillance**
- **Automotive**
- **Media and Video**
- **Embedded and Industrial**

Pin Description

Pin No.	Pin Name	Pin Type	Description
1	OE1	I	Output Enable for Bank1 (CLK0 and CLK3); active high – See Table 1
2	NC	NA	Leave unconnected or connect to ground
3	VSS	Power	Ground
4	VSS	Power	Ground
5	CLK0-	O	Complement output of differential pair 0 (off when in LVCMOS format)
6	CLK0+	O	True output of differential pair 0 or LVCMOS output 0
7	CLK1-	O	Complement output of differential pair 1 (off when in LVCMOS format)
8	CLK1+	O	True output of differential pair 1 or LVCMOS output 1
9	VDD2	Power	Power Supply for Bank2 (CLK1 and CLK2)
10	FSB2	I	Input for selecting pre-configured frequencies on Bank2 (CLK1 and CLK2)
11	OE2	I	Output Enable for Bank2 (CLK1 and CLK2); active high – See Table 1
12	NC	NA	Leave unconnected or connect to ground
13	VSS	Power	Ground
14	VSS	Power	Ground
15	CLK2-	O	Complement output of differential pair 2 (off when in LVCMOS format)
	CLK2+	O	True output of differential pair 2 or LVCMOS output 2
17	CLK3-	O	Complement output of differential pair 3 (off when in LVCMOS format)
18	CLK3+	O	True output of differential pair 3 or LVCMOS output 3
19	VDD1	Power	Power Supply for Bank1 (CLK0 and CLK3)
20	FSB1	I	Input for selecting pre-configured frequencies on Bank1 (CLK0 and CLK3)

Pin Diagram



20 QFN 5.0 × 3.2mm

Operational Description

The DSC400 is a crystal-less™ clock generator. Unlike older clock generators in the industry, it does not require an external crystal to operate; it relies on the integrated MEMS resonator that interfaces with internal PLLs. This technology enhances performance and reliability by allowing tighter frequency stability over a far wider temperature range. In addition, the higher resistance to shock and vibration decreases the aging rate to allow for much improved product life in the system.

Inputs

There are 4 input signals in the device. Each has an internal (40kΩ) pull up to default the selection to a high (1). Inputs can be controlled through hardware strapping method with a resistor to ground to assert the input low (0). Inputs may also be controlled by other components' GPIOs

In case more than one frequency set is desired, FSB1 and FSB2 are used for independently selecting one of two sets per bank. FSB1 selects the pre-configured set on Bank1 (CLK0 and CLK3) and FSB2 selects the pre-configured set on Bank2 (CLK1 and CLK2), as shown in table 2.

If there is a requirement to disable outputs, the inputs OE1 and OE2 are used in conjunction to disable the banks of outputs. Outputs are disabled in tristate (Hi-Z) mode, see Table 1 below.

Table 1: Output Enable (OE) Selection Table

OE1	OE2	Bank1 (CLK0 & CLK3)	Bank2 (CLK1 & CLK2)
0	0	Hi-Z	Hi-Z
0	1	Hi-Z	Running
1	0	Running	Hi-Z
1	1	Running	Running

Outputs

The four outputs are grouped into two banks. Each bank is supplied by an independent VDD to allow for optimized noise isolation between the two banks. Each bank provides two synchronous outputs generated by a common PLL:

- Bank1 is composed of outputs CLK0 and CLK3
- Bank2 is composed of outputs CLK1 and CLK2

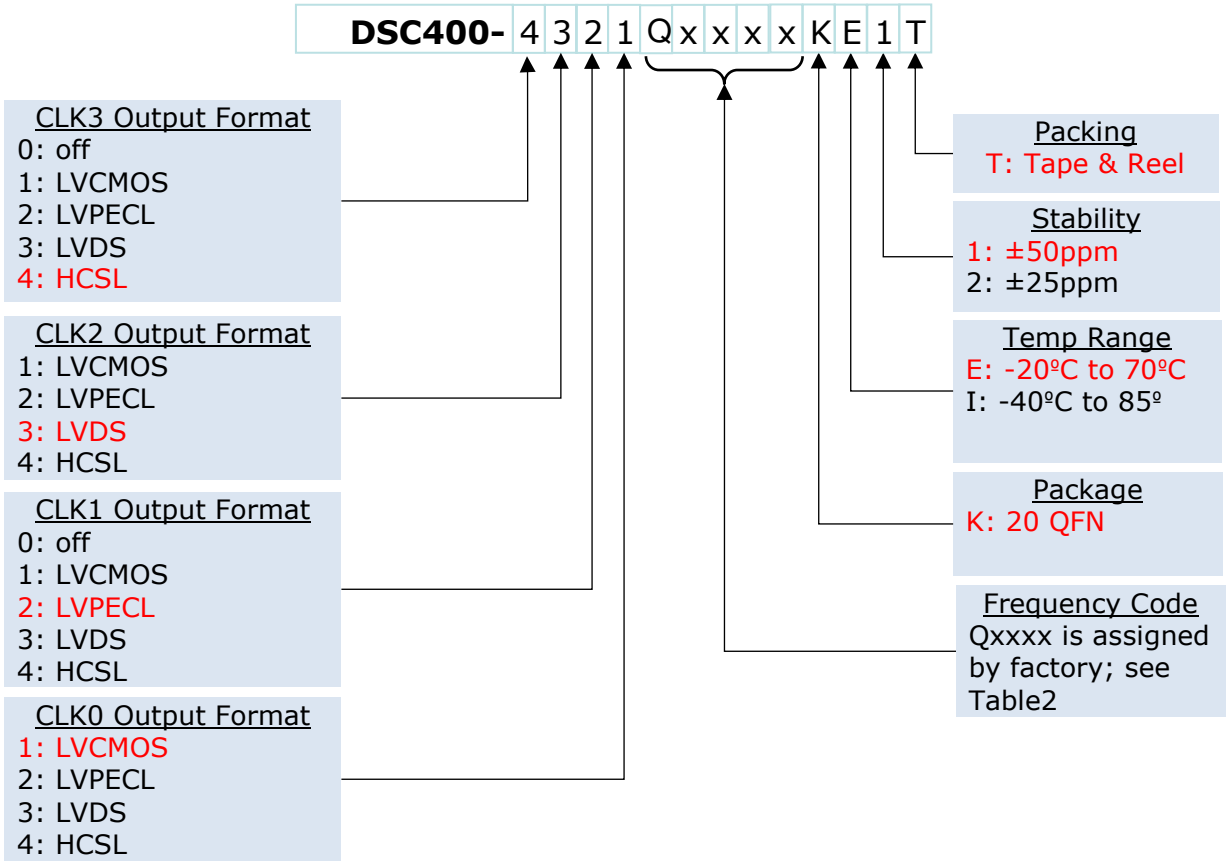
Each output maybe pre-configured independently to be one of the following formats: LVCMOS, LVDS, LVPECL or HCSL. In case the output is configured to be the single ended LVCMOS, the frequency is generated on the true output (CLKx**+**) and the complement output (CLKx**-**) is shut off in a low state. Frequencies can be chosen from 2.3MHz to 460MHz for differential outputs and from 2.3MHz to 170MHz on LVCMOS outputs.

Power

VDD1 and VDD2 supply the power to banks 1 and 2 respectively. Each VDD may have different supply voltage from the other as long as it is within the 2.25V to 3.6V range. Each VDD pin should have a 0.1µF capacitor to filter high frequency noise. VSS is common to the entire device.

Ordering Information

(Example shown in red font)



Factory configuration code assignment of Qxxxx

The DSC400 is meant for customers to define their own frequency requirements at the four available outputs. The Qxxxx number identifies these specific customer requirements and is assigned by the factory.

Table 2: Example of how FSB1 and FSB2 are applied and the Qxxxx code assignment

Bank1		FSB1		Qxxxx number
	Outputs	1 (default)	0	Q0001
	CLK0	125 MHz	150 MHz	
	CLK3	50 MHz	25 MHz	
Bank2		FSB2		
	Outputs	1 (default)	0	
	CLK1	156.25 MHz	100 MHz	
	CLK2	156.25 MHz	100 MHz	

Absolute Maximum Ratings

Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	V_{DD}+0.3	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD HBM MM CDM	-	 4000 400 1500	V	

Note: 1000+ years of data retention on internal memory

Specifications (Unless specified otherwise: Ta =25° C, VDD = 3.3V)

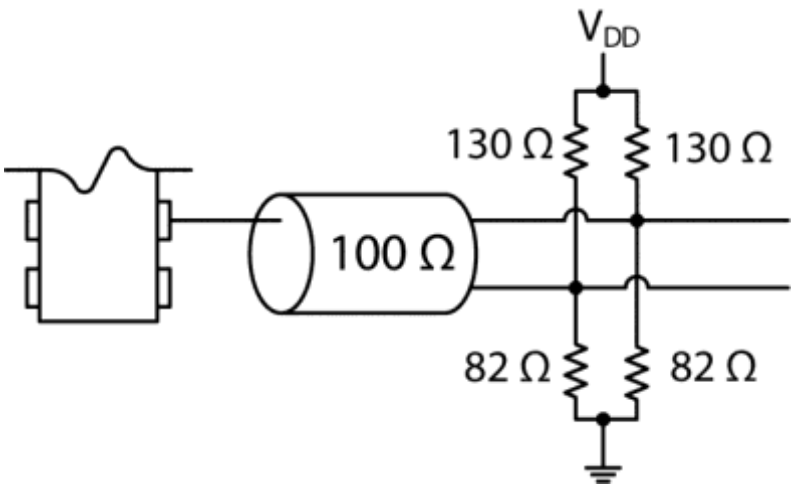
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage[1]	V_{DD}		2.25		3.6	V
Supply Current – Core[2]	I_{DDcore}	OE(1:2) = 0 All outputs are disabled		40	44	mA
Frequency Stability	Δf	All temp and VDD ranges			±25 ±50	ppm
Aging – first year	Δf_{Y1}	1 year @25°C			±5	ppm
Aging – after first year	Δf_{Y2}^{+}	Year 2 and beyond @25°C			<±1/yr	ppm
Startup Time[3]	t_{SU}	T=25°C			5	ms
Input Logic Levels Input logic high Input logic low	 V_{IH} V_{IL}		 0.75xV_{DD} -		 - 0.25xV_{DD}	V
Output Disable Time[4]	t_{DA}	OE(1:2) transition from 1 to 0			5	ns
Output Enable Time[4]	t_{EN}	OE(1:2) transition from 0 to 1			20	ns
Pull-Up Resistor	R_{PU}	All input pins have an internal pull-up		40		kΩ

Notes:
1. V_{DD} pins should be filtered with a 0.1µF capacitor connected between V_{DD} and V_{SS}.
2. The addition of IDD_{core} and IDD_{io} provides total current consumption of the device
3. t_{su} is time to 100 ppm stable output frequency after V_{DD} is applied and outputs are enabled.
4. Output Waveform figures below the parameters. See Output Waveform section

LVPECL Outputs[6]						
Output Logic Levels Output logic high Output logic low	 V_{OH} V_{OL}	R_L=50Ω	 V_{DD}-1.08 -		 - V_{DD}-1.55	V
Pk to Pk Output Swing		Single-Ended		800		mV
Output Transition time[4] Rise Time Fall Time	 t_R t_F	20% to 80% R_L=50Ω		250		ps
Frequency	f_0	Single Frequency	2.3		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Supply Current – IO[2]	I_{DDio}	Per output at 125MHz		35	38	mA
Period Jitter[5]	J_{PER}	CLK(0:3) = 156.25 MHz		2.5		ps_{RMS}
Integrated Phase Noise	J_{PH}	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.25 0.38 1.7	 2	ps_{RMS}

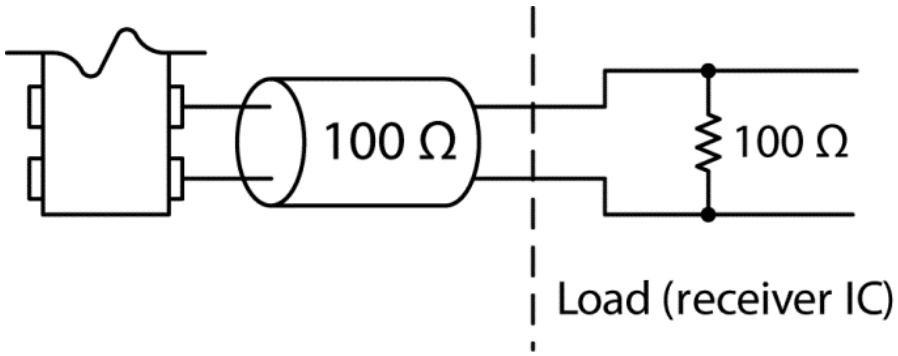
Notes:
5. Period Jitter includes crosstalk from adjacent output
6. LVPECL applicable to ext. commercial temperature only

LVPECL: Typical Termination Scheme



LVDS Outputs						
Output offset Voltage	V_{OS}	R=100Ω Differential	1.125		1.4	V
Delta Offset Voltage	ΔV_{OS}				50	mV
Pk to Pk Output Swing	V_{PP}	Single-Ended		350		mV
Output Transition time[3] Rise Time Fall Time	 t_R t_F	 20% to 80% R_L=50Ω, C_L= 2pF		200		ps
Frequency	f_0	Single Frequency	2.3		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Supply Current – IO[2]	I_{DDio}	Per output at 125MHz		9	12	mA
Period Jitter	J_{PER}			2.5		ps_{RMS}
Integrated Phase Noise	J_{PH}	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.28 0.4 1.7	 2	ps_{RMS}

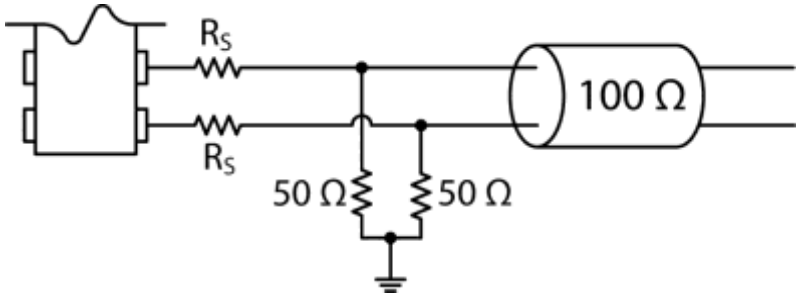
LVDS: Typical Termination Scheme



If the 100Ω clamping resistor does not exist inside the receiving device, it should be added externally on the PCB and placed as close as possible to the receiver.

HCSL Outputs						
Output Logic Levels Output logic high Output logic low	 V_{OH} V_{OL}	 R_L=50Ω	 0.725 -	 	 - 0.1	V
Pk to Pk Output Swing		Single-Ended		750		mV
Output Transition time[3] Rise Time Fall Time	 t_R t_F	 20% to 80% R_L=50Ω, C_L= 2pF	 200	 	 400	ps
Frequency	f_0	Single Frequency	2.3		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Supply Current – IO[2]	I_{DDio}	Per output at 125MHz		20	22	mA
Period Jitter	J_{PER}			2.5		ps_{RMS}
Integrated Phase Noise	J_{PH}	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.25 0.37 1.7	 2	ps_{RMS}

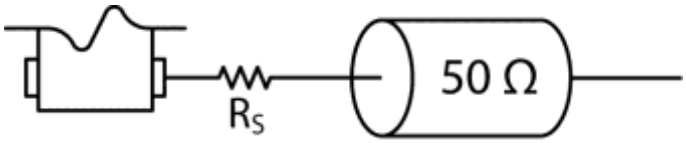
HCSL: Typical Termination Scheme



R_S is a series resistor implemented to match the trace impedance. Depending on the board layout, the value may range from 0 to 30Ω

LVCMOS Outputs						
Output Logic Levels Output logic high Output logic low	 V_{OH} V_{OL}	I=±6mA	 0.9xV_{DD} -		 - 0.1xV_{DD}	V
Output Transition time[3] Rise Time Fall Time	 t_R t_F	20% to 80% C_L=15pF		 1.1 1.3	 2 2	ns
Frequency	f_0	All temp range except Auto Auto temp range	2.3		170 100	MHz
Output Duty Cycle	SYM		45		55	%
Supply Current – IO[2]	I_{DDio}	Per output at 125MHz, C_L=15pF		11	14	mA
Period Jitter	J_{PER}	CLK(0:3) =125MHz		3		ps_{RMS}
Integrated Phase Noise	J_{PH}	200kHz to 20MHz @ 125MHz 100kHz to 20MHz @ 125MHz 12kHz to 20MHz @ 125MHz		0.3 0.38 1.7	 2	ps_{RMS}

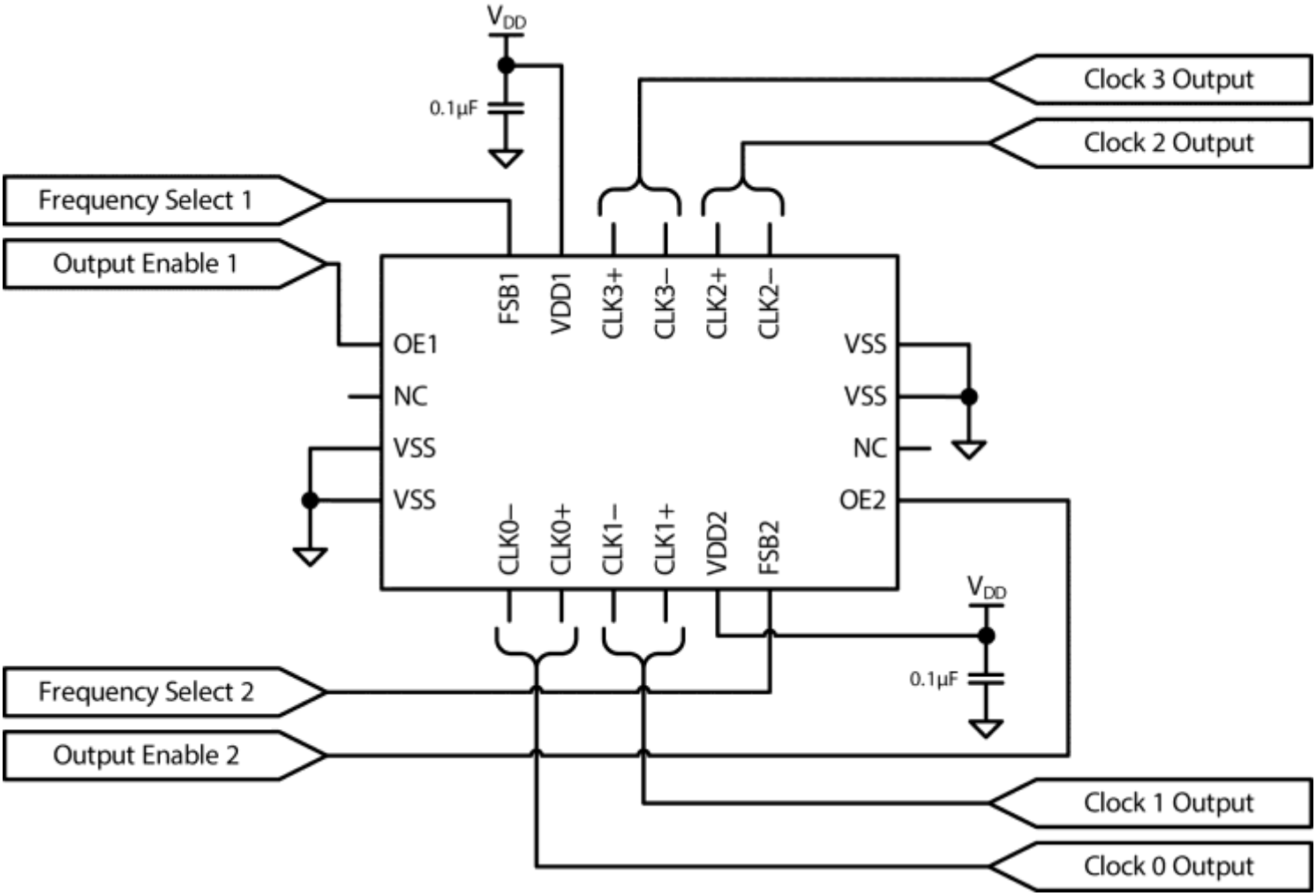
LVCMOS: Typical Termination Scheme



R_S is a series resistor implemented to match the trace impedance to that of the clock output. Depending on the board layout, the value may range from 0 to 27Ω

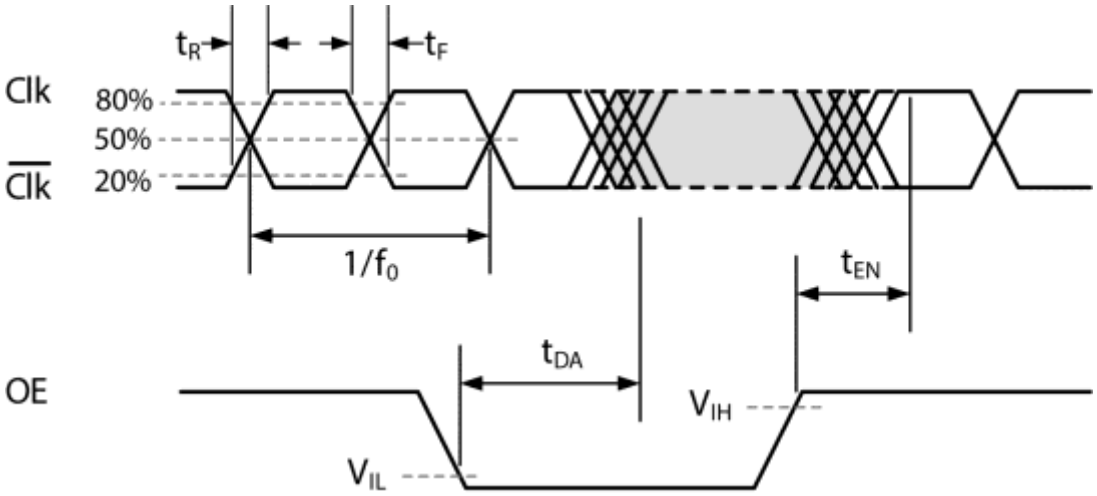
Connection Diagram:

The connection Diagram below includes recommended capacitors to be placed on each VDD for noise filtering.

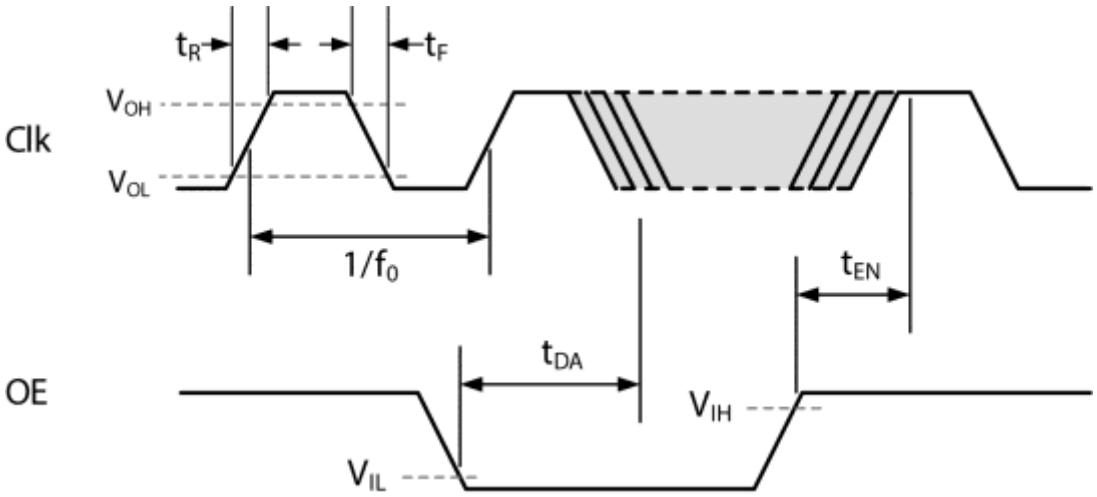


Output Waveform

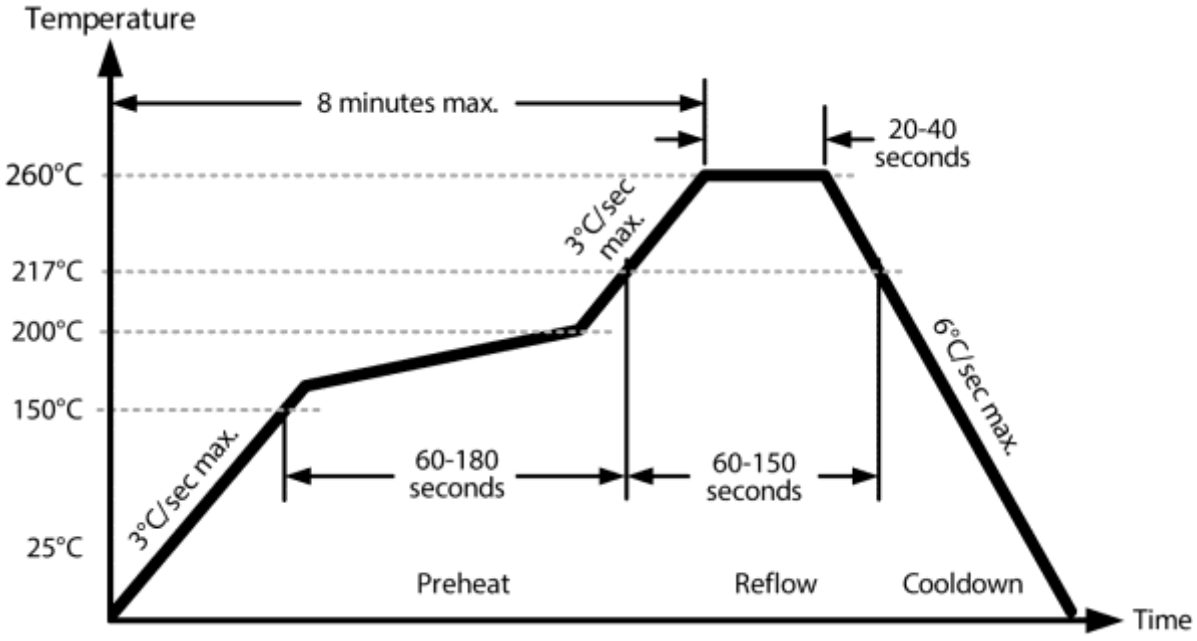
- **Differential Output (LVDS, LVPECL, HCSL)**



- **LVCMOS Output**

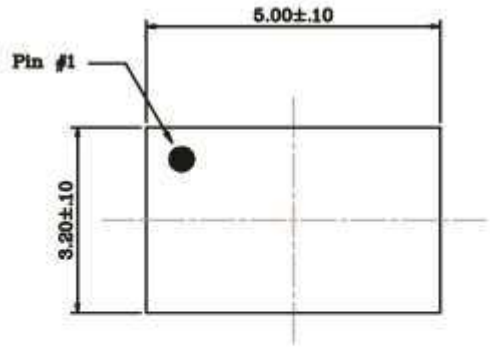


Solder Reflow Profile

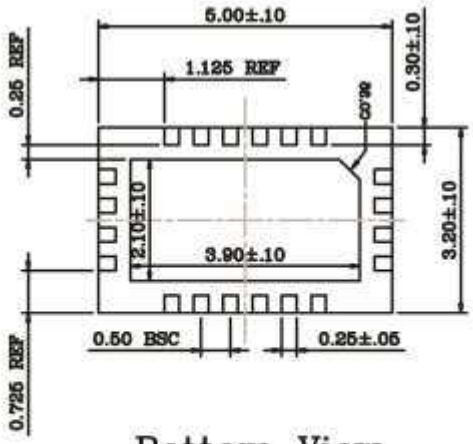


MSL 1 @ 260°C refer to JSTD-020C	
Ramp-up rate (200°C to peak temp)	3°C/sec max.
Preheat time 150°C to 200°C	60-180 sec
Time maintained above 217°C	60-150 sec
Peak temperature	255-260°C
Time within 5°C of actual peak	20-40 sec
Ramp-down rate	6°C/sec max.
Time 25°C to peak temperature	8 min max.

Package Dimensions 20 QFN, 5.0mm x 3.2 mm

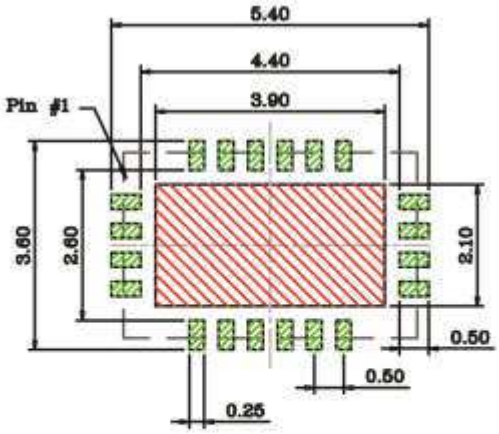


Top View



Bottom View

Side View

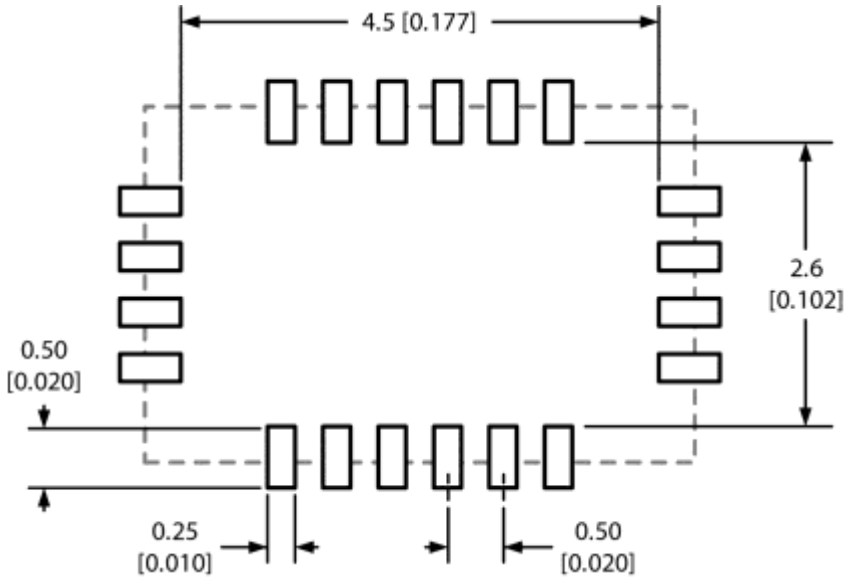


Recommended Land Pattern

NOTE:
1. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
2. Red shaded rectangle in Recommended Land Pattern is keep-out area.

Recommended Solder Pad Layout

units: mm[inches]



Connect the center pad to ground plane for best thermal performance

Disclaimer:

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