

Aerospace and defense N-channel 100 V, 2.3 mΩ typ., 180 A STripFET™ F7 Power MOSFET in a TO-220 package

Datasheet - target specification

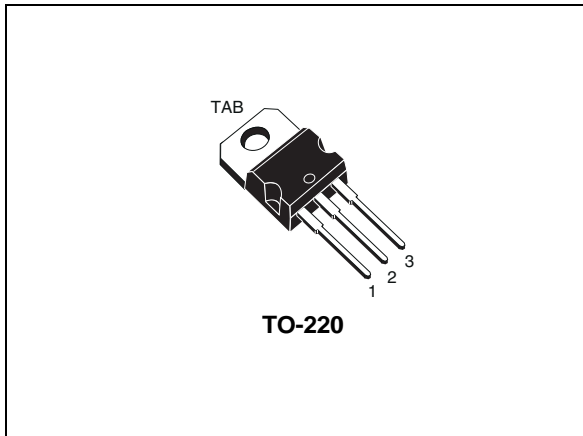
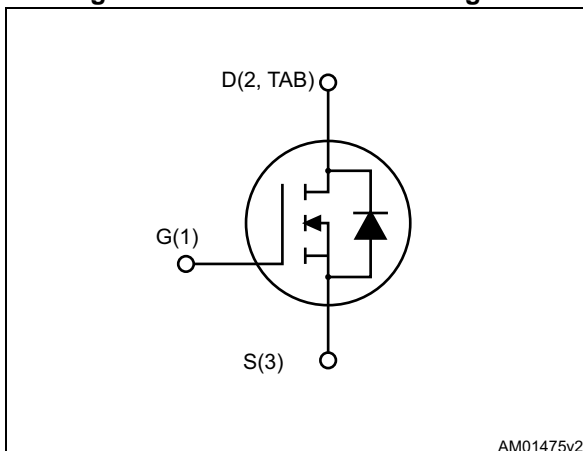


Figure 1. Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
RTP315N10F7	100 V	2.7 mΩ	180 A

- Intended for use in aerospace and defense applications
- Dedicated traceability and part marking
- Production parts approval documents available
- Adapted extended life time and obsolescence management
- Extended product change notification process
- Designed and manufactured to meet sub ppm quality goals
- Extended screening capability on request
- Ultra low on-resistance
- 100% avalanche tested

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes the STripFET™ F7 technology with enhanced trench-gate structure that result in very low on-state resistance while also reducing internal capacitances and gate charge for faster and very efficient switching.

Table 1. Device summary

Order code	Marking	Package	Packaging
RTP315N10F7	R315N10F7	TO-220	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	180	A
$I_D^{(1)}$	Drain current (continuous) at $T_C=100^\circ\text{C}$	120	A
$I_{DM}^{(2)}$	Drain current (pulsed)	720	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	315	W
	Derating factor	2.1	W/ $^\circ\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy ($T_J = 25^\circ\text{C}$, $L=0.55\text{ mH}$, $I_{AS}=65\text{ A}$)	1	J
T_j	Operating junction temperature	- 55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature		$^\circ\text{C}$

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. Starting $T_J=25^\circ\text{C}$, $I_D=60\text{ A}$, $V_{DD}=50\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.48	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C/W}$

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 250\ \mu A$	100			V
I_{DSS}	Zero gate voltage drain current ()	$V_{GS} = 0, V_{DS} = 100\ V$			1	μA
		$V_{GS} = 0, V_{DS} = 100\ V, T_C = 125\text{ °C}$			100	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0, V_{GS} = 20\ V$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu A$	2.5	3.5	4.5	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\ V, I_D = 60\ A$		2.3	2.7	m Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0, V_{DS} = 25\ V, f = 1\ MHz$	-	12800	-	pF
C_{oss}	Output capacitance		-	3500	-	pF
C_{rss}	Reverse transfer capacitance		-	170	-	pF
Q_g	Total gate charge	$V_{DD} = 50\ V, I_D = 180\ A, V_{GS} = 10\ V$ (see Figure 14)	-	180	-	nC
Q_{gs}	Gate-source charge		-	78	-	nC
Q_{gd}	Gate-source charge		-	34	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\ V, I_D = 90\ A, R_G = 4.7\ \Omega, V_{GS} = 10\ V$ (see Figure 13 , Figure 18)	-	62	-	ns
t_r	Rise time		-	108	-	ns
$t_{d(off)}$	Turn-off delay time		-	148	-	ns
t_f	Fall time		-	40	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		180	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		720	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=60\text{ A}$, $V_{GS}=0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD}=180\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=80\text{ V}$, $T_j=150^\circ\text{C}$ (see Figure 15)	-	85		ns
Q_{rr}	Reverse recovery charge		-	200		nC
I_{RRM}	Reverse recovery current		-	4.7		A

1. Pulse width limited by safe operating area.

2. Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

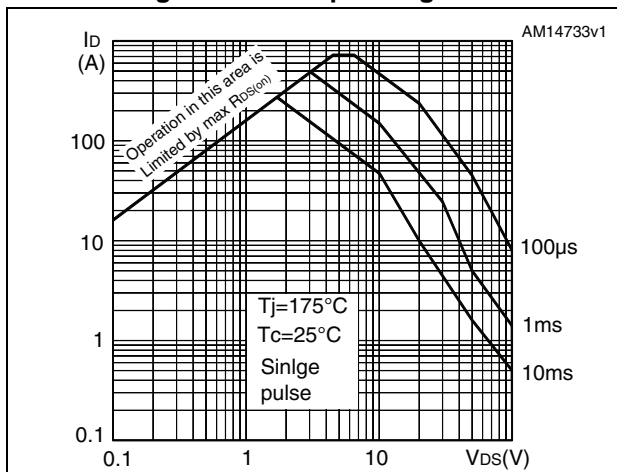


Figure 3. Thermal impedance

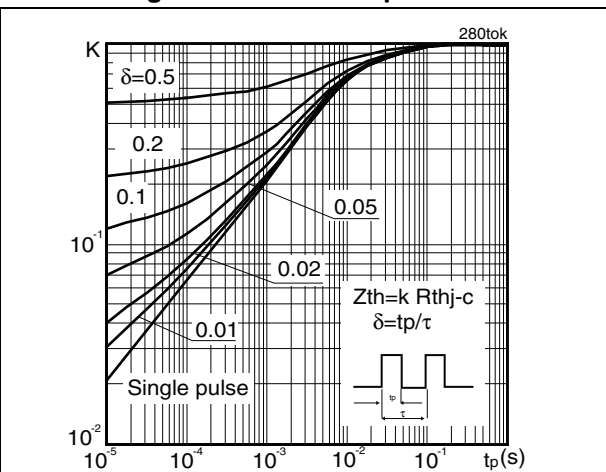


Figure 4. Output characteristics

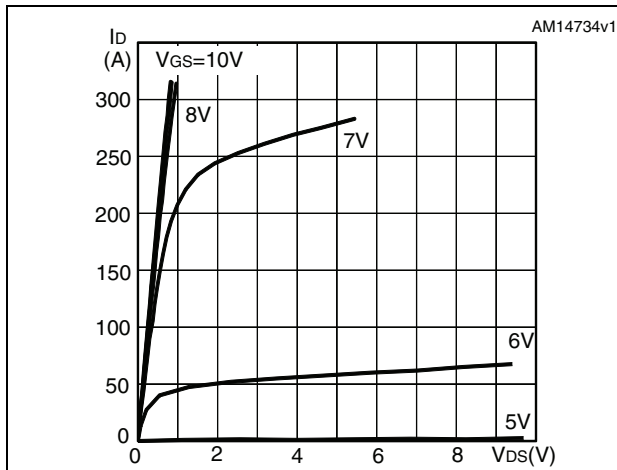


Figure 5. Transfer characteristics

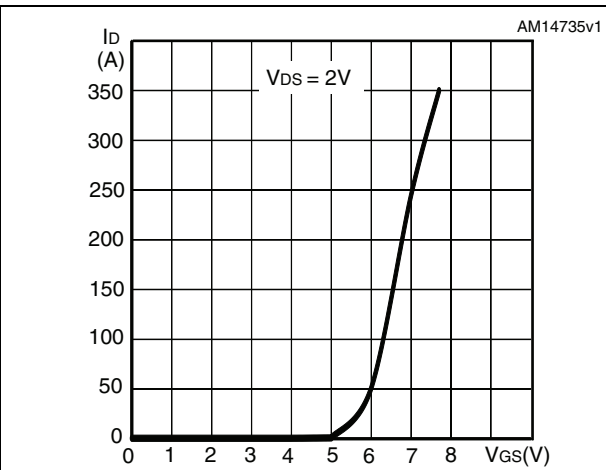


Figure 6. Gate charge vs gate-source voltage

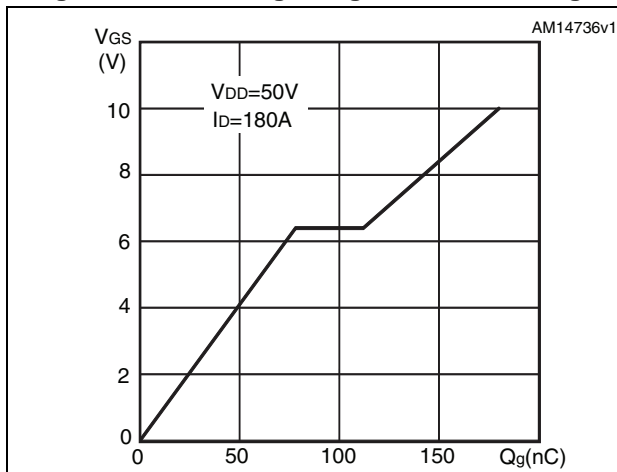


Figure 7. Static drain-source on-resistance

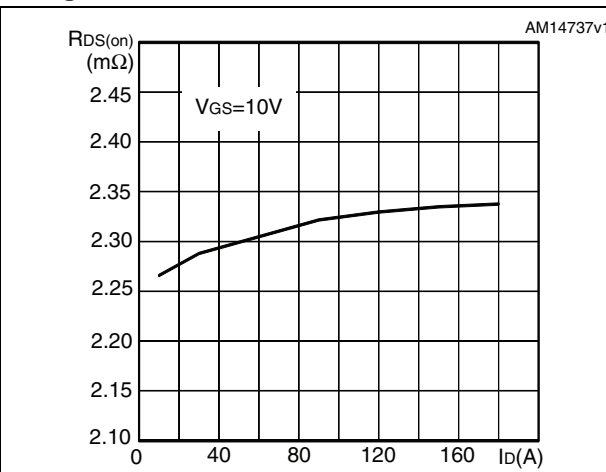


Figure 8. Capacitance variations

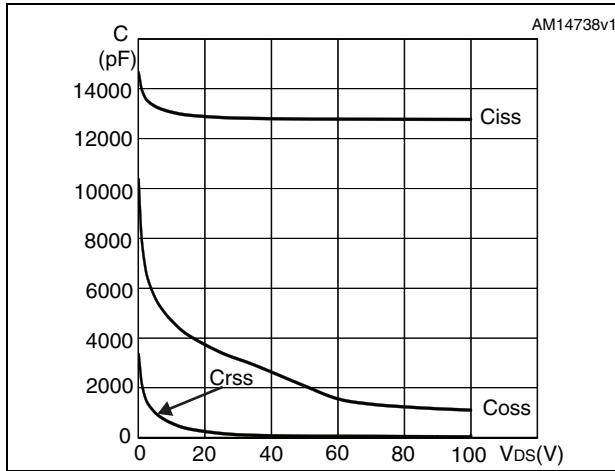


Figure 9. Source-drain diode forward characteristics

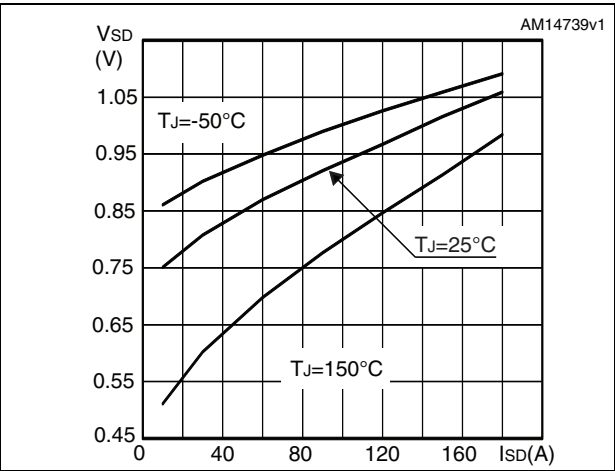


Figure 10. Normalized gate threshold voltage vs temperature

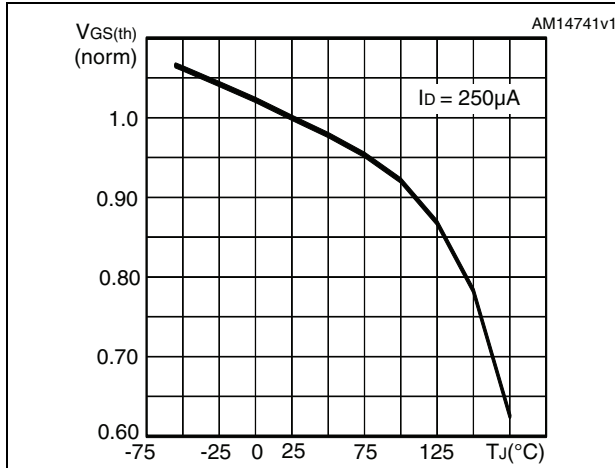


Figure 11. Normalized on-resistance vs temperature

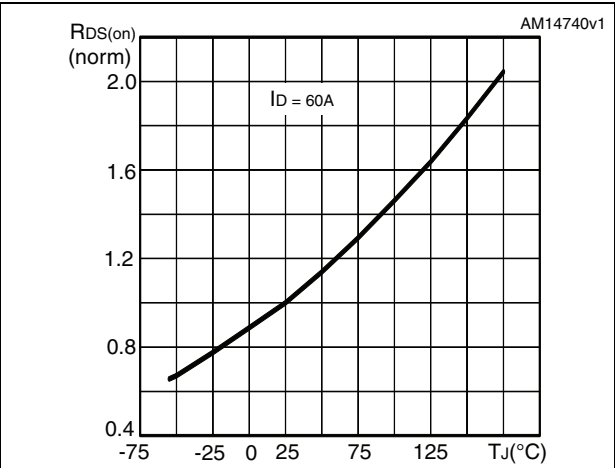
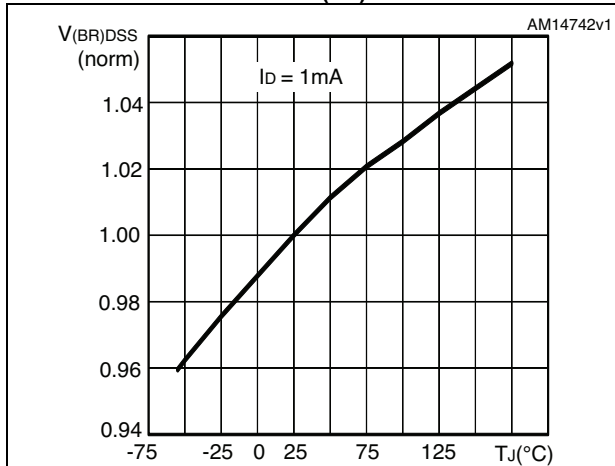


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 13. Switching times test circuit for resistive load

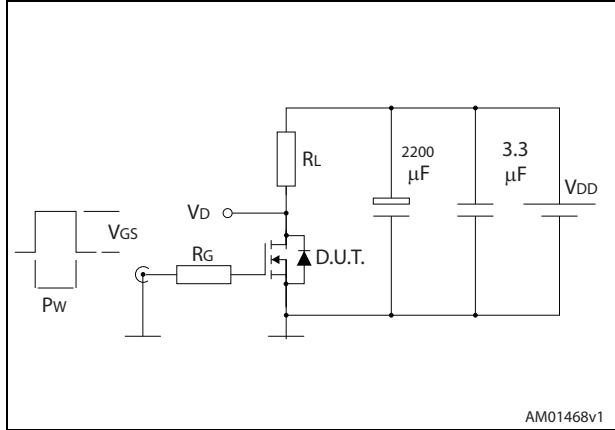


Figure 14. Gate charge test circuit

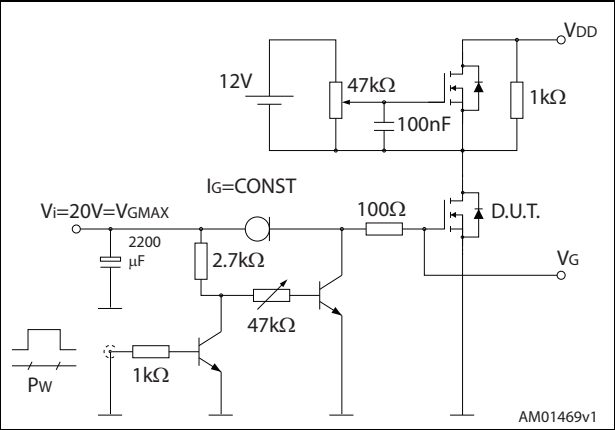


Figure 15. Test circuit for inductive load switching and diode recovery times

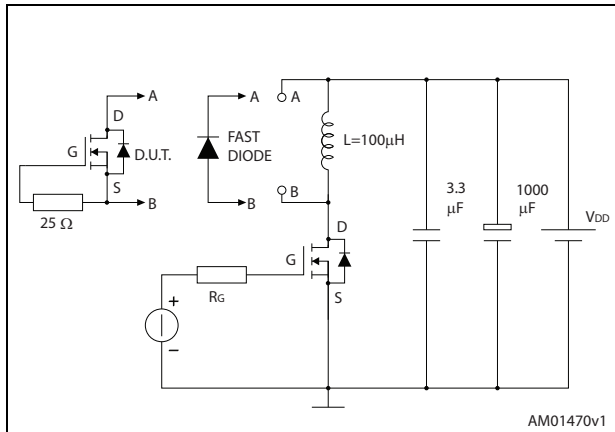


Figure 16. Unclamped inductive load test circuit

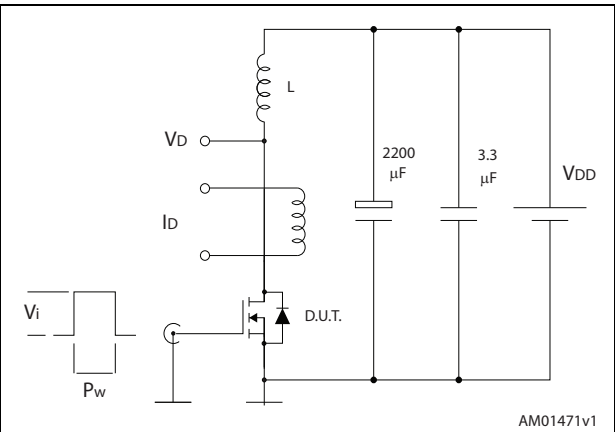


Figure 17. Unclamped inductive waveform

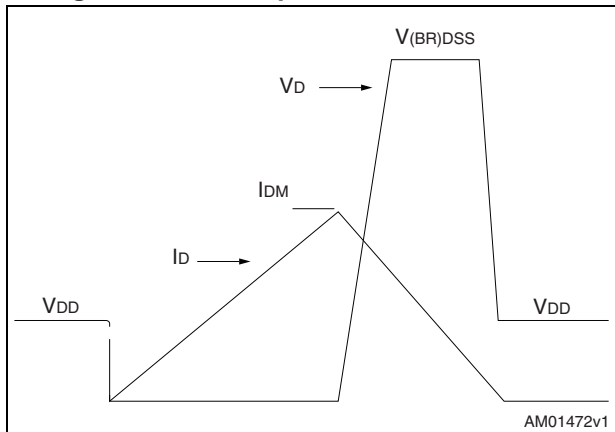
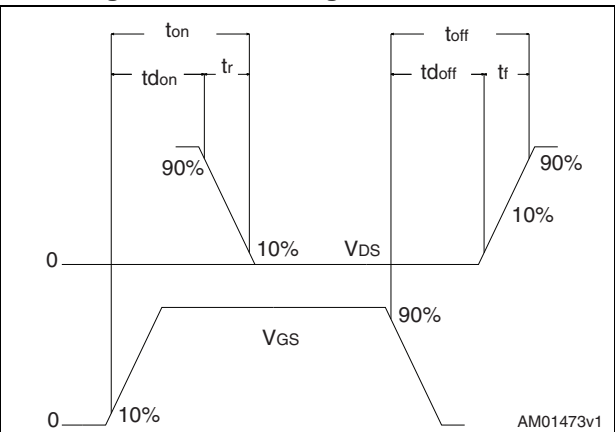


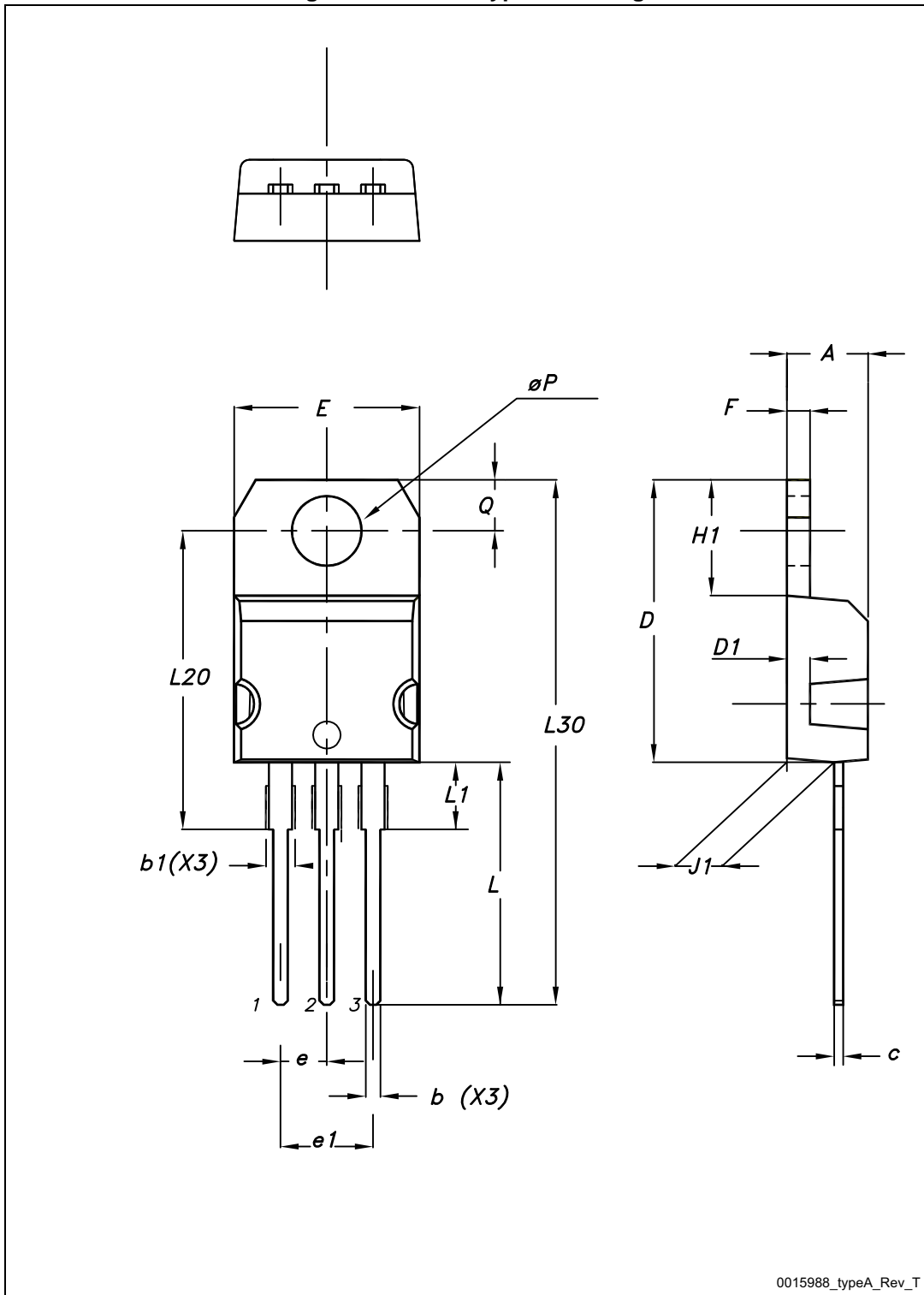
Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 19. TO-220 type A drawing



0015988_typeA_Rev_T

Table 8. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
26-Sep-2014	1	Initial version.

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