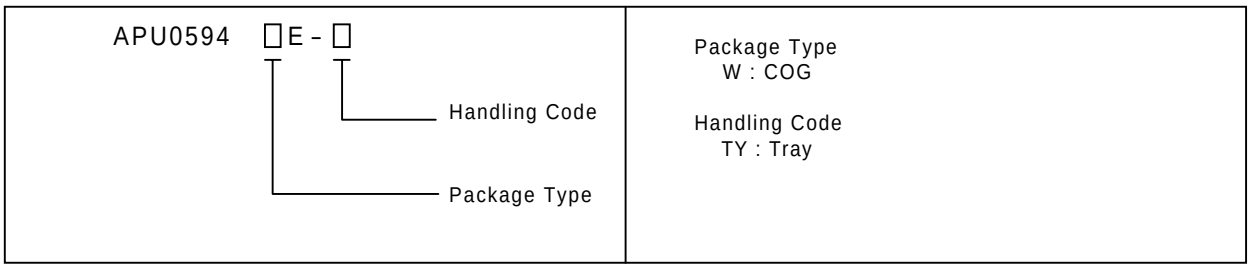
80 Segment / 17 Common Controller
for Dot Matrix LCD

## FEATURES

- General-purpose 8-bit MPU interface :
  Allows direct connection with the 80 or 68-family MPU over bus
- Not designed or rated as radiation hardened
- Format of font character 5 × 8 dots including 1 dot which also serves for display a cursor
- Operating temperature : -30 to +85°C
- Packaging : Chip ( 184 pads )
- CMOS silicon gate process
  ( p-type silicon circuit substrate )
- Built-in LCD drive power circuit
  - Built-in Booster circuit : Enables two or three times higher voltage
  - Built-in voltage conversion circuit : Generates LCD drive voltage ( $V_0$, $V_1$, $V_2$, $V_3$ or $V_4$ ) based on stepped-up voltage.
  - Bias ratio of built-in power source : 1 / 4, 1 / 5
  - Built-in electronic control : Controllable in 16 steps
- Allows serial interfacing ( ∗I²CBUS format )
  - Display duty ratio : 1 / 8, 1 / 9, 1 / 16, 1 / 17
  - Command features
  - Display of 2 lines by 16 characters
  - Display ON / OFF
  - Normal / reverse display control
  - Busy flag read-out
  - Cursor display
  - Blinking ( per character )
  - Display double fonts lengthwise
  - Power saving mode
- Built-in CGROM : 240 characters ( 5 × 8 × 240 = 9600 bits )
- Built-in CGRAM : 8 characters ( 5 × 8 × 8 = 320 bits )
- Built-in SEGRAM : 80 segments ( 16 × 7 = 112 bits )
- Built-in display data RAM : 32 characters ( 32 × 8 = 256 bits)
- Power source : Supply voltage for logic system : +2.7V to +5.5V
  LCD drive voltage : +4.0V to +11.0V

## ORDERING INFORMATION

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Rev. A.07 - FEB., 2002

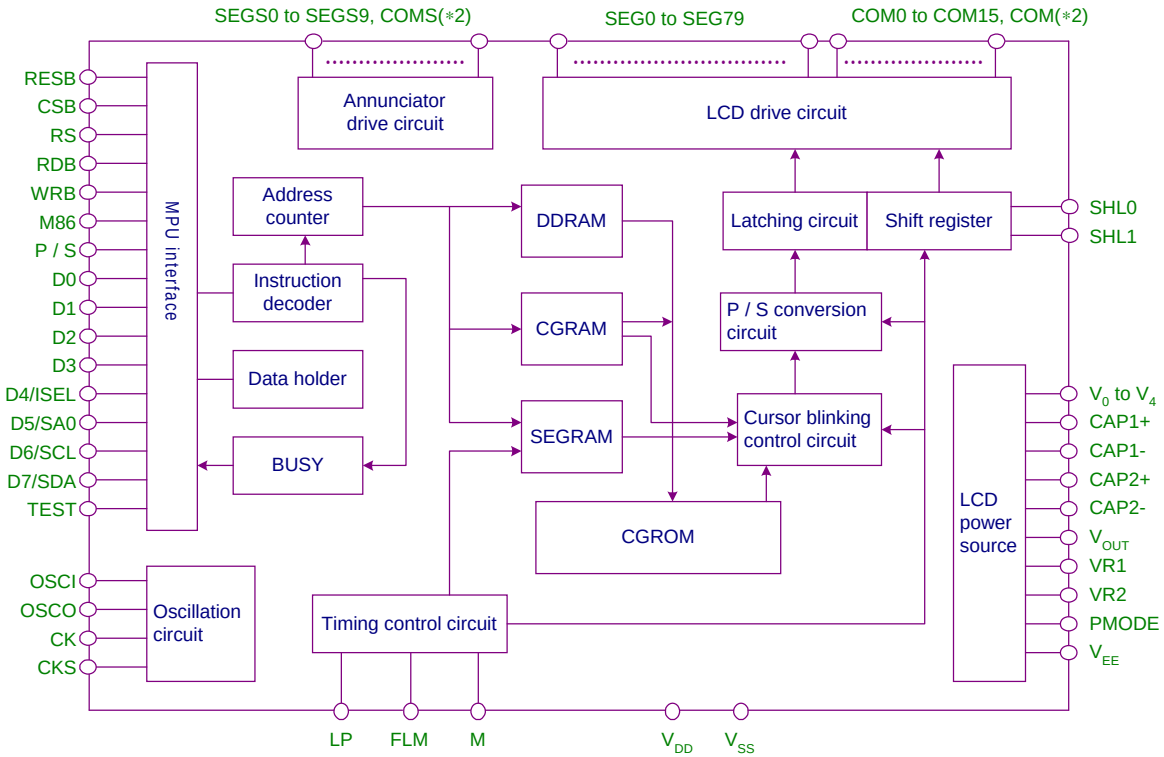
## Summary

The APU0594 is a dot matrix LCD driver with a built-in character ROM, which can be connected to a microcomputer via a bus. Eight-bit or serial data sent by a microcomputer is used to generate LCD drive signals for displaying characters.

Incorporating the character ROM, which has font, characters configured in the format of 5 × 8 dots and the APU0594 has 80 output pins for a segment driver circuit and 17 output pins for a common driver circuit in a single chip, a display system for 16 characters × 2 lines can be implemented easily.

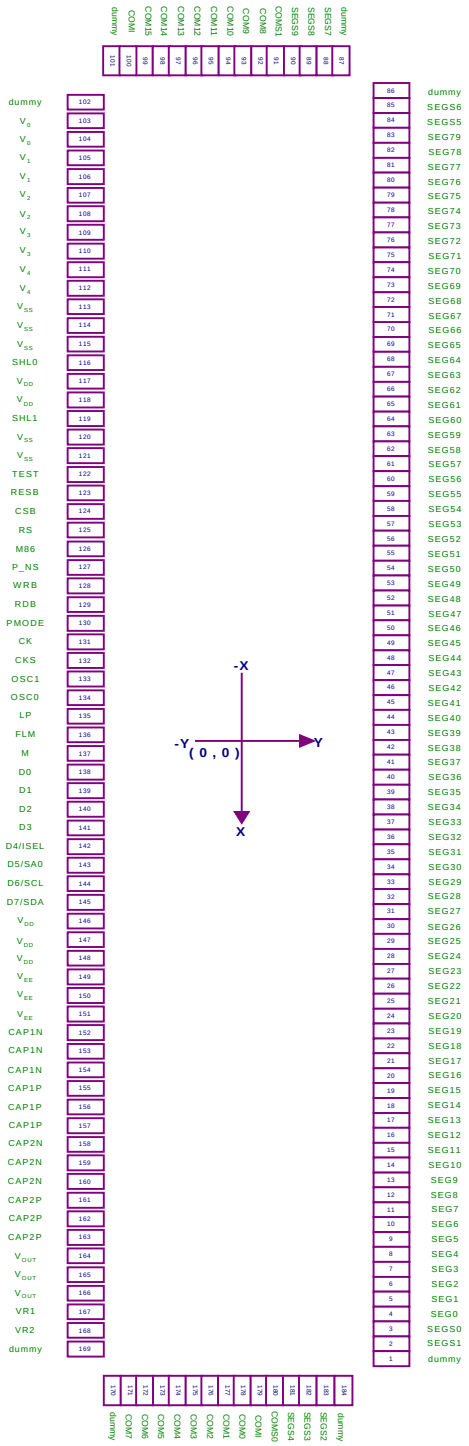
Because of its lower power consumption and wider operating voltage range, the APU0594 makes itself most suited for a LCD unit on battery-operated portable information-oriented equipment.

## BLOCK DIAGRAM



# PAD CONFIGURATION

## 1. PAD ASSIGNMENT




bump size : 78 × 100µm
pad size : 90 × 119µm
bump height : ±18µm
die thickness : 625µm
upper_pad pitch : 110µm
die size : 9838µm × 2065µm = 20.31mm$^2$

## 2. PAD LOCATION (1/2)

| No. | Symbol | X | Y | No. | Symbol | X | Y | No. | Symbol | X | Y |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | dummy | 4675 | 917 | 35 | SEG31 | 935 | 917 | 69 | SEG65 | -2805 | 917 |
| 2 | SEGS1 | 4565 | 917 | 36 | SEG32 | 825 | 917 | 70 | SEG66 | -2915 | 917 |
| 3 | SEGS0 | 4455 | 917 | 37 | SEG33 | 715 | 917 | 71 | SEG67 | -3025 | 917 |
| 4 | SEG0 | 4345 | 917 | 38 | SEG34 | 605 | 917 | 72 | SEG68 | -3135 | 917 |
| 5 | SEG1 | 4235 | 917 | 39 | SEG35 | 495 | 917 | 73 | SEG69 | -3245 | 917 |
| 6 | SEG2 | 4125 | 917 | 40 | SEG36 | 385 | 917 | 74 | SEG70 | -3355 | 917 |
| 7 | SEG3 | 4015 | 917 | 41 | SEG37 | 275 | 917 | 75 | SEG71 | -3465 | 917 |
| 8 | SEG4 | 3905 | 917 | 42 | SEG38 | 165 | 917 | 76 | SEG72 | -3575 | 917 |
| 9 | SEG5 | 3795 | 917 | 43 | SEG39 | 55 | 917 | 77 | SEG73 | -3685 | 917 |
| 10 | SEG6 | 3685 | 917 | 44 | SEG40 | -55 | 917 | 78 | SEG74 | -3795 | 917 |
| 11 | SEG7 | 3575 | 917 | 45 | SEG41 | -165 | 917 | 79 | SEG75 | -3905 | 917 |
| 12 | SEG8 | 3465 | 917 | 46 | SEG42 | -275 | 917 | 80 | SEG76 | -4015 | 917 |
| 13 | SEG9 | 3355 | 917 | 47 | SEG43 | -385 | 917 | 81 | SEG77 | -4125 | 917 |
| 14 | SEG10 | 3245 | 917 | 48 | SEG44 | -495 | 917 | 82 | SEG78 | -4235 | 917 |
| 15 | SEG11 | 3135 | 917 | 49 | SEG45 | -605 | 917 | 83 | SEG79 | -4345 | 917 |
| 16 | SEG12 | 3025 | 917 | 50 | SEG46 | -715 | 917 | 84 | SEGS5 | -4455 | 917 |
| 17 | SEG13 | 2915 | 917 | 51 | SEG47 | -825 | 917 | 85 | SEGS6 | -4565 | 917 |
| 18 | SEG14 | 2805 | 917 | 52 | SEG48 | -935 | 917 | 86 | dummy | -4675 | 917 |
| 19 | SEG15 | 2695 | 917 | 53 | SEG49 | -1045 | 917 | 87 | dummy | -4792 | 795 |
| 20 | SEG16 | 2585 | 917 | 54 | SEG50 | -1155 | 917 | 88 | SEGS7 | -4792 | 685 |
| 21 | SEG17 | 2475 | 917 | 55 | SEG51 | -1265 | 917 | 89 | SEGS8 | -4792 | 575 |
| 22 | SEG18 | 2365 | 917 | 56 | SEG52 | -1375 | 917 | 90 | SEGS9 | -4792 | 465 |
| 23 | SEG19 | 2255 | 917 | 57 | SEG53 | -1485 | 917 | 91 | COMS | -4792 | 355 |
| 24 | SEG20 | 2145 | 917 | 58 | SEG54 | -1595 | 917 | 92 | COM8 | -4792 | 245 |
| 25 | SEG21 | 2035 | 917 | 59 | SEG55 | -1705 | 917 | 93 | COM9 | -4792 | 135 |
| 26 | SEG22 | 1925 | 917 | 60 | SEG56 | -1815 | 917 | 94 | COM10 | -4792 | 25 |
| 27 | SEG23 | 1815 | 917 | 61 | SEG57 | -1925 | 917 | 95 | COM11 | -4792 | -84 |
| 28 | SEG24 | 1705 | 917 | 62 | SEG58 | -2035 | 917 | 96 | COM12 | -4792 | -194 |
| 29 | SEG25 | 1595 | 917 | 63 | SEG59 | -2145 | 917 | 97 | COM13 | -4792 | -304 |
| 30 | SEG26 | 1485 | 917 | 64 | SEG60 | -2255 | 917 | 98 | COM14 | -4792 | -414 |
| 31 | SEG27 | 1375 | 917 | 65 | SEG61 | -2365 | 917 | 99 | COM15 | -4792 | -524 |
| 32 | SEG28 | 1265 | 917 | 66 | SEG62 | -2475 | 917 | 100 | COM1 | -4792 | -634 |
| 33 | SEG29 | 1155 | 917 | 67 | SEG63 | -2585 | 917 | 101 | dummy | -4792 | -744 |
| 34 | SEG30 | 1045 | 917 | 68 | SEG64 | -2695 | 917 | 102 | dummy | -4658 | -894 |

## PAD LOCATION (2/2)

| No. | Symbol | X | Y | No. | Symbol | X | Y | No. | Symbol | X | Y |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 103 | $V_0$ | -4548 | -894 | 131 | CK | -1093 | -894 | 159 | CAP2- | 3458 | -894 |
| 104 | $V_0$ | -4438 | -894 | 132 | CKS | -963 | -894 | 160 | CAP2- | 3568 | -894 |
| 105 | $V_1$ | -4303 | -894 | 133 | OSCI | -833 | -894 | 161 | CAP2+ | 3703 | -894 |
| 106 | $V_1$ | -4193 | -894 | 134 | OSCO | -703 | -894 | 162 | CAP2+ | 3813 | -894 |
| 107 | $V_2$ | -4058 | -894 | 135 | LP | -397 | -894 | 163 | CAP2+ | 3923 | -894 |
| 108 | $V_2$ | -3948 | -894 | 136 | FLM | -267 | -894 | 164 | $V_{OUT}$ | 4058 | -894 |
| 109 | $V_3$ | -3813 | -894 | 137 | M | 38 | -894 | 165 | $V_{OUT}$ | 4168 | -894 |
| 110 | $V_3$ | -3703 | -894 | 138 | D0 | 168 | -894 | 166 | $V_{OUT}$ | 4278 | -894 |
| 111 | $V_4$ | -3568 | -894 | 139 | D1 | 474 | -894 | 167 | VR1 | 4412 | -894 |
| 112 | $V_4$ | -3458 | -894 | 140 | D2 | 604 | -894 | 168 | VR2 | 4548 | -894 |
| 113 | $V_{SS}$ | -3331 | -894 | 141 | D3 | 910 | -894 | 169 | dummy | 4658 | -894 |
| 114 | $V_{SS}$ | -3221 | -894 | 142 | D4 / ISEL | 1040 | -894 | 170 | dummy | 4792 | -744 |
| 115 | $V_{SS}$ | -3111 | -894 | 143 | D5 / SA0 | 1346 | -894 | 171 | COM7 | 4792 | -634 |
| 116 | SHL0 | -2988 | -894 | 144 | D6 / SCL | 1476 | -894 | 172 | COM6 | 4792 | -524 |
| 117 | $V_{DD}$ | -2858 | -894 | 145 | D7 / SDA | 1782 | -894 | 173 | COM5 | 4792 | -414 |
| 118 | $V_{DD}$ | -2748 | -894 | 146 | $V_{DD}$ | 1912 | -894 | 174 | COM4 | 4792 | -304 |
| 119 | SHL1 | -2618 | -894 | 147 | $V_{DD}$ | 2022 | -894 | 175 | COM3 | 4792 | -194 |
| 120 | $V_{SS}$ | -2494 | -894 | 148 | $V_{DD}$ | 2132 | -894 | 176 | COM2 | 4792 | -84 |
| 121 | $V_{SS}$ | -2384 | -894 | 149 | $V_{EE}$ | 2283 | -894 | 177 | COM1 | 4792 | 25 |
| 122 | TEST | -2261 | -894 | 150 | $V_{EE}$ | 2393 | -894 | 178 | COM0 | 4792 | 135 |
| 123 | RESB | -2131 | -894 | 151 | $V_{EE}$ | 2503 | -894 | 179 | COMI | 4792 | 245 |
| 124 | CSB | -2001 | -894 | 152 | CAP1- | 2638 | -894 | 180 | COMS | 4792 | 355 |
| 125 | RS | -1872 | -894 | 153 | CAP1- | 2748 | -894 | 181 | SEGS4 | 4792 | 465 |
| 126 | M86 | -1742 | -894 | 154 | CAP1- | 2858 | -894 | 182 | SEGS3 | 4792 | 575 |
| 127 | P / S | -1612 | -894 | 155 | CAP1+ | 2993 | -894 | 183 | SEGS2 | 4792 | 685 |
| 128 | WRB | -1482 | -894 | 156 | CAP1+ | 3103 | -894 | 184 | dummy | 4792 | 795 |
| 129 | RDB | -1352 | -894 | 157 | CAP1+ | 3213 | -894 | | | | |
| 130 | PMODE | -1223 | -894 | 158 | CAP2- | 3348 | -894 | | | | |

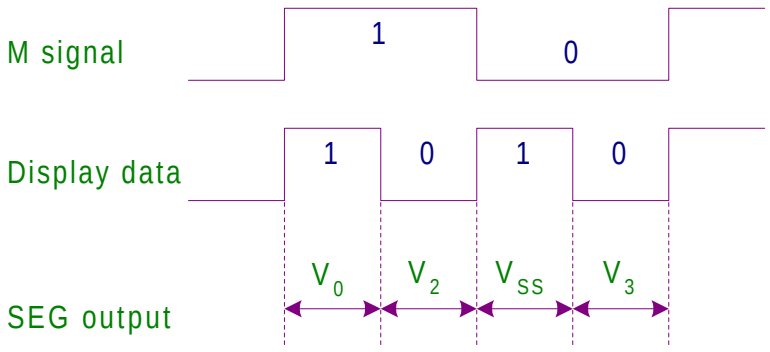
# DESCRIPTION OF PINS

## 1. SYSTEM BUS PINS

| Symbol | I / O | Pin Description |
|---|---|---|
| RESB | I | Used to reset the APU0594.<br>The APU0594 is reset when “0” is entered. |
| D0<br>D1<br>D2<br>D3<br>D4 / ISEL<br>D5 / SA0<br>D6 / SCL<br>D7 / SDA | I / O | • When set to parallel interface mode (P / S = ”H”)<br>Used as an 8-bit bi-directional data bus, (D0-D7) which is connected to data bus in 8-bit MPU.<br>• When set to serial interface mode (P / S = ”L”)<br>Used as serial interface signals (SDA, SCL, and ISEL).<br>SDA : I / O for the $I^2$CBUS data line when serial interface is selected.<br>Must be connecting to a positive supply via pull-up resistor.<br>SCL : Input for the $I^2$CBUS clock signal when serial interface is selected.<br>Must be connecting to a positive supply via pull-up resistor.<br>SA0 : Used for LSB bit of slave address for $I^2$CBUS (7 bits width) .<br>Must be fixed at “H” or “L”.<br>ISEL : Used to identify $I^2$CBUS. When use $I^2$CBUS; need to fix “H”.<br>If ISEL is set “L”, APU0594 operation is not warranty. |
| CSB | I | Used to enter chip select signal. Normally, address bus signal is decoded and then entered. |
| RS | I | Used to identify data sent by MPU at D0 to D7. |
| RDB<br>(E) | I | • When connected to 80-family MPU :<br>Used to connect RDB signal for 80-family MPU.<br>When this signal becomes “L”, data bus in the APU0594 enters the output mode.<br>• When connected to 68-family MPU :<br>Used to connect enable clock E signal for 68-family MPU.<br>When this signal becomes ”H”, APU0594 is made active. |
| WRB<br>(R / W) | I | • When connected to 80-family MPU :<br>Used to connect WRB signal for 80-family MPU.<br>When this signal becomes “L”, APU0594 is made active and any signal over data bus is captured at leading edge of WRB signal.<br>• When connected to 68-family MPU :<br>Used to connect read / write control signal for 68-family MPU.<br>R / W = “H” : READ<br>R / W = “L” : WRITE |
| M86 | I | Used to select MPU interface type.<br>Fixed at either M86 = “H” for 68-family interface<br>Or M86 = “L” for 80-family interface. |
| P / S | I | Used to switch between parallel and serial interface.<br>P / S = “H” for parallel interface. Fixes SDA and SCL at “H” or “L”.<br>P / S = “L” for serial interface. Fixes D7 to D0 at HI -Z ;<br>RDB and WRB at “H” or “L”. |
| TEST | I | Used for testing purpose. Must be fixed at “L”. |

## 2. LCD DRIVE PINS

<table>
<tr><th>Symbol</th><th>I / O</th><th>Pin Description</th></tr>
<tr><td>LP</td><td>O</td><td>Used as latch signal output pin for display data.<br>Outputs LCD drive signal when LP signal fall.</td></tr>
<tr><td>FLM</td><td>O</td><td>Used as LCD sync signal (first line marker) output pin .</td></tr>
<tr><td>M</td><td>O</td><td>Used as alternation signal output pin for LCD drive output .</td></tr>
<tr><td>COM0 to COM15</td><td>O</td><td>Used as common driver output pin for LCD drive (for character display) .<br>Among $V_0$, $V_1$, $V_4$, and $V_{SS}$ levels, one level is selected depending on the combination of scanned data and M signal .
<table>
<tr><th>Data</th><th>M</th><th>Output level</th></tr>
<tr><td>H</td><td>H</td><td>$V_{SS}$</td></tr>
<tr><td>L</td><td>H</td><td>$V_1$</td></tr>
<tr><td>H</td><td>L</td><td>$V_0$</td></tr>
<tr><td>L</td><td>L</td><td>$V_4$</td></tr>
</table></td></tr>
<tr><td>COM1</td><td>O</td><td>Used as common output pin for marker display .<br>Becomes common output pin when duty + 1 (PLUS) command is executed .<br>Having two output pins for COM1, they output same level , it is able to select output pin for COM1 when wiring pattern ,
<table>
<tr><th></th><th>Duty + 1 ON</th><th>Duty + 1 OFF</th></tr>
<tr><td>COM1 state</td><td>COM16 (when displaying 2 lines) ,<br>COM8 (when displaying 1 line)</td><td>$V_0$ or $V_4$</td></tr>
</table></td></tr>
<tr><td>SEG0 to SEG79</td><td>O</td><td>Used as segment driver output pin for LCD drive .<br>Among $V_0$, $V_2$, $V_3$, and $V_{SS}$ levels, one level is selected depending on the combination of M signal and display data .</td></tr>
<tr><td>COMS</td><td>O</td><td>Used as common driver output pin for static LCD drive (for annunciator display) .<br>Having two output pins for COMS, they output same level , it is able to select output pin for COMS when wiring pattern.<br>When DA = “0”, outputs $V_{SS}$ level .</td></tr>
<tr><td>SEGS0 to SEGS9</td><td>O</td><td>Used as segment driver output pin for static LCD drive (for annunciator display) .<br>Among $V_{DD}$ and $V_{SS}$ levels, one level is selected depending on the combination of COMS signal and display data .<br>When DA = “0”, outputs $V_{SS}$ level .</td></tr>
<tr><td>SHL0, SHL1</td><td>I</td><td>Input pin to control the transfer direction of the segment and common signal output data .<br>SHL0 = “0” : Segment data display direction is SEG0 to SEG79 .<br>SHL0 = “1” : Segment data display direction is SEG79 to SEG0 .<br>SHL1 = “0” : Common data display direction is COM0 to COM15 .<br>SHL1 = “1” : Common data display direction is COM15 to COM0 .</td></tr>
</table>



## 3. PINS FOR OSCILLATION CIRCUIT

| Symbol | I / O | Pin Description |
|---|---|---|
| OSCI | I | Used as oscillation circuit input pin (Feedback resistor must be inserted between this pin and OSCO) . |
| OSCO | O | Used as oscillation circuit output pin .<br>The CK pin must be fixed at $V_{SS}$ oscillation circuit is used as source oscillation clock . |
| CK | I | Used as external clock input pin .<br>The OSCI pin must be fixed at $V_{SS}$ if this pin is used for original oscillation input . |
| CKS | I | Used as external clock select pin .<br>CKS = "H" : External clock is input at the CK pin .<br>CKS = "L" : Oscillation circuit using the OSCI and OSCO pins is used . |

## 4. POWER SUPPLY PINS

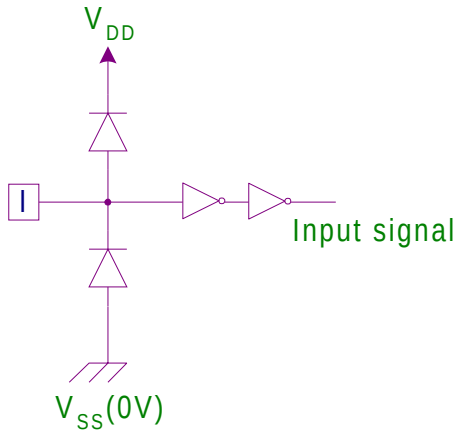
| Symbol | I / O | Pin Description |
|---|---|---|
| $V_{DD}$ | Power source | Used as logic system power pin , which must be connected to +2.7 to +5.5 V . |
| $V_{SS}$ | Power source | Used as ground pin , which must be connected to 0 V . |
| $V_0$<br>$V_1$<br>$V_2$<br>$V_3$<br>$V_4$ | Power source | Used as bias power pin for LCD drive voltage .<br>• When using an external power supply , convert Impedance by using resistance-division of LCD drive power supply or operation amplifier before adding voltage to the pins .<br>• When using the external power supply , maintain the following power supply conditions .<br>$V_{SS} < V_4 < V_3 < V_2 < V_1 < V_0$<br>• When the power supply circuit is ON , LCD drive voltage of $V_0$ to $V_4$ are generated by the built in booster and voltage converter .<br>• When using the built-in power supply , be sure to connect each capacitor between $V_0$ to $V_4$ and $V_{SS}$ . |

**5.**

| Symbol | I / O | Pin Description |
|---|---|---|
| CAP1+ | O | Used to connect positive side of capacitor for built-in booster circuit . A capacitor must be connecting between this pin and the CAP1- pin . |
| CAP1- | O | Used to connect negative side of capacitor for built-in booster circuit . A capacitor must be connecting between this pin and the CAP1+pin . |
| CAP2+ | O | Used to connect positive side of capacitor for built-in booster circuit . A capacitor must be connecting between this pin and the CAP2- pin. |
| CAP2- | O | Used to connect negative side of capacitor for built-in booster circuit . A capacitor must be connecting between this pin and the CAP2+ pin. |
| $V_{EE}$ | Power pin | Used to apply voltage for generating booster voltage . Normally this pin must be set at the same level as at the $V_{DD}$ pin. |
| $V_{OUT}$ | Power pin | Used as output pin when built-in booster circuit is used . A capacitor must be connected between this pin and the $V_{SS}$ pin . If only voltage conversion circuit is used , voltage must be input so that the condition of $V_{OUT} > V_0$ is satisfied . |
| VR1 | I | Used as input pin for voltage conversion circuit . Voltage must be input between the $V_{OUT}$ and $V_{SS}$ pins by dividing voltage by resistor , and must be input so that the condition of VR1 ≥ VR2 > 4.0 V is satisfied . |
| VR2 | I | Used as input pin for voltage conversion circuit . Voltage must be input between the $V_{OUT}$ and $V_{SS}$ pins by dividing voltage by resistor , and must be input so that the condition of VR1 ≥ VR2 > 4.0 V is satisfied . |
| PMODE | I | Used as LCD power control pin . The operation condition of power circuit must be selected using the combination of the PMODE pin and the power circuit ON / OFF command (PON). |

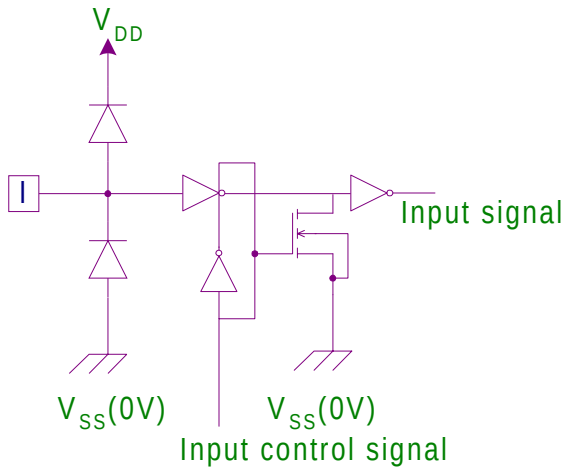
## 6. INPUT / OUTPUT CIRCUIT TYPES

### (a-1) Input circuit 1



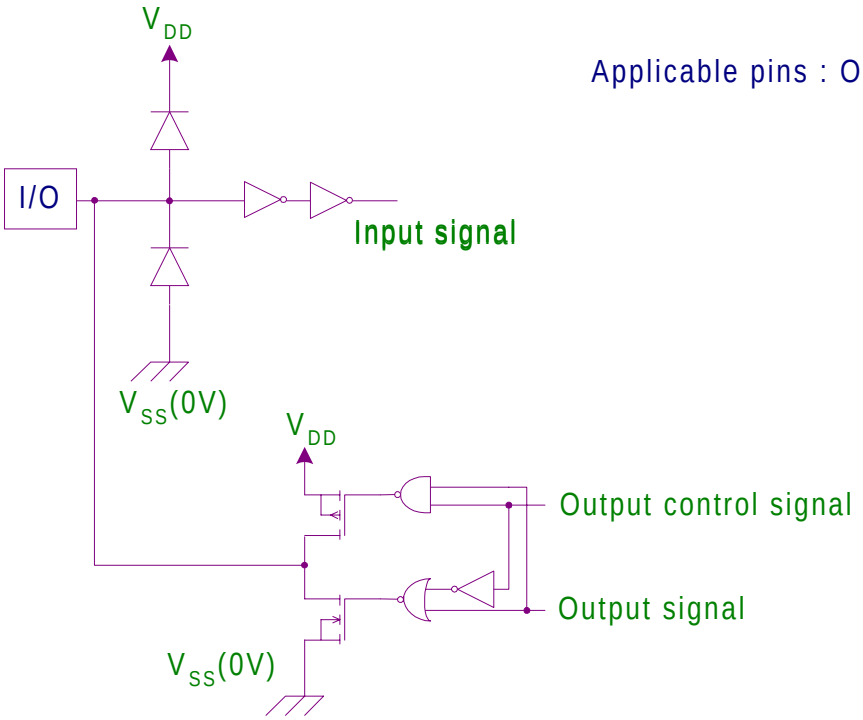

Applicable pins : M86, P / S, SHL0, SHL1, OSCI, CK, CKS, PMODE, RESB, TEST

### (a-2) Input circuit 2



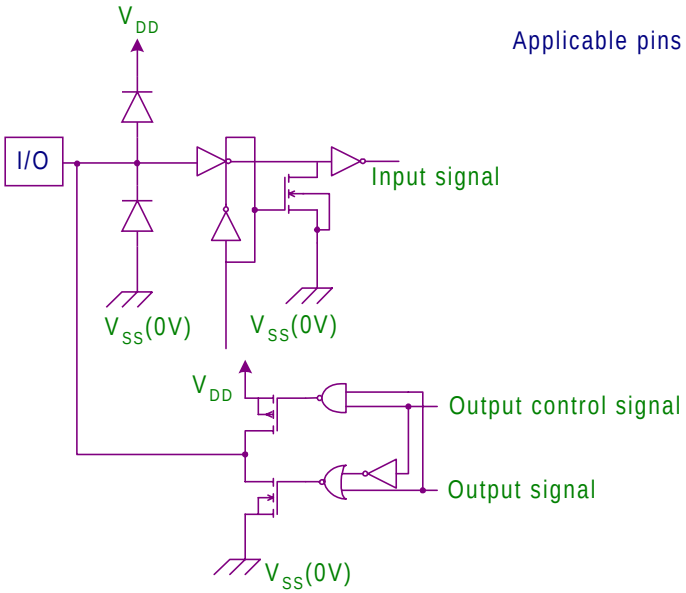

Applicable pins : CSB, RS, WRB, RDB

### (b-1) Input / output circuit 1



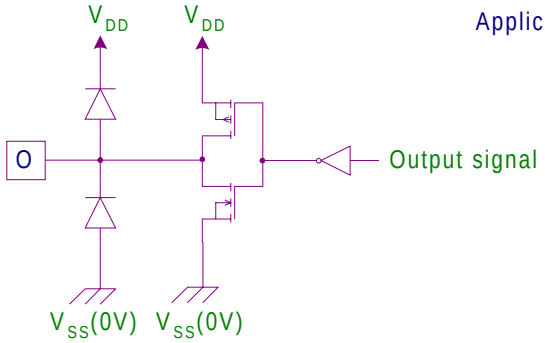

Applicable pins : OSCO

**(b-2) Input / output circuit 2**



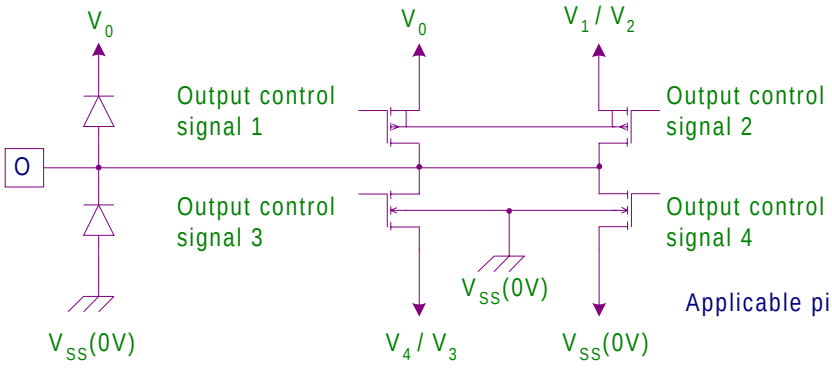

Applicable pins : D0 to D7

**(c) Output circuit**




Applicable pins : LP, FLM, M,
SEGS0 to SEGS9,
COMS

**(d) LCD Output circuit**




Applicable pins : SEG0 to SEG79,
COM0 to COM15,
COM

# Description of Functions

## 1. INTERFACE TYPE SELECTION

The APU0594 performs data transfer via the 8-bit data bus or the serial data input (the SDA or SCL pin) .

The parallel or serial interface is selected by setting the polarity of the P / S pin to “H” or “L”.

| P / S | I / F type | CSB | RS | RDB | WRB | M86 | SDA | SCL | Data bus |
|---|---|---|---|---|---|---|---|---|---|
| H | Parallel | CSB | RS | RDB | WRB | M86 | — | — | D0 to D7 |
| L | Serial | — | — | — | — | — | SDA | SCL | — |

## 2. PARALLEL INPUT

The APU0594 allows parallel data transfer by directly connecting the data bus to an 8-bit MPU if the parallel interface is selected with the P / S pin .

For this 8-bit MPU, the 80-family or 68-family MPU type interface can be selected with the M86 pin.

| M86 | MPU type | CSB | RS | RDB | WRB | D0 to D7 |
|---|---|---|---|---|---|---|
| H | 68-family MPU | CSB | RS | E | R / W | D0 to D7 |
| L | 80-family MPU | CSB | RS | RDB | WRB | D0 to D7 |

## 3. DATA IDENTIFICATION

The APU0594 identifies data types over the 8-bit data bus by combinations of RS, RDB, and WRB signals.

| RS | 68-family R / W | 80-family | | Function |
|---|---|---|---|---|
| | | RDB | WRB | |
| 0 | 1 | 0 | 1 | Reads out busy flags |
| 0 | 0 | 1 | 0 | Writes commands |
| 1 | 1 | 0 | 1 | Reads out RAM data |
| 1 | 0 | 1 | 0 | Writes RAM data |

## 4. SERIAL INTERFACE

The serial interface for the APU0594 is $I^2CBUS$ format.

$I^2CBUS$ is for bi-directional, two-line communication between different ICs or other modules.

APU0594 always operated for Slave device, Sending data start and stop is controlled by Start / Stop bit, which are sent by Master device.

∗ $I^2CBUS$ is a PHILIPS’s registered trademark

## 5. BUSY FLAG

When the busy flag is “1”, this indicates that the APU0594 is internally operating. In this state, the APU0594 does not accept the next instruction. As shown in the instruction table, the busy flag is output to the data bus D7 when RS is “0” or R / W is “1” (for 68-family interface) , and when RS is “0” or RDB is “0” (for the 80-family interface) . The busy flag is generated only when the display clear command or the ACL command is executed. It must be checked that the busy flag is “0” before the next instruction can be executed.

## 6. ADDRESS COUNTER (AC)

The address counter (AC) is used to address the DDRAM, or SEGRAM. When the addressing instruction is written into the AC, the address information is transferred to the AC. Simultaneously, the instruction also determines which RAM is to be selected among the DDRAM, CGRAM, and SEGRAM. After data is written into (read out into) the DDRAM, CGRAM , or SEGRAM , the AC is automatically counted up or down by one . As shown in the instruction table, the AC outputs data to the data buses D6 to D0 when RS is “0” or R / W is “1” (for the 68-family interface) .

## 7. DISPLAY DATA RAM (DDRAM)

The DDRAM stores display data presented with 8-bit character codes. Its capacity is 32 characters in the format of 8 bits.

## 8. CHARACTER GENERATOR ROM (CGROM)

The CGRAM generates 240 different character patterns in the format of $5 \times 8$ dots from 8-bit character codes.

## 9. CHARACTER GENERATOR RAM (CGRAM)

The CGRAM allows you to freely overwrite characters with your program.

Eight different types of characters can be written by the format of $5 \times 8$ dots.

## 10. SEGMENT RAM (SEGRAM)

The SEGRAM allows you to freely control Icons and marks with your program. When the COM1 outputs the select signal, the data stored in the SEGRAM is read out to display 80 segments.

## 11. TIMING GENERATOR CIRCUIT

The timing generator circuit generates the timing signals to operate the internal circuits including the DDRAM, CGROM, CGRAM, and SEGRAM as well as those for segment and common driver outputs. Read-out of the display data to the LCD drive circuit is completely independent of MPU. Therefore, MPU that has no relationship the read-out operation of the display data can access.

## 12. CURSOR BLINKING CONTROL CIRCUIT

This circuit generates the cursor, the blinking cursor, or the reverse-display cursor.
The cursor or the blinking cursor appears in the digit that corresponds to the address in the DDRAM, which was specified in the address, counter.

## 13. OSCILLATION CIRCUIT

This is the CR oscillation circuit, which controls the oscillation frequency with feedback resistor RF. This circuit is used as the source of display timing signals and the boost clock for the Booster circuit.
If external clock is used, maintain OSCI pin at $V_{SS}$ and OSCO pin opens (NC) , and feed the clock to CK pin. The duty cycle of the external clock must be 50%.
The CKS pin is used to switch between the oscillation circuit and the external clock input.

| CKS | Oscillation circuit | External clock |
|---|---|---|
| "L" | Enabled | Disabled |
| "H" | Disabled | Enabled |

## 14. LCD DRIVER CIRCUIT

This is the drive circuit, which generates 4-value levels for LCD drive.
It consists of 17 common drivers and 80 segment drivers.
Character data is transferred by 60 bits from the CGROM or the CGRAM to the segment driver circuit.
The combination of the transferred display data and the M signal is used to output LCD drive voltage.
Among the common outputs, one output (COM1) is used to marker display.
The common driver circuit has a shift register and sequentially outputs common scan select signals.

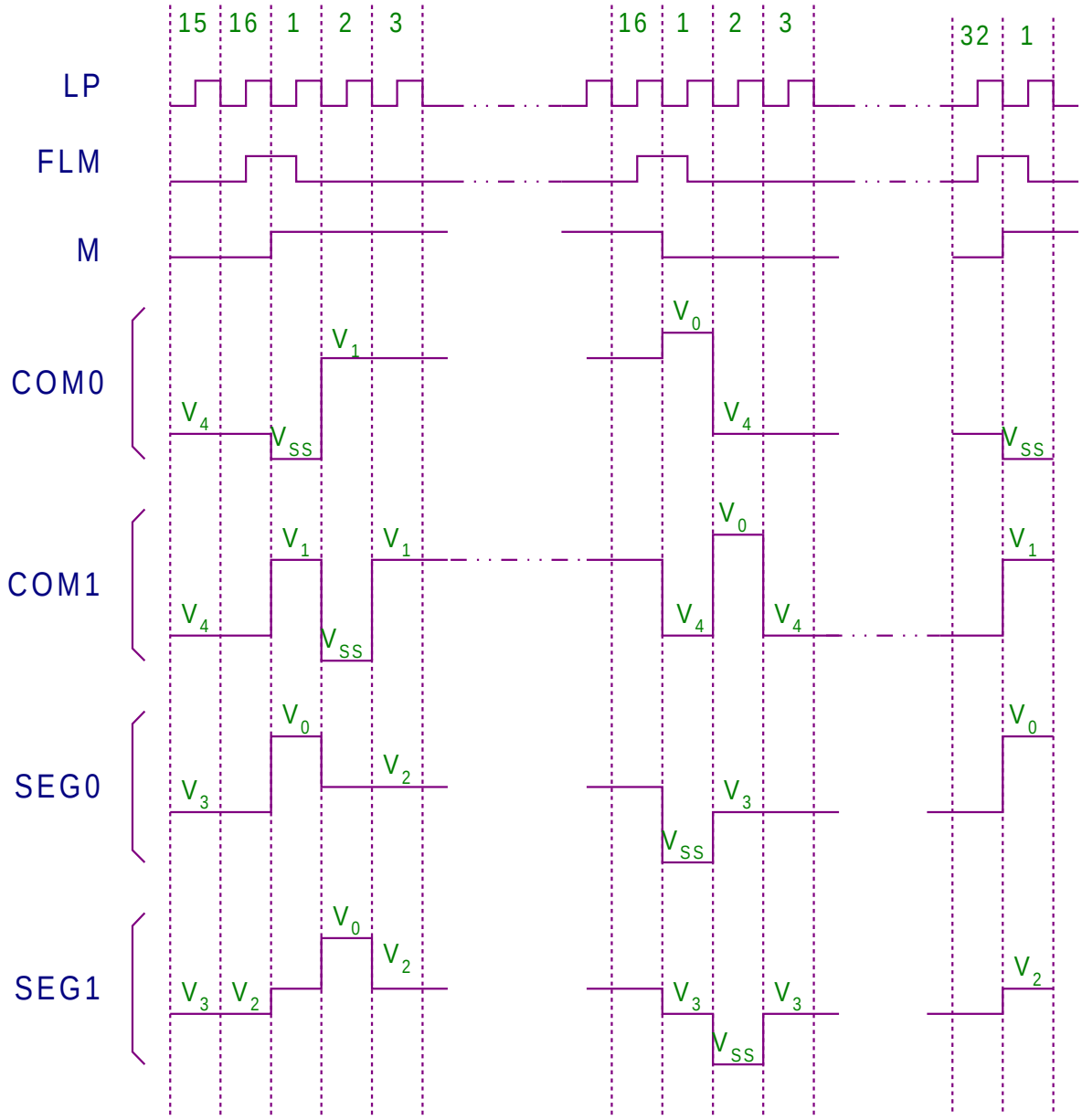
## 15. ANNUNCIATOR CIRCUIT

This is the drive circuit, which generates 2-value levels for static LCD drive.
This circuit provides displaying annunciators for Icons or Marks. It consists of common drivers (COMS × 2) and 10 segment drivers (SEGS0 to SEGS9) .
Among $V_{DD}$ and $V_{SS}$ levels, one level is selected for static LCD drive. When this circuit is not displaying annunciator , it outputs $V_{SS}$ level.

## 16. LCD DRIVE VOLTAGE GENERATION CIRCUIT

The voltage conversion circuit incorporates a voltage generation circuit, which divides the electric potential at the $V_0$ pin with resistors to generate the electric potentials $V_0$, $V_1$, $V_2$, $V_3$, and $V_4$ which are required for LCD drive. The LCD drives voltage bias for the APU0594 is 1 / 4 or 1 / 5.
If the built-in power source is used, the capacitor C2 for voltage stabilization must be connected to the LCD power pin.
In order to stabilize the input voltages at the VR1 and VR2, the capacitor C2 must be connected for the actual system by selecting its value as appropriate.

## 17. LCD DRIVER OUTPUT TIMING



## 18. POWER SUPPLY CIRCUIT

The power supply circuit generates the voltage required for LCD drive.

It consists of a booster circuit, an electronic volume, and a voltage conversion circuit. High voltage boosted by the booster circuit is input to the voltage conversion circuit so that the necessary voltages for LCD drive ($V_0$, $V_1$, $V_2$, $V_3$, and $V_4$) are generated. If the number of pixels on your LCD panel is large, i.e., the display capacity is large; the built-in power circuit should not be used for driving that LCD panel. If used, this could greatly deteriorate the display quality. In this case, an external power source should be used.

The power circuit is off, the booster circuit and the power circuit ON / OFF command (PON) . When the built-in power circuit is off, the booster circuit and the voltage conversion circuit are also off. If an external power source is used, LCD drive voltages $V_0$, $V_1$, $V_2$, $V_3$, and $V_4$ must be externally supplied with the built-in power circuit off; the CAP1+, CAP1-, CAP2+, CAP2-, $V_{OUT}$, $V_{EE}$, VR1, and VR2 pins must be opened; and the PMODE pin must be connected to the $V_{SS}$ pin.

The function of the power circuit can be selected depending on the status of the PMODE pin. Some functions of the external power source and the built-in power source can be combined to use together.

| PON | PMODE | Booster circuit | Voltage conversion circuit | External voltage input | Remarks |
|---|---|---|---|---|---|
| 0 | 0 | Disabled | Disabled | $V_0$, $V_1$, $V_2$, $V_3$, and $V_4$ are supplied | ∗1 |
| 0 | 1 | Disabled | Disabled | $V_0$, $V_1$, $V_2$, $V_3$, and $V_4$ are supplied | ∗1 |
| 1 | 0 | Enabled | Enabled | — | |
| 1 | 1 | Disabled | Enabled | $V_{OUT}$, VR1, and $V_2$ are supplied | ∗2 |

∗1 : The power circuit does not operate . Therefore, open the CAP1+, CAP1-, and CAP2+ , CAP2-, $V_{OUT}$, $V_{EE}$, VR1, and VR2 pin; and externally supply LCD drive voltages.

∗2 : The booster circuit does not operate . Therefore, open the CAP1+, CAP1-, CAP2+, CAP2-, and $V_{EE}$ pins; supply power for the voltage conversion circuit at the $V_{OUT}$ pin; and supply reference voltage for LCD drive at the VR1 and VR2 pins.

## 19. ELECTRONIC VOLUME

The voltage conversion circuit incorporates an electronic volume, which allows the LCD drive voltage level $V_0$ to be controlled with a command and also allows the tone of LCD display to be controlled.

If 4-bit data is stored in the register of the electronic volume, one level can be selected among 16 voltage values for the LCD drive voltage $V_0$.

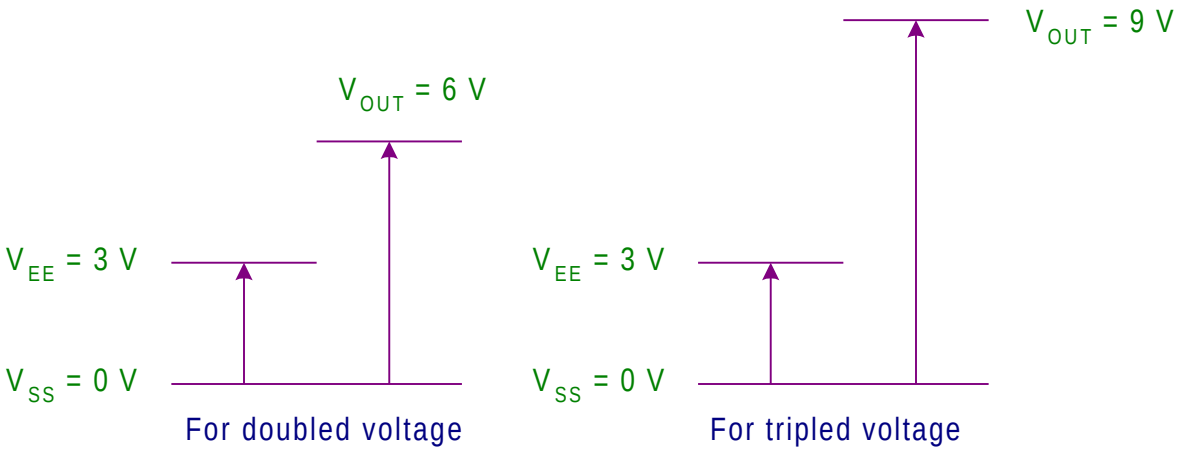
The input voltage determines the voltage control range of the electronic control levels at the VR1 and VR2. This means that the voltage range of (VR1 – VR2) is the controllable voltage range of the electronic volume. The electric potential relation between the VR1 and VR2 pins must be VR1 > VR2. The input voltage levels at the VR1 and VR2 pins must be selected in accordance with the voltage levels to be obtained with electronic volume.

## 20. BOOSTER CIRCUIT

The capacitor C1 is connected between the CAP1+ and CAP1-, between the CAP2+ and CAP2- and between the $V_{OUT}$ and $V_{SS}$ so that the electric potential between the $V_{EE}$ and $V_{SS}$ is tripled and then output at the $V_{OUT}$ pin. For the doubled electric potential, the capacitor between the CAP2+ and CAP2- is removed from the above connections and the CAP1+ and CAP2+ are short-circuited. Then the doubled voltage can be obtained at the $V_{OUT}$ pin.

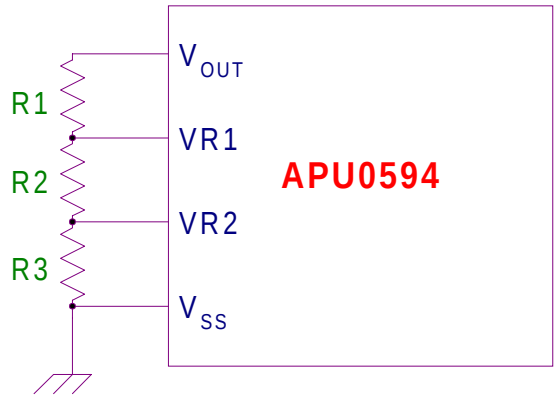
The booster circuit uses the clock signal from the oscillation circuit or the CK pin as the booster signal. This requires that the oscillation circuit is operating or that the clock signal is input at the CK pin.

You must take care that the output level at the $V_{OUT}$ pin does not exceed the recommended maximum operating voltage (11.0 V) when the voltage is doubled or tripled. If this value is exceeded, the operation of the APU0594 is not warranty.




## 21. VOLTAGE CONTROL CIRCUIT

The boosted voltage at the $V_{OUT}$ pin is connected to the VR1 and VR2 pins and then the LCD drive voltages ($V_0$, $V_1$ , $V_2$ , $V_3$ , and $V_4$) are generated via the voltage conversion circuit . The input level at the VR1 and VR2 must meet the electric potential condition of VR1 > VR2. The built-in electric volume divides the electric potential between the VR1 and VR2 into 16 segments. Since the VR1 and VR2 pins have high input impedance, the input voltage levels at the VR1 and VR2 are determined by the resistance ratio of R1, R2, and R3. The current flowing between the $V_{OUT}$ and $V_{SS}$ pins is determined by the combined resistance of R1, R2, and R3.Therefore, R1, R2, and R3 must be selected in accordance with the above current as well as the input voltage levels at the VR1 and VR2.The boosted voltage at the $V_{OUT}$ pin originates from the voltage supplied at the $V_{EE}$ pin. Thus, the DC path current generated with R1, R2, and R3 connected between the $V_{OUT}$ and $V_{SS}$ pins is consumed as consumption current at the $V_{EE}$ pin. The electric current value three times large than the DC path current generated between the $V_{OUT}$ and $V_{SS}$ pins when the voltage is tripled is added as consumption current at the $V_{EE}$ pin (two times larger current is added for doubled voltage). You must take sufficient care that the input levels at the VR1 and VR2 pins do not fluctuate with external noise.



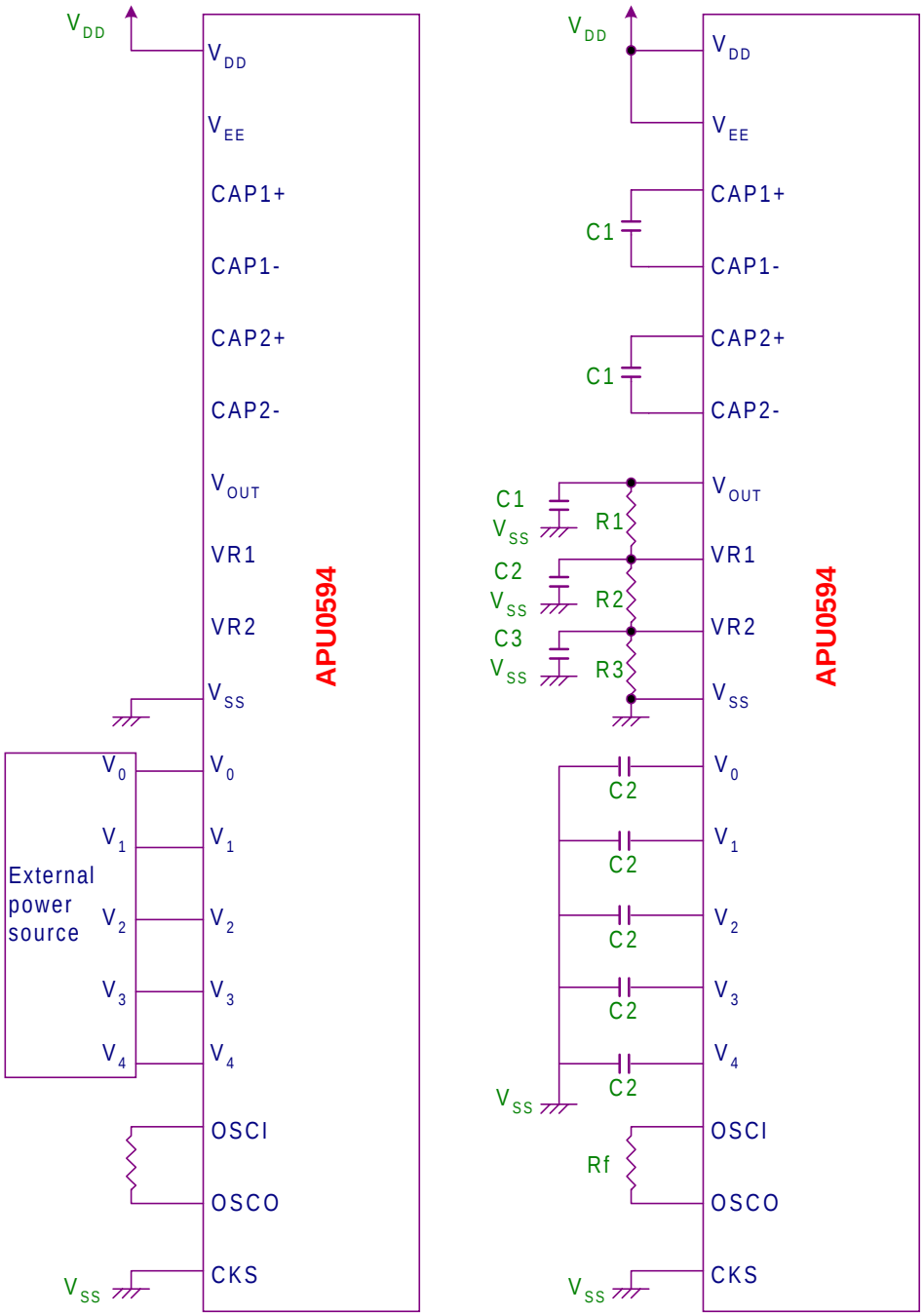

Example of voltage control circuit

## 22. RESETTING FUNCTION

Setting the RESB pin to the “L” level can initialize the APU0594. Normally, the RESB pin is connected to the reset pin on the MPU so that the APU0594 can be initialized together with the MPU. When the APU0594 is turned on, the resetting must be performed.

| Item | Pin Description |
|---|---|
| Function set | RE = 0 : Writes to expanded register disabled .<br>BE = 0 : SEGRAM blink off<br>DUB = 0 : Normal display mode .<br>(Displaying double fonts lengthwise OFF)<br>BT = 0 : Blinking type is normal / reverse display . |
| Entry mode set | I / D = 1 : Increments by one<br>S = 0 : No shift occurs . |
| Display mode set | NL = 0 : Display 2 lines . |
| Display control 1 | D = 0 : Display OFF<br>C = 0 : Cursor OFF<br>B = 0 : Blink OFF |
| Display control 2 | PLUS = 0 : 1 / 16 duty<br>REV = 0 : Normal display<br>ALON = 0 : Normal display |
| Power control | HALT = 0 : Power saving OFF<br>PON = 0 : Power circuit OFF<br>ACL = 0 : ACL operation OFF<br>BIAS : 1 / 5 bias |
| Register in electronic volume | (1 , 1 , 1 , 1) |
| Annunciator control | DA = 0 : Display annunciator OFF<br>I0 to I7 = (0 , 0 , 0 , 0 , 0 , 0 , 0 , 0 , 0 , 0) |
| RAM data | DDRAM : Not determined<br>CGRAM : Not determined<br>SEGRAM : Not determined |

## 23. EXAMPLE OF POWER CIRCUIT CONNECTION




When built-in power circuit is not used

Recommended values

| | |
|---|---|
| C1 | 1.0 to 5.0 µF |
| C2 | 0.1 µF |
| Rf | 1MΩ |
| R1+R2+R3 | 2.0 to 4.0 MΩ |

# DESCRIPTION OF COMMAND (FUNCTIONS)

Since the instructions for the APU0594 are executed which execution cycle time, the MPU can be operated at a high speed without waiting time. The busy state check is only necessary when the display clear command or the ACL command is executed.

## 1. LIST OF COMMAND FUNCTIONS

| Instruction | Instruction code | | | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Display clear | 0 / 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Specifies address 0 from DDRAM in AC after clearing all display. |
| Cursor home | 0 / 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | Allocates address 0 for DDRAM In AC and resets shifted display. |
| Entry mode set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I / D | S | Specifies cursor moving direction and whether or not to shift display. |
| Display mode set | 1 | | | | | | | | * | NL | Sets display 2lines or 1line (NL). |
| Display control 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Turns ON / OFF all display (D); turns ON / OFF cursor (C); or specifies blinking character indicated by cursor (B). |
| Display control 2 | 1 | | | | | | | PLUS | REV | ALON | Specifies duty + 1 (PLUS); displays data in reverse Display (REV); or Turns ON all display (ALON). |
| Cursor / Display shift | 0 | 0 | 0 | 0 | 0 | 1 | S / C | R / L | * | * | Moves cursor and shifts display without changing data in DDRAM. |
| Power control | 1 | | | | | | BIAS | HALT | PON | ACL | Specifies power saving (HALT); Turn ON power circuit (PON); or specifies resetting (ACL). Sets bias ratio (BIAS). |
| Function set | 0 / 1 | 0 | 0 | 0 | 1 | BE | DUB | RE | BT | * | Enables writes to expanded register (RE). Enables blinking for SEGRAM (BE). Enables display double font lengthwise (DUB). Sets blinking character type (BT). |
| CGRAM address set | 0 | 0 | 0 | 1 | | | | | | | CGRAM address set |
| SEGRAM address set | 1 | | | | * | * | | | | | SEGRAM address set |
| DDRAM address set | 0 | 0 | 1 | 0 | * | | | | | | DDRAM address set |
| Electronic volume set | 1 | | | | * | * | | | | | Electronic volume set |
| Annunciator control | 0 | 0 | 1 | 1 | I5 | I4 | I3 | I2 | I1 | I0 | Sets data for annunciator (I0 to I9). Enables display annunciator (DA). |
| | 1 | | | | DA | * | I9 | I8 | I7 | I6 | |
| Busy flag / address Read | 0 / 1 | 0 | BF | * | | | | | | | Reads out busy flag and data from AC. |
| RAM data write | 0 / 1 | 1 | | | | | | | | | RAM data write |
| RAM data read | 0 / 1 | 1 | | | | | | | | | RAM data read |

## 2. DESCRIPTION OF INSTRUCTIONS

### 2-1. Display clear

| RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 / 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Space code “20H” (for 32 characters) is written to all addresses in the DDRAM.
The address counter specifies DDRAM address 0.
If the display is shifted, it is reset in place. This means that the display is cleared and the cursor or blinking cursor, if displayed , returns to the left end in the first line .Set the I / D of the increment mode to “Increment”, “S” will not change.
If you start clearing the display, the busy flag is generated. Therefore, to execute .
Instructions after clearing the display, monitor the busy flag and then execute the next instruction after checking that the flag has been released, or allow an waiting period for 34 times the source clock frequency.

### 2-2. Cursor home

| RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 / 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * |

Specify DDRAM address 0 in the address counter. If the display is shifted, it is reset in place. The data in the DDRAM remains unchanged .The cursor or the blinking cursor, if displayed, returns to the left end in the first line.

### 2-3. Entry mode set

| RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I / D | S |

When the extended register enable bit (RE) is “0” , the following I / S , and S bits are accessed :

I / D : When any character code is written into or read out from the DDRAM , the DDRAM address is shifted by + 1 (I / D = 1) or +1 (I / D = 0). In case of +1, the cursor or the blinking cursor moves to the right. This is also applicable when any data is written into or read out from the CGRAM or SEGRAM.

S : If S = 1 , the entire display is shifted to either the left or right when any character code is written into the DDRAM. If I / D = 1, the entire display is shifted to the left; or if I / S = 0 , the entire display is shifted to the right . Therefore, if I / D = 1, the cursor looks stationary with only the display shifted . When any character code is read out from the DDRAM, the display is not shifted. If S = 0, the display remains unshifted. When any data is written into or read out from the CGRAM or SEGRAM, the display also remains unshifted.

When duty + 1 command is ON (PLUS = 1), if S = 1 and any code is written into DDRAM, the line that COM1 scans is also shifted , so that this command is allowed only duty + 1 command is OFF (PLUS = 0) state.

### 2-4. Display mode set

When the extended register enable bit (RE) is “1”, the following NL bit is accessed :

NL : This command selects the displaying lines .

NL = “0” : Displays 2 lines . Display duty ratio is 1 / 16.

NL = “1” : Displays 1 line . Display duty ratio is 1 / 8.

| RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | NL |

### 2-5. Display control 1

| RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

When the extended register enable bit (RE) is “0”, the following D, C, and B bits are accessed :

D : Turns ON the display if D = 1; or turns OFF the display if D = 0.
Since the data in the DDRAM is retained, the display can be resumed by specifying D = 1.

C : Displays the cursor if C = 1; or hides the cursor if C = 0. Even if the cursor is hidden, I / D and other features remain unchanged when the display data is written. The cursor is shown using 5 dots in the 8$^{th}$ line .

B : Blinks the character in the cursor position if B = 1. This blinking turns ON / OFF all dots displayed in reverse. The blinking frequency is ms when $f_{OSC}$ = K Hz and displays 2lines. This value caries in proportion to the inverse number of $f_{OSC}$ .

### 2-6. Display control 2

| RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

When the extended register enable bit (RE) is “1”, the PLUS , REV , and ALON bits are accessed. Once the specified values are stored in the register, they are retained even if the RE bit is set to “0”.

PLUS : Specifies “Duty + 1“ . Toggles the display duty. The COM1 pin functions as the COM8 (when displaying 1 line) or COM16 (when displaying 2 lines) for marker. When the COM1 is scanned, the data in the SEGRAM is output as display data from the segment driver.
PLUS = ”0” : Sets the display duty to 1 / 8 (when displaying 1 line) or 1 / 16 (when displaying 2 lines).
PLUS = “1” : Sets the display duty to 1 / 9 (when displaying 1 line) or 1 / 17 (when displaying 2 lines).

REV : Toggles between normal and reverse video for display.
REV = “0” : Normal video
REV = “1” : Reverse video

ALON : Toggles between normal and full lit-up display regardless the data type in the DDRAM. The setting of this bit takes priority over that of REV.
ALON = “0” : Normal display
ALON = “1” : Full lit-up display

### 2-7. Cursor / Display shift

| RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | S / C | R / L | * | * |

When the extended register enable bit (RE) is “0”, the following S / C and R / L bits may be set. The cursor position or the display is shifted to the left or right without writing the display data or reading it out. This may be used to modify or search the display. The cursor movement from the 1st to 2nd line occurs after the 16th digit in the 1st line. Note that all the lines are shifted simultaneously.
When duty + 1 command is ON (PLUS = 1), if S = 1 and any code is written into DDRAM, the line that COM1 scans is also shifted, so that this command is allowed only duty + 1 command is OFF (PLUS = 0) state.

### 2-8. Power control

| RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 1 | BIAS | HALT | PON | ACL |

BIAS : This command selects the displaying bias ratio.
BIAS = “0” : 1 / 5 bias.
BIAS = “1” : 1 / 4 bias.

HALT : Turns ON / OFF the power saving mode. When the APU0594 enters the power saving mode, the consumed current can be decreased to nearly the standby current value.
HALT = “0” : Normal mode.
HALT = “1” : Power saving mode.
The internal state in the power saving mode is decried below

- The oscillation and power circuits are stopped.
- The LCD drive is disabled. The output from the segment and common drivers are made at the $V_{SS}$ level.
- The clock input at the CK pin is inhibited.

PON : Turns ON / OFF the internal power circuit.
PON = “0” : Turns OFF the power circuit.
PON = “1” : Turns ON the power circuit.
The booster circuit and the voltage conversion circuit become active when the power circuit is turned on. The operating section in the circuits varies depending on the setting of the PMODE pin. For further details, see the description of functions.

ACL : The internal circuit can be initialized.
ACL = “0” : normal mode.
ACL = “1” : ACL operation is ON.
If you turn ON ACL command, the busy flag is generated. Therefore, to execute an instruction after ACL operation, monitor the busy flag and then execute the next period for 2 times the source clock frequency.

### 2-9. Function set

| RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 / 1 | 0 | 0 | 0 | 1 | BE | DUB | RE | BT | * |

RE : This bit is the enable bit for extended register. If RE = “1”, the extended function setting can be accessed.
When setting instruction, it is necessary to follow the state of RE bit.(refer to instruction code.)

BE : When BE = “1”, the information which was stored in the SEGRAM using its upper 2 bits may be used to allow for blinking the display data from the SEGRAM.

DUB : This bit is toggled the display double fonts lengthwise.
DUB = “0” : Display normal mode.
DUB = “1” : Display double fonts lengthwise.
*Note : Double fonts lengthwise is able to display only first line.
*Note : Not using these setting, when displaying 1 line mode. (NL = 1)

BT : This command selects the character blinking type.
BT = “0” : Displaying normal / reverse per 32 frames.
BT = “1” : Displaying normal / black per 32 frames.

### 2-10. CGRAM address set

| RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | A | A | A | A | A | A |

If the extended register enable bit (RE) is “0”, CGRAM addresses may be specified. In the above example, the address had shown in binary number for “AAAAAA” is allocated in the address counter. Subsequently data is written for read from the MPU by referencing the CGRAM.

### 2-11. SEGRAM address set

| RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | * | * | A | A | A | A |

If the extended register enable bit (RE) is “1”, SEGRAM addresses may be specified. The address had shown in binary number for “AAAA” is allocated in the address counter. Subsequently data is written or read from the MPU in referencing the SCGRAM.

### 2-12. DDRAM address set

| RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | * | A | A | A | A | A |

If the extended register enable bit (RE) is “0”, DDRAM addresses may be specified. The DDRAM address had shown in binary number for “AAAAA” is allocated in the address counter. Subsequently data is written or read from the MPU in referencing to the DDRAM.

### 2-13. Electronic volume register set

| RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | * | * | MSB.....LSB | | | |

The LCD drove voltage $V_0$ output from the built-in power circuit can be controlled and the display tone on the LCD can be also controlled.

The LCD drive voltage $V_0$ takes one out of 16 voltage values by setting 4 bit data register.

| MSB ····· LSB | $V_0$ |
|---|---|
| 0 0 0 0 | Smaller |
| 1 1 1 1 | Larger |

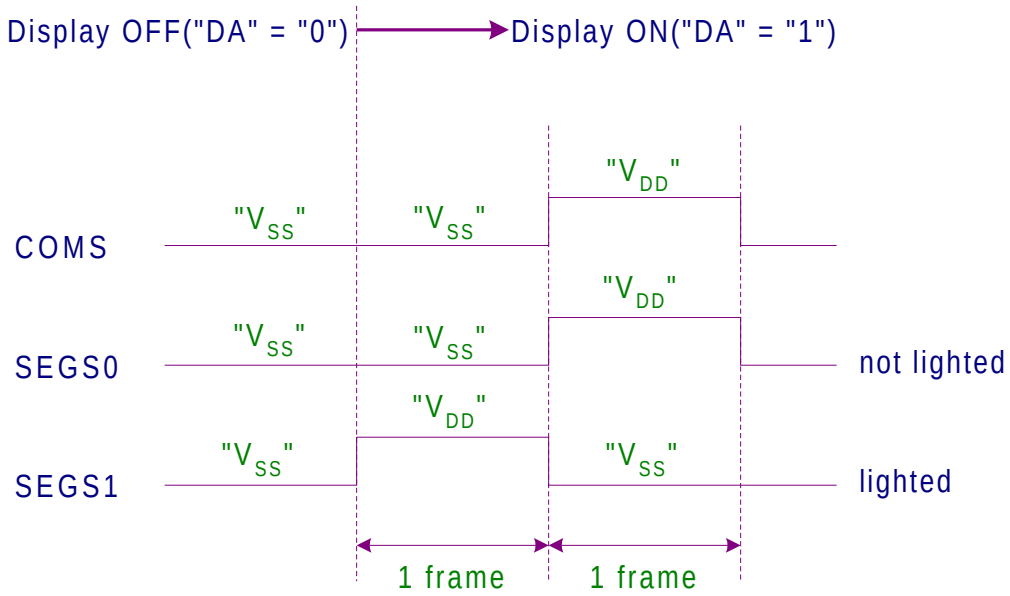
If the electronic control is not used, specify (1, 1, 1, and 1) in the 4-bit data register. After the APU0594 is reset, the 4-bit data register is automatically set to (1, 1, 1, 1).

### 2-14. Annunciator control

| RE | RS | D7 | D8 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | I5 | I4 | I3 | I2 | I1 | I0 |
| 1 | | | | DA | * | I9 | I8 | I7 | I6 |

I0 to I9 : These bits are setting data for annunclator. I0 to I9 correspond to SEGS0 to SEGS9 for static LCD drive outputs.

DA : When DA = “1”, outputs pin for static LCD drive (for annunciator display). Among $V_{DD}$ and $V_{SS}$ levels, one level is selected depending on the combination of COMS signal and display data (I0 to I9). When DA = “0”, outputs $V_{SS}$ level.




Example of outputs for annunciator (DA = "1", I0 = "0", I1 = "1")

### 2-15. Busy flag / address read

| RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 / 1 | 0 | BF | * | A | A | A | A | A | A |

"BF = 1" indicates that the APU0594 is internally operating and the next instruction is not accepted until "BF = 0". The busy flag is only generated when the display clear or the ACL command is executed. Therefore, any other instruction can be executed without monitoring the busy flag. Simultaneously, the address counter value presented in binary number for "AAAAAA" is read out. The address counter is used by the DDRAM, CGRAM, and SEGRAM. The data read out from the RAMs is determined by specifying a command before this.

### 2-16. Write data to RAM

| RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 / 1 | 1 | D | D | D | D | D | D | D | D |

Writes binary 8-bit data D0 to D7 to the CGRAM or DDRAM or SEGRAM.
Whether the CGRAM or DDRAM or SEGRAM is to be written into is determined by the previous specification of CGRAM or DDRAM or SEGRAM address setting. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode.

### 2-17. Read data to RAM

| RE | RS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 0 / 1 | 1 | D | D | D | D | D | D | D | D |

Reads binary 8-bit data D0 to D7 from the CGRAM or DGRAM or DDRAM or SEGRAM.
The most recent Set Address command determines whether the CGRAM or DDRAM or SEGRAM is to be read. After writing, the address automatically increments or decrements by 1, in accordance with the entry mode.

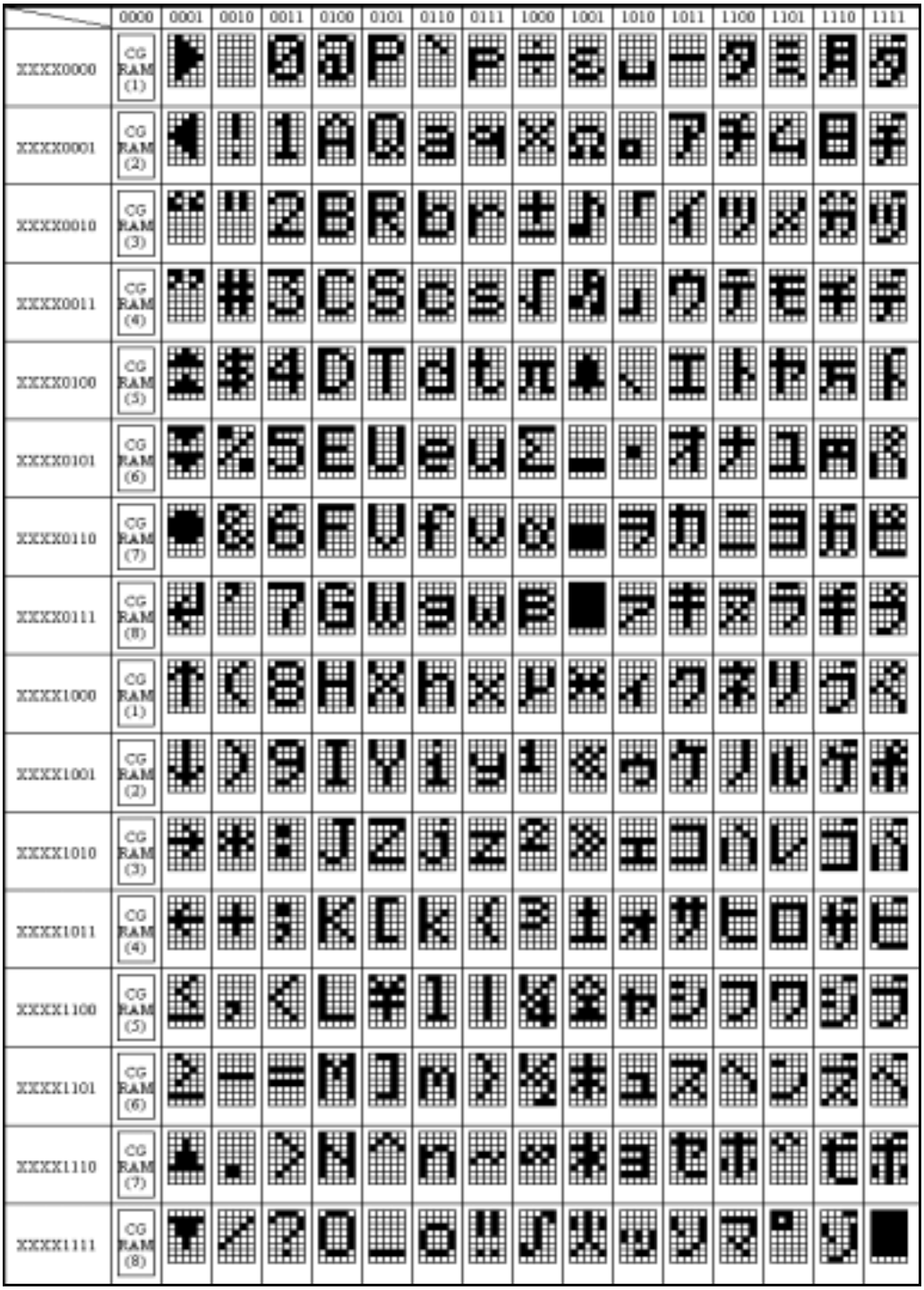
### 2-18. Example of instructions vs. display

| No. | Instruction<br>RS D7 D6 D5 D4 D3 D2 D1 D0 | Display | Action |
|---|---|---|---|
| 1 | Power ON | | No display appears. |
| 2 | Function set<br>0 0 0 1 * * 0 0 * | | “0” is written to RE bit. |
| 3 | Display clear<br>0 0 0 0 0 0 0 0 1 | | Display is cleared. |
| 4 | Display ON / OFF control<br>0 0 0 0 0 1 1 1 0 | – | Turns ON display and cursor. If Display clear, display is filled with blank spaces. |
| 5 | Entry mode set<br>0 0 0 0 0 0 1 1 0 | – | Counts up address by one and moves cursor to right when data is written to RAM. |
| 6 | DDRAM data write<br>1 0 1 0 0 0 0 0 1 | A_ | Writes “A”. |
| 7 | : | | |
| 8 | DDRAM data write<br>1 0 1 0 0 0 0 1 1 | ANPEC_ | Writes “C”. |
| 9 | DDRAM address set<br>0 1 * * 1 0 0 0 0 | ANPEC<br>_ | Set DRAM address so that cursor Is positioned at top of 2nt line. |
| 10 | DDRAM data write<br>1 0 1 0 0 1 1 0 0 | ANPEC<br>L_ | Writes “L”. |
| 11 | : | | |
| 12 | DDRAM data write<br>1 0 1 0 1 0 0 1 0 | ANPEC<br>LCDDRIVER_ | Writes “R”. |
| 13 | : | | |
| 14 | Cursor home<br>0 0 0 0 0 0 0 1 * | ANPEC<br>LCDDRIVER | Resets both display and cursor in place (address 0) |

## CONFIGURATION OF CGROM

Character codes vs. character patterns

Low order High order



## CONFIGURATION OF CGRAM

CGRAM addresses vs. character codes (DDRAM) and character patterns

| Character code | | | | | | | | CGRAM address | | | | | | CGRAM data | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A5 | A4 | A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 0 | 1 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 1 | 1 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 1 | 1 | | | | 0 | 1 | 0 | 1 | 0 | |
| | | | | | | | | | | | 1 | 0 | 0 | | | | 0 | 0 | 1 | 0 | 0 | |
| | | | | | | | | | | | 1 | 0 | 1 | | | | 0 | 0 | 1 | 0 | 0 | |
| | | | | | | | | | | | 1 | 1 | 0 | | | | 0 | 0 | 1 | 0 | 0 | (Y) |
| | | | | | | | | | | | 1 | 1 | 1 | | | | 0 | 0 | 0 | 0 | 0 | |
| 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 0 | 1 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 1 | 1 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 1 | 1 | | | | 0 | 1 | 0 | 1 | 0 | |
| | | | | | | | | | | | 1 | 0 | 0 | | | | 0 | 0 | 1 | 0 | 0 | |
| | | | | | | | | | | | 1 | 0 | 1 | | | | 0 | 0 | 1 | 0 | 0 | |
| | | | | | | | | | | | 1 | 1 | 0 | | | | 0 | 0 | 1 | 0 | 0 | (H) |
| | | | | | | | | | | | 1 | 1 | 1 | | | | 0 | 0 | 0 | 0 | 0 | |

(CGRAM).

∗mark shows “Don’t care”. Upper section : Character pattern 1 (Y display)

Lower section : Character pattern 2 (H display)

Note :

1. Character code bits D2 to D0 correspond to CGRAM addresses A5 to A3 (3 bits : 8 types)
2. CGRAM addressed A2 to A0 correspond to line positions of the character pattern (3 bits : 8 lines)
3. The columns of the character pattern are laid out with bit 0 allocated to the right end. Therefore, the pattern of bits 4 to 0 is displayed.
4. If the upper 4 bits (7 to 4) of the character code are zeros, the CGRAM is selected. Since bit D3 are “Don’t care”, “00H” and “08H” are the same CGRAM address.
5. If the CGRAM data is “1” data is displayed; if “0”, data isn’t displayed.

## CONFIGURATION OF SEGRAM

SEGRAM Addresses vs. Display Patterns

| SEGRAM address | | | | SEGRAM data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 0 | 0 | 0 | B1 | B0 | * | S0 | S1 | S2 | S3 | S4 |
| 0 | 0 | 0 | 1 | B1 | B0 | * | S5 | S6 | S7 | S8 | S9 |
| 0 | 0 | 1 | 0 | B1 | B0 | * | S10 | S11 | S12 | S13 | S14 |
| 0 | 0 | 1 | 1 | B1 | B0 | * | S15 | S16 | S17 | S18 | S19 |
| 0 | 1 | 0 | 0 | B1 | B0 | * | S20 | S21 | S22 | S23 | S24 |
| 0 | 1 | 0 | 1 | B1 | B0 | * | S25 | S26 | S27 | S28 | S29 |
| 0 | 1 | 1 | 0 | B1 | B0 | * | S30 | S31 | S32 | S33 | S34 |
| 0 | 1 | 1 | 1 | B1 | B0 | * | S35 | S36 | S37 | S38 | S39 |
| 1 | 0 | 0 | 0 | B1 | B0 | * | S40 | S41 | S42 | S43 | S44 |
| 1 | 0 | 0 | 1 | B1 | B0 | * | S45 | S46 | S47 | S48 | S49 |
| 1 | 0 | 1 | 0 | B1 | B0 | * | S50 | S51 | S52 | S53 | S54 |
| 1 | 0 | 1 | 1 | B1 | B0 | * | S55 | S56 | S57 | S58 | S29 |
| 1 | 1 | 0 | 0 | B1 | B0 | * | S60 | S61 | S62 | S63 | S64 |
| 1 | 1 | 0 | 1 | B1 | B0 | * | S65 | S66 | S67 | S68 | S69 |
| 1 | 1 | 1 | 0 | B1 | B0 | * | S70 | S71 | S72 | S73 | S74 |
| 1 | 1 | 1 | 1 | B1 | B0 | * | S75 | S76 | S77 | S78 | S79 |

*mark shows “Don’t care”.

Blink control (D7 and D6)

Pattern displayed (D4 to D0)

Note :

1. Data stored in the SEGRAM is output for one-line display when COM1 is selected.
2. Pins S0 to S79 are segment driver pins. **These segment physical positions will not be changed when either SHL 0 = “0” or “1”.**
3. After output at pin S79, that at pin S0 is repeated.
4. For SEGRAM data, the lower 5 bits are used for display data.
5. If BE bit control the blinking of the lower 5-bit pattern. When D7 is set to “1”, the lower 5-bit display blinks. If bit D6 is “1”, only the pattern of bit D4 can be blinked.
6. If SEGRAM data is “1”, data is displayed; or if “0”, data isn’t displayed.

## CONFIGURATION OF DDRAM

Display positions vs. display data RAM (DDRAM) addresses

| digit | 1st | 2nd | 3rd | 4th | 5th | 6th | 7th | 8th | 9th | 10th | 11th | 12th | 13th | 14th | 15th | 16th |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| COM0 to 7 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F |
| COM8 to 15 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F |

The above addressing is used because 16 digits are displayed. The DDRAM stores data for 32 characters.

If the display data is shifted, the DDRAM addresses are changed as follows :

Shift to right

| digit | 1st | 2nd | 3rd | 4th | 5th | 6th | 7th | 8th | 9th | 10th | 11th | 12th | 13th | 14th | 15th | 16th |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| COM0 to 7 | 1F | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E |
| COM8 to 15 | 0F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E |

Shift to left

| digit | 1st | 2nd | 3rd | 4th | 5th | 6th | 7th | 8th | 9th | 10th | 11th | 12th | 13th | 14th | 15th | 16th |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| COM0 to 7 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 |
| COM8 to 15 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 00 |

Note : The memory in the DDRAM is configured as follows :

Display area (16 characters x 2 line)

As shown above, the 2nd data appears following the end of the data in the 1st line. Notice that the addresses are consecutive.

# DESCRIPTION OF SERIAL INTERFACE

APU0594 built-in I²CBUS format interface.

The I²CBUS is for bi-directional, two-line communication between different ICs or modules.

## 1. I²CBUS PROTOCOL

I²CBUS protocol consists of data receiver and data transmitter.

The device, which control protocol, is Master, the device that is controlled is Slave.

Master controls data translation and provides clock signal.

The APU0594 is used as Slave receiver or Slave receiver Slave transmitter.

### 1-1. Data transfer

The change of SDA-state is allowed during SCL is low level. If SDA change during SCL is High, this action is recognized as Start bit or Stop bit.

### 1-2. Start signal

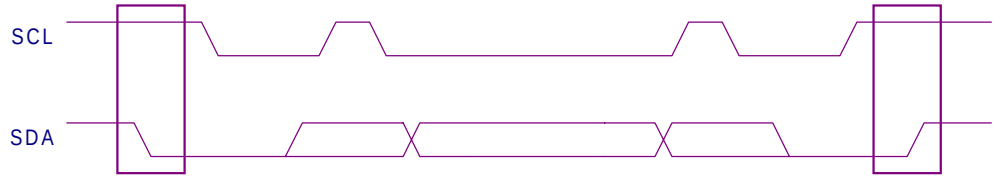
When the bus is not busy, SDA transfer High to Low during SCL is High.

This state is defined as the start condition.

### 1-3. Stop signal

When the bus is not busy, SDA transfer Low to High during SCL is High.

This state is defined as the stop condition.



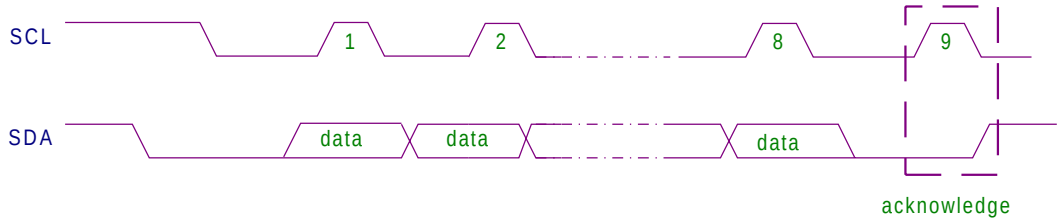

Start / Stop timing

### 1-4. Acknowledge

Acknowledge bit is used to confirm data translation.

Transmitters (Master or Slave) release bus lines after receive 8 bit data.

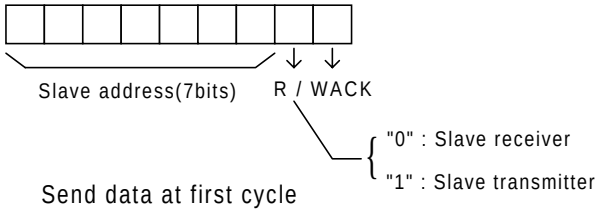
During next clock (9th clock) receiver, put Low Level on the bus to indicate data receive completely.




Acknowledge timing

### 1-5. Device Address code

After sending start bit, Master device must transfer 8bit device address code at first. Address code consists of 7bits-slave address and 1 bit R / W.




When read operation, R / W bit is “1”. When write operation, R / W bit is “0”.

### 1-6. Device addressing

Bus master must generate start-condition to start data translation between 2 devices. After generate start condition, Master puts 8 bit word on SDA bus line. APU0594 is fixed higher order bits (corresponding to DB7 to DB2) for identify device, it is fixed “011101”. Next 1 bit is used to select LCD driver among some devices connecting to same bus. APU0594 can connect to same bus up to 2 chips. SA0 is used for LSB bit for identify device.

8th bit (R / W bit) define operation mode.

R/W = “0” : Write operation

R/W = “1” : Read operation

| 0 | 1 | 1 | 1 | 0 | 1 | SA0 | R/W |
|---|---|---|---|---|---|---|---|

APU0594 Slave address

### 1-7. Second transferred data

After received start condition, first cycles of 1 byte, when Slave receive mode, APU0594 is specified control-byte waiting mode, Control-bye consists of 3 bits.

These bits are used to specify function mode for operating instruction.

Co : This bit define translation mode.

“0” : last control byte, only data bytes to follow

“1” : next two bytes are a data byte and another are control byte

RS : RS is correspond to “RS” signal in instruction table. This bit specified translation data,

R/W : This bit specified Read/Write mode.

“0” : Readable mode

“1” : Write enable mode.

| Co | RS | R/W | | | | | |
|---|---|---|---|---|---|---|---|

Send Data at second cycle

## 2. DESCRIPTION OF PIN CONNECTED WITH THE I²CBUS

- SCL
  Serial clock input pin
  SCL is used for clock of all data I/O
- SDA
  SDA is bi-directional pin, which is used to data I/O.
  SDA is open drain pin, so please connect to $V_{DD}$ via pull-up resistor.
- SA0
  SA0 is used for LSB bit of slave address (7 bits width). Must be fixed at “H” or “L” externally.
- ISEL
  ISEL select to use I²CBUS or not
  When ISEL is “H”, I²CBUS is enable.
  If ISEL is LOW, I²CBUS-operation of APU0594 is not warranty.

## 3. EXAMPLE OF I²CBUS OPERATION (1/3)

| STEP | I²C BYTE | | | | | | | | | DISPLAY | OPERATION |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | I²C START | | | | | | | | | | Initialized. Nothing display |
| 2 | Writing Slave address | | | | | | | | | | During the acknowledge cycle SDA will be pull-downed by UC037 |
| | SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 | R/W | ACK | | |
| | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | | |
| 3 | Send a control byte | | | | | | | | | | Control bits RS and Co and R/W are specified |
| | Co | RS | R/W | | | | | | ACK | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | |
| 4 | Function set | | | | | | | | | | Set RE bit “0” |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | ACK | | |
| | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | | |
| 5 | Display Clear | | | | | | | | | | Display clear |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | ACK | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | | |
| 6 | Display ON/OFF control | | | | | | | | | — | Display and cursor are ON<br>All Display are clear by operating Display clear |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | ACK | | |
| | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | | |
| 7 | Entry mode set | | | | | | | | | — | Entry mode set. When RAM writing, address is up by 1 and cursor is shifted right. |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | ACK | | |
| | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | | |
| 8 | CGRAM address set | | | | | | | | | — | Set address to write into CGRAM |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | ACK | | |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | |
| 9 | Start condition | | | | | | | | | — | Set RS bit “1” and generated start condition for writing |
| 10 | Send Slave address | | | | | | | | | — | |
| | SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 | R/W | ACK | | |
| | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | | |

## EXAMPLE OF I²CBUS OPERATION (2/3)

| STEP | I²C BYTE | | | | | | | | | DISPLAY | OPERATION |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 11 | Send Control byte | | | | | | | | | — | |
| | Co | RS | R/W | | | | | | ACK | | |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | |
| 12 | CGRAM data write | | | | | | | | | — | Write CGRAM data |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | ACK | | |
| | 0 | 0 | 0 | CG4 | CG3 | CG2 | CG1 | CG0 | 1 | | |
| 13 | : | | | | | | | | | | |
| | : | | | | | | | | | | |
| | : | | | | | | | | | | |
| 14 | Start condition | | | | | | | | | — | Generated start condition again for setting RS “0” |
| 15 | Send condition | | | | | | | | | — | |
| 16 | Send control byte | | | | | | | | | — | |
| | Co | RS | R/W | | | | | | ACK | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | |
| 17 | Set DDRAM address | | | | | | | | | — | Setting address for DDRAM writing |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | ACK | | |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | |
| 18 | Start condition | | | | | | | | | — | Set RS “1” and generated start condition again for DDRAM writing |
| 19 | Send Slave address | | | | | | | | | — | |
| | SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 | R/W | ACK | | |
| | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | | |
| 20 | Send control byte | | | | | | | | | — | |
| | Co | RS | R/W | | | | | | ACK | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | |
| 21 | Write DDRAM data | | | | | | | | | A_ | Write “A” |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | ACK | | |
| | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | | |
| 22 | : | | | | | | | | | | |
| | : | | | | | | | | | | |
| 23 | Send DDRAM data | | | | | | | | | ANPEC_ | Write ”C” |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | ACK | | |
| | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | | |
| 24 | Start condition | | | | | | | | | ANPEC_ | Set RS ”1” and generated start condition again for DDRAM writing |
| 25 | Send Slave address | | | | | | | | | ANPEC_ | |
| | SA6 | SA5 | SA4 | SA3 | SA2 | SA1 | SA0 | R/W | ACK | | |
| | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | | |
| 26 | Send control byte | | | | | | | | | ANPEC_ | |
| | Co | RS | R/W | | | | | | ACK | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | |
| 27 | Send DDRAM address | | | | | | | | | ANPEC_ | Set DDRAM address for cursor set ahead of 2nd line |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | ACK | | |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | | |
| 28 | Start condition | | | | | | | | | ANPEC_ | Set RS “1” and generated start Condition again for DDRAM Writing |

## EXAMPLE OF I²CBUS OPERATION (3/3)

| STEP | I²C BYTE | DISPLAY | OPERATION |
|---|---|---|---|
| 29 | Send Slave address<br>SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK<br>0 1 1 1 0 1 0 0 1 | ANPEC_ | |
| 30 | Send control byte<br>Co RS R/W ACK<br>0 1 0 0 0 0 0 0 1 | ANPEC_ | |
| 31 | Write DDRAM data<br>D7 D6 D5 D4 D3 D2 D1 D0 ACK<br>0 1 0 0 0 0 0 0 1 | ANPEC<br>L_ | Write “L” |
| 32 | : | | |
| 33 | Write DDRAM data<br>D7 D6 D5 D4 D3 D2 D1 D0 ACK<br>0 1 0 1 0 0 1 0 1 | ANPEC<br>LCDDRIVER_ | Write “R” |
| 34 | Start condition | ANPEC<br>LCDDRIVER_ | Set RS “1” and generated start condition again for DDRAM writing |
| 35 | Send Slave address<br>SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK<br>0 1 1 1 0 1 0 0 1 | ANPEC<br>LCDDRIVER_ | |
| 36 | Send control byte<br>Co RS R/W ACK<br>1 0 0 0 0 0 0 0 1 | ANPEC<br>LCDDRIVER_ | Set control bit Co “1” |
| 37 | Set DDRAM address<br>D7 D6 D5 D4 D3 D2 D1 D0 ACK<br>1 0 0 0 0 0 0 0 1 | ANPEC<br>LCDDRIVER_ | Set address for read-out DDRAM data |
| 38 | Send control byte<br>Co RS R/W ACK<br>0 1 1 0 0 0 0 0 1 | ANPEC<br>LCDDRIVER _ | Set control bit RS “1” and R/W “1” |
| 39 | Start condition | ANPEC<br>LCDDRIVER _ | Set RS “1” and generated start condition again for DDRAM writing |
| 40 | Send Slave address<br>SA6 SA5 SA4 SA3 SA2 SA1 SA0 R/W ACK<br>0 1 1 1 0 1 0 1 1 | ANPEC<br>LCDDRIVER _ | Set R/W “1” for read-out DDRAM data |
| 41 | Read out data<br>D7 D6 D5 D4 D3 D2 D1 D0 ACK<br>MSB …… LSB | ANPEC<br>LCDDRIVER _ | Read-out DDRAM data from MSB to LSB<br>Master doing acknowledge |
| 42 | : | | |
| 43 | Read out data<br>D7 D6 D5 D4 D3 D2 D1 D0 ACK<br>MSB …… LSB 1 | ANPEC<br>LCDDRIVER _ | As master don’t acknowledge, data will not be output in next cycle |
| 44 | Stop condition | ANPEC<br>LCDDRIVER _ | Generated Stop condition and finish |

## ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Condition | Applicable pin | Rated value | Unit |
|---|---|---|---|---|---|
| Supply voltage (1) | $V_{DD}$ | Relative to $V_{SS}$ (0 V) : Ta = +25°C | $V_{DD}$ | -0.3 to +7.0 | V |
| Supply voltage (2) | $V_{EE}$ | | $V_{EE}$ | -0.3 to +7.0 | V |
| Supply voltage (3) | $V_{OUT}$ | | $V_{OUT}$ | -0.3 to +13.0 | V |
| Supply voltage (3) | VR | | VR | -0.3 to +13.0 | V |
| Supply voltage (3) | $V_0$ | | $V_0$ | -0.3 to +13.0 | V |
| Supply voltage (4) | $V_1$,$V_2$,$V_3$,$V_4$ | | $V_1$,$V_2$,$V_3$,$V_4$ | -0.3 to $V_0$ +0.3 | V |
| Input voltage | $V_I$ | | ∗1 | -0.3 to $V_{DD}$ +0.3 | V |
| Storage temperature | Tstg | | | -45 to +125 | °C |

∗1 : D0 to D7, CSB, RS, M86, RDB, WRB, CK, CKS, OSCI, P/S, RESB, PMODE, SHL0, SHL1 and TEST pins

## RECOMMENDED OPERATING CONDITIONS

| Item | Symbol | Applicable pin | MIN | TYP | MAX | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD}$ | 2.7 | | 5.5 | V | ∗1 |
| Recommended operating voltage | $V_0$ | $V_0$ | 4 | | 11 | V | ∗2 |
| | $V_{OUT}$ | $V_{OUT}$ | 4 | | 11 | V | |
| Operating temperature | Topr | | -30 | | 85 | °C | |

∗1 : This is the voltage applied to the $V_{SS}$ pin.

∗2 : The voltage relation shall meet the condition of $V_{SS} < V_4 < V_3 < V_2 < V_1 < V_0$.

## Customer Service

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# ELECTRICAL CHARACTERISTICS

## 1. DC CHARACTERISTICS

Unless otherwise specified, $V_{SS}$ = 0V, $V_{DD}$ = +2.7 to +5.5V and Ta = -30 to +85°C

| Item | Symbol | Applicable condition | | MIN | TYP | MAX | Unit | Applicable pin |
|---|---|---|---|---|---|---|---|---|
| High-level input voltage(1) | VIH | | | 0.8 $V_{DD}$ | | $V_{DD}$ | V | ∗1 |
| Low-level input voltage(1) | VIL | | | 0 | | 0.2 $V_{DD}$ | V | ∗1 |
| High-level output voltage(1) | VOH | IOH = -0.4 mA | | $V_{DD}$ -0.4 | | | V | ∗2 |
| Low-level output voltage(1) | VOL | IOL = 0.4 mA | | | | 0.4 | V | ∗2 |
| Input leak current | ILI | $V_I$ = $V_{SS}$ or $V_{DD}$ | | -10 | | 10 | µA | ∗3 |
| Output leak current | ILO | $V_I$ = $V_{SS}$ or $V_{DD}$ | | -10 | 4 | 10 | µA | ∗4 |
| Resistance when LCD driver output is turned ON | RON1 | \| ΔVon\| = 0.5V | $V_0$ = 8V | | | 8 | kΩ | ∗5 |
| Resistance when static LCD driver output is turned ON | RON2 | \| ΔVon\| = 0.5V | | | | 8 | kΩ | ∗6 |
| Standby current | ISTB | CK = 0V<br>CSB = $V_{DD}$ | $V_{DD}$ =3V<br>$V_{DD}$ =5V | | | 5<br>10 | µA | ∗7 |
| Oscillation frequency | fosc | Rf = Ω±2% | $V_{DD}$ =3V | | 46 | | kHz | ∗8 |
| Booster input voltage | $V_{EE}$ | | | 2.4 | | 5.5 | V | ∗9 |
| Booster output voltage | $V_{OUT}$ | When voltage is tripled ($V_{EE}$ = 3V)<br>When voltage is doubled ($V_{EE}$ = 3V) | | 8.6<br>5.7 | | | V | ∗10 |
| Current consumption(1) | IDD1 | $V_0$ = 6V, $V_{DD}$ = 3V (triple voltage) | | | | | µA | ∗11 |
| Current consumption(2) | IDD2 | $V_0$ = 5V, $V_{DD}$ = 3V (double voltage) | | | | | µA | ∗12 |
| Reset “L” pulse width | tRW | | | 10 | | | µs | ∗13 |

Applicable pins :

∗1 : D0 to D7, CSB, RS M86, RDB, WRB, CK, CKS, P/S, RESB, PMODE, SHL0, SHL1 and TEST pins.

∗2 : D0 to D7, LP, FLM and M pins.

∗3 : CSB, RS, M86, RDB, WRB, CK, CKS, P/S, RESB, PMODE, SHL0, SHL1 and TEST pins.

∗4 : Applicable when D0 to D7 are at high impedance.

∗5 : SEG0 to SEG79, COM0 to COM15 and COM1 pins.
Resistance value when 0.5V is applied between each output pin and each power source ($V_0$, $V_1$, $V_2$, $V_3$, $V_4$ or $V_{SS}$).
Applicable when power is supplied at the power bias ratio of 1/7 in the external power supply mode.

∗6 : SEGS0 to SEGS9 and COMS pins.

∗7 : Current at the $V_D$ pin when the source oscillation frequency clock is stopped; the chip is not selected (CSB = $V_{DD}$); and no load is used.

∗8 : Oscillation frequency when feedback resistor Rf of 1MΩ is connected between OSCI and OSCO.

∗9 : If the step-up circuit is used, the primary power $V_{EE}$ must be used within the above range. If the drive voltage for the LCD panel you are mounting can boost using the voltage level at the $V_{DD}$ pin, connect to the normal $V_{DD}$ power supply.

∗10 : $V_{OUT}$ pin

Applicable when the built-in oscillation circuit (Rf = Ω) and power circuit (PMODE = ”L”) are used. Measuring conditions : C1 = 1µF; $V_{OUT}$ pin is connected only C1 and the LCD driver pin is not loaded.

∗11 : Applicable if no access is made by the MPU when the built-in oscillation circuit (Rf = Ω) and power circuit (PMODE = ”L”) are used . The electronic control is not used (The code is “1111”). The step-up circuit is used for tripling voltage. The display is full lit-up (ALON = ”1”) and the LCD driver pin is not loaded.

Measuring conditions : $V_{DD}$ = $V_{EE}$; VR1 = VR2; C1 = 1µF; C2 = 0.1µF; R1+R2+R3 = 4MΩ; the current flowing through voltage control resistors (R1, R2 and R3) is included.

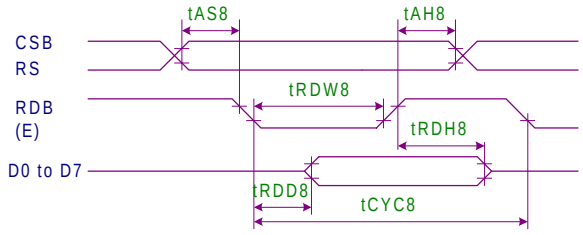
∗12 : Applicable if no access is made by the MPU when the built-in oscillation circuit (Rf = kΩ) and power circuit (PMODE = ”L”) are used. The electronic control is not used (The code is “1111”). The step-up circuit is used for double voltage. The display is full lit-up (ALON = ”1”) and the LCD driver pin is not loaded. Measuring conditions : $V_{DD}$ = $V_{EE}$; VR1 = VR2; C1 = 1µF; C2 = 0.1µF; R1+R2+R3 = 4MΩ; the current flowing through voltage control resistors (R1, R2 and R3) is included.

∗13 : RESB pin

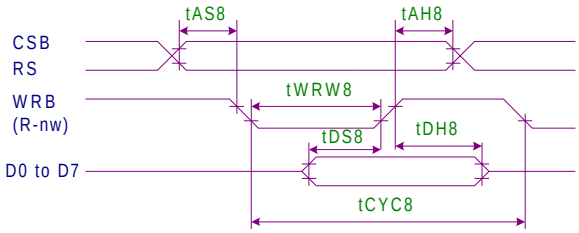
## 2. AC CHARACTERISTICS

### 2-1.System bus read / write timing (80-family MPU)

(Read timing)




(Write timing)



(80-family MPU timing characteristics)

($V_{DD}$ = 4.5 to 5.5V, Ta = -30 to +85°C)

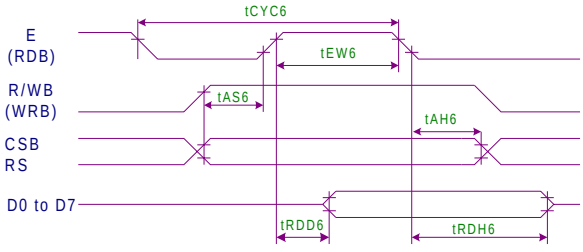
| Item | Symbol | Measuring condition | MIX | MAX | Unit | Applicable pin |
|---|---|---|---|---|---|---|
| Address hold time<br>Address setup time | tAH8<br>tAS8 | | | | ns | CSB<br>RS |
| System cycle time<br>Read pulse width<br>Write pules width | tCYC8<br>tRDW8<br>tWRW8 | | | | ns | WRB<br>RDB |
| Data setup time<br>Data hold time | tDS8<br>tDH8 | | | | ns | D0 to D7 |
| Read data output delay time<br>Read data hold time | tRDD8<br>tRDH8 | CL = 15 pF | | | ns | D0 to D7 |
| Input signal rise and fall time | tr, tf | | | | ns | All of above pins |

($V_{DD}$ = 4.5 to 5.5V, Ta = -30 to +85°C)

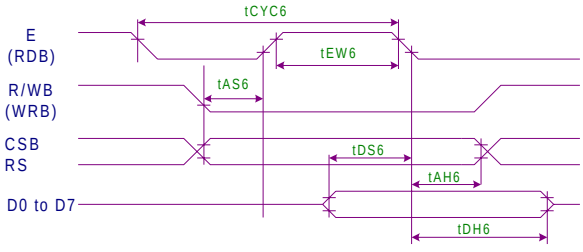
| Item | Symbol | Measuring condition | MIX | MAX | Unit | Applicable pin |
|---|---|---|---|---|---|---|
| Address hold time<br>Address setup time | tAH8<br>tAS8 | | | | ns | CSB<br>RS |
| System cycle time<br>Read pulse width<br>Write pules width | tCYC8<br>tRDW8<br>tWRW8 | | | | ns | WRB<br>RDB |
| Data setup time<br>Data hold time | tDS8<br>tDH8 | | | | ns | D0 to D7 |
| Read data output delay time<br>Read data hold time | tRDD8<br>tRDH8 | CL = 15 pF | | | ns | D0 to D7 |
| Input signal rise and fall time | tr, tf | | | | ns | All of above pins |

**2-2. System bus read/write timing (68-family MPU)**

(Read timing)



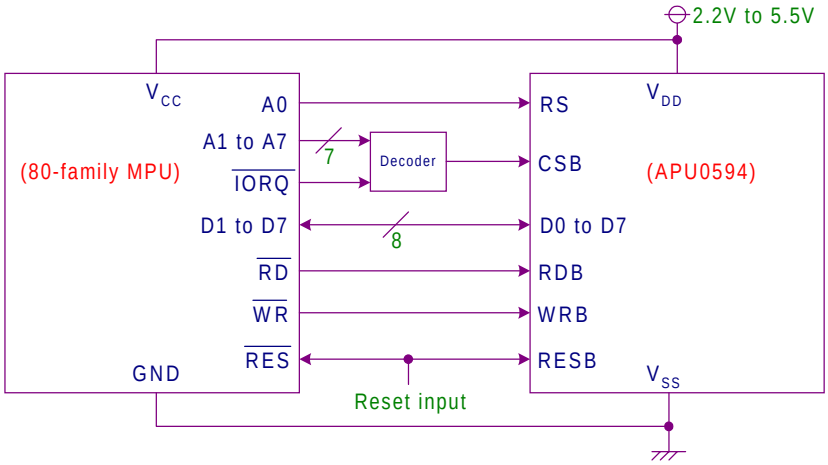

(Write timing)



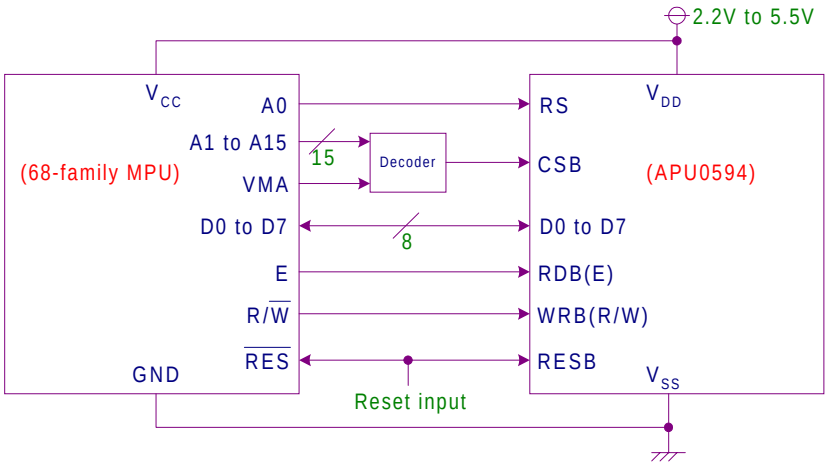
# TYPICAL APPLICATION (FOR REFERENCE)

## CONNECTION TO THE MPU

**1. Connection to the 80-family MPU**




**2. Connection to the 68-family MPU**




# TYPICAL EXAMPLE OF CHARACTERISTICS

| Item | Condition | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| Basic gate propagation delay time | Ta = +25°C, $V_{SS}$ = 0V, $V_{DD}$ = 5.0V | | 10 | | ns |