

# EFM8 Busy Bee Family

## EFM8BB1 Data Sheet



The EFM8BB1, part of the Busy Bee family of MCUs, is a multi-purpose line of 8-bit microcontrollers with a comprehensive feature set in small packages.

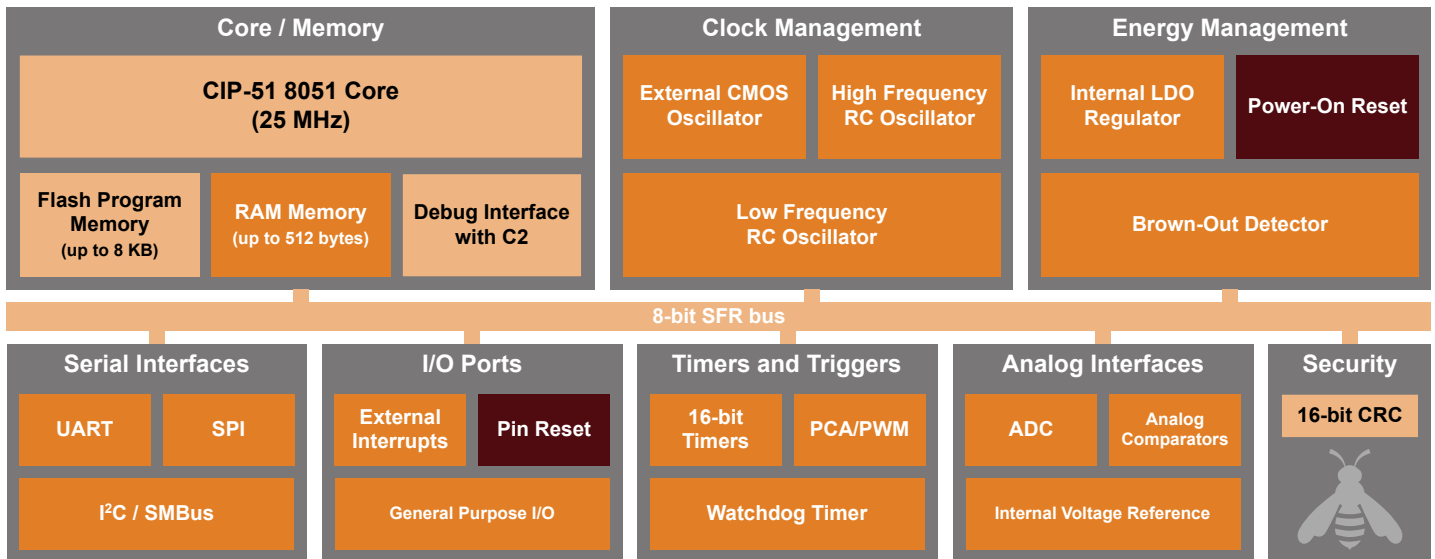
These devices offer high-value by integrating advanced analog and communication peripherals into small packages, making them ideal for space-constrained applications. With an efficient 8051 core, enhanced pulse-width modulation, and precision analog, the EFM8BB1 family is also optimal for embedded applications.

EFM8BB1 applications include the following:

- Motor control
- Consumer electronics
- Sensor controllers
- Medical equipment
- Lighting systems
- I/O port expander

### KEY FEATURES

- Pipelined 8-bit C8051 core with 25 MHz maximum operating frequency
- Up to 18 multifunction, 5 V tolerant I/O pins
- One 12-bit Analog to Digital converter (ADC)
- Two low-current analog comparators
- Integrated temperature sensor
- 3-channel enhanced PWM / PCA
- Four 16-bit timers
- UART, SPI and SMBus/I2C
- Priority crossbar for flexible pin mapping



Lowest power mode with peripheral operational:

Normal
  Idle
  Shutdown

## 1. Feature List

The EFM8BB1 highlighted features are listed below.

- Core:
  - Pipelined CIP-51 Core
  - Fully compatible with standard 8051 instruction set
  - 70% of instructions execute in 1-2 clock cycles
  - 25 MHz maximum operating frequency
- Memory:
  - Up to 8 kB flash memory, in-system re-programmable from firmware.
  - Up to 512 bytes RAM (including 256 bytes standard 8051 RAM and 256 bytes on-chip XRAM)
- Power:
  - Internal LDO regulator for CPU core voltage
  - Power-on reset circuit and brownout detectors
- I/O: Up to 18 total multifunction I/O pins:
  - All pins 5 V tolerant under bias
  - Flexible peripheral crossbar for peripheral routing
  - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
  - Internal 24.5 MHz oscillator with  $\pm 2\%$  accuracy
  - Internal 80 kHz low-frequency oscillator
  - External CMOS clock option
- Timers/Counters and PWM:
  - 3-channel programmable counter array (PCA) supporting PWM, capture/compare, and frequency output modes
  - 4 x 16-bit general-purpose timers
  - Independent watchdog timer, clocked from the low frequency oscillator
- Communications and Digital Peripherals:
  - UART
  - SPI™ Master / Slave
  - SMBus™/I2C™ Master / Slave
  - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
- Analog:
  - 12-Bit Analog-to-Digital Converter (ADC)
  - 2 x Low-current analog comparators with adjustable reference
- On-Chip, Non-Intrusive Debugging
  - Full memory and register inspection
  - Four hardware breakpoints, single-stepping
- Pre-loaded UART bootloader
- Temperature range -40 to 85 °C
- Single power supply 2.2 to 3.6 V
- QSOP24, SOIC16, and QFN20 packages

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8BB1 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Each device is specified for 2.2 to 3.6 V operation, is AEC-Q100 qualified, and is available in 20-pin QFN, 16-pin SOIC or 24-pin QSOP packages. All package options are lead-free and RoHS compliant.

## 2. Ordering Information

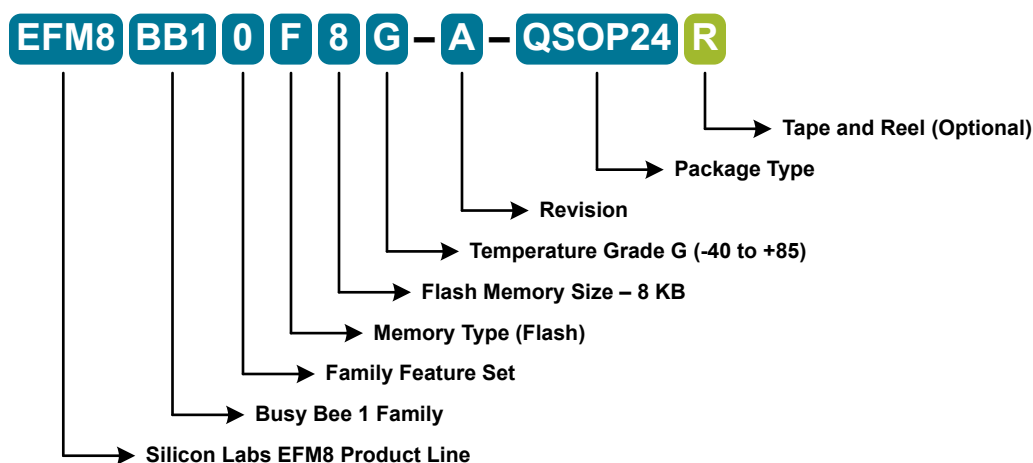


Figure 2.1. EFM8BB1 Part Numbering

All EFM8BB1 family members have the following features:

- CIP-51 Core running up to 25 MHz
- Two Internal Oscillators (24.5 MHz and 80 kHz)
- SMBus / I2C
- SPI
- UART
- 3-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 4 16-bit Timers
- 2 Analog Comparators
- 12-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, and temperature sensor
- 16-bit CRC Unit
- AEC-Q100 qualified
- Pre-loaded UART bootloader

In addition to these features, each part number in the EFM8BB1 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

| Ordering Part Number | Flash Memory (kB) | RAM (Bytes) | Digital Port I/Os (Total) | ADC Channels | Comparator 0 Inputs | Comparator 1 Inputs | Pb-free (RoHS Compliant) | Temperature Range | Package |
|----------------------|-------------------|-------------|---------------------------|--------------|---------------------|---------------------|--------------------------|-------------------|---------|
| EFM8BB10F8G-A-QSOP24 | 8                 | 512         | 18                        | 16           | 8                   | 8                   | Yes                      | -40 to +85 C      | QSOP24  |
| EFM8BB10F8G-A-QFN20  | 8                 | 512         | 16                        | 15           | 8                   | 7                   | Yes                      | -40 to +85 C      | QFN20   |
| EFM8BB10F8G-A-SOIC16 | 8                 | 512         | 13                        | 12           | 6                   | 6                   | Yes                      | -40 to +85 C      | SOIC16  |
| EFM8BB10F4G-A-QFN20  | 4                 | 512         | 16                        | 15           | 8                   | 7                   | Yes                      | -40 to +85 C      | QFN20   |
| EFM8BB10F2G-A-QFN20  | 2                 | 256         | 16                        | 15           | 8                   | 7                   | Yes                      | -40 to +85 C      | QFN20   |

### 3. System Overview

#### 3.1 Introduction

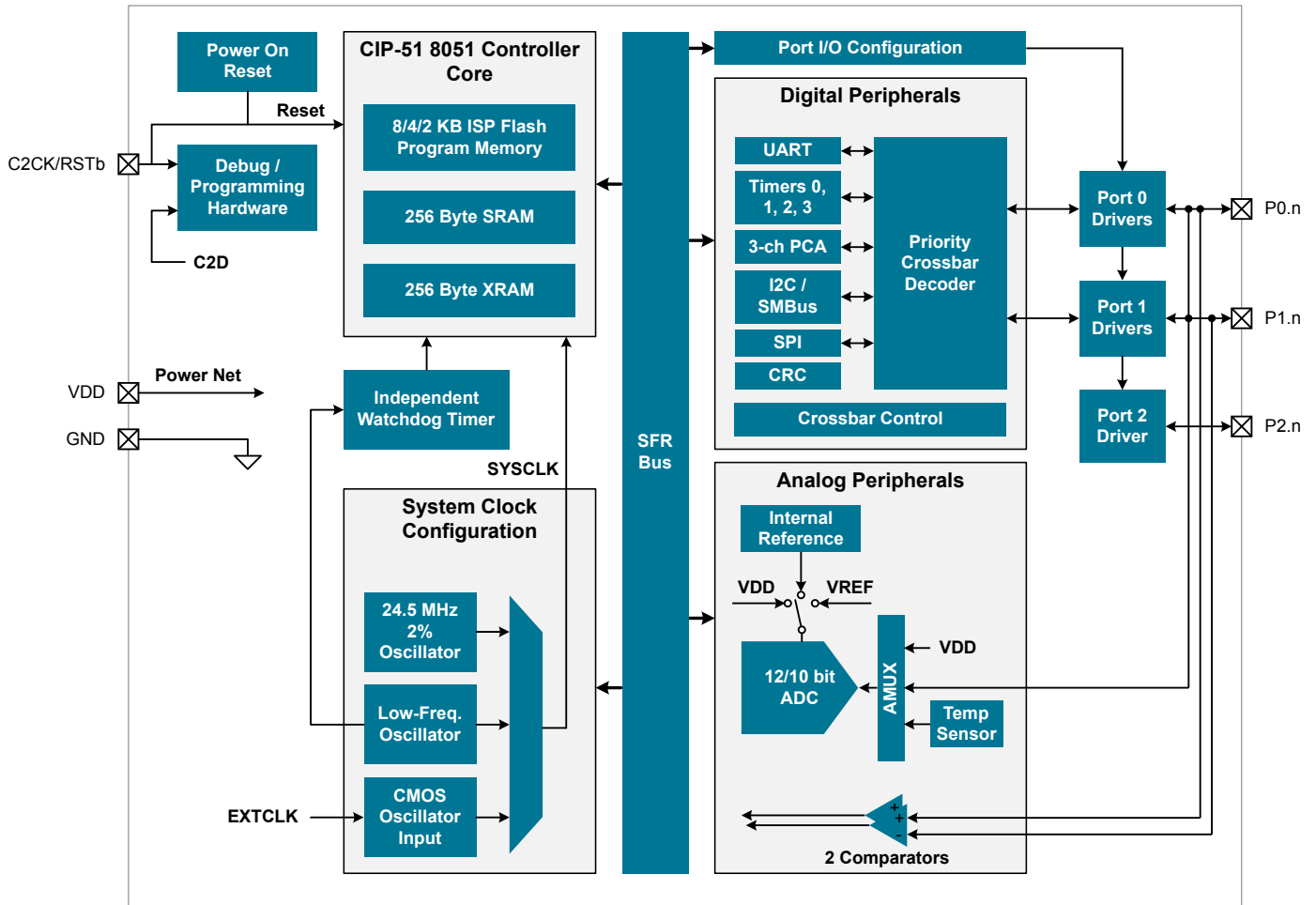


Figure 3.1. Detailed EFM8BB1 Block Diagram

### 3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

**Table 3.1. Power Modes**

| Power Mode | Details                                                                                                                                                            | Mode Entry                                                                                                | Wake-Up Sources                                                                          |
|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------|
| Normal     | Core and all peripherals clocked and fully operational                                                                                                             | —                                                                                                         | —                                                                                        |
| Idle       | <ul style="list-style-type: none"> <li>Core halted</li> <li>All peripherals clocked and fully operational</li> <li>Code resumes execution on wake event</li> </ul> | Set IDLE bit in PCON0                                                                                     | Any interrupt                                                                            |
| Shutdown   | <ul style="list-style-type: none"> <li>All internal power nets shut down</li> <li>Pins retain state</li> <li>Exit on pin or power-on reset</li> </ul>              | <ol style="list-style-type: none"> <li>Set STOPCF bit in REG0CN</li> <li>Set STOP bit in PCON0</li> </ol> | <ul style="list-style-type: none"> <li>RSTb pin reset</li> <li>Power-on reset</li> </ul> |

### 3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P1.7 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.0 and P2.1 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P2.0.

- Up to 18 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 16 direct-pin interrupt sources with shared interrupt vector (Port Match).

### 3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to  $\pm 2\%$  over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External CMOS clock input (EXTCLK).
- Clock divider with eight settings for flexible clock scaling: Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.

## 3.5 Counters/Timers and PWM

### Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to three independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware “kill” signal from comparator 0

### Timers (Timer 0, Timer 1, Timer 2, and Timer 3)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2 and Timer 3 are 16-bit timers including the following features:

- Clock sources include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8.
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- External pin capture (Timer 2)
- LFOSC0 capture (Timer 3)

### Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- Programmable timeout interval
- Runs from the low-frequency oscillator
- Lock-out feature to prevent any modification until a system reset

## 3.6 Communications and Other Digital Peripherals

### Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions
- Baud rates up to  $\text{SYSCLK}/2$  (transmit) or  $\text{SYSCLK}/8$  (receive)
- 8- or 9-bit data
- Automatic start and stop generation

### Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

The SPI module includes the following features:

- Supports 3- or 4-wire operation in master or slave modes.
- Supports external clock frequencies up to  $\text{SYSCLK} / 2$  in master mode and  $\text{SYSCLK} / 10$  in slave mode.
- Support for four clock phase and polarity options.
- 8-bit dedicated clock rate generator.
- Support for multiple masters on the same data lines.

### System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I<sup>2</sup>C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to inhibit all slave states.
- Programmable data setup/hold times.

### 16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

## 3.7 Analog

### 12-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12-, 10-, and 8-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 16 external inputs.
- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 200 ksps samples per second in 12-bit mode or 800 ksps samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Support for burst mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal fast-settling reference with two levels (1.65 V and 2.4 V) and support for external reference and signal ground.
- Integrated temperature sensor.

### Low Current Comparators (CMP0, CMP1)

Analog comparators are used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator module includes the following features:

- Up to 8 external positive inputs.
- Up to 8 external negative inputs.
- Additional input options:
  - Internal connection to LDO output.
  - Direct connection to GND.
- Synchronous and asynchronous outputs can be routed to pins via crossbar.
- Programmable hysteresis between 0 and  $\pm 20$  mV
- Programmable response time.
- Interrupts generated on rising, falling, or both edges.



### 3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset

### 3.9 Debugging

The EFM8BB1 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

### 3.10 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in flash and can be erased if it is not needed.

## 4. Electrical Specifications

### 4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in [Table 4.1 Recommended Operating Conditions on page 9](#), unless stated otherwise.

**Table 4.1. Recommended Operating Conditions**

| Parameter                        | Symbol              | Test Condition | Min | Typ | Max | Unit |
|----------------------------------|---------------------|----------------|-----|-----|-----|------|
| Operating Supply Voltage on VDD  | V <sub>DD</sub>     |                | 2.2 | —   | 3.6 | V    |
| System Clock Frequency           | f <sub>SYSCLK</sub> |                | 0   | —   | 25  | MHz  |
| Operating Ambient Temperature    | T <sub>A</sub>      |                | −40 | —   | 85  | °C   |
| All voltages with respect to GND |                     |                |     |     |     |      |

**Table 4.2. Power Consumption**

| Parameter                                                                               | Symbol             | Test Condition                                                     | Min | Typ  | Max  | Unit |
|-----------------------------------------------------------------------------------------|--------------------|--------------------------------------------------------------------|-----|------|------|------|
| Digital Core Supply Current                                                             |                    |                                                                    |     |      |      |      |
| Normal Mode—Full speed with code executing from flash                                   | I <sub>DD</sub>    | F <sub>SYSCLK</sub> = 24.5 MHz <sup>2</sup>                        | —   | 4.45 | 4.85 | mA   |
|                                                                                         |                    | F <sub>SYSCLK</sub> = 1.53 MHz <sup>2</sup>                        | —   | 915  | 1150 | μA   |
|                                                                                         |                    | F <sub>SYSCLK</sub> = 80 kHz <sup>3</sup> , T <sub>A</sub> = 25 °C | —   | 250  | 290  | μA   |
|                                                                                         |                    | F <sub>SYSCLK</sub> = 80 kHz <sup>3</sup>                          | —   | 250  | 380  | μA   |
| Idle Mode—Core halted with peripherals running                                          | I <sub>DD</sub>    | F <sub>SYSCLK</sub> = 24.5 MHz <sup>2</sup>                        | —   | 2.05 | 2.3  | mA   |
|                                                                                         |                    | F <sub>SYSCLK</sub> = 1.53 MHz <sup>2</sup>                        | —   | 550  | 700  | μA   |
|                                                                                         |                    | F <sub>SYSCLK</sub> = 80 kHz <sup>3</sup> , T <sub>A</sub> = 25 °C | —   | 125  | 130  | μA   |
|                                                                                         |                    | F <sub>SYSCLK</sub> = 80 kHz <sup>3</sup>                          | —   | 125  | 200  | μA   |
| Stop Mode—Core halted and all clocks stopped, Internal LDO On, Supply monitor off.      | I <sub>DD</sub>    | T <sub>A</sub> = 25 °C                                             | —   | 105  | 120  | μA   |
|                                                                                         |                    | T <sub>A</sub> = −40 to +85 °C                                     | —   | 105  | 170  | μA   |
| Shutdown Mode—Core halted and all clocks stopped, Internal LDO Off, Supply monitor off. | I <sub>DD</sub>    |                                                                    | —   | 0.2  | —    | μA   |
| Analog Peripheral Supply Currents                                                       |                    |                                                                    |     |      |      |      |
| High-Frequency Oscillator                                                               | I <sub>HFOSC</sub> | Operating at 24.5 MHz,<br>T <sub>A</sub> = 25 °C                   | —   | 155  | —    | μA   |
| Low-Frequency Oscillator                                                                | I <sub>LFOSC</sub> | Operating at 80 kHz,<br>T <sub>A</sub> = 25 °C                     | —   | 3.5  | —    | μA   |

| Parameter                                                                               | Symbol              | Test Condition                                                                                                        | Min | Typ | Max  | Unit |
|-----------------------------------------------------------------------------------------|---------------------|-----------------------------------------------------------------------------------------------------------------------|-----|-----|------|------|
| ADC0 Always-on <sup>4</sup>                                                             | I <sub>ADC</sub>    | 800 ksps, 10-bit conversions or<br>200 ksps, 12-bit conversions<br>Normal bias settings<br>V <sub>DD</sub> = 3.0 V    | —   | 845 | 1200 | μA   |
|                                                                                         |                     | 250 ksps, 10-bit conversions or<br>62.5 ksps 12-bit conversions<br>Low power bias settings<br>V <sub>DD</sub> = 3.0 V | —   | 425 | 580  | μA   |
| ADC0 Burst Mode, 10-bit single conversions, external reference                          | I <sub>ADC</sub>    | 200 ksps, V <sub>DD</sub> = 3.0 V                                                                                     | —   | 370 | —    | μA   |
|                                                                                         |                     | 100 ksps, V <sub>DD</sub> = 3.0 V                                                                                     | —   | 185 | —    | μA   |
|                                                                                         |                     | 10 ksps, V <sub>DD</sub> = 3.0 V                                                                                      | —   | 19  | —    | μA   |
| ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings | I <sub>ADC</sub>    | 200 ksps, V <sub>DD</sub> = 3.0 V                                                                                     | —   | 490 | —    | μA   |
|                                                                                         |                     | 100 ksps, V <sub>DD</sub> = 3.0 V                                                                                     | —   | 245 | —    | μA   |
|                                                                                         |                     | 10 ksps, V <sub>DD</sub> = 3.0 V                                                                                      | —   | 23  | —    | μA   |
| ADC0 Burst Mode, 12-bit single conversions, external reference                          | I <sub>ADC</sub>    | 100 ksps, V <sub>DD</sub> = 3.0 V                                                                                     | —   | 530 | —    | μA   |
|                                                                                         |                     | 50 ksps, V <sub>DD</sub> = 3.0 V                                                                                      | —   | 265 | —    | μA   |
|                                                                                         |                     | 10 ksps, V <sub>DD</sub> = 3.0 V                                                                                      | —   | 53  | —    | μA   |
| ADC0 Burst Mode, 12-bit single conversions, internal reference                          | I <sub>ADC</sub>    | 100 ksps, V <sub>DD</sub> = 3.0 V,<br>Normal bias                                                                     | —   | 950 | —    | μA   |
|                                                                                         |                     | 50 ksps, V <sub>DD</sub> = 3.0 V,<br>Low power bias                                                                   | —   | 420 | —    | μA   |
|                                                                                         |                     | 10 ksps, V <sub>DD</sub> = 3.0 V,<br>Low power bias                                                                   | —   | 85  | —    | μA   |
| Internal ADC0 Reference, Always-on <sup>5</sup>                                         | I <sub>VREFFS</sub> | Normal Power Mode                                                                                                     | —   | 680 | 790  | μA   |
|                                                                                         |                     | Low Power Mode                                                                                                        | —   | 160 | 210  | μA   |
| Temperature Sensor                                                                      | I <sub>TSENSE</sub> |                                                                                                                       | —   | 75  | 120  | μA   |
| Comparator 0 (CMP0),<br>Comparator 1 (CMP1)                                             | I <sub>CMP</sub>    | CPMD = 11                                                                                                             | —   | 0.5 | —    | μA   |
|                                                                                         |                     | CPMD = 10                                                                                                             | —   | 3   | —    | μA   |
|                                                                                         |                     | CPMD = 01                                                                                                             | —   | 10  | —    | μA   |
|                                                                                         |                     | CPMD = 00                                                                                                             | —   | 25  | —    | μA   |
| Voltage Supply Monitor (VMON0)                                                          | I <sub>VMON</sub>   |                                                                                                                       | —   | 15  | 20   | μA   |

| Parameter                                                                                                                                                                           | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|----------------|-----|-----|-----|------|
| <b>Note:</b>                                                                                                                                                                        |        |                |     |     |     |      |
| 1. Currents are additive. For example, where $I_{DD}$ is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount. |        |                |     |     |     |      |
| 2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.                                                                                  |        |                |     |     |     |      |
| 3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.                                                                                   |        |                |     |     |     |      |
| 4. ADC0 always-on power excludes internal reference supply current.                                                                                                                 |        |                |     |     |     |      |
| 5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.                                                                                  |        |                |     |     |     |      |

**Table 4.3. Reset and Supply Monitor**

| Parameter                                                         | Symbol     | Test Condition                                          | Min  | Typ   | Max  | Unit    |
|-------------------------------------------------------------------|------------|---------------------------------------------------------|------|-------|------|---------|
| $V_{DD}$ Supply Monitor Threshold                                 | $V_{VDDM}$ |                                                         | 1.85 | 1.95  | 2.1  | V       |
| Power-On Reset (POR) Threshold                                    | $V_{POR}$  | Rising Voltage on $V_{DD}$                              | —    | 1.4   | —    | V       |
|                                                                   |            | Falling Voltage on $V_{DD}$                             | 0.75 | —     | 1.36 | V       |
| $V_{DD}$ Ramp Time                                                | $t_{RMP}$  | Time to $V_{DD} \geq 2.2$ V                             | 10   | —     | —    | $\mu$ s |
| Reset Delay from POR                                              | $t_{POR}$  | Relative to $V_{DD} \geq V_{POR}$                       | 3    | 10    | 31   | ms      |
| Reset Delay from non-POR source                                   | $t_{RST}$  | Time between release of reset source and code execution | —    | 39    | —    | $\mu$ s |
| RST Low Time to Generate Reset                                    | $t_{RSTL}$ |                                                         | 15   | —     | —    | $\mu$ s |
| Missing Clock Detector Response Time (final rising edge to reset) | $t_{MCD}$  | $F_{SYSCLK} > 1$ MHz                                    | —    | 0.625 | 1.2  | ms      |
| Missing Clock Detector Trigger Frequency                          | $F_{MCD}$  |                                                         | —    | 7.5   | 13.5 | kHz     |
| $V_{DD}$ Supply Monitor Turn-On Time                              | $t_{MON}$  |                                                         | —    | 2     | —    | $\mu$ s |

**Table 4.4. Flash Memory**

| Parameter                                        | Symbol      | Test Condition                       | Min | Typ  | Max | Units   |
|--------------------------------------------------|-------------|--------------------------------------|-----|------|-----|---------|
| Write Time <sup>1,2</sup>                        | $t_{WRITE}$ | One Byte,<br>$F_{SYSCLK} = 24.5$ MHz | 19  | 20   | 21  | $\mu$ s |
| Erase Time <sup>1,2</sup>                        | $t_{ERASE}$ | One Page,<br>$F_{SYSCLK} = 24.5$ MHz | 5.2 | 5.35 | 5.5 | ms      |
| $V_{DD}$ Voltage During Programming <sup>3</sup> | $V_{PROG}$  |                                      | 2.2 | —    | 3.6 | V       |
| Endurance (Write/Erase Cycles)                   | $N_{WE}$    |                                      | 20k | 100k | —   | Cycles  |

**Note:**

- Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
- The internal High-Frequency Oscillator has a programmable output frequency using the HFO0CAL register, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.
- Flash can be safely programmed at any voltage above the supply monitor threshold ( $V_{VDDM}$ ).
- Data Retention Information is published in the Quarterly Quality and Reliability Report.

**Table 4.5. Internal Oscillators**

| Parameter                              | Symbol         | Test Condition                    | Min | Typ  | Max | Unit   |
|----------------------------------------|----------------|-----------------------------------|-----|------|-----|--------|
| High Frequency Oscillator 0 (24.5 MHz) |                |                                   |     |      |     |        |
| Oscillator Frequency                   | $f_{HFOSC0}$   | Full Temperature and Supply Range | 24  | 24.5 | 25  | MHz    |
| Power Supply Sensitivity               | $PSS_{HFOSC0}$ | $T_A = 25\text{ }^\circ\text{C}$  | —   | 0.5  | —   | %/V    |
| Temperature Sensitivity                | $TS_{HFOSC0}$  | $V_{DD} = 3.0\text{ V}$           | —   | 40   | —   | ppm/°C |
| Low Frequency Oscillator (80 kHz)      |                |                                   |     |      |     |        |
| Oscillator Frequency                   | $f_{LFOSC}$    | Full Temperature and Supply Range | 75  | 80   | 85  | kHz    |
| Power Supply Sensitivity               | $PSS_{LFOSC}$  | $T_A = 25\text{ }^\circ\text{C}$  | —   | 0.05 | —   | %/V    |
| Temperature Sensitivity                | $TS_{LFOSC}$   | $V_{DD} = 3.0\text{ V}$           | —   | 65   | —   | ppm/°C |

**Table 4.6. External Clock Input**

| Parameter                                           | Symbol      | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------------------------|-------------|----------------|-----|-----|-----|------|
| External Input CMOS Clock Frequency (at EXTCLK pin) | $f_{CMOS}$  |                | 0   | —   | 25  | MHz  |
| External Input CMOS Clock High Time                 | $t_{CMOSH}$ |                | 18  | —   | —   | ns   |
| External Input CMOS Clock Low Time                  | $t_{CMOSL}$ |                | 18  | —   | —   | ns   |

**Table 4.7. ADC**

| Parameter                         | Symbol     | Test Condition                                   | Min | Typ | Max  | Unit |
|-----------------------------------|------------|--------------------------------------------------|-----|-----|------|------|
| Resolution                        | $N_{bits}$ | 12 Bit Mode                                      |     | 12  |      | Bits |
|                                   |            | 10 Bit Mode                                      |     | 10  |      | Bits |
| Throughput Rate (High Speed Mode) | $f_S$      | 12 Bit Mode                                      | —   | —   | 200  | ksps |
|                                   |            | 10 Bit Mode                                      | —   | —   | 800  | ksps |
| Throughput Rate (Low Power Mode)  | $f_S$      | 12 Bit Mode                                      | —   | —   | 62.5 | ksps |
|                                   |            | 10 Bit Mode                                      | —   | —   | 250  | ksps |
| Tracking Time                     | $t_{TRK}$  | High Speed Mode                                  | 230 | —   | —    | ns   |
|                                   |            | Low Power Mode                                   | 450 | —   | —    | ns   |
| Power-On Time                     | $t_{PWR}$  |                                                  | 1.2 | —   | —    | μs   |
| SAR Clock Frequency               | $f_{SAR}$  | High Speed Mode, Reference is 2.4 V internal     | —   | —   | 6.25 | MHz  |
|                                   |            | High Speed Mode, Reference is not 2.4 V internal | —   | —   | 12.5 | MHz  |
|                                   |            | Low Power Mode                                   | —   | —   | 4    | MHz  |

| Parameter                                                                                       | Symbol       | Test Condition                                                           | Min | Typ        | Max         | Unit             |
|-------------------------------------------------------------------------------------------------|--------------|--------------------------------------------------------------------------|-----|------------|-------------|------------------|
| Conversion Time                                                                                 | $t_{CNV}$    | 10-Bit Conversion,<br>SAR Clock = 12.25 MHz,<br>System Clock = 24.5 MHz. |     | 1.1        |             | $\mu s$          |
| Sample/Hold Capacitor                                                                           | $C_{SAR}$    | Gain = 1                                                                 | —   | 5          | —           | pF               |
|                                                                                                 |              | Gain = 0.5                                                               | —   | 2.5        | —           | pF               |
| Input Pin Capacitance                                                                           | $C_{IN}$     |                                                                          | —   | 20         | —           | pF               |
| Input Mux Impedance                                                                             | $R_{MUX}$    |                                                                          | —   | 550        | —           | $\Omega$         |
| Voltage Reference Range                                                                         | $V_{REF}$    |                                                                          | 1   | —          | $V_{DD}$    | V                |
| Input Voltage Range*                                                                            | $V_{IN}$     | Gain = 1                                                                 | 0   | —          | $V_{REF}$   | V                |
|                                                                                                 |              | Gain = 0.5                                                               | 0   | —          | $2xV_{REF}$ | V                |
| Power Supply Rejection Ratio                                                                    | $PSRR_{ADC}$ |                                                                          | —   | 70         | —           | dB               |
| DC Performance                                                                                  |              |                                                                          |     |            |             |                  |
| Integral Nonlinearity                                                                           | INL          | 12 Bit Mode                                                              | —   | $\pm 1$    | $\pm 2.3$   | LSB              |
|                                                                                                 |              | 10 Bit Mode                                                              | —   | $\pm 0.2$  | $\pm 0.6$   | LSB              |
| Differential Nonlinearity (Guaranteed Monotonic)                                                | DNL          | 12 Bit Mode                                                              | -1  | $\pm 0.7$  | 1.9         | LSB              |
|                                                                                                 |              | 10 Bit Mode                                                              | —   | $\pm 0.2$  | $\pm 0.6$   | LSB              |
| Offset Error                                                                                    | $E_{OFF}$    | 12 Bit Mode, $V_{REF} = 1.65 V$                                          | -3  | 0          | 3           | LSB              |
|                                                                                                 |              | 10 Bit Mode, $V_{REF} = 1.65 V$                                          | -2  | 0          | 2           | LSB              |
| Offset Temperature Coefficient                                                                  | $TC_{OFF}$   |                                                                          | —   | 0.004      | —           | LSB/ $^{\circ}C$ |
| Slope Error                                                                                     | $E_M$        | 12 Bit Mode                                                              | —   | $\pm 0.02$ | $\pm 0.1$   | %                |
|                                                                                                 |              | 10 Bit Mode                                                              | —   | $\pm 0.06$ | $\pm 0.24$  | %                |
| Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, Max throughput, using AGND pin |              |                                                                          |     |            |             |                  |
| Signal-to-Noise                                                                                 | SNR          | 12 Bit Mode                                                              | 61  | 66         | —           | dB               |
|                                                                                                 |              | 10 Bit Mode                                                              | 53  | 60         | —           | dB               |
| Signal-to-Noise Plus Distortion                                                                 | SNDR         | 12 Bit Mode                                                              | 61  | 66         | —           | dB               |
|                                                                                                 |              | 10 Bit Mode                                                              | 53  | 60         | —           | dB               |
| Total Harmonic Distortion (Up to 5th Harmonic)                                                  | THD          | 12 Bit Mode                                                              | —   | 71         | —           | dB               |
|                                                                                                 |              | 10 Bit Mode                                                              | —   | 70         | —           | dB               |
| Spurious-Free Dynamic Range                                                                     | SFDR         | 12 Bit Mode                                                              | —   | -79        | —           | dB               |
|                                                                                                 |              | 10 Bit Mode                                                              | —   | -74        | —           | dB               |
| <b>Note:</b>                                                                                    |              |                                                                          |     |            |             |                  |
| 1. Absolute input pin voltage is limited by the $V_{DD}$ supply.                                |              |                                                                          |     |            |             |                  |

**Table 4.8. Voltage Reference**

| Parameter                        | Symbol | Test Condition | Min | Typ | Max | Unit |
|----------------------------------|--------|----------------|-----|-----|-----|------|
| Internal Fast Settling Reference |        |                |     |     |     |      |

| Parameter                                             | Symbol                 | Test Condition                         | Min  | Typ  | Max  | Unit   |
|-------------------------------------------------------|------------------------|----------------------------------------|------|------|------|--------|
| Output Voltage<br>(Full Temperature and Supply Range) | V <sub>REFFS</sub>     | 1.65 V Setting                         | 1.62 | 1.65 | 1.68 | V      |
|                                                       |                        | 2.4 V Setting, V <sub>DD</sub> ≥ 2.6 V | 2.35 | 2.4  | 2.45 | V      |
| Temperature Coefficient                               | TC <sub>REFFS</sub>    |                                        | —    | 50   | —    | ppm/°C |
| Turn-on Time                                          | t <sub>REFFS</sub>     |                                        | —    | —    | 1.5  | μs     |
| Power Supply Rejection                                | PSRR <sub>REF FS</sub> |                                        | —    | 400  | —    | ppm/V  |
| External Reference                                    |                        |                                        |      |      |      |        |
| Input Current                                         | I <sub>EXTREF</sub>    | Sample Rate = 800 ksps; VREF = 3.0 V   | —    | 5    | —    | μA     |

**Table 4.9. Temperature Sensor**

| Parameter                                                           | Symbol           | Test Condition        | Min | Typ  | Max | Unit  |
|---------------------------------------------------------------------|------------------|-----------------------|-----|------|-----|-------|
| Offset                                                              | V <sub>OFF</sub> | T <sub>A</sub> = 0 °C | —   | 757  | —   | mV    |
| Offset Error <sup>1</sup>                                           | E <sub>OFF</sub> | T <sub>A</sub> = 0 °C | —   | 17   | —   | mV    |
| Slope                                                               | M                |                       | —   | 2.85 | —   | mV/°C |
| Slope Error <sup>1</sup>                                            | E <sub>M</sub>   |                       | —   | 70   | —   | μV/°C |
| Linearity                                                           |                  |                       | —   | 0.5  | —   | °C    |
| Turn-on Time                                                        |                  |                       | —   | 1.8  | —   | μs    |
| <b>Note:</b><br>1. Represents one standard deviation from the mean. |                  |                       |     |      |     |       |

**Table 4.10. Comparators**

| Parameter                                    | Symbol             | Test Condition       | Min | Typ  | Max | Unit |
|----------------------------------------------|--------------------|----------------------|-----|------|-----|------|
| Response Time, CPMD = 00<br>(Highest Speed)  | t <sub>RESP0</sub> | +100 mV Differential | —   | 100  | —   | ns   |
|                                              |                    | –100 mV Differential | —   | 150  | —   | ns   |
| Response Time, CPMD = 11 (Low-<br>est Power) | t <sub>RESP3</sub> | +100 mV Differential | —   | 1.5  | —   | μs   |
|                                              |                    | –100 mV Differential | —   | 3.5  | —   | μs   |
| Positive Hysteresis<br>Mode 0 (CPMD = 00)    | HYS <sub>CP+</sub> | CPHYP = 00           | —   | 0.4  | —   | mV   |
|                                              |                    | CPHYP = 01           | —   | 8    | —   | mV   |
|                                              |                    | CPHYP = 10           | —   | 16   | —   | mV   |
|                                              |                    | CPHYP = 11           | —   | 32   | —   | mV   |
| Negative Hysteresis<br>Mode 0 (CPMD = 00)    | HYS <sub>CP-</sub> | CPHYN = 00           | —   | -0.4 | —   | mV   |
|                                              |                    | CPHYN = 01           | —   | -8   | —   | mV   |
|                                              |                    | CPHYN = 10           | —   | -16  | —   | mV   |
|                                              |                    | CPHYN = 11           | —   | -32  | —   | mV   |

| Parameter                                 | Symbol             | Test Condition         | Min   | Typ  | Max                   | Unit  |
|-------------------------------------------|--------------------|------------------------|-------|------|-----------------------|-------|
| Positive Hysterisis<br>Mode 1 (CPMD = 01) | HYS <sub>CP+</sub> | CPHYP = 00             | —     | 0.5  | —                     | mV    |
|                                           |                    | CPHYP = 01             | —     | 6    | —                     | mV    |
|                                           |                    | CPHYP = 10             | —     | 12   | —                     | mV    |
|                                           |                    | CPHYP = 11             | —     | 24   | —                     | mV    |
| Negative Hysterisis<br>Mode 1 (CPMD = 01) | HYS <sub>CP-</sub> | CPHYN = 00             | —     | -0.5 | —                     | mV    |
|                                           |                    | CPHYN = 01             | —     | -6   | —                     | mV    |
|                                           |                    | CPHYN = 10             | —     | -12  | —                     | mV    |
|                                           |                    | CPHYN = 11             | —     | -24  | —                     | mV    |
| Positive Hysterisis<br>Mode 2 (CPMD = 10) | HYS <sub>CP+</sub> | CPHYP = 00             | —     | 0.7  | —                     | mV    |
|                                           |                    | CPHYP = 01             | —     | 4.5  | —                     | mV    |
|                                           |                    | CPHYP = 10             | —     | 9    | —                     | mV    |
|                                           |                    | CPHYP = 11             | —     | 18   | —                     | mV    |
| Negative Hysterisis<br>Mode 2 (CPMD = 10) | HYS <sub>CP-</sub> | CPHYN = 00             | —     | -0.6 | —                     | mV    |
|                                           |                    | CPHYN = 01             | —     | -4.5 | —                     | mV    |
|                                           |                    | CPHYN = 10             | —     | -9   | —                     | mV    |
|                                           |                    | CPHYN = 11             | —     | -18  | —                     | mV    |
| Positive Hysterisis<br>Mode 3 (CPMD = 11) | HYS <sub>CP+</sub> | CPHYP = 00             | —     | 1.5  | —                     | mV    |
|                                           |                    | CPHYP = 01             | —     | 4    | —                     | mV    |
|                                           |                    | CPHYP = 10             | —     | 8    | —                     | mV    |
|                                           |                    | CPHYP = 11             | —     | 16   | —                     | mV    |
| Negative Hysterisis<br>Mode 3 (CPMD = 11) | HYS <sub>CP-</sub> | CPHYN = 00             | —     | -1.5 | —                     | mV    |
|                                           |                    | CPHYN = 01             | —     | -4   | —                     | mV    |
|                                           |                    | CPHYN = 10             | —     | -8   | —                     | mV    |
|                                           |                    | CPHYN = 11             | —     | -16  | —                     | mV    |
| Input Range (CP+ or CP-)                  | V <sub>IN</sub>    |                        | -0.25 | —    | V <sub>DD</sub> +0.25 | V     |
| Input Pin Capacitance                     | C <sub>CP</sub>    |                        | —     | 7.5  | —                     | pF    |
| Common-Mode Rejection Ratio               | CMRR <sub>CP</sub> |                        | —     | 70   | —                     | dB    |
| Power Supply Rejection Ratio              | PSRR <sub>CP</sub> |                        | —     | 72   | —                     | dB    |
| Input Offset Voltage                      | V <sub>OFF</sub>   | T <sub>A</sub> = 25 °C | -10   | 0    | 10                    | mV    |
| Input Offset Tempco                       | TC <sub>OFF</sub>  |                        | —     | 3.5  | —                     | µV/°C |

Table 4.11. Port I/O

| Parameter                        | Symbol          | Test Condition           | Min                   | Typ | Max | Unit |
|----------------------------------|-----------------|--------------------------|-----------------------|-----|-----|------|
| Output High Voltage (High Drive) | V <sub>OH</sub> | I <sub>OH</sub> = -3 mA  | V <sub>DD</sub> - 0.7 | —   | —   | V    |
| Output Low Voltage (High Drive)  | V <sub>OL</sub> | I <sub>OL</sub> = 8.5 mA | —                     | —   | 0.6 | V    |
| Output High Voltage (Low Drive)  | V <sub>OH</sub> | I <sub>OH</sub> = -1 mA  | V <sub>DD</sub> - 0.7 | —   | —   | V    |
| Output Low Voltage (Low Drive)   | V <sub>OL</sub> | I <sub>OL</sub> = 1.4 mA | —                     | —   | 0.6 | V    |



| Parameter                                          | Symbol   | Test Condition                     | Min            | Typ | Max | Unit    |
|----------------------------------------------------|----------|------------------------------------|----------------|-----|-----|---------|
| Input High Voltage                                 | $V_{IH}$ |                                    | $V_{DD} - 0.6$ | —   | —   | V       |
| Input Low Voltage                                  | $V_{IL}$ |                                    | —              | —   | 0.6 | V       |
| Pin Capacitance                                    | $C_{IO}$ |                                    | —              | 7   | —   | pF      |
| Weak Pull-Up Current<br>( $V_{IN} = 0$ V)          | $I_{PU}$ | $V_{DD} = 3.6$                     | -30            | -20 | -10 | $\mu$ A |
| Input Leakage (Pullups off or Analog)              | $I_{LK}$ | $GND < V_{IN} < V_{DD}$            | -1.1           | —   | 1.1 | $\mu$ A |
| Input Leakage Current with $V_{IN}$ above $V_{DD}$ | $I_{LK}$ | $V_{DD} < V_{IN} < V_{DD} + 2.0$ V | 0              | 5   | 150 | $\mu$ A |

## 4.2 Thermal Conditions

**Table 4.12. Thermal Conditions**

| Parameter           | Symbol        | Test Condition   | Min | Typ | Max | Unit           |
|---------------------|---------------|------------------|-----|-----|-----|----------------|
| Thermal Resistance* | $\theta_{JA}$ | SOIC-16 Packages | —   | 70  | —   | $^{\circ}$ C/W |
|                     |               | QFN-20 Packages  | —   | 60  | —   | $^{\circ}$ C/W |
|                     |               | QSOP-24 Packages | —   | 65  | —   | $^{\circ}$ C/W |

**Note:**

1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

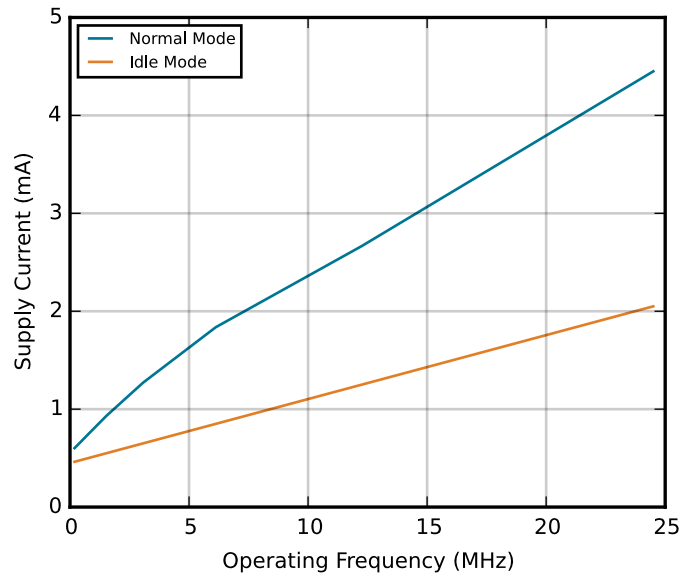
### 4.3 Absolute Maximum Ratings

Stresses above those listed in [Table 4.13 Absolute Maximum Ratings on page 17](#) may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

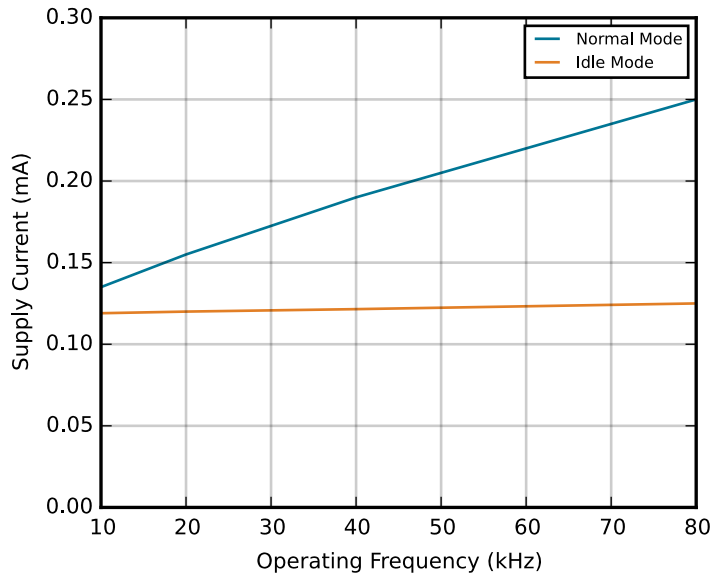
**Table 4.13. Absolute Maximum Ratings**

| Parameter                                                                                 | Symbol     | Test Condition      | Min     | Max          | Unit     |
|-------------------------------------------------------------------------------------------|------------|---------------------|---------|--------------|----------|
| Ambient Temperature Under Bias                                                            | $T_{BIAS}$ |                     | -55     | 125          | °C       |
| Storage Temperature                                                                       | $T_{STG}$  |                     | -65     | 150          | °C       |
| Voltage on VDD                                                                            | $V_{DD}$   |                     | GND-0.3 | 4.2          | V        |
| Voltage on I/O pins or RST                                                                | $V_{IN}$   | $V_{DD} \geq 3.3$ V | GND-0.3 | 5.8          | V        |
|                                                                                           |            | $V < 3.3$ V         | GND-0.3 | $V_{DD}+2.5$ | V        |
| Total Current Sunk into Supply Pin                                                        | $I_{VDD}$  |                     | —       | 400          | mA<br>DD |
| Total Current Sourced out of Ground Pin                                                   | $I_{GND}$  |                     | 400     | —            | mA       |
| Current Sourced or Sunk by Any I/O Pin or RSTb                                            | $I_{IO}$   |                     | -100    | 100          | mA       |
| Operating Junction Temperature                                                            | $T_J$      |                     | -40     | 105          | °C       |
| Exposure to maximum rating conditions for extended periods may affect device reliability. |            |                     |         |              |          |

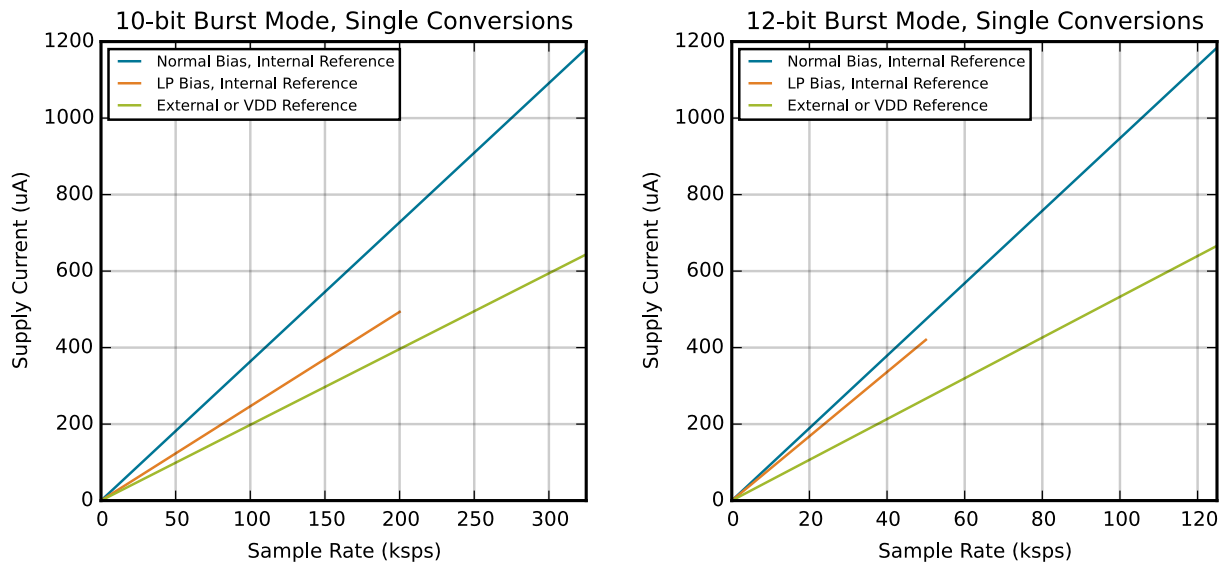
#### 4.4 Typical Performance Curves



**Figure 4.1. Typical Operating Supply Current using HFOSC0**



**Figure 4.2. Typical Operating Supply Current using LFOSC**



**Figure 4.3. Typical ADC0 and Internal Reference Supply Current in Burst Mode**

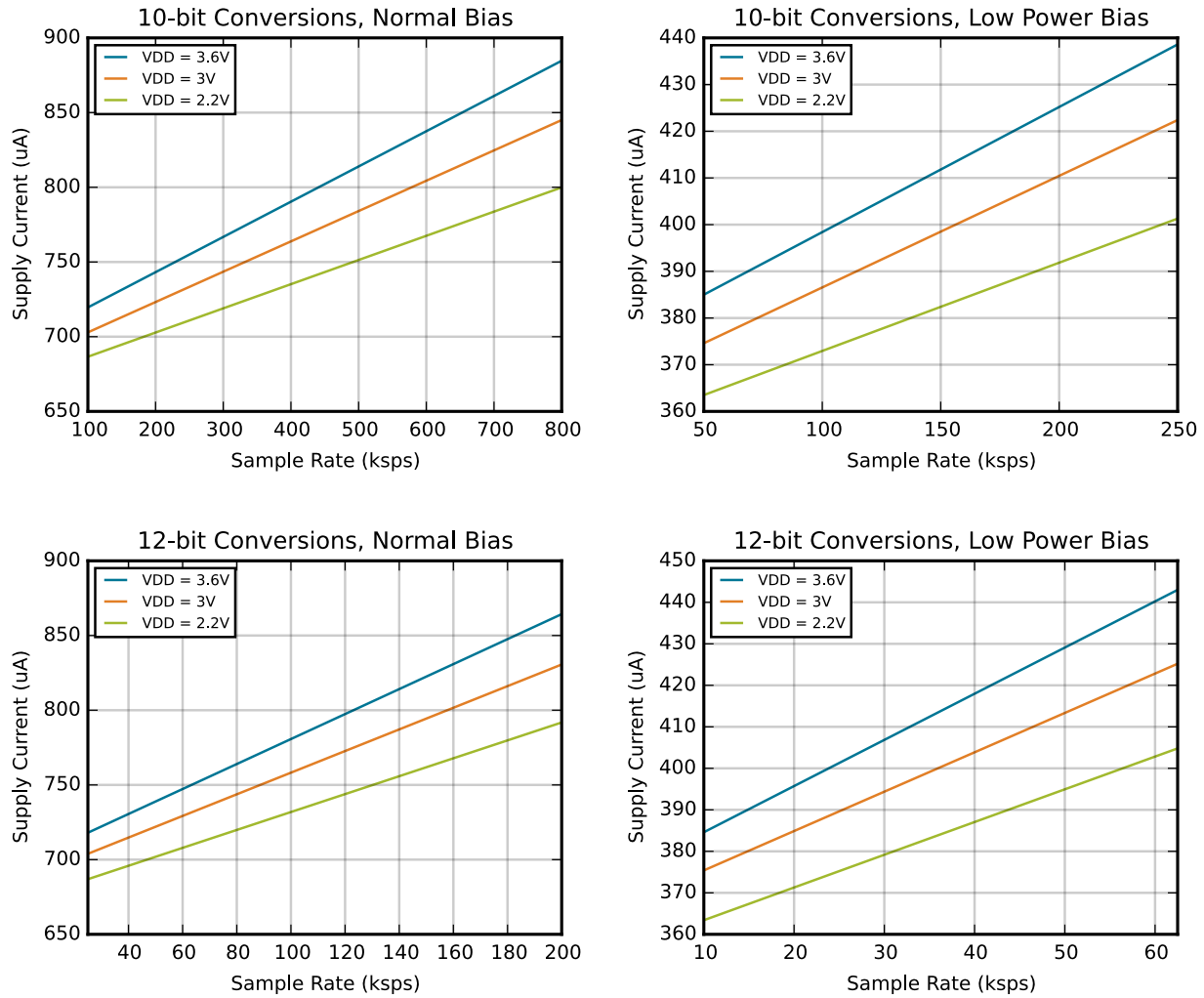


Figure 4.4. Typical ADC0 Supply Current in Normal (always-on) Mode

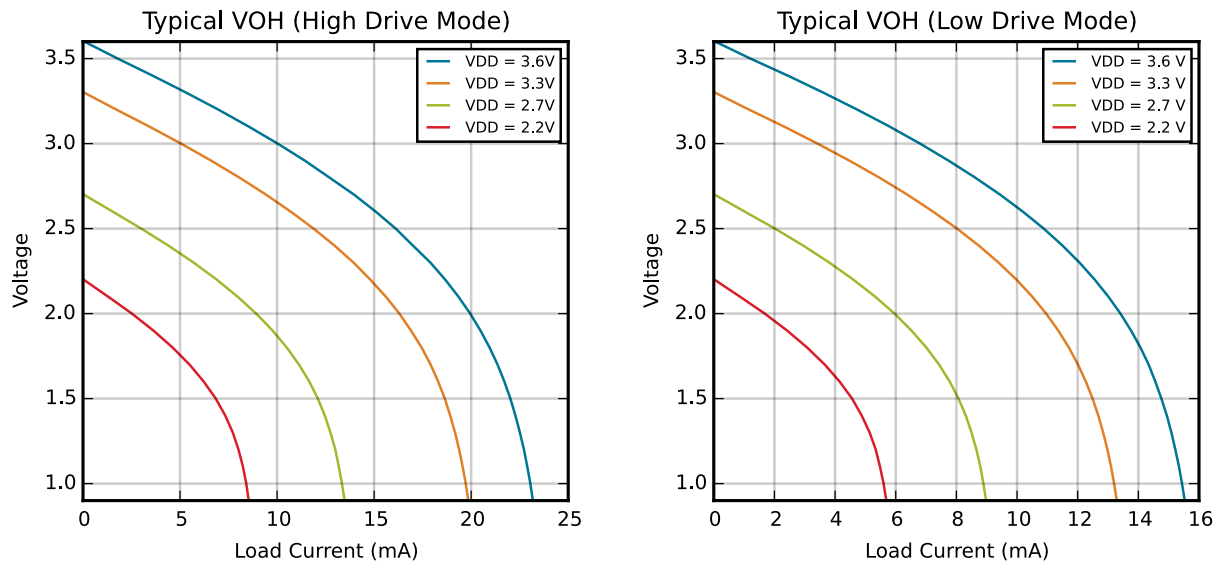


Figure 4.5. Typical  $V_{OH}$  Curves

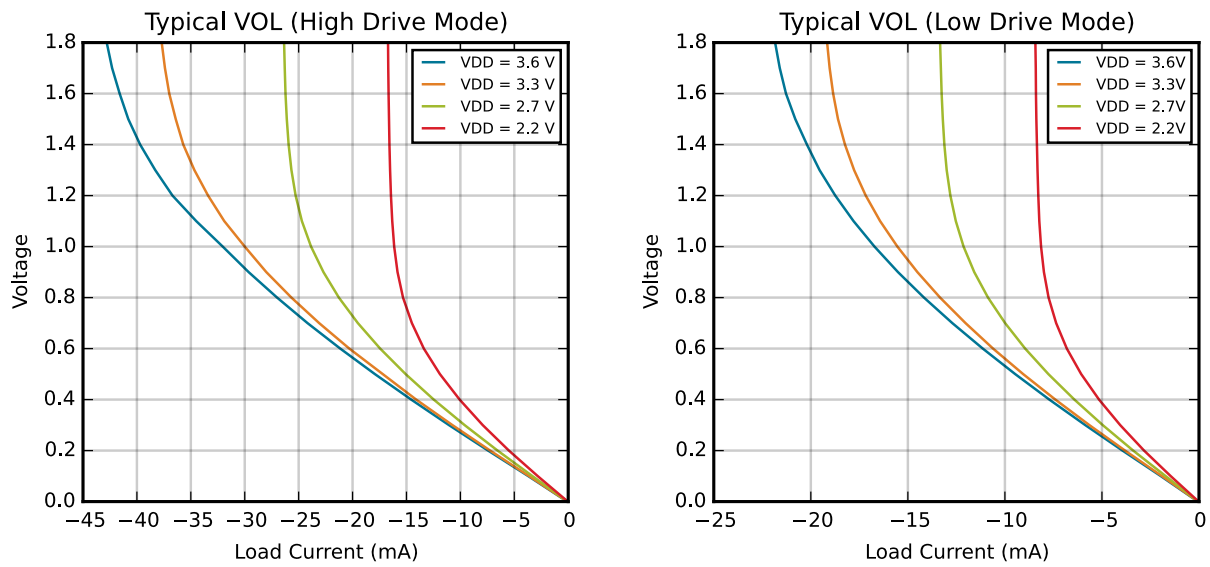


Figure 4.6. Typical  $V_{OL}$  Curves

## 5. Typical Connection Diagrams

### 5.1 Power

Figure 5.1 Power Connection Diagram on page 22 shows a typical connection diagram for the power pins of the EFM8BB1 devices.

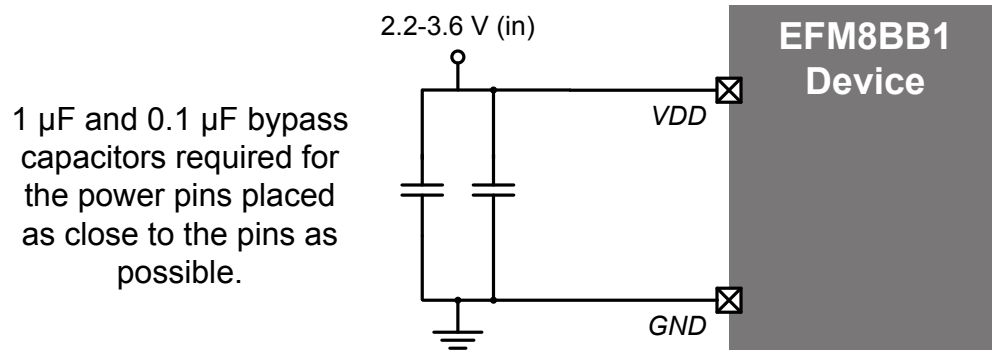


Figure 5.1. Power Connection Diagram

### 5.2 Other Connections

Other components or connections may be required to meet the system-level requirements. Application Note AN203: "8-bit MCU Printed Circuit Board Design Notes" contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website ([www.silabs.com/8bit-appnotes](http://www.silabs.com/8bit-appnotes)).

## 6. Pin Definitions

### 6.1 EFM8BB1x-QSOP24 Pin Definitions

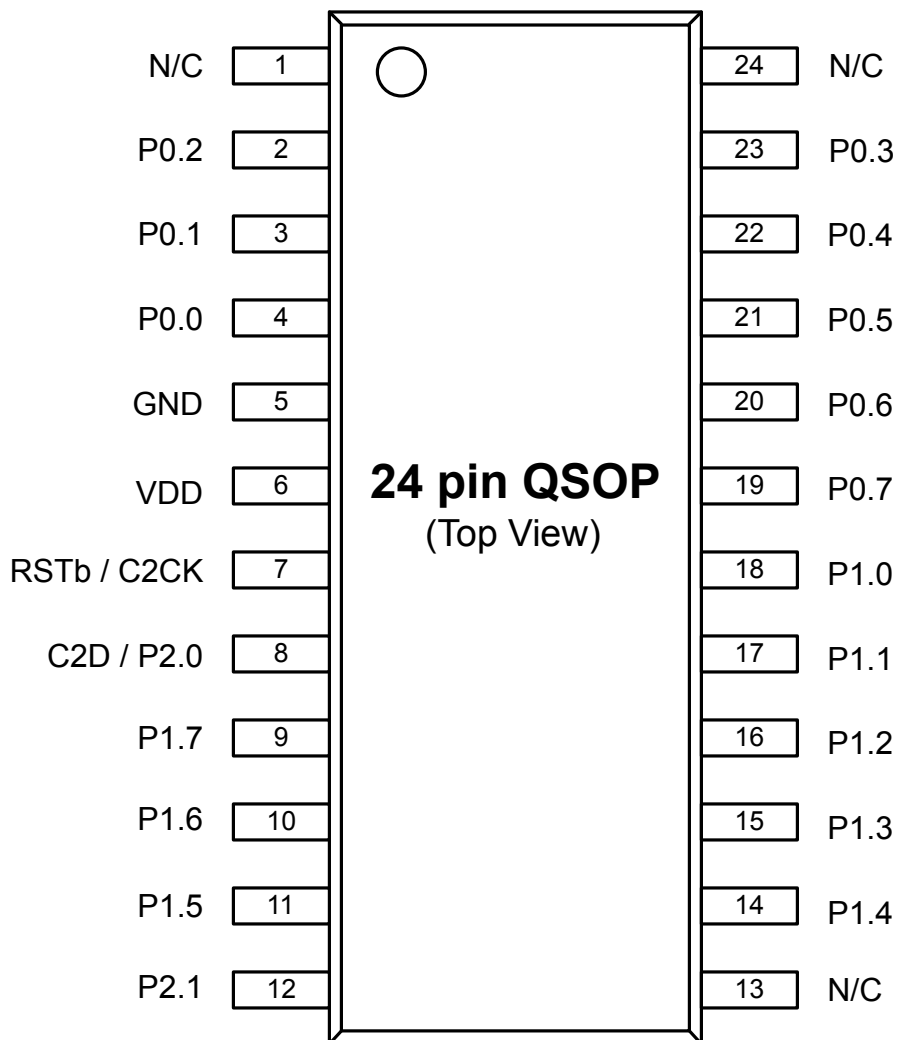


Figure 6.1. EFM8BB1x-QSOP24 Pinout

Table 6.1. Pin Definitions for EFM8BB1x-QSOP24

| Pin Number | Pin Name | Description       | Crossbar Capability | Additional Digital Functions | Analog Functions             |
|------------|----------|-------------------|---------------------|------------------------------|------------------------------|
| 1          | N/C      | No Connection     |                     |                              |                              |
| 2          | P0.2     | Multifunction I/O | Yes                 | P0MAT.2<br>INT0.2<br>INT1.2  | ADC0.2<br>CMP0P.2<br>CMP0N.2 |



| Pin Number | Pin Name       | Description                          | Crossbar Capability | Additional Digital Functions | Analog Functions                     |
|------------|----------------|--------------------------------------|---------------------|------------------------------|--------------------------------------|
| 3          | P0.1           | Multifunction I/O                    | Yes                 | P0MAT.1<br>INT0.1<br>INT1.1  | ADC0.1<br>CMP0P.1<br>CMP0N.1<br>AGND |
| 4          | P0.0           | Multifunction I/O                    | Yes                 | P0MAT.0<br>INT0.0<br>INT1.0  | ADC0.0<br>CMP0P.0<br>CMP0N.0<br>VREF |
| 5          | GND            | Ground                               |                     |                              |                                      |
| 6          | VDD            | Supply Power Input                   |                     |                              |                                      |
| 7          | RSTb /<br>C2CK | Active-low Reset /<br>C2 Debug Clock |                     |                              |                                      |
| 8          | P2.0 /<br>C2D  | Multifunction I/O /<br>C2 Debug Data |                     |                              |                                      |
| 9          | P1.7           | Multifunction I/O                    | Yes                 | P1MAT.7                      | ADC0.15<br>CMP1P.7<br>CMP1N.7        |
| 10         | P1.6           | Multifunction I/O                    | Yes                 | P1MAT.6                      | ADC0.14<br>CMP1P.6<br>CMP1N.6        |
| 11         | P1.5           | Multifunction I/O                    | Yes                 | P1MAT.5                      | ADC0.13<br>CMP1P.5<br>CMP1N.5        |
| 12         | P2.1           | Multifunction I/O                    |                     |                              |                                      |
| 13         | N/C            | No Connection                        |                     |                              |                                      |
| 14         | P1.4           | Multifunction I/O                    | Yes                 | P1MAT.4                      | ADC0.12<br>CMP1P.4<br>CMP1N.4        |
| 15         | P1.3           | Multifunction I/O                    | Yes                 | P1MAT.3                      | ADC0.11<br>CMP1P.3<br>CMP1N.3        |
| 16         | P1.2           | Multifunction I/O                    | Yes                 | P1MAT.2                      | ADC0.10<br>CMP1P.2<br>CMP1N.2        |

| Pin Number | Pin Name | Description       | Crossbar Capability | Additional Digital Functions          | Analog Functions             |
|------------|----------|-------------------|---------------------|---------------------------------------|------------------------------|
| 17         | P1.1     | Multifunction I/O | Yes                 | P1MAT.1                               | ADC0.9<br>CMP1P.1<br>CMP1N.1 |
| 18         | P1.0     | Multifunction I/O | Yes                 | P1MAT.0                               | ADC0.8<br>CMP1P.0<br>CMP1N.0 |
| 19         | P0.7     | Multifunction I/O | Yes                 | P0MAT.7<br>INT0.7<br>INT1.7           | ADC0.7<br>CMP0P.7<br>CMP0N.7 |
| 20         | P0.6     | Multifunction I/O | Yes                 | P0MAT.6<br>CNVSTR<br>INT0.6<br>INT1.6 | ADC0.6<br>CMP0P.6<br>CMP0N.6 |
| 21         | P0.5     | Multifunction I/O | Yes                 | P0MAT.5<br>INT0.5<br>INT1.5           | ADC0.5<br>CMP0P.5<br>CMP0N.5 |
| 22         | P0.4     | Multifunction I/O | Yes                 | P0MAT.4<br>INT0.4<br>INT1.4           | ADC0.4<br>CMP0P.4<br>CMP0N.4 |
| 23         | P0.3     | Multifunction I/O | Yes                 | P0MAT.3<br>EXTCLK<br>INT0.3<br>INT1.3 | ADC0.3<br>CMP0P.3<br>CMP0N.3 |
| 24         | N/C      | No Connection     |                     |                                       |                              |

6.2 EFM8BB1x-QFN20 Pin Definitions

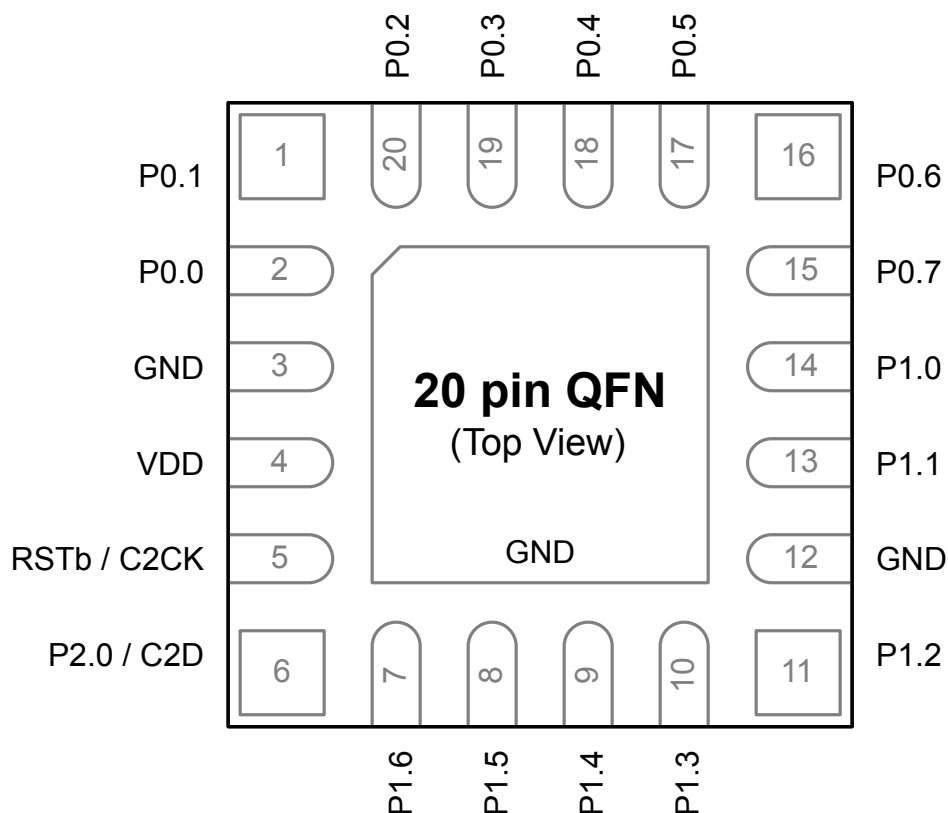


Figure 6.2. EFM8BB1x-QFN20 Pinout

Table 6.2. Pin Definitions for EFM8BB1x-QFN20

| Pin Number | Pin Name | Description       | Crossbar Capability | Additional Digital Functions | Analog Functions                     |
|------------|----------|-------------------|---------------------|------------------------------|--------------------------------------|
| 1          | P0.1     | Multifunction I/O | Yes                 | P0MAT.1<br>INT0.1<br>INT1.1  | ADC0.1<br>CMP0P.1<br>CMP0N.1<br>AGND |
| 2          | P0.0     | Multifunction I/O | Yes                 | P0MAT.0<br>INT0.0<br>INT1.0  | ADC0.0<br>CMP0P.0<br>CMP0N.0<br>VREF |

| Pin Number | Pin Name       | Description                          | Crossbar Capability | Additional Digital Functions          | Analog Functions              |
|------------|----------------|--------------------------------------|---------------------|---------------------------------------|-------------------------------|
| 3          | GND            | Ground                               |                     |                                       |                               |
| 4          | VDD            | Supply Power Input                   |                     |                                       |                               |
| 5          | RSTb /<br>C2CK | Active-low Reset /<br>C2 Debug Clock |                     |                                       |                               |
| 6          | P2.0 /<br>C2D  | Multifunction I/O /<br>C2 Debug Data |                     |                                       |                               |
| 7          | P1.6           | Multifunction I/O                    | Yes                 | P1MAT.6                               | ADC0.14<br>CMP1P.6<br>CMP1N.6 |
| 8          | P1.5           | Multifunction I/O                    | Yes                 | P1MAT.5                               | ADC0.13<br>CMP1P.5<br>CMP1N.5 |
| 9          | P1.4           | Multifunction I/O                    | Yes                 | P1MAT.4                               | ADC0.12<br>CMP1P.4<br>CMP1N.4 |
| 10         | P1.3           | Multifunction I/O                    | Yes                 | P1MAT.3                               | ADC0.11<br>CMP1P.3<br>CMP1N.3 |
| 11         | P1.2           | Multifunction I/O                    | Yes                 | P1MAT.2                               | ADC0.10<br>CMP1P.2<br>CMP1N.2 |
| 12         | GND            | Ground                               |                     |                                       |                               |
| 13         | P1.1           | Multifunction I/O                    | Yes                 | P1MAT.1                               | ADC0.9<br>CMP1P.1<br>CMP1N.1  |
| 14         | P1.0           | Multifunction I/O                    | Yes                 | P1MAT.0                               | ADC0.8<br>CMP1P.0<br>CMP1N.0  |
| 15         | P0.7           | Multifunction I/O                    | Yes                 | P0MAT.7<br>INT0.7<br>INT1.7           | ADC0.7<br>CMP0P.7<br>CMP0N.7  |
| 16         | P0.6           | Multifunction I/O                    | Yes                 | P0MAT.6<br>CNVSTR<br>INT0.6<br>INT1.6 | ADC0.6<br>CMP0P.6<br>CMP0N.6  |

| Pin Number | Pin Name | Description       | Crossbar Capability | Additional Digital Functions          | Analog Functions             |
|------------|----------|-------------------|---------------------|---------------------------------------|------------------------------|
| 17         | P0.5     | Multifunction I/O | Yes                 | P0MAT.5<br>INT0.5<br>INT1.5           | ADC0.5<br>CMP0P.5<br>CMP0N.5 |
| 18         | P0.4     | Multifunction I/O | Yes                 | P0MAT.4<br>INT0.4<br>INT1.4           | ADC0.4<br>CMP0P.4<br>CMP0N.4 |
| 19         | P0.3     | Multifunction I/O | Yes                 | P0MAT.3<br>EXTCLK<br>INT0.3<br>INT1.3 | ADC0.3<br>CMP0P.3<br>CMP0N.3 |
| 20         | P0.2     | Multifunction I/O | Yes                 | P0MAT.2<br>INT0.2<br>INT1.2           | ADC0.2<br>CMP0P.2<br>CMP0N.2 |
| Center     | GND      | Ground            |                     |                                       |                              |

6.3 EFM8BB1x-SOIC16 Pin Definitions

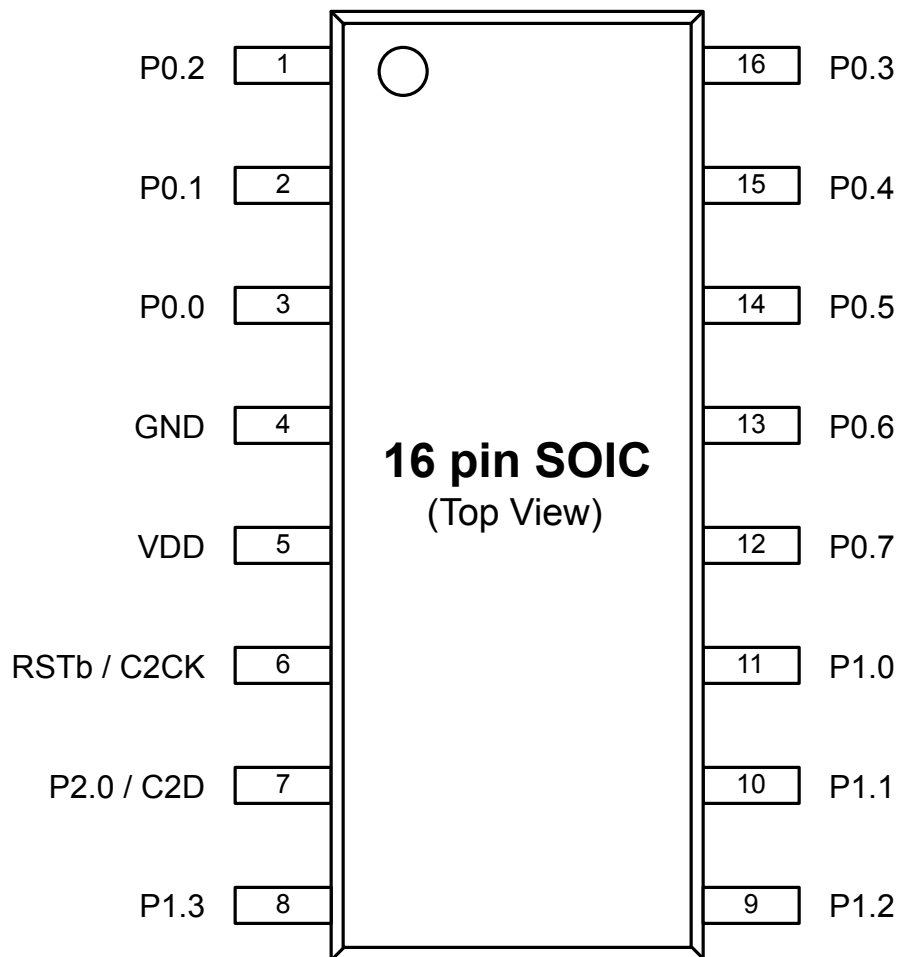


Figure 6.3. EFM8BB1x-SOIC16 Pinout

Table 6.3. Pin Definitions for EFM8BB1x-SOIC16

| Pin Number | Pin Name | Description       | Crossbar Capability | Additional Digital Functions | Analog Functions             |
|------------|----------|-------------------|---------------------|------------------------------|------------------------------|
| 1          | P0.2     | Multifunction I/O | Yes                 | P0MAT.2<br>INT0.2<br>INT1.2  | ADC0.2<br>CMP0P.2<br>CMP0N.2 |
| 2          | P0.1     | Multifunction I/O | Yes                 | P0MAT.1<br>INT0.1<br>INT1.1  | ADC0.1<br>CMP0P.1<br>CMP0N.1 |
| 3          | P0.0     | Multifunction I/O | Yes                 | P0MAT.0<br>INT0.0<br>INT1.0  | ADC0.0<br>CMP0P.0<br>CMP0N.0 |

| Pin Number | Pin Name       | Description                          | Crossbar Capability | Additional Digital Functions          | Analog Functions              |
|------------|----------------|--------------------------------------|---------------------|---------------------------------------|-------------------------------|
| 4          | GND            | Ground                               |                     |                                       |                               |
| 5          | VDD            | Supply Power Input                   |                     |                                       |                               |
| 6          | RSTb /<br>C2CK | Active-low Reset /<br>C2 Debug Clock |                     |                                       |                               |
| 7          | P2.0 /<br>C2D  | Multifunction I/O /<br>C2 Debug Data |                     |                                       |                               |
| 8          | P1.3           | Multifunction I/O                    | Yes                 | P1MAT.3                               | ADC0.11<br>CMP1P.5<br>CMP1N.5 |
| 9          | P1.2           | Multifunction I/O                    | Yes                 | P1MAT.2                               | ADC0.10<br>CMP1P.4<br>CMP1N.4 |
| 10         | P1.1           | Multifunction I/O                    | Yes                 | P1MAT.1                               | ADC0.9<br>CMP1P.3<br>CMP1N.3  |
| 11         | P1.0           | Multifunction I/O                    | Yes                 | P1MAT.0                               | ADC0.8<br>CMP1P.2<br>CMP1N.2  |
| 12         | P0.7           | Multifunction I/O                    | Yes                 | P0MAT.7<br>INT0.7<br>INT1.7           | ADC0.7<br>CMP1P.1<br>CMP1N.1  |
| 13         | P0.6           | Multifunction I/O                    | Yes                 | P0MAT.6<br>CNVSTR<br>INT0.6<br>INT1.6 | ADC0.6<br>CMP1P.0<br>CMP1N.0  |
| 14         | P0.5           | Multifunction I/O                    | Yes                 | P0MAT.5<br>INT0.5<br>INT1.5           | ADC0.5<br>CMP0P.5<br>CMP0N.5  |
| 15         | P0.4           | Multifunction I/O                    | Yes                 | P0MAT.4<br>INT0.4<br>INT1.4           | ADC0.4<br>CMP0P.4<br>CMP0N.4  |
| 16         | P0.3           | Multifunction I/O                    | Yes                 | P0MAT.3<br>EXTCLK<br>INT0.3<br>INT1.3 | ADC0.3<br>CMP0P.3<br>CMP0N.3  |

## 7. QSOP24 Package Specifications

### 7.1 QSOP24 Package Dimensions

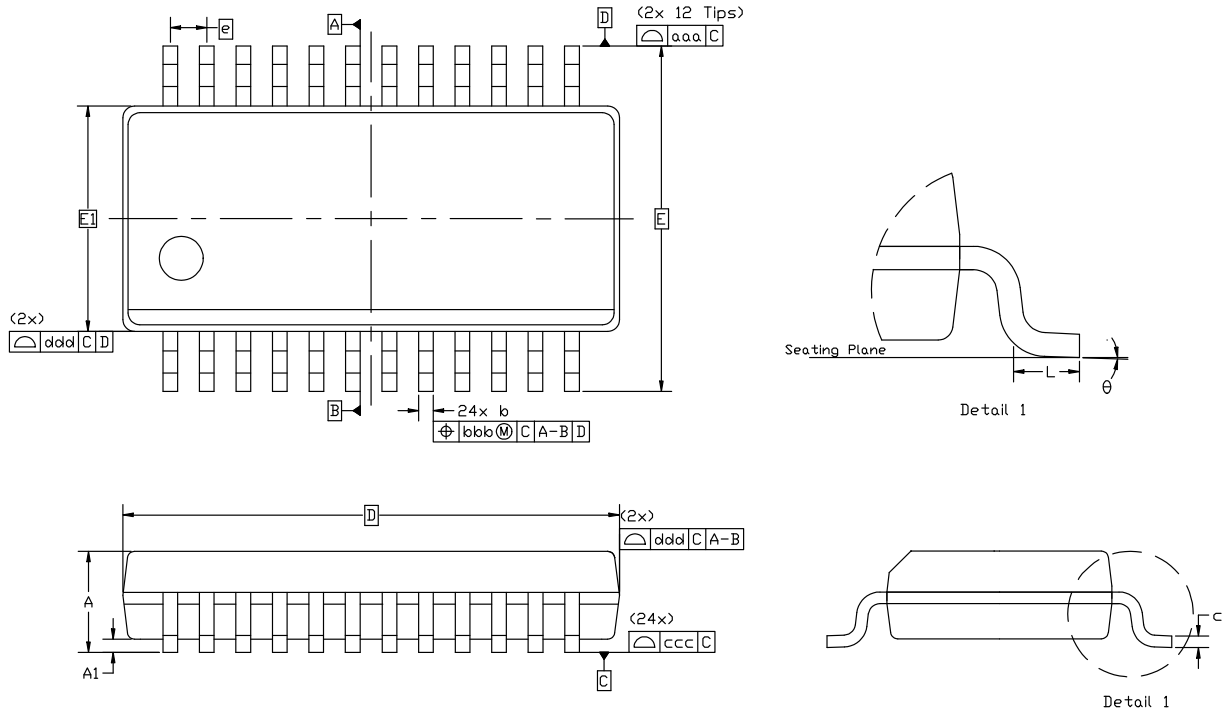


Figure 7.1. QSOP24 Package Drawing

Table 7.1. QSOP24 Package Dimensions

| Dimension | Min       | Typ | Max  |
|-----------|-----------|-----|------|
| A         | —         | —   | 1.75 |
| A1        | 0.10      | —   | 0.25 |
| b         | 0.20      | —   | 0.30 |
| c         | 0.10      | —   | 0.25 |
| D         | 8.65 BSC  |     |      |
| E         | 6.00 BSC  |     |      |
| E1        | 3.90 BSC  |     |      |
| e         | 0.635 BSC |     |      |
| L         | 0.40      | —   | 1.27 |
| theta     | 0°        | —   | 8°   |



| Dimension | Min | Typ  | Max |
|-----------|-----|------|-----|
| aaa       |     | 0.20 |     |
| bbb       |     | 0.18 |     |
| ccc       |     | 0.10 |     |
| ddd       |     | 0.10 |     |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-137, variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 7.2 QSOP24 PCB Land Pattern

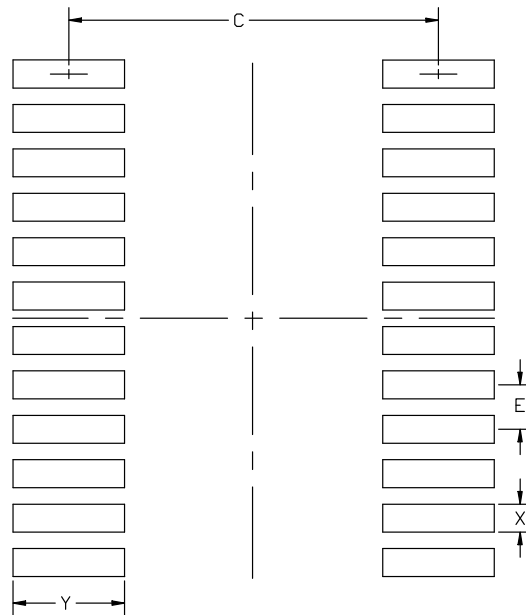


Figure 7.2. QSOP24 PCB Land Pattern Drawing

Table 7.2. QSOP24 PCB Land Pattern Dimensions

| Dimension | Min       | Max  |
|-----------|-----------|------|
| C         | 5.20      | 5.30 |
| E         | 0.635 BSC |      |
| X         | 0.30      | 0.40 |
| Y         | 1.50      | 1.60 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 7.3 QSOP24 Package Marking



Figure 7.3. QSOP24 Package Marking

The package marking consists of:

- P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 8. QFN20 Package Specifications

### 8.1 QFN20 Package Dimensions

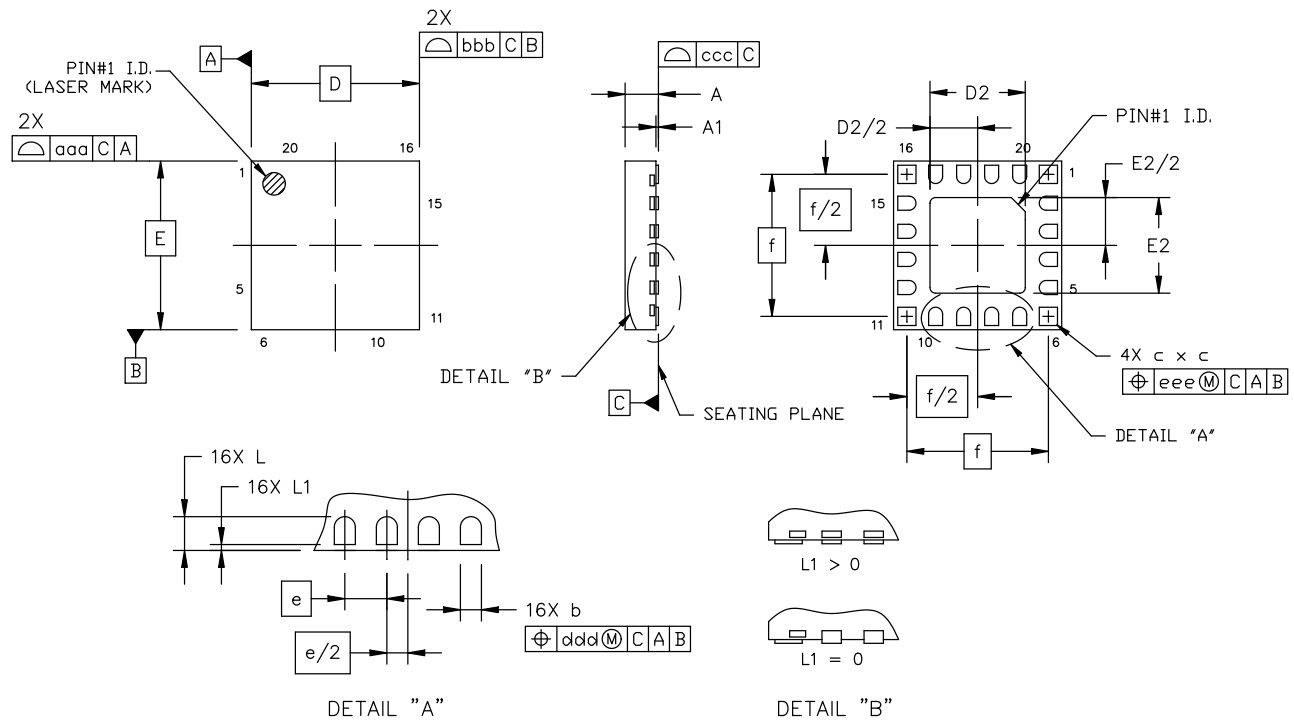


Figure 8.1. QFN20 Package Drawing

Table 8.1. QFN20 Package Dimensions

| Dimension | Min      | Typ  | Max  |
|-----------|----------|------|------|
| A         | 0.50     | 0.55 | 0.60 |
| A1        | 0.00     | 0.02 | 0.05 |
| b         | 0.20     | 0.25 | 0.30 |
| c         | 0.27     | 0.32 | 0.37 |
| D         | 3.00 BSC |      |      |
| D2        | 1.6      | 1.70 | 1.8  |
| e         | 0.50 BSC |      |      |
| E         | 3.00 BSC |      |      |
| E2        | 1.6      | 1.70 | 1.8  |
| f         | 2.53 BSC |      |      |
| L         | 0.3      | 0.40 | 0.5  |
| L1        | 0.00     | —    | 0.10 |
| aaa       | —        | —    | 0.05 |

| Dimension | Min | Typ | Max  |
|-----------|-----|-----|------|
| bbb       | —   | —   | 0.05 |
| ccc       | —   | —   | 0.08 |
| ddd       | —   | —   | 0.10 |
| eee       | —   | —   | 0.10 |

**Note:**

1. All dimensions are shown in millimeters unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

8.2 QFN20 PCB Land Pattern

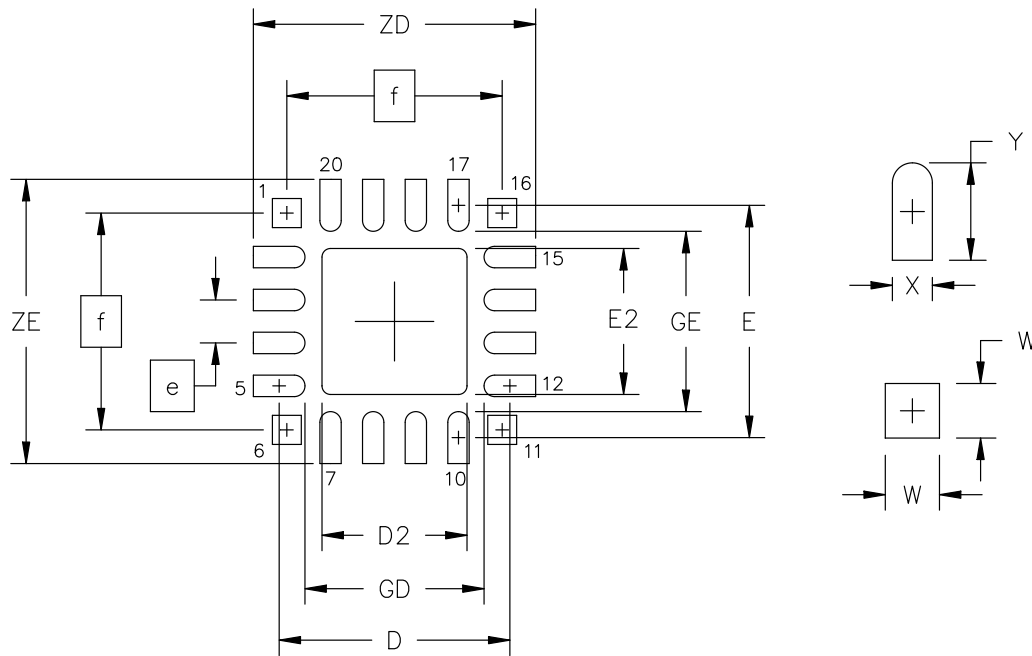


Figure 8.2. QFN20 PCB Land Pattern Drawing

Table 8.2. QFN20 PCB Land Pattern Dimensions

| Dimension | Min  | Max      |
|-----------|------|----------|
| D         |      | 2.71 REF |
| D2        | 1.60 | 1.80     |
| e         |      | 0.50 BSC |
| E         |      | 2.71 REF |
| E2        | 1.60 | 1.80     |
| f         |      | 2.53 BSC |
| GD        | 2.10 | —        |
| GE        | 2.10 | —        |
| W         | —    | 0.34     |
| X         | —    | 0.28     |
| Y         |      | 0.61 REF |
| ZE        | —    | 3.31     |
| ZD        | —    | 3.31     |

| Dimension                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | Min | Max |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|
| <p><b>Note:</b></p> <ol style="list-style-type: none"> <li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li> <li>2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.</li> <li>3. This Land Pattern Design is based on IPC-SM-782 guidelines.</li> <li>4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.</li> <li>5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.</li> <li>6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.</li> <li>7. The stencil thickness should be 0.125 mm (5 mils).</li> <li>8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.</li> <li>9. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component stand-off.</li> <li>10. A No-Clean, Type-3 solder paste is recommended.</li> <li>11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</li> </ol> |     |     |

### 8.3 QFN20 Package Marking

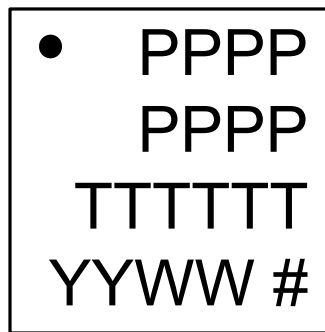


Figure 8.3. QFN20 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

## 9. SOIC16 Package Specifications

### 9.1 SOIC16 Package Dimensions

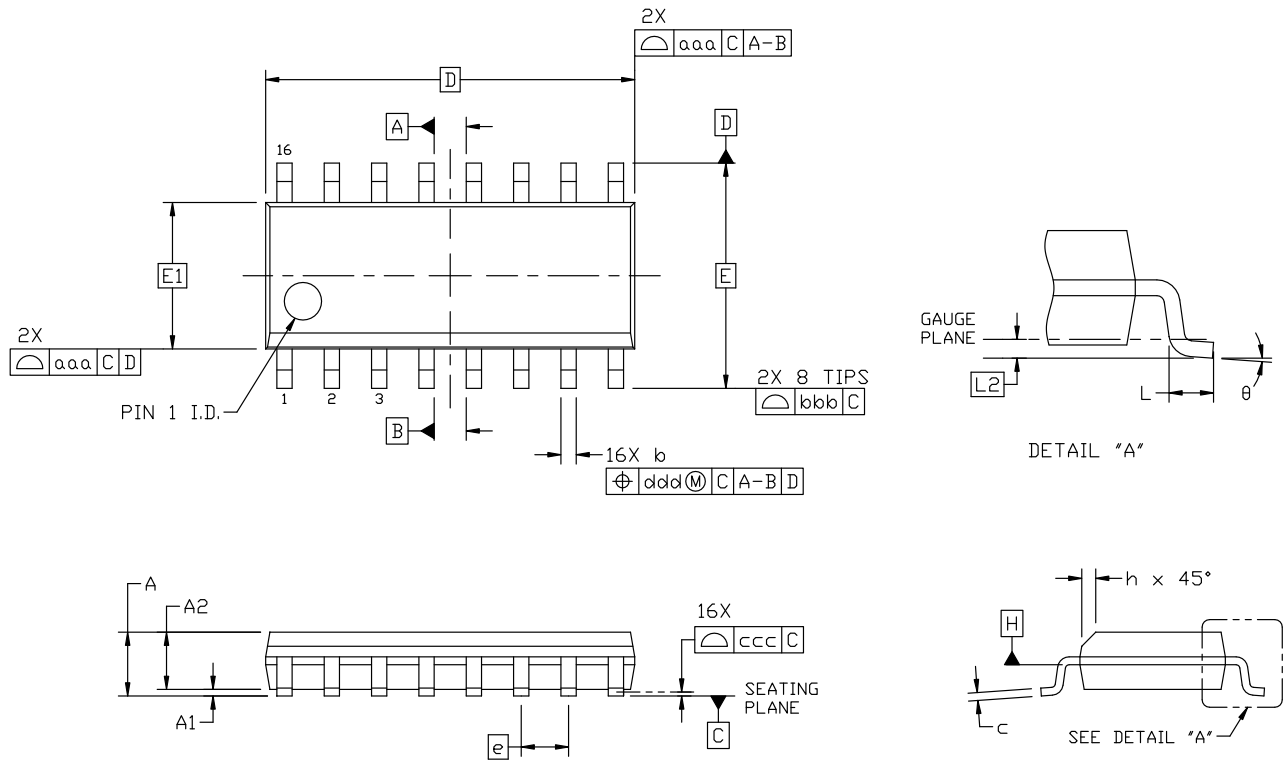


Figure 9.1. SOIC16 Package Drawing

Table 9.1. SOIC16 Package Dimensions

| Dimension | Min      | Typ | Max  |
|-----------|----------|-----|------|
| A         | —        | —   | 1.75 |
| A1        | 0.10     | —   | 0.25 |
| A2        | 1.25     | —   | —    |
| b         | 0.31     | —   | 0.51 |
| c         | 0.17     | —   | 0.25 |
| D         | 9.90 BSC |     |      |
| E         | 6.00 BSC |     |      |
| E1        | 3.90 BSC |     |      |
| e         | 1.27 BSC |     |      |
| L         | 0.40     | —   | 1.27 |
| L2        | 0.25 BSC |     |      |



| Dimension | Min  | Typ | Max  |
|-----------|------|-----|------|
| h         | 0.25 | —   | 0.50 |
| $\theta$  | 0°   | —   | 8°   |
| aaa       | 0.10 |     |      |
| bbb       | 0.20 |     |      |
| ccc       | 0.10 |     |      |
| ddd       | 0.25 |     |      |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.2 SOIC16 PCB Land Pattern

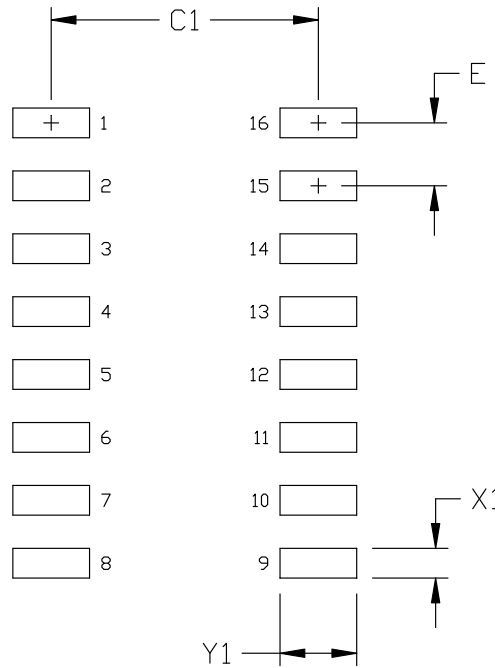


Figure 9.2. SOIC16 PCB Land Pattern Drawing

Table 9.2. SOIC16 PCB Land Pattern Dimensions

| Dimension | Feature            | (mm) |
|-----------|--------------------|------|
| C1        | Pad Column Spacing | 5.40 |
| E         | Pad Row Pitch      | 1.27 |
| X1        | Pad Width          | 0.60 |
| Y1        | Pad Length         | 1.55 |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
3. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

### 9.3 SOIC16 Package Marking



Figure 9.3. SOIC16 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

|                                                  |           |
|--------------------------------------------------|-----------|
| <b>1. Feature List</b>                           | <b>1</b>  |
| <b>2. Ordering Information</b>                   | <b>2</b>  |
| <b>3. System Overview</b>                        | <b>3</b>  |
| 3.1 Introduction                                 | 3         |
| 3.2 Power                                        | 4         |
| 3.3 I/O                                          | 4         |
| 3.4 Clocking                                     | 4         |
| 3.5 Counters/Timers and PWM                      | 5         |
| 3.6 Communications and Other Digital Peripherals | 6         |
| 3.7 Analog                                       | 7         |
| 3.8 Reset Sources                                | 8         |
| 3.9 Debugging                                    | 8         |
| 3.10 Bootloader                                  | 8         |
| <b>4. Electrical Specifications</b>              | <b>9</b>  |
| 4.1 Electrical Characteristics                   | 9         |
| 4.2 Thermal Conditions                           | 16        |
| 4.3 Absolute Maximum Ratings                     | 17        |
| 4.4 Typical Performance Curves                   | 18        |
| <b>5. Typical Connection Diagrams</b>            | <b>22</b> |
| 5.1 Power                                        | 22        |
| 5.2 Other Connections                            | 22        |
| <b>6. Pin Definitions</b>                        | <b>23</b> |
| 6.1 EFM8BB1x-QSOP24 Pin Definitions              | 23        |
| 6.2 EFM8BB1x-QFN20 Pin Definitions               | 26        |
| 6.3 EFM8BB1x-SOIC16 Pin Definitions              | 29        |
| <b>7. QSOP24 Package Specifications</b>          | <b>31</b> |
| 7.1 QSOP24 Package Dimensions                    | 31        |
| 7.2 QSOP24 PCB Land Pattern                      | 33        |
| 7.3 QSOP24 Package Marking                       | 34        |
| <b>8. QFN20 Package Specifications</b>           | <b>35</b> |
| 8.1 QFN20 Package Dimensions                     | 35        |
| 8.2 QFN20 PCB Land Pattern                       | 37        |
| 8.3 QFN20 Package Marking                        | 38        |
| <b>9. SOIC16 Package Specifications</b>          | <b>39</b> |
| 9.1 SOIC16 Package Dimensions                    | 39        |

---

|                                       |           |
|---------------------------------------|-----------|
| 9.2 SOIC16 PCB Land Pattern . . . . . | .41       |
| 9.3 SOIC16 Package Marking . . . . .  | .42       |
| <b>Table of Contents . . . . .</b>    | <b>43</b> |



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