EDI Electronic Designs Inc.

256Kx4 Monolithic High Speed Synchronous Static RAM

ADVANCE INFORMATION

The EDI2040C is a high performance, 1 megabit synchronous static RAM organized as 256Kx4, available in six versions.

Inputs are registered or latched on the rising edge of CLK (K), depending on version. The output can be self-timed, registered, or latched, also depending on version.

Address, Data, and Control need to be held valid for a small percentage of cycle time and output timing can be matched to very tight system constraints.

These options allow the designer tremendous flexibility in the design of very high speed computer systems.

Features

256Kx4 bit Synchronous Static
Random Access Memory
- Fast Access Times 15, 20 and 25ns
- Works with System Clocks to 65Mhz
- Separate Data Input/Output

Thru-hole and Surface Mount Package Options
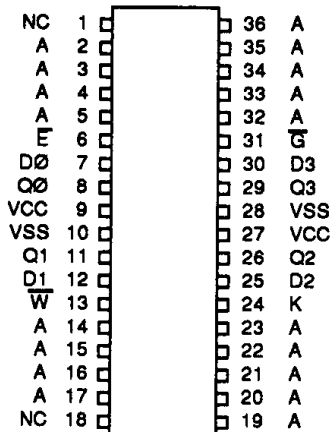JEDEC Pinout
- 36 Pin DIP, 400 mils Wide
- 36 Lead SOJ

Single +5V (±10%) Supply Operation

Pin Names

AØ-A15	Address Inputs
E	Chip Enable
W	Write Enable
G1-G2	Output Enables
K1-K2	Clock
DØ-D3	Data Input
QØ-Q3	Data Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

Part No.	Input	Output	#CLK
EDI2040C	Latched	Latched	1
EDI2041C	Registered	Registered	1
EDI2042C	Latched	Asynchronous	1
EDI2043C	Registered	Asynchronous	1
EDI2044C	Latched	Registered	2
EDI2045C	Registered	Registered	2

JEDEC Pinout

```
NC   1      36  A
 A   2      35  A
 A   3      34  A
 A   4      33  A
 A   5      32  A
 E   6      31  G
DØ   7      30  D3
QØ   8      29  Q3
VCC  9      28  VSS
VSS 10      27  VCC
 Q1 11      26  Q2
 D1 12      25  D2
 W  13      24  K
 A  14      23  A
 A  15      22  A
 A  16      21  A
 A  17      20  A
NC  18      19  A
```

Functional Block Diagram