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74AC/ACT11470

Octal transceiver/register with dual enable (3-State)

FEATURES

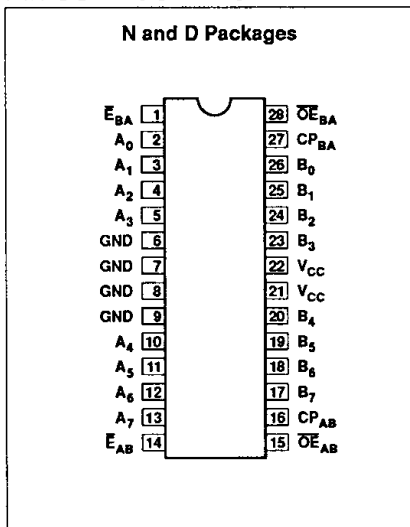
- Combines '245 and '374 type functions in one chip
- 8-bit octal transceiver with D-type flip-flops
- 3-State buffers
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11470 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11470 Octal Transceiver/Register contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. Dual Enable (\overline{E}_{AB} , \overline{E}_{BA}) and Output Enable (\overline{OE}_{AB} , \overline{OE}_{BA}) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

PIN CONFIGURATION



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS		TYPICAL		UNIT
		T _{amb} = 25°C; GND = 0V; V _{CC} = 5.0V		AC	ACT	
t _{PLH} / t _{PHL}	Propagation delay CP _{XX} to A _n or B _n	C _L = 50pF		5.3	7.1	ns
C _{PD}	Power dissipation capacitance per register ¹	f = 1MHz;	Enabled	38	41	pF
		C _L = 50pF	Disabled	23	27	
C _{IN}	Input capacitance	V _I = 0V or V _{CC}		4.5	4.5	pF
C _{I/O}	I/O capacitance	V _{I/O} = 0V or V _{CC} ; Disabled		12.0	12.0	pF
I _{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f _{MAX}	Maximum clock frequency	C _L = 50pF		135	125	MHz

Note:

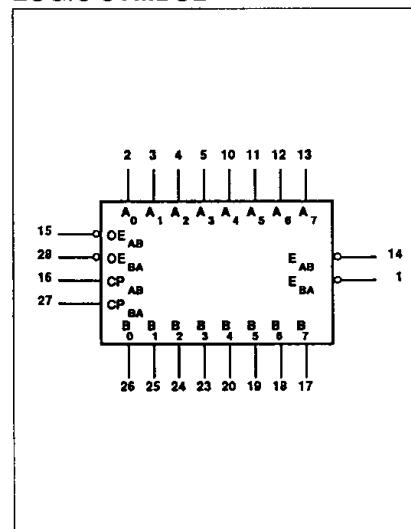
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O)$$
 where:
 f_I = input frequency in MHz, C_L = output load capacitance in pF,
 f_O = output frequency in MHz, V_{CC} = supply voltage in V,
 Σ (C_L × V_{CC}² × f_O) = sum of outputs

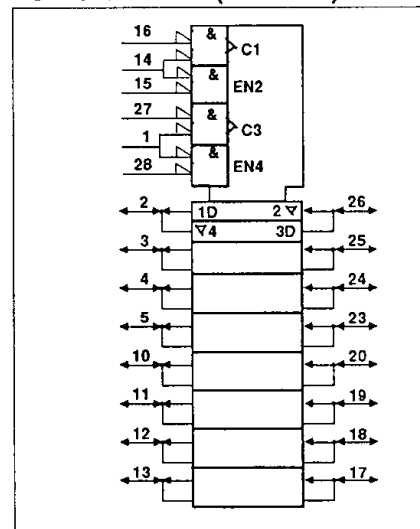
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11470N 74ACT11470N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11470D 74ACT11470D

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal transceiver/register with dual enable (3-State)

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PIN DESCRIPTION

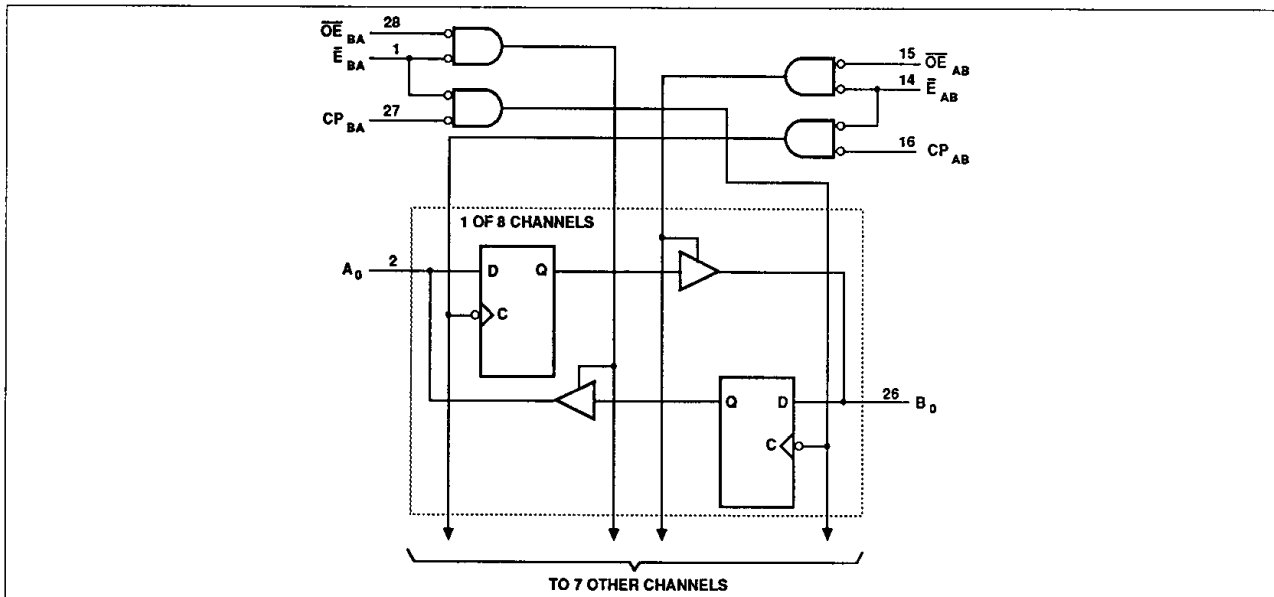
PIN NUMBER	SYMBOL	NAME AND FUNCTION
16	CP _{AB}	A-to-B clock input (active Low)
27	CP _{BA}	B-to-A clock input (active Low)
15	\overline{OE}_{AB}	A-to-B output enable input (active Low)
28	\overline{OE}_{BA}	B-to-A output enable input (active Low)
14	\overline{E}_{AB}	A-to-B enable input (active Low)
1	\overline{E}_{BA}	B-to-A enable input (active Low)
2, 3, 4, 5, 10, 11, 12, 13	A ₀ - A ₇	Data inputs/outputs (A side)
26, 25, 24, 23, 20, 19, 18, 17	B ₀ - B ₇	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V _{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
\overline{OE}_{xx}	\overline{E}_{xx}	CP _{xx}	Data		
H	X	X	X	Z	Outputs disabled
X	H	X	X	Z	Outputs and clock disabled
L	L	↑	l h	L H	Load register
X	↑	L	l h	Z	Load register and disable outputs

H = High voltage level
 h = High state present one setup time before the Low-to-High transition
 L = Low voltage level
 l = Low state present one setup time before the Low-to-High transition
 ↑ = Low-to-High transition
 X = Don't care
 Z = High-impedance state

LOGIC DIAGRAM



Octal transceiver/register with dual enable (3-State)

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11470			74ACT11470			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0 ¹	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta V/\Delta t$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current ²	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
I_{OK} or V_O	DC output diode current ²	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current per output pin	$V_O = 0$ to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±400	mA
	DC ground current		±400	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal transceiver/register with dual enable (3-State)

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC}	74AC11470				74ACT11470				UNIT	
				T _{amb} = +25°C		T _{amb} = -40°C to +85°C		T _{amb} = +25°C		T _{amb} = -40°C to +85°C			
				Min	Max	Min	Max	Min	Max	Min	Max		
V _{IH}	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V _{IL}	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V _{OH}	High-level output voltage	V _I = V _{IL} or V _{IH}	I _{OH} = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I _{OH} = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
I _{OH} = -75mA ¹	5.5			3.85				3.85					
V _{OL}	Low-level output voltage	V _I = V _{IL} or V _{IH}	I _{OL} = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
				5.5		0.1		0.1		0.1			0.1
			I _{OL} = 12mA	3.0		0.36		0.44					
				4.5		0.36		0.44		0.36			0.44
			I _{OL} = 24mA	4.5		0.36		0.44		0.36			0.44
				5.5		0.36		0.44		0.36			0.44
I _{OL} = 75mA ¹	5.5				1.65				1.65				
I _I	Input leakage current	V _I = V _{CC} or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I _{OZ}	3-State output off-state current	V _I = V _{IL} or V _{IH} , V _O = V _{CC} or GND	5.5		±0.5		5.0		±0.5		5.0	μA	
I _{CC}	Quiescent supply current	V _I = V _{CC} or GND, I _O = 0mA	5.5		8.0		80		8.0		80	μA	
ΔI _{CC}	Supply current, TTL inputs High ²	One input at 3.4V, other inputs at V _{CC} or GND	5.5						0.9		1.0	mA	

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
- This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Octal transceiver/register with dual enable (3-State)

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AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11470					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum clock frequency	1	75	110		75		MHz
t _{PLH} t _{PHL}	Propagaion delay, CP _{BA} to A _n or CP _{AB} to B _n	1	4.1 4.8	7.3 7.8	8.9 9.3	4.1 4.8	9.8 10.2	ns
t _{PZH} t _{PZL}	Output enable time \overline{OE}_{BA} to A _n or \overline{OE}_{AB} to B _n	2	4.3 5.3	7.5 8.7	9.2 10.5	4.3 5.3	10.1 11.6	ns
t _{PZH} t _{PZL}	Output enable time \overline{E}_{BA} to A _n or \overline{E}_{AB} to B _n	2	5.0 6.0	8.2 9.4	9.9 11.2	5.0 6.0	10.8 12.3	ns
t _{PHZ} t _{PLZ}	Output disable time \overline{OE}_{BA} to A _n or \overline{OE}_{AB} to B _n	2	4.0 4.0	6.8 6.8	8.6 8.7	4.0 4.0	9.2 9.1	ns
t _{PHZ} t _{PLZ}	Output disable time \overline{E}_{BA} to A _n or \overline{E}_{AB} to B _n	2	4.3 4.4	7.2 7.2	8.9 9.1	4.3 4.4	9.5 9.6	ns
t _S	Setup time, High or Low A _n to CP _{AB} or B _n to CP _{BA}	3	2.0			2.0		ns
t _H	Hold time, High or Low CP _{BA} to A _n or CP _{AB} to B _n	3	1.5			1.5		ns
t _S	Setup time, High or Low A _n to \overline{E}_{AB} or B _n to \overline{E}_{BA}	3	2.0			2.0		ns
t _H	Hold time, High or Low \overline{E}_{BA} to A _n or \overline{E}_{AB} to B _n	3	1.5			1.5		ns
t _w	Clock pulse width High or Low	1	6.5			6.5		ns

Octal transceiver/register with dual enable (3-State)

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AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11470					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum clock frequency	1	110	130		110		MHz
t _{PLH} t _{PHL}	Propagation delay, CP _{BA} to A _n or CP _{AB} to B _n	1	2.1 2.7	4.8 5.7	6.4 7.6	2.1 2.7	7.0 8.4	ns
t _{PZH} t _{PZL}	Output enable time OE _{BA} to A _n or OE _{AB} to B _n	2	2.6 3.5	5.1 6.5	6.8 8.6	2.6 3.5	7.4 9.4	ns
t _{PZH} t _{PZL}	Output enable time E _{BA} to A _n or E _{AB} to B _n	2	3.1 3.9	5.6 7.0	7.3 9.0	3.1 3.9	8.0 9.8	ns
t _{PHZ} t _{PLZ}	Output disable time OE _{BA} to A _n or OE _{AB} to B _n	2	3.1 3.2	5.5 5.5	7.2 7.6	3.1 3.2	7.6 7.9	ns
t _{PHZ} t _{PLZ}	Output disable time E _{BA} to A _n or E _{AB} to B _n	2	3.3 3.4	5.6 5.8	7.5 7.7	3.3 3.4	7.9 8.1	ns
t _S	Setup time, High or Low A _n to CP _{AB} or B _n to CP _{BA}	3	1.5			1.5		ns
t _H	Hold time, High or Low CP _{BA} to A _n or CP _{AB} to B _n	3	1.5			1.5		ns
t _S	Setup time, High or Low A _n to E _{AB} or B _n to E _{BA}	3	2.0			2.0		ns
t _H	Hold time, High or Low E _{BA} to A _n or E _{AB} to B _n	3	1.0			1.0		ns
t _W	Clock pulse width High or Low	1	4.5			4.5		ns

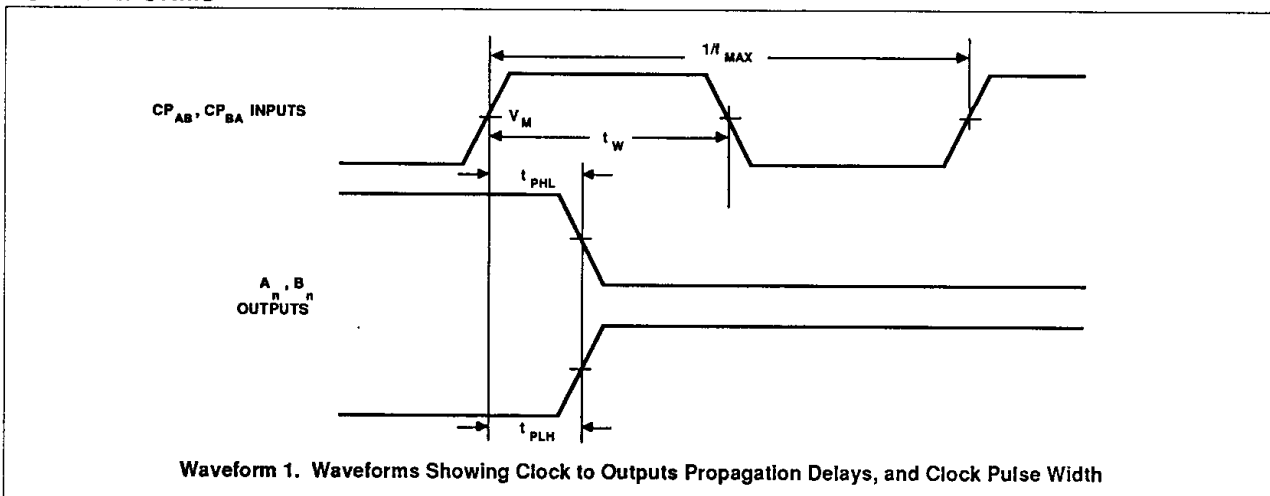
Octal transceiver/register with dual enable (3-State)

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AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11470					UNIT
			T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum clock frequency	1	90	120		90		MHz
t _{PLH} t _{PHL}	Propagaion delay, CP _{BA} to A _n or CP _{AB} to B _n	1	3.4 4.2	6.5 7.6	8.3 9.5	3.4 4.2	9.1 10.4	ns
t _{PZH} t _{PZL}	Output enable time OE _{BA} to A _n or OE _{AB} to B _n	2	3.3 4.3	6.3 7.8	8.5 10.3	3.3 4.3	9.2 11.4	ns
t _{PZH} t _{PZL}	Output enable time E _{BA} to A _n or E _{AB} to B _n	2	3.4 4.6	6.5 8.1	8.8 10.7	3.4 4.6	9.6 11.7	ns
t _{PHZ} t _{PLZ}	Output disable time OE _{BA} to A _n or OE _{AB} to B _n	2	4.8 5.1	7.4 7.3	8.8 8.8	4.8 5.1	9.4 9.3	ns
t _{PHZ} t _{PLZ}	Output disable time E _{BA} to A _n or E _{AB} to B _n	2	5.1 5.1	7.4 7.5	9.1 8.9	5.1 5.1	9.8 9.5	ns
t _S	Setup time, High or Low A _n to CP _{AB} or B _n to CP _{BA}	3	2.0			2.0		ns
t _H	Hold time, High or Low CP _{BA} to A _n or CP _{AB} to B _n	3	3.0			3.0		ns
t _S	Setup time, High or Low A _n to E _{AB} or B _n to E _{BA}	3	2.0			2.0		ns
t _H	Hold time, High or Low E _{BA} to A _n or E _{AB} to B _n	3	2.5			2.5		ns
t _W	Clock pulse width High or Low	1	5.5			5.5		ns

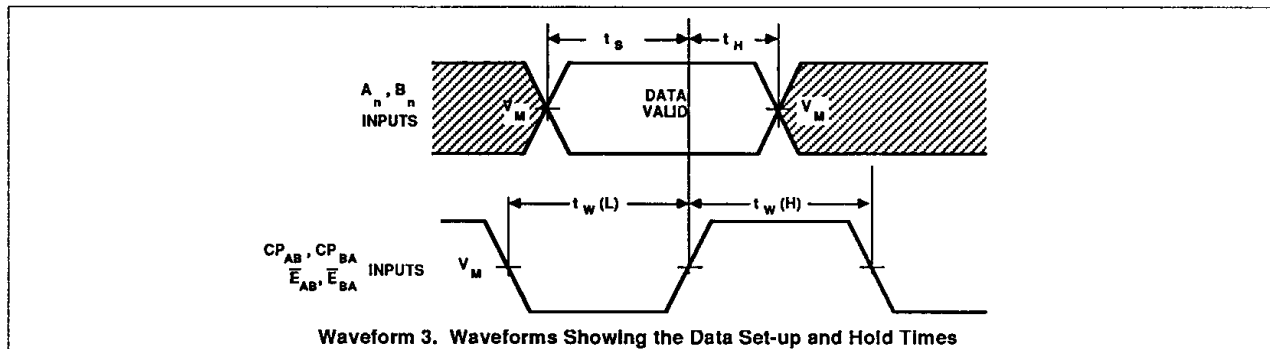
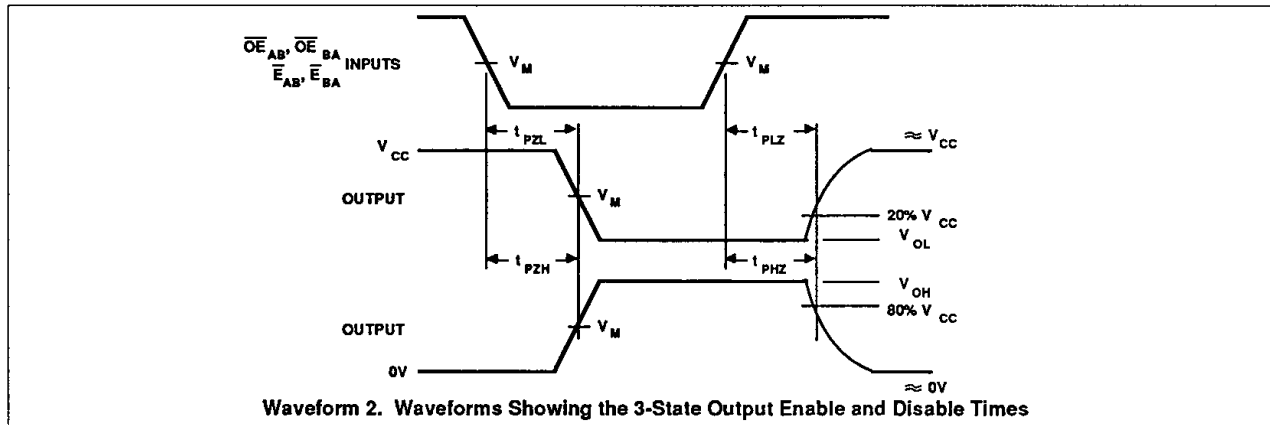
AC WAVEFORMS



Octal transceiver/register with dual enable (3-State)

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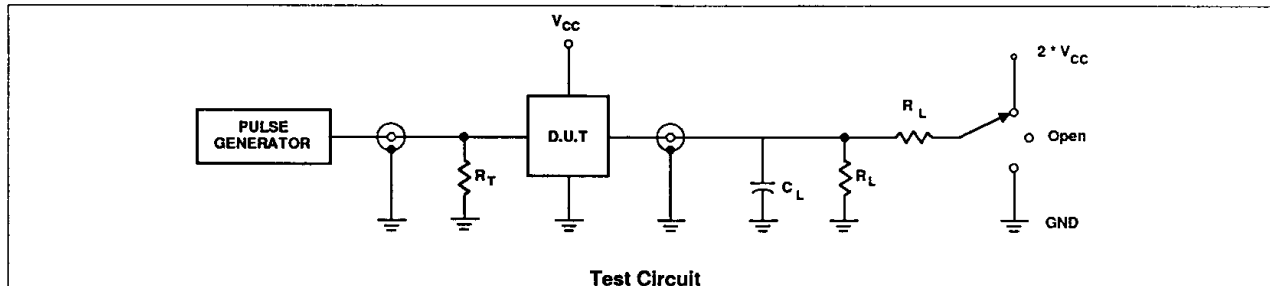
AC WAVEFORMS (Continued)



WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	$V_{IN} = \text{GND to } V_{CC}$ $V_M = 50\% V_{CC}$	$V_{OUT} = V_{OL} \text{ to } V_{OH}$
ACT	$V_{IN} = \text{GND to } 3.0V$ $V_M = 1.5V$	$V_M = 50\% V_{CC}$

TEST CIRCUIT



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \cdot V_{CC}$
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance
 R_L = Load resistor, 500Ω
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators
 Input pulses: PRR ≤ 10MHz
 $t_r = t_f = 3ns$