ESDAULC6-3BP6
ESDAULC6-3BF2

ESD protection for high speed interface

Main applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phones handsets and accessories
- Video equipment

Features

- Ultra low capacitance 1.25 pF max.
- Bi-directional protection
- RoHS package

Description

The ESDAULC6-3Bxx is a monolithic application specific discrete device dedicated to ESD protection of high speed interfaces such as USB2.0.

The device is ideal for applications where both reduced print circuit board space and power absorption capability are required.

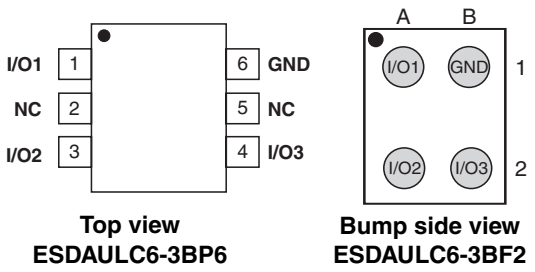
Benefits

- Ultra low capacitance bidirectional ESD protection
- Low PCB space consumption:
  2.5 mm^2 max footprint (1.7 mm^2 for Flip-Chip)
- Enhanced ESD protection:
  - 15 kV contact discharge
  - 15 kV air discharge
- No insertion loss to 3.0 GHz
- Ultra low leakage current
- High reliability offered by monolithic integration

SOT-666
ESDAULC6-3BP6

Flip-Chip
ESDAULC6-3BF2

Figure 1. Functional diagram



Top view
ESDAULC6-3BP6

Bump side view
ESDAULC6-3BF2

Figure 2. Pin configuration

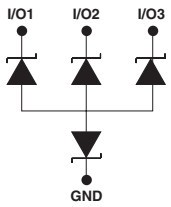


Table 1. Order codes

Part number	Marking
ESDAULC6-3BP6	3
ESDAULC6-3BF2	3B

Complies with the following standards:

IEC 61000-4-2 level 4:

8 kV (contact discharge)
15 kV (air discharge)

MIL STD 883G-Method 3015-7: class 3B

HBM (Human Body Model)

1 Characteristics

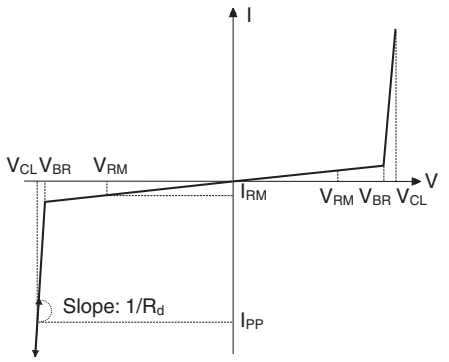
Table 2. Absolute maximum ratings

Symbol	Parameter		Value (min.)	Unit
V_{PP}	Peak pulse voltage (1)	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	15 15	kV
T_j	Maximum operating junction temperature		150	°C
T_{stg}	Storage temperature range		-55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s at 5 mm for case		260	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Table 3. Electrical characteristics (T_{amb} = 25° C)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
C	Capacitance
R_d	Dynamic resistance



Parameter	Test condition		Min	Typ	Max	Unit
V_{BR} (1)	I_R = 1 mA		6.0		9.2	V
I_{RM}	V_{RM} = 5 V				0.5	µA
R_d	Square pulse, I_{PP} = 6 A, t_p = 2.5 µs			1.4		Ω
αT					1.2	10^{-4}/°C
$C_{i/o-i/o}$	$V_{I/O}$ = 0 V, F = 1 MHz, V_{OSC} = 30 mV	SOT-666		1.0	1.25	pF
		Flip-Chip		1.25	1.5	
	$V_{I/O}$ = 1.65 V, V_{CC} = 4.3 V, F = 1 MHz, V_{OSC} = 400 mV	SOT-666		0.75	0.9	
		Flip-Chip		0.9	1.20	

1. Same value for I/O to I/O and I/O to GND

Figure 3. Relative variation of peak pulse power versus initial junction temperature (SOT-666)

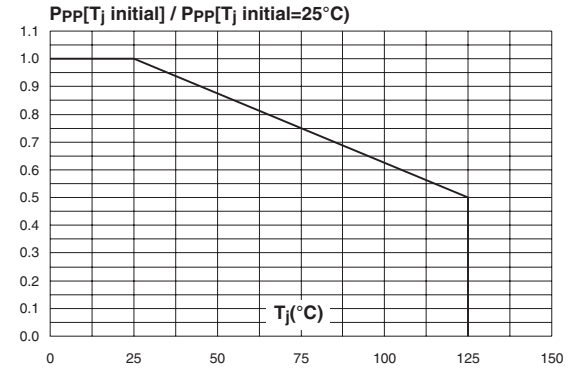


Figure 4. Relative variation of peak pulse power versus initial junction temperature (Flip-Chip)

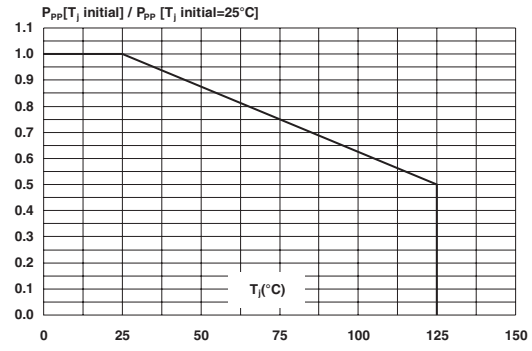


Figure 5. Peak pulse power versus exponential pulse duration (SOT-666)

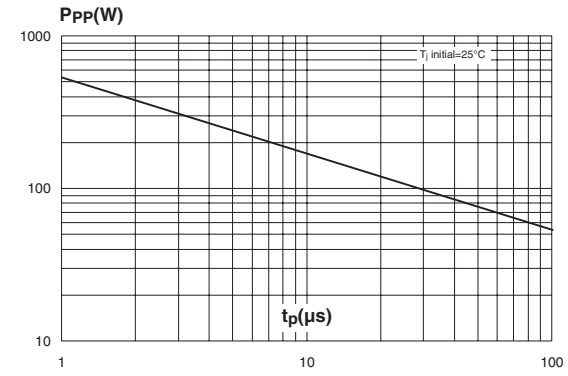


Figure 6. Peak pulse power versus exponential pulse duration (Flip-Chip)

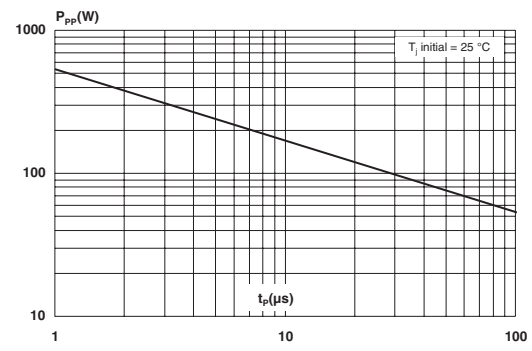


Figure 7. Clamping voltage versus peak pulse current (typical values) (SOT-666)

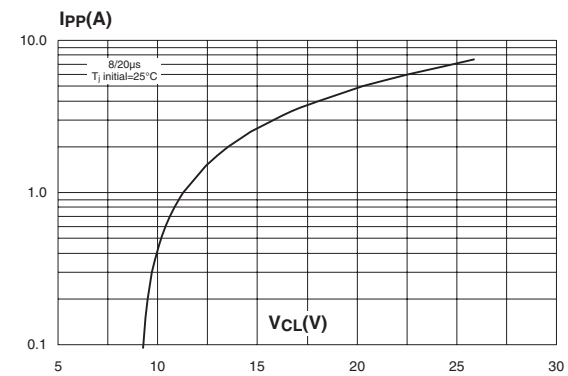


Figure 8. Clamping voltage versus peak pulse current (typical values) (Flip-Chip)

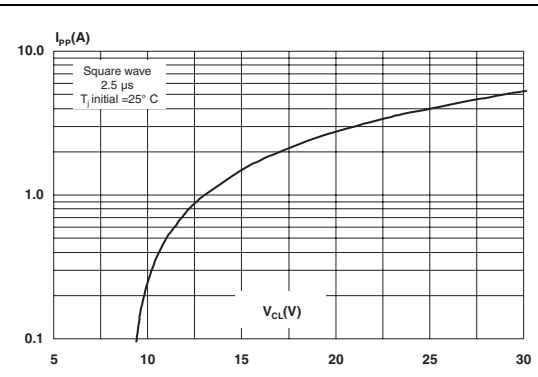


Figure 9. Junction capacitance versus reverse voltage applied (typical values) (SOT-666)

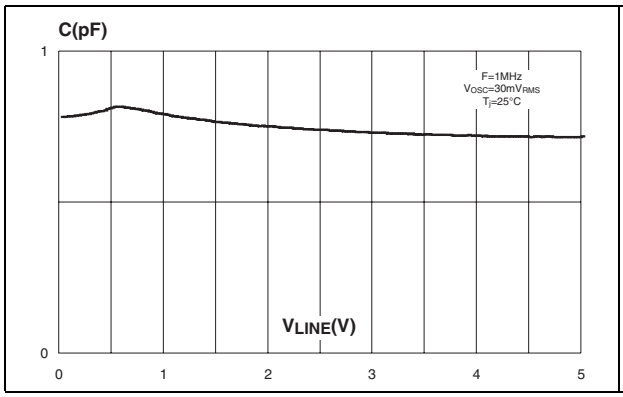


Figure 10. Junction capacitance versus reverse voltage applied (typical values) (Flip-Chip)

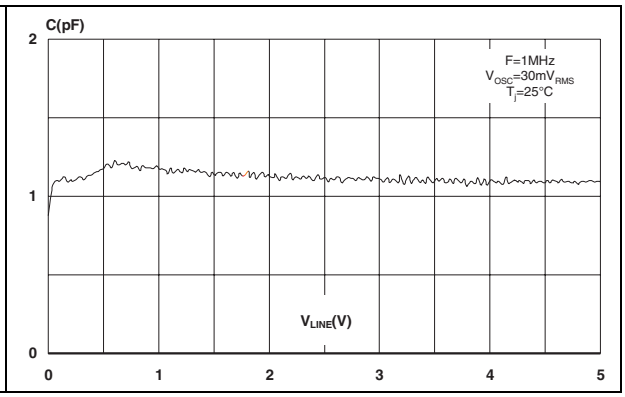


Figure 11. Relative variation of leakage current versus junction temperature (typical values) (SOT-666)

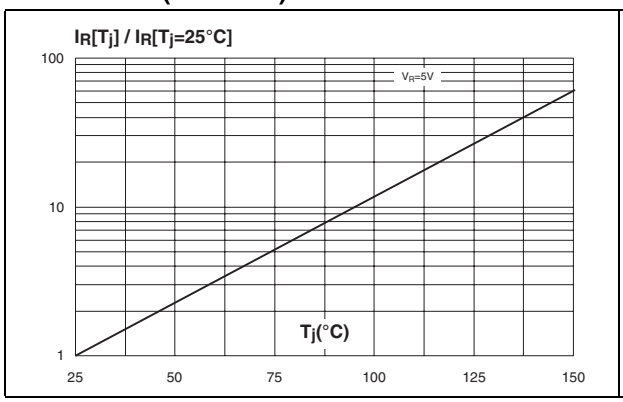


Figure 12. Relative variation of leakage current versus junction temperature (typical values) (Flip-Chip)

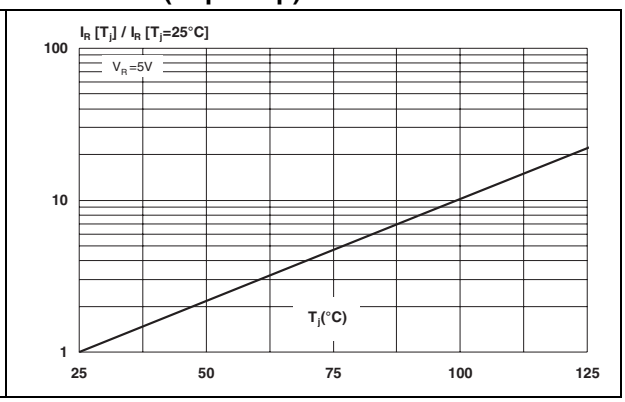


Figure 13. Remaining voltage after ESDAULC6-3BP6 during ESD 15 kV positive surge (air discharge) (SOT-666)

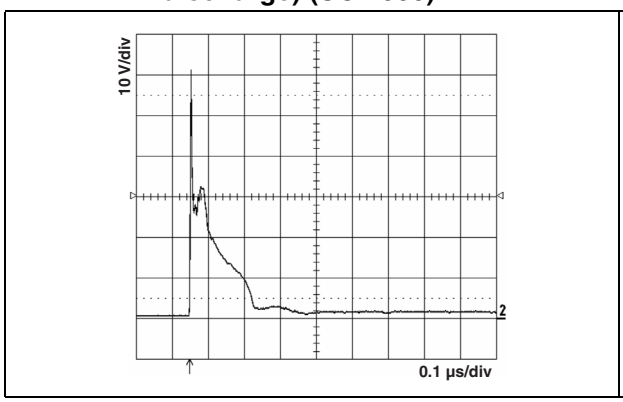


Figure 14. Remaining voltage after ESDAULC6-3BF2 during ESD 15 kV positive surge (air discharge) (Flip-Chip)

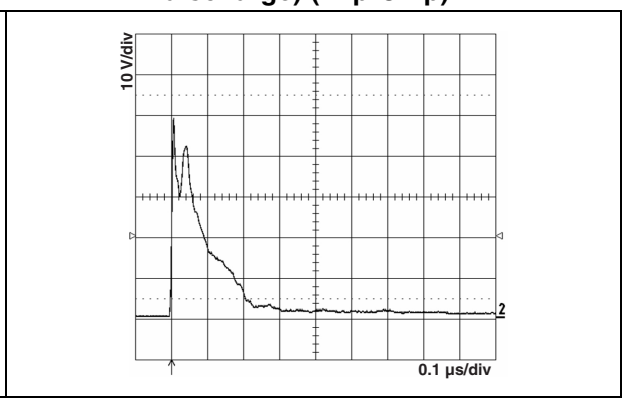


Figure 15. Remaining voltage after ESDAULC6-3BP6 during ESD 15 kV negative surge (air discharge) (SOT-666)

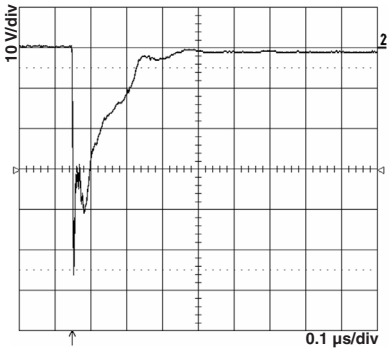


Figure 16. Remaining voltage after ESDAULC6-3BF2 during ESD 15 kV negative surge (air discharge) (Flip-Chip)

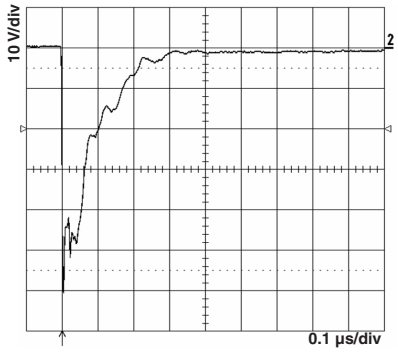


Figure 17. S21 attenuation measurement results of each channel (SOT-666)

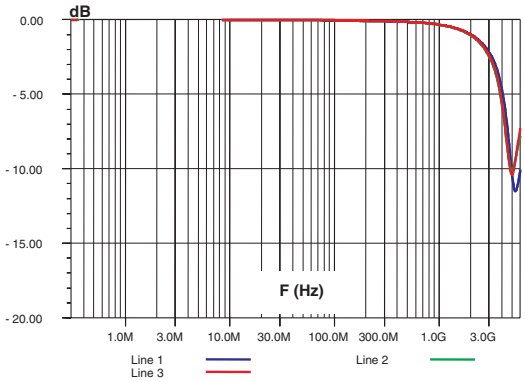


Figure 18. S21 attenuation measurement results of channel 1 (Flip-Chip)

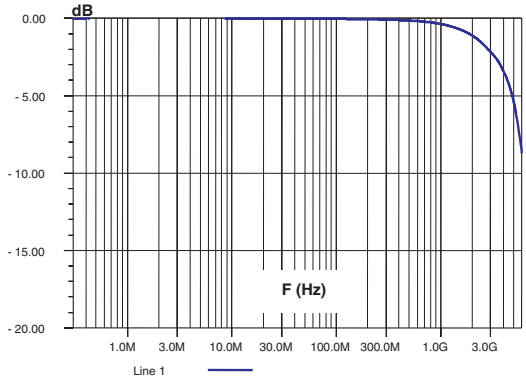


Figure 19. Analog crosstalk measurements between channels (SOT-666)

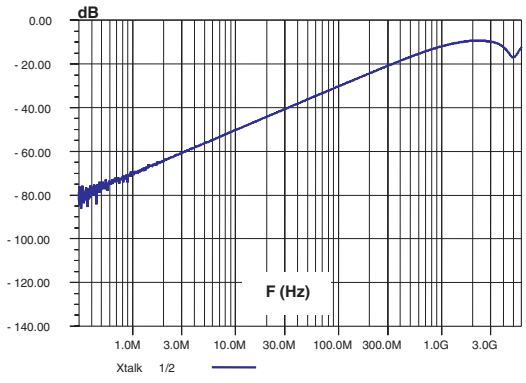
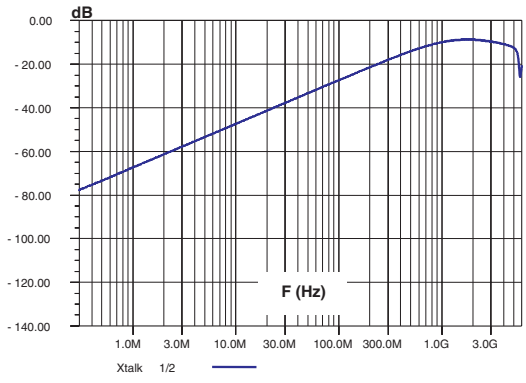


Figure 20. Analog crosstalk measurements between channels (Flip-Chip)



2 Application examples

Figure 21. USB2.0 (high speed) protection application schematic

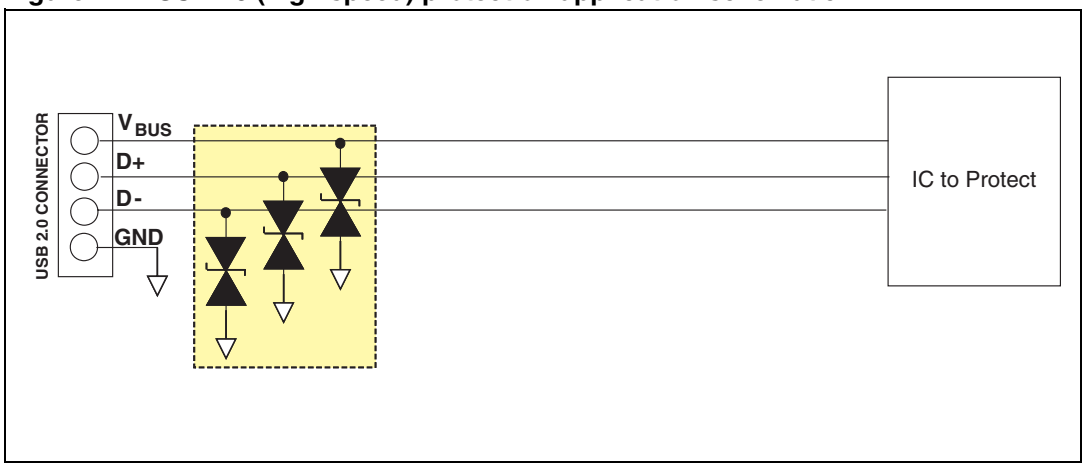


Figure 22. Audio jack protection application schematic

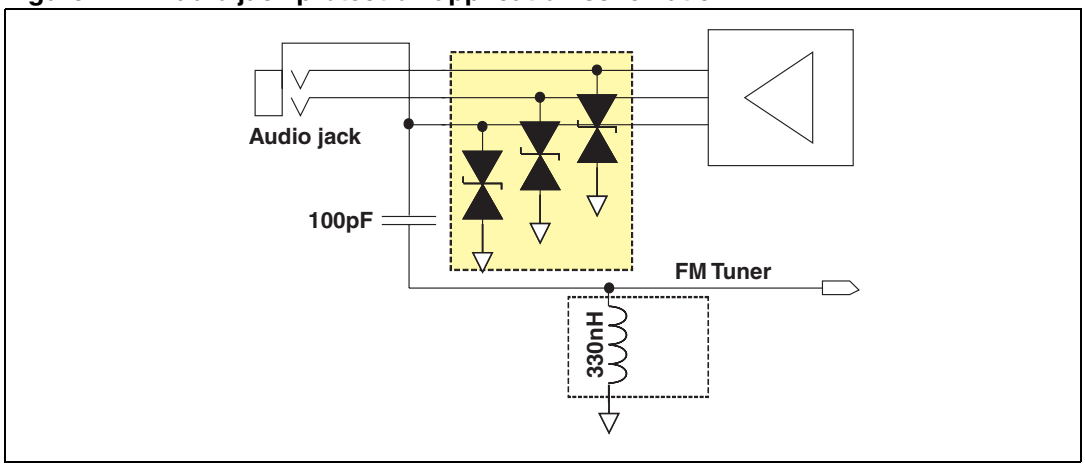
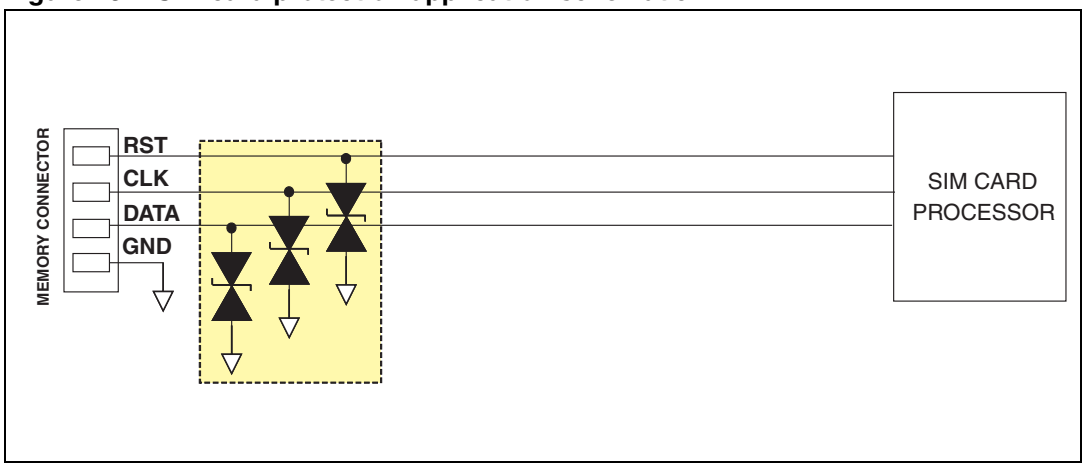
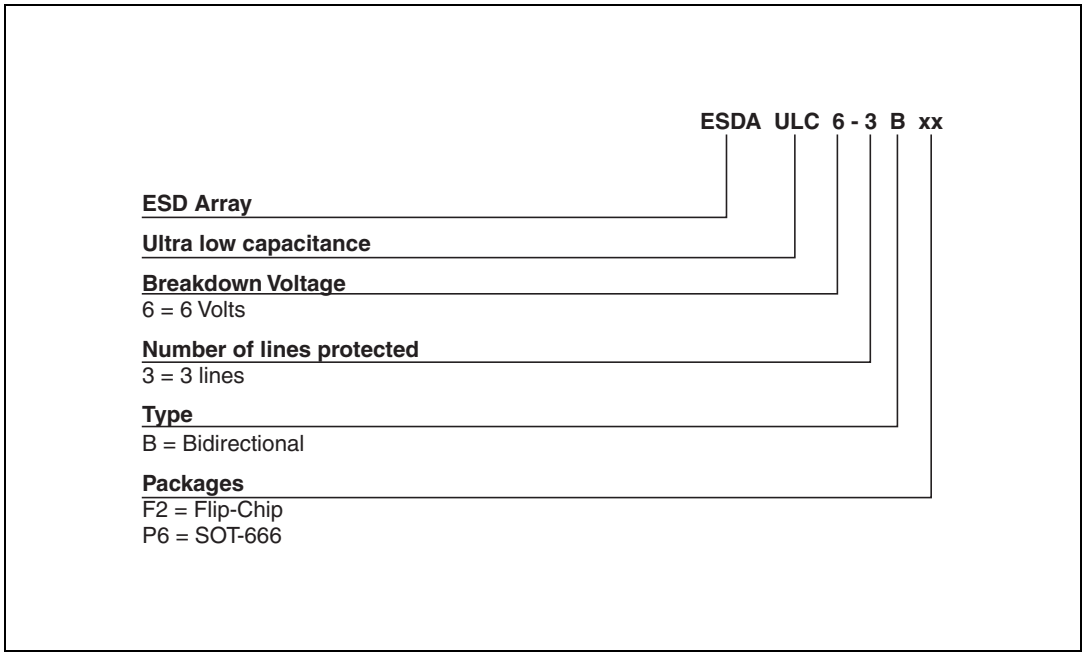


Figure 23. SIM card protection application schematic



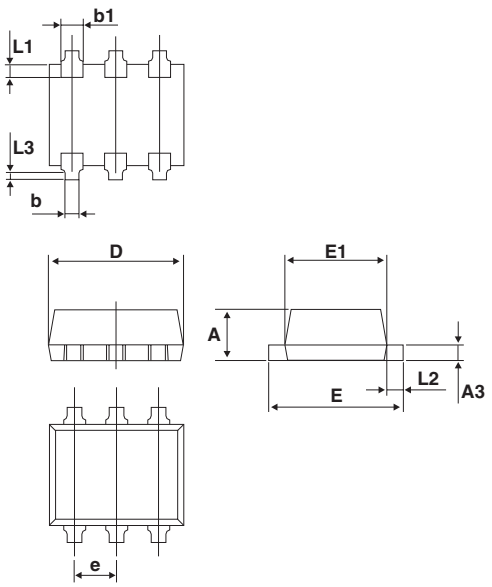
3 Ordering information scheme



4 Package information

- Epoxy meets UL 94, V0

Table 4. SOT-666 dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45		0.60	0.018		0.024
A3	0.08		0.18	0.003		0.007
b	0.17		0.34	0.007		0.013
b1	0.19	0.27	0.34	0.007	0.011	0.013
D	1.50		1.70	0.059		0.067
E	1.50		1.70	0.059		0.067
E1	1.10		1.30	0.043		0.051
e		0.50			0.020	
L1		0.19			0.007	
L2	0.10		0.30	0.004		0.012
L3		0.10			0.004	

Figure 24. SOT-666 footprint (dimensions in mm)

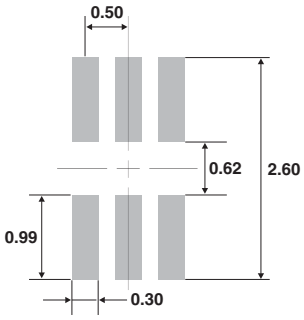


Figure 25. Flip-Chip dimensions

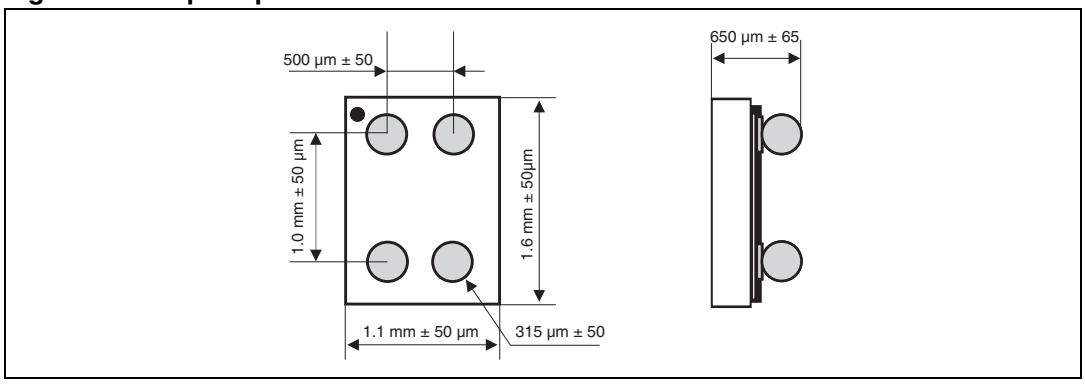


Figure 26. Flip-Chip footprint

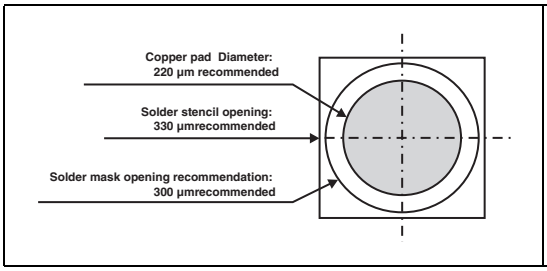


Figure 27. Flip-Chip marking

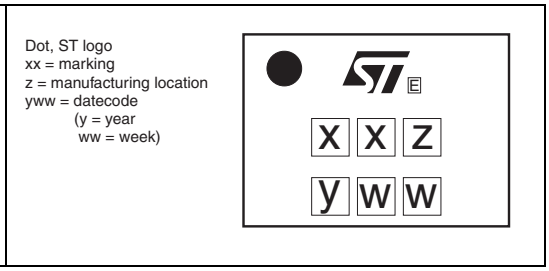
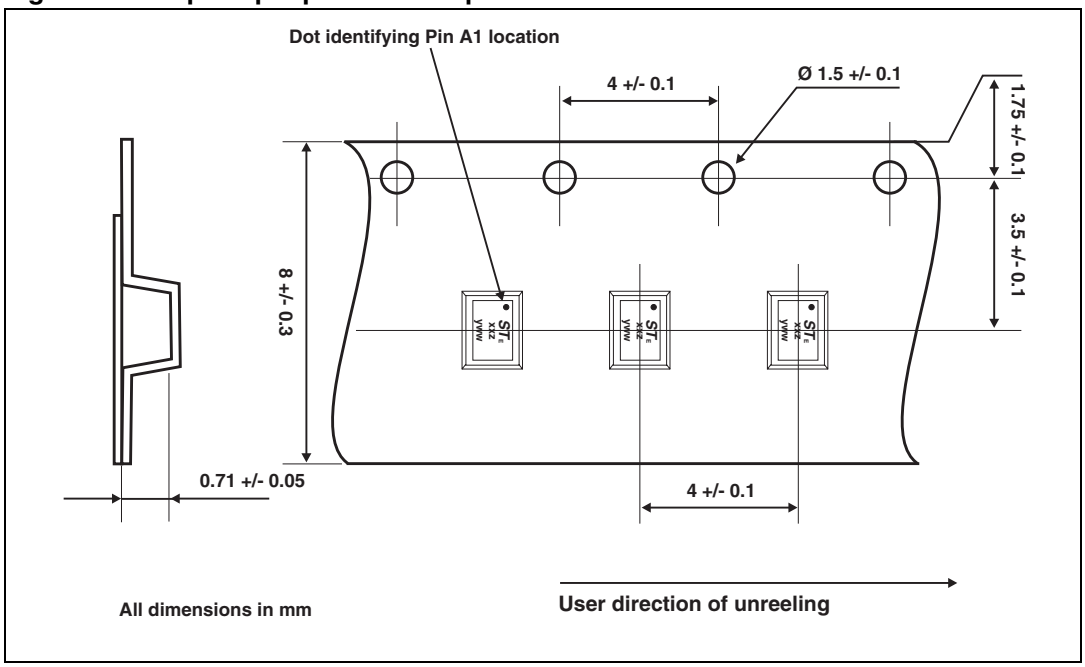


Figure 28. Flip-Chip tape and reel specifications



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5 Ordering information

Table 5. Ordering information

Part number	Marking	Package	Weight	Base qty	Delivery mode
ESDAULC6-3BP6	3	SOT-666	2.9 mg	5000	Tape and reel
ESDAULC6-3BF2	3B	Flip-Chip	2.22 mg	5000	Tape and reel

6 Revision history

Table 6. Revision history

Datet	Revision	Changes
03-Jul-2007	1	Initial release

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