# Low-Voltage, Low $R_{ON}$, Single Analog Switch In miniQFN-6 Package

## DESCRIPTION

The DG2511, DG2512, DG2513 are low on-resistance, single-pole/double-throw or single-pole/single-throw monolithic CMOS analog switch. It is designed for low voltage applications. The DG2511, DG2512, DG2513 are ideal for portable and battery powered equipment, requiring high performance and efficient use of board space. In additional to the low on-resistance (1.3 Ω at 2.7 V).

The DG2511 is an SPDT and the DG2512, DG2513 are SPST. The switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

The DG2511, DG2512, DG2513 are built on Vishay Siliconix's low voltage JI5L process. An epitaxial layer prevents latchup.

Break-before-make is guaranteed.

The DG2511, DG2512, DG2513 represents a breakthrough in packaging development for analog switching products. The miniQFN-6 package (1.2 x 1.0 mm).

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For analog switching products manufactured with NiPdAu device terminations, the lead (Pb)-free "-E4" suffix is being used as a designator.

## FEATURES

- Low voltage operation (1.8 V to 5.5 V)
- Low on-resistance - $R_{ON}$: 1.3 Ω at 2.7 V
- Low charge injection
- Latch-up current > 300 mA (JESD78A)
- miniQFN-6 package (1.2 x 1.0 mm)
- **Compliant to RoHS Directive 2002/95/EC**

Pb-free
RoHS COMPLIANT

## BENEFITS

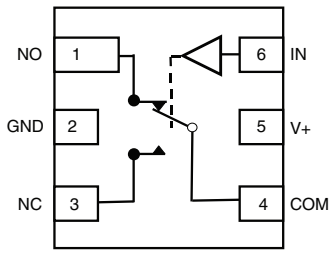
- Reduced power consumption
- Simple logic interface
- High accuracy
- Reduce board space
- Guaranteed 2 V operation

## APPLICATIONS

- Cellular phones
- Communication systems
- Portable test equipment
- Battery operated systems
- Sample and hold circuits
- ADC and DAC applications
- Low voltage data acquisition systems

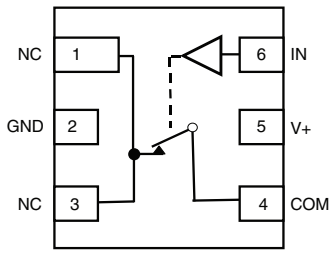
## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

**DG2511**
**miniQFN-6**



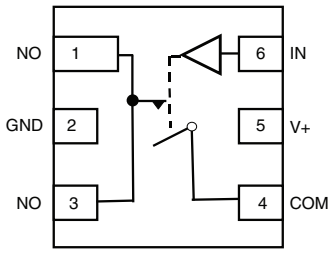

Top View

**DG2512**
**miniQFN-6**

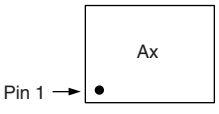



Top View

**DG2513**
**miniQFN-6**




Top View




Device Marking: Ax for DG2511
Bx for DG2512
Cx for DG2513
x = Date/Lot Traceability Code
Note: Pin 1 has long lead

**TRUTH TABLE**

| Logic | NC | NO |
|---|---|---|
| 0 | On | Off |
| 1 | Off | On |

**COMMERCIAL ORDERING INFORMATION**

| Temp Range | Package | Part Number |
|---|---|---|
| - 40 °C to 85 °C | miniQFN-6<br>Lead (Pb)-free<br>with Tape and Reel | DG2511DN-T1-E4<br>DG2512DN-T1-E4<br>DG2513DN-T1-E4 |

## ABSOLUTE MAXIMUM RATINGS

| Parameter | | Limit | Unit |
|---|---|---|---|
| Reference V+ to GND | | - 0.3 to + 6 | V |
| IN, COM, NC, NO[a] | | - 0.3 to (V+ + 0.3) | |
| Continuous Current (NO, NC, COM pins) | | ± 150 | mA |
| Peak Current (Pulsed at 1 ms, 10 % duty cycle) | | ± 300 | |
| Storage Temperature | D Suffix | - 65 to 150 | °C |
| Power Dissipation (Packages)[b] | miniQFN-6[c] | 160 | mW |

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 2 mW/°C above 70 °C.

## SPECIFICATIONS (V+ = 3 V)

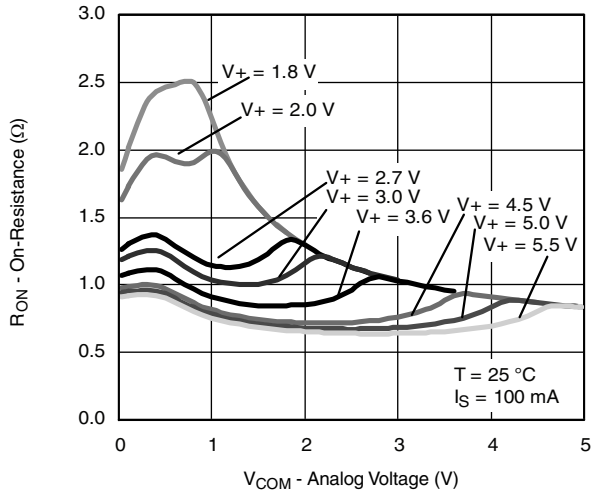
| Parameter | Symbol | Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, $V_{IN}$ = 0.4 V or 2 V[e] | Temp.[a] | Limits - 40 °C to 85 °C Min.[b] | Typ.[c] | Max.[b] | Unit |
|---|---|---|---|---|---|---|---|
| **Analog Switch** | | | | | | | |
| Analog Signal Range[d] | $V_{NO}$, $V_{NC}$, $V_{COM}$ | | Full | 0 | | V+ | V |
| On-Resistance | $R_{ON}$ | V+ = 2.7 V, $V_{COM}$ = 0.5 V/1.5 V, $I_{NO}$, $I_{NC}$ = 100 mA | Room<br>Full | | 1.4 | 1.7<br>1.9 | Ω |
| $R_{ON}$ Match | $\Delta R_{ON}$ | | Room | | | 0.15 | |
| $R_{ON}$ Flatness | $R_{ON}$ Flatness | | Room | | 0.3 | 0.4 | |
| Switch Off Leakage Current[f] | $I_{NO(off)}$<br>$I_{NC(off)}$ | V+ = 3.3 V, $V_{NO}$, $V_{NC}$= 1 V/3 V, $V_{COM}$ = 3 V/1 V | Room<br>Full | - 2<br>- 20 | | 2<br>20 | nA |
| | $I_{COM(off)}$ | | Room<br>Full | - 2<br>- 20 | | 2<br>20 | |
| Channel-On Leakage Current[f] | $I_{COM(on)}$ | V+ = 3.3 V, $V_{NO}$, $V_{NC}$ = $V_{COM}$ = 1 V/3 V | Room<br>Full | - 2<br>- 20 | | 2<br>20 | |
| **Digital Control** | | | | | | | |
| Input High Voltage | $V_{INH}$ | | Full | 1.6 | | | V |
| Input Low Voltage | $V_{INL}$ | | Full | | | 0.4 | |
| Input Capacitance | $C_{in}$ | | Full | | 4 | | pF |
| Input Current | $I_{INL}$ or $I_{INH}$ | $V_{IN}$ = 0 or V+ | Full | 1 | | 1 | µA |
| **Dynamic Characteristics** | | | | | | | |
| Turn-On Time | $t_{ON}$ | V+ = 2.7 V, $V_{NO}$ or $V_{NC}$ = 1.5 V, $R_L$ = 50 Ω, $C_L$ = 35 pF | Room<br>Full | | 18 | 43<br>49 | ns |
| Turn-Off Time | $t_{OFF}$ | | Room<br>Full | | 7 | 32<br>34 | |
| Break-Before-Make Time | $t_{BBM}$ | | Room | 1 | 12 | | |
| Charge Injection[d] | $Q_{INJ}$ | $C_L$ = 1 nF, $V_{GEN}$ = 0 V, $R_{GEN}$ = 0 Ω | Room | | 3 | | pC |
| Off-Isolation[d] | OIRR | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz | Room | | - 58 | | dB |
| Crosstalk[d] | $X_{TALK}$ | | Room | | - 64 | | |
| $N_O$, $N_C$ Off Capacitance[d] | $C_{NO(off)}$<br>$C_{NC(off)}$ | $V_{IN}$ = 0 or V+, f = 1 MHz | Room | | 21 | | pF |
| Channel-On Capacitance[d] | $C_{ON}$ | | Room | | 61 | | |
| **Power Supply** | | | | | | | |
| Power Supply Range | V+ | | | 1.8 | | 5.5 | V |
| Power Supply Current | I+ | $V_{IN}$ = 0 or V+ | | | 0.01 | 1 | µA |

| **SPECIFICATIONS** (V+ = 5 V) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Conditions Otherwise Unless Specified** V+ = 5 V, ± 10 %, $V_{IN}$ = 0.6 V or 1.8 V[e] | **Temp.[a]** | **Limits - 40 °C to 85 °C Min.[b]** | **Typ.[c]** | **Max.[b]** | **Unit** |
| **Analog Switch** | | | | | | | |
| Analog Signal Range[d] | $V_{NO}$, $V_{NC}$, $V_{COM}$ | | Full | 0 | | V+ | V |
| On-Resistance | $R_{ON}$ | V+ = 4.5 V, $V_{COM}$ = 0.5 V/2.5 V, $I_{NO}$, $I_{NC}$ = 100 mA | Room<br>Full | | 1 | 1.3<br>1.45 | Ω |
| $R_{ON}$ Match | $\Delta R_{ON}$ | | Room | | | 0.15 | |
| $R_{ON}$ Flatness | $R_{ON}$ Flatness | | Room | | 0.3 | 0.4 | |
| Switch Off Leakage Current | $I_{NO(off)}$<br>$I_{NC(off)}$ | V+ = 5.5 V, $V_{NO}$, $V_{NC}$= 1 V/4.5 V, $V_{COM}$ = 4.5 V/1 V | Room<br>Full | - 2<br>- 20 | | 2<br>20 | nA |
| | $I_{COM(off)}$ | | Room<br>Full | - 2<br>- 20 | | 2<br>20 | |
| Channel-On Leakage Current | $I_{COM(on)}$ | V+ = 5.5 V, $V_{NO}$, $V_{NC}$ = $V_{COM}$ = 1 V/4.5 V | Room<br>Full | - 2<br>- 20 | | 2<br>20 | |
| **Digital Control** | | | | | | | |
| Input High Voltage | $V_{INH}$ | | Full | 1.8 | | | V |
| Input Low Voltage | $V_{INL}$ | | Full | | | 0.6 | |
| Input Capacitance | $C_{in}$ | | Full | | 4 | | pF |
| Input Current | $I_{INL}$ or $I_{INH}$ | $V_{IN}$ = 0 or V+ | Full | 1 | | 1 | µA |
| **Dynamic Characteristics** | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{NO}$ or $V_{NC}$ = 2.5 V, $R_L$ = 50 Ω, $C_L$ = 35 pF | Room<br>Full | | 11 | 35<br>39 | ns |
| Turn-Off Time | $t_{OFF}$ | | Room<br>Full | | 6 | 31<br>33 | |
| Break-Before-Make Time | $t_{BBM}$ | | Room | 1 | 5 | | |
| Charge Injection[d] | $Q_{INJ}$ | $C_L$ = 1 nF, $V_{GEN}$ = 0 V, $R_{GEN}$ = 0 Ω | Room | | 14 | | pC |
| Off-Isolation[d] | OIRR | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz | Room | | - 58 | | dB |
| Crosstalk[d] | $X_{TALK}$ | | Room | | - 64 | | |
| $N_O$, $N_C$ Off Capacitance[d] | $C_{NO(off)}$<br>$C_{NC(off)}$ | $V_{IN}$ = 0 or V+, f = 1 MHz | Room | | 19 | | pF |
| Channel-On Capacitance[d] | $C_{ON}$ | | Room | | 61 | | |
| **Power Supply** | | | | | | | |
| Power Supply Range | V+ | $V_{IN}$ = 0 or V+ | | 1.8 | | 5.5 | V |
| Power Supply Current | I+ | | | | 0.01 | 1 | µA |

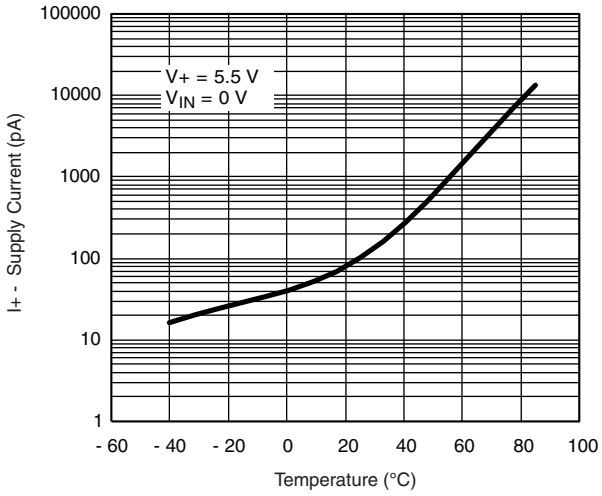
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, nor subjected to production test.
e. $V_{IN}$ = input voltage to perform proper function.
f. Guaranteed by 5 V leakage testing, not production tested.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

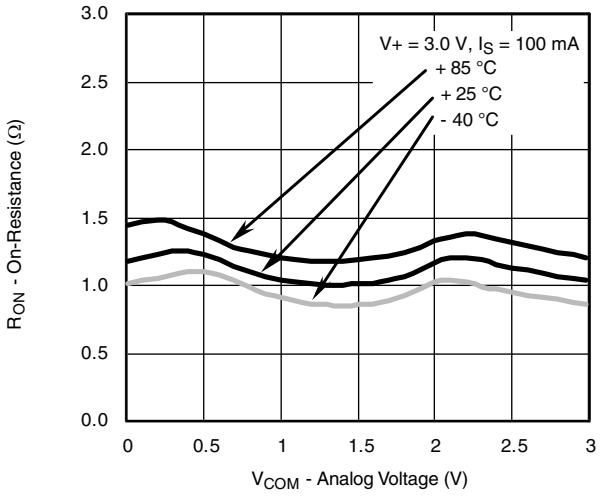
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



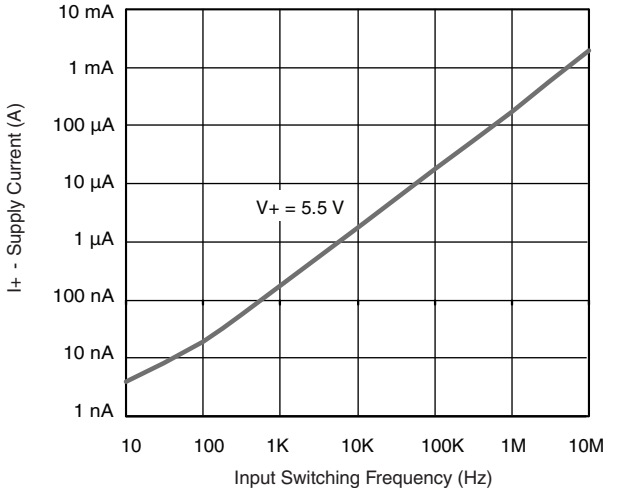

**$R_{ON}$ vs. $V_{COM}$ and Supply Voltage**



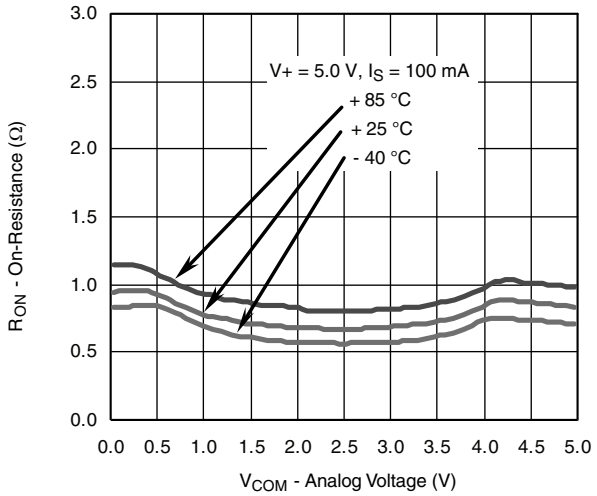

**Supply Current vs. Temperature**



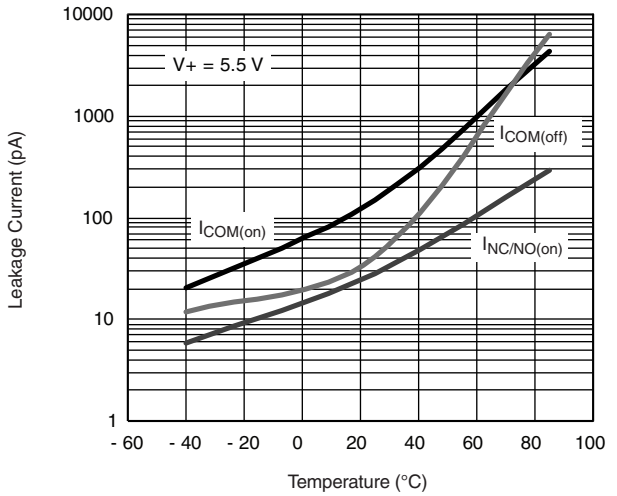

**$R_{ON}$ vs. Analog Voltage and Temperature**




**Supply Current vs. Input Switching Frequency**

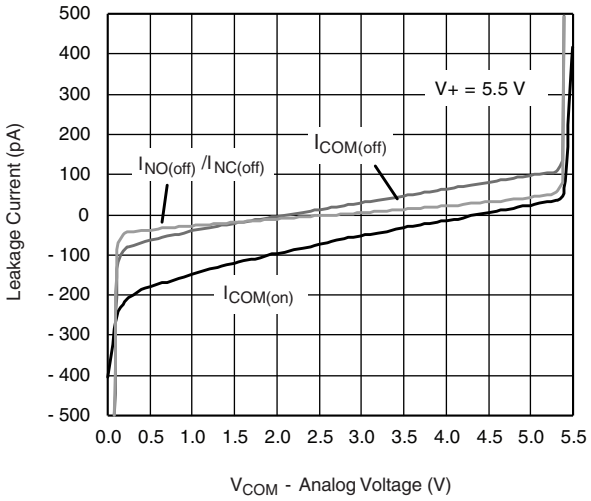



**$R_{ON}$ vs. Analog Voltage and Temperature**

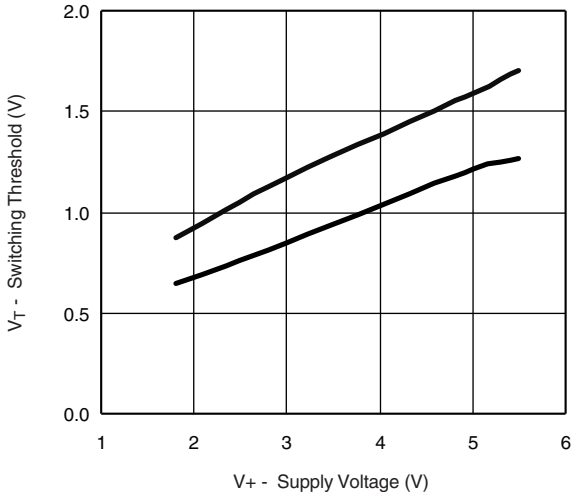



**Leakage Current vs. Temperature**

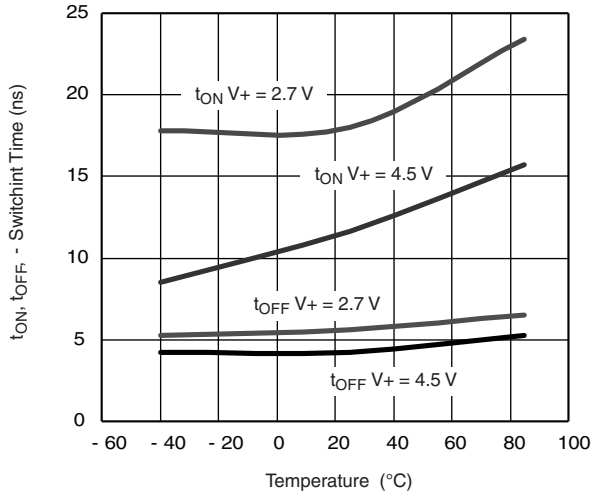
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



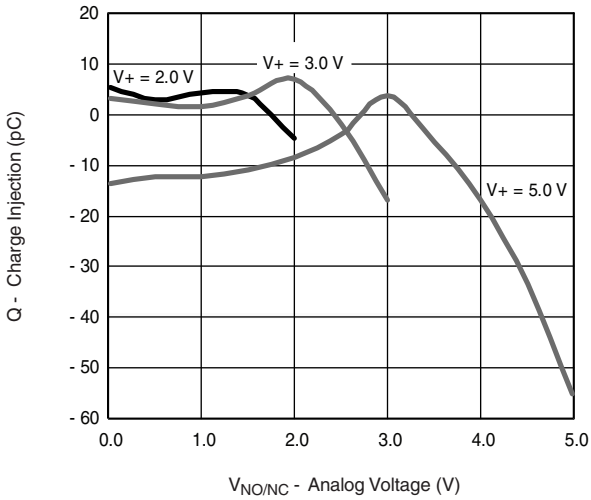

**Leakage vs. Analog Voltage**



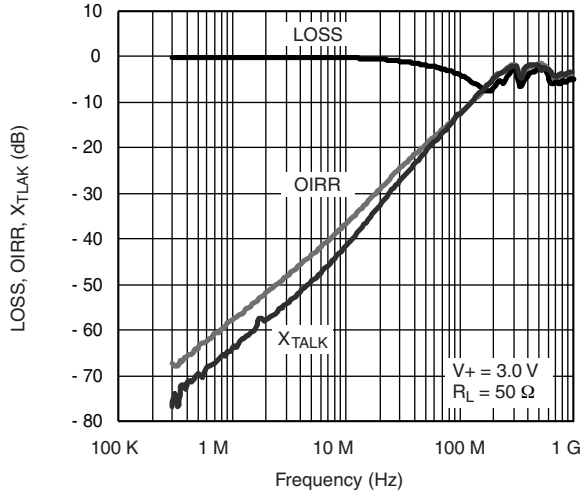

**Switching Threshold vs. Supply Voltage**




**Switching Time vs. Temperature and Supply Voltage**

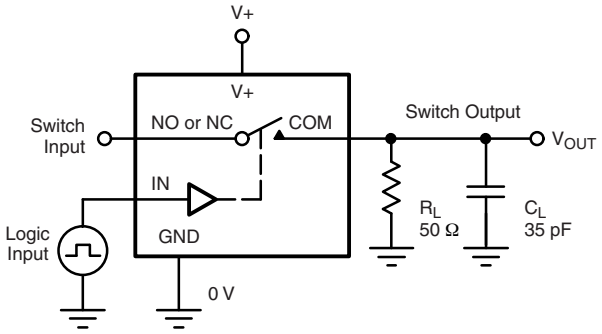



**Charge Injection vs. Analog Voltage**



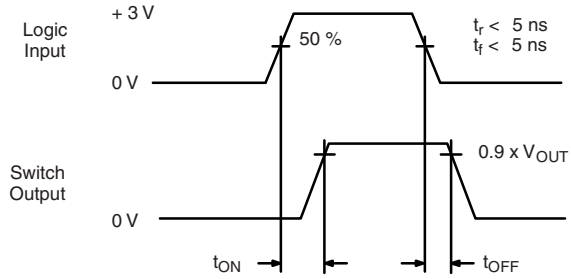

**Insertion Loss, Off-Isolation, Crosstalk vs. Frequency**

## TEST CIRCUITS



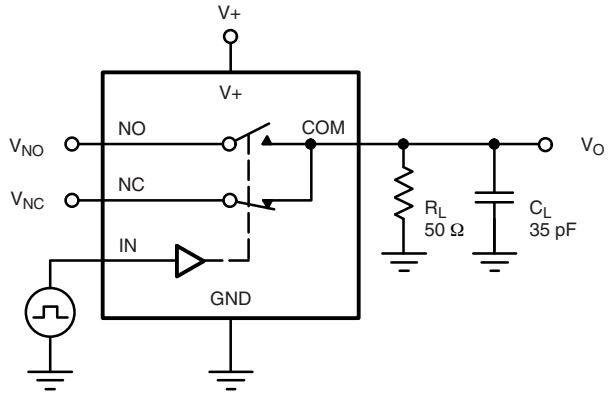

$C_L$ (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$




Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

**Figure 1. Switching Time**




$C_L$ (includes fixture and stray capacitance)

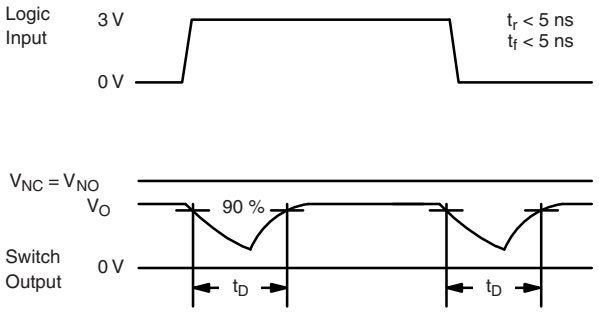
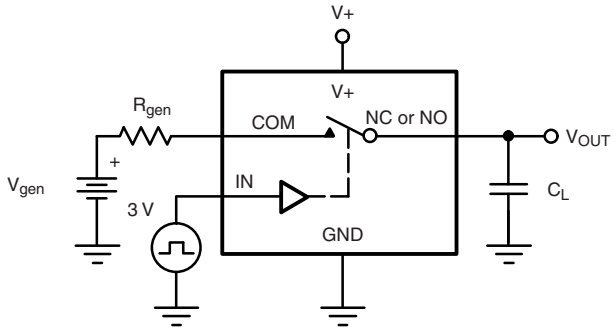
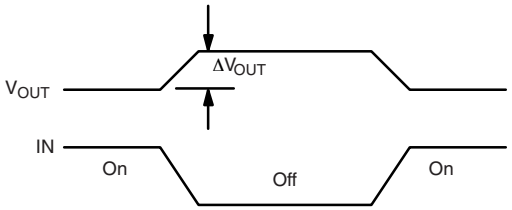



**Figure 2. Break-Before-Make Interval**




$$Q = \Delta V_{OUT} \times C_L$$

IN depends on switch configuration: input polarity determined by sense of switch.

**Figure 3. Charge Injection**

## TEST CIRCUITS

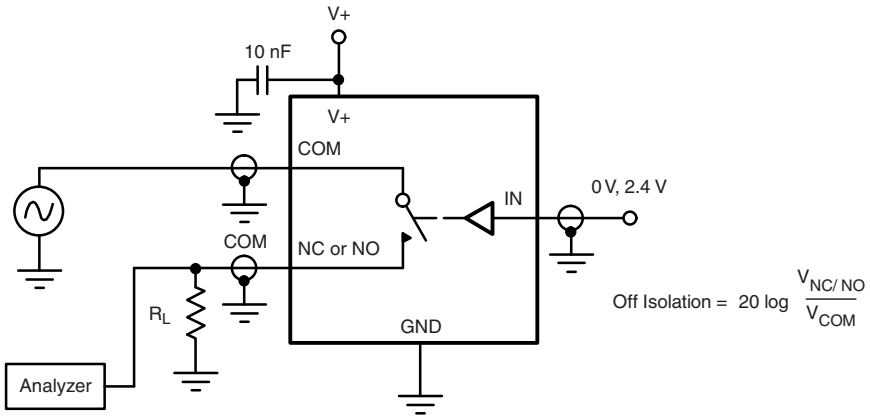



**Figure 4. Off-Isolation**

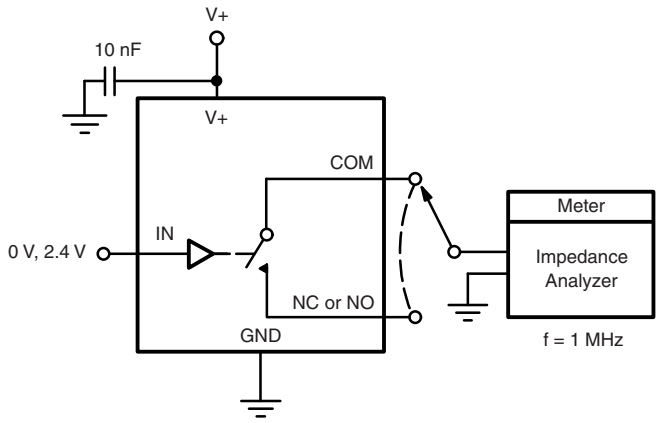
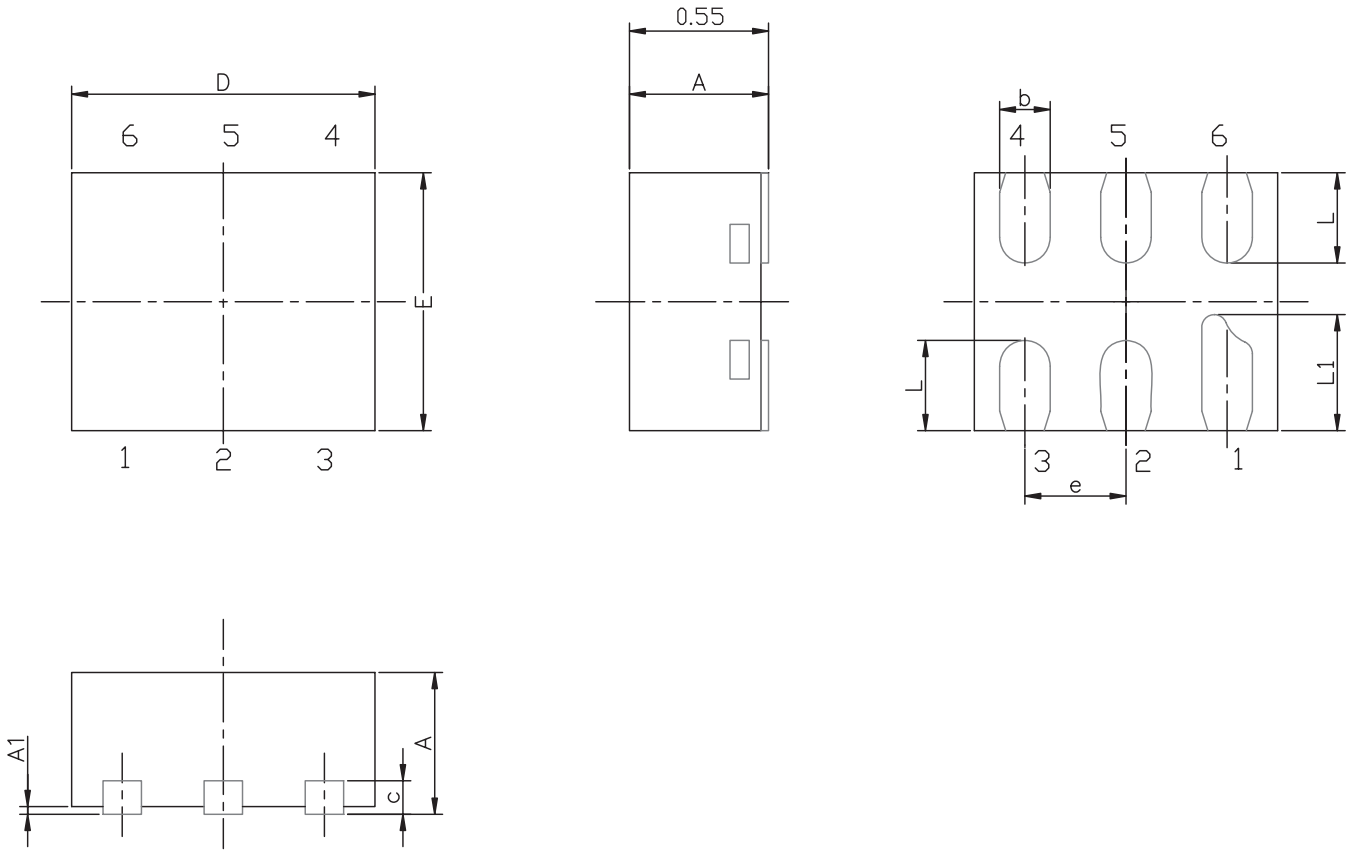



**Figure 5. Channel Off/On Capacitance**

## MINI QFN-6L CASE OUTLINE




| DIM | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN. | NAM. | MAX. | MIN. | NAM. | MAX. |
| A | 0.50 | 0.55 | 0.60 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.00 | - | 0.05 | 0.000 | - | 0.002 |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| c | 0.15 REF | | | 0.006 REF | | |
| D | 1.15 | 1.20 | 1.25 | 0.045 | 0.047 | 0.049 |
| E | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| e | 0.40 BSC | | | 0.016 BSC | | |
| L | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| L1 | 0.40 | 0.45 | 0.50 | 0.016 | 0.018 | 0.020 |

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DWG: 5958

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