

# NCS2001

## 0.9 V, Rail-to-Rail, Single Operational Amplifier

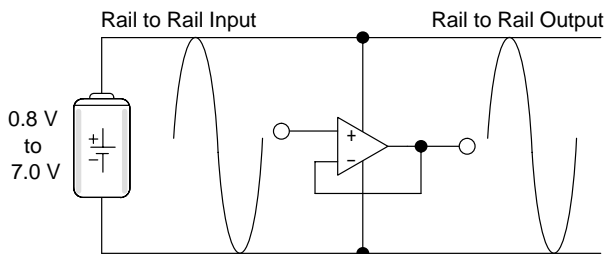
The NCS2001 is an industry first sub-one volt operational amplifier that features a rail-to-rail common mode input voltage range, along with rail-to-rail output drive capability. This amplifier is guaranteed to be fully operational down to 0.9 V, providing an ideal solution for powering applications from a single cell Nickel Cadmium (NiCd) or Nickel Metal Hydride (NiMH) battery. Additional features include no output phase reversal with overdriven inputs, trimmed input offset voltage of 0.5 mV, extremely low input bias current of 40 pA, and a unity gain bandwidth of 1.4 MHz at 5.0 V. The tiny NCS2001 is the ideal solution for small portable electronic applications and is available in the space saving SOT23-5 and SC70-5 packages with two industry standard pinouts.

### Features

- 0.9 V Guaranteed Operation
- Rail-to-Rail Common Mode Input Voltage Range
- Rail-to-Rail Output Drive Capability
- No Output Phase Reversal for Over-Driven Input Signals
- 0.5 mV Trimmed Input Offset
- 10 pA Input Bias Current
- 1.4 MHz Unity Gain Bandwidth at  $\pm 2.5$  V, 1.1 MHz at  $\pm 0.5$  V
- Tiny SC70-5 and SOT23-5 Packages

### Typical Applications

- Single Cell NiCd/NiMH Battery Powered Applications
- Cellular Telephones
- Pagers
- Personal Digital Assistants
- Electronic Games
- Digital Cameras
- Camcorders
- Hand Held Instruments



This device contains 63 active transistors.

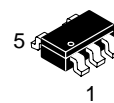
**Figure 1. Typical Application**



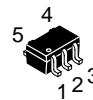
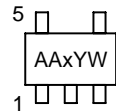
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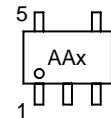
### MARKING DIAGRAMS



**SOT23-5**  
(TSOP-5/SC59-5)  
SN SUFFIX  
CASE 483

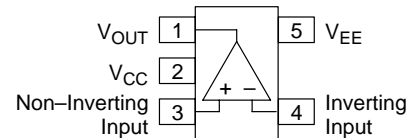


**SC70-5**  
(SC-88A / SOT-353)  
SQ SUFFIX  
CASE 419A

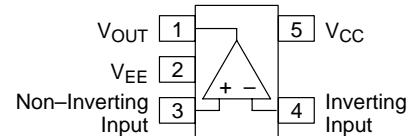


x = G for SN1      Y = Year  
H for SN2      W = Work Week  
I for SQ1  
J for SQ2

### PIN CONNECTIONS



Style 1 Pinout (SN1T1, SQ1T1)



Style 2 Pinout (SN2T1, SQ2T1)

### ORDERING INFORMATION

See detailed ordering and shipping information in the dimensions section on page 15 of this data sheet.

# NCS2001

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage ( $V_{CC}$ to $V_{EE}$ )	$V_S$	7.0	V
Input Differential Voltage Range (Note 1)	$V_{IDR}$	$V_{EE} - 300$ mV to 7.0 V	V
Input Common Mode Voltage Range (Note 1)	$V_{ICR}$	$V_{EE} - 300$ mV to 7.0 V	V
Output Short Circuit Duration (Note 2)	$t_{Sc}$	Indefinite	sec
Junction Temperature	$T_J$	150	°C
Power Dissipation and Thermal Characteristics			
SOT23-5 Package			
Thermal Resistance, Junction to Air	$R_{\theta JA}$	235	°C/W
Power Dissipation @ $T_A = 70^\circ\text{C}$	$P_D$	340	mW
SC70-5 Package			
Thermal Resistance, Junction to Air	$R_{\theta JA}$	280	°C/W
Power Dissipation @ $T_A = 70^\circ\text{C}$	$P_D$	286	mW
Storage Temperature Range	$T_{stg}$	-65 to 150	°C
ESD Protection at any Pin Human Body Model (Note 3)	$V_{ESD}$	2000	V

1. Either or both inputs should not exceed the range of  $V_{EE} - 300$  mV to  $V_{EE} + 7.0$  V.
2. Maximum package power dissipation limits must be observed to ensure that the maximum junction temperature is not exceeded.  
 $T_J = T_A + (P_D R_{\theta JA})$
3. ESD data available upon request.

## DC ELECTRICAL CHARACTERISTICS

( $V_{CC} = 2.5$  V,  $V_{EE} = -2.5$  V,  $V_{CM} = V_O = 0$  V,  $R_L$  to Gnd,  $T_A = 25^\circ\text{C}$  unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage $V_{CC} = 0.45$ V, $V_{EE} = -0.45$ V $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $105^\circ\text{C}$ $V_{CC} = 1.5$ V, $V_{EE} = -1.5$ V $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $105^\circ\text{C}$ $V_{CC} = 2.5$ V, $V_{EE} = -2.5$ V $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $105^\circ\text{C}$	$V_{IO}$	-6.0 -8.5 -9.5	0.5 - -	6.0 8.5 9.5	mV
Input Offset Voltage Temperature Coefficient ( $R_S = 50$ ) $T_A = -40^\circ\text{C}$ to $105^\circ\text{C}$	$\Delta V_{IO}/\Delta T$	-	8.0	-	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ( $V_{CC} = 1.0$ V to 5.0 V)	$I_{IB}$	-	10	-	pA
Input Common Mode Voltage Range	$V_{ICR}$	-	$V_{EE}$ to $V_{CC}$	-	V
Large Signal Voltage Gain $V_{CC} = 0.45$ V, $V_{EE} = -0.45$ V $R_L = 10$ k $R_L = 2.0$ k $V_{CC} = 1.5$ V, $V_{EE} = -1.5$ V $R_L = 10$ k $R_L = 2.0$ k $V_{CC} = 2.5$ V, $V_{EE} = -2.5$ V $R_L = 10$ k $R_L = 2.0$ k	$A_{VOL}$	- - - - 20 15	40 20 40 40 40 40	- - - - - -	kV/V

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## DC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = 2.5\text{ V}$ ,  $V_{EE} = -2.5\text{ V}$ ,  $V_{CM} = V_O = 0\text{ V}$ ,  $R_L$  to Gnd,  $T_A = 25^\circ\text{C}$  unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage Swing, High State Output ( $V_{ID} = +0.5\text{ V}$ )	$V_{OH}$				V
$V_{CC} = 0.45\text{ V}$ , $V_{EE} = -0.45\text{ V}$					
$T_A = 25^\circ\text{C}$					
$R_L = 10\text{ k}$		0.40	0.494	–	
$R_L = 2.0\text{ k}$		0.35	0.466	–	
$T_A = 0^\circ\text{C to } 70^\circ\text{C}$					
$R_L = 10\text{ k}$		0.40	–	–	
$R_L = 2.0\text{ k}$		0.35	–	–	
$T_A = -40^\circ\text{C to } 105^\circ\text{C}$					
$R_L = 10\text{ k}$		0.40	–	–	
$R_L = 2.0\text{ k}$		0.35	–	–	
$V_{CC} = 1.5\text{ V}$ , $V_{EE} = -1.5\text{ V}$					
$T_A = 25^\circ\text{C}$					
$R_L = 10\text{ k}$		1.45	1.498	–	
$R_L = 2.0\text{ k}$		1.40	1.480	–	
$T_A = 0^\circ\text{C to } 70^\circ\text{C}$					
$R_L = 10\text{ k}$		1.45	–	–	
$R_L = 2.0\text{ k}$		1.40	–	–	
$T_A = -40^\circ\text{C to } 105^\circ\text{C}$					
$R_L = 10\text{ k}$		1.45	–	–	
$R_L = 2.0\text{ k}$		1.40	–	–	
$V_{CC} = 2.5\text{ V}$ , $V_{EE} = -2.5\text{ V}$					
$T_A = 25^\circ\text{C}$					
$R_L = 10\text{ k}$		2.45	2.498	–	
$R_L = 2.0\text{ k}$		2.40	2.475	–	
$T_A = 0^\circ\text{C to } 70^\circ\text{C}$					
$R_L = 10\text{ k}$		2.45	–	–	
$R_L = 2.0\text{ k}$		2.40	–	–	
$T_A = -40^\circ\text{C to } 105^\circ\text{C}$					
$R_L = 10\text{ k}$		2.45	–	–	
$R_L = 2.0\text{ k}$		2.40	–	–	
Output Voltage Swing, Low State Output ( $V_{ID} = -0.5\text{ V}$ )	$V_{OL}$				V
$V_{CC} = 0.45\text{ V}$ , $V_{EE} = -0.45\text{ V}$					
$T_A = 25^\circ\text{C}$					
$R_L = 10\text{ k}$		–	–0.494	–0.40	
$R_L = 2.0\text{ k}$		–	–0.480	–0.35	
$T_A = 0^\circ\text{C to } 70^\circ\text{C}$					
$R_L = 10\text{ k}$		–	–	–0.40	
$R_L = 2.0\text{ k}$		–	–	–0.35	
$T_A = -40^\circ\text{C to } 105^\circ\text{C}$					
$R_L = 10\text{ k}$		–	–	–0.40	
$R_L = 2.0\text{ k}$		–	–	–0.35	
$V_{CC} = 1.5\text{ V}$ , $V_{EE} = -1.5\text{ V}$					
$T_A = 25^\circ\text{C}$					
$R_L = 10\text{ k}$		–	–1.493	–1.45	
$R_L = 2.0\text{ k}$		–	–1.480	–1.40	
$T_A = 0^\circ\text{C to } 70^\circ\text{C}$					
$R_L = 10\text{ k}$		–	–	–1.45	
$R_L = 2.0\text{ k}$		–	–	–1.40	
$T_A = -40^\circ\text{C to } 105^\circ\text{C}$					
$R_L = 10\text{ k}$		–	–	–1.45	
$R_L = 2.0\text{ k}$		–	–	–1.40	
$V_{CC} = 2.5\text{ V}$ , $V_{EE} = -2.5\text{ V}$					
$T_A = 25^\circ\text{C}$		–			
$R_L = 10\text{ k}$		–	–2.492	–2.45	
$R_L = 2.0\text{ k}$		–	–2.479	–2.40	
$T_A = 0^\circ\text{C to } 70^\circ\text{C}$					
$R_L = 10\text{ k}$		–	–	–2.45	
$R_L = 2.0\text{ k}$		–	–	–2.40	
$T_A = -40^\circ\text{C to } 105^\circ\text{C}$					
$R_L = 10\text{ k}$		–	–	–2.45	
$R_L = 2.0\text{ k}$		–	–	–2.40	

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## DC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = 2.5\text{ V}$ ,  $V_{EE} = -2.5\text{ V}$ ,  $V_{CM} = V_O = 0\text{ V}$ ,  $R_L$  to Gnd,  $T_A = 25^\circ\text{C}$  unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Common Mode Rejection Ratio ( $V_{in} = 0$ to $5.0\text{ V}$ )	CMRR	60	70	–	dB
Power Supply Rejection Ratio ( $V_{CC} = 0.5\text{ V}$ to $2.5\text{ V}$ , $V_{EE} = -2.5\text{ V}$ )	PSRR	55	65	–	dB
Output Short Circuit Current $V_{CC} = 0.45\text{ V}$ , $V_{EE} = -0.45\text{ V}$ , $V_{ID} = \pm 0.4\text{ V}$ Source Current High Output State Sink Current Low Output State $V_{CC} = 1.5\text{ V}$ , $V_{EE} = -1.5\text{ V}$ , $V_{ID} = \pm 0.5\text{ V}$ Source Current High Output State Sink Current Low Output State $V_{CC} = 2.5\text{ V}$ , $V_{EE} = -2.5\text{ V}$ , $V_{ID} = \pm 0.5\text{ V}$ Source Current High Output State Sink Current Low Output State	$I_{sc}$	0.5 – 15 – 40 –	1.2 –3.0 29 –40 76 –96	– –1.5 – –20 – –50	mA
Power Supply Current (Per Amplifier, $V_O = 0\text{ V}$ ) $V_{CC} = 0.45\text{ V}$ , $V_{EE} = -0.45\text{ V}$ $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $105^\circ\text{C}$ $V_{CC} = 1.5\text{ V}$ , $V_{EE} = -1.5\text{ V}$ $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $105^\circ\text{C}$ $V_{CC} = 2.5\text{ V}$ , $V_{EE} = -2.5\text{ V}$ $T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $105^\circ\text{C}$	$I_D$	– – – – – – – –	0.51 – – 0.72 – – – 0.82 – – –	1.10 1.10 1.10 1.40 1.40 1.40 1.50 1.50 1.50	mA

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = 2.5\text{ V}$ ,  $V_{EE} = -2.5\text{ V}$ ,  $V_{CM} = V_O = 0\text{ V}$ ,  $R_L$  to Gnd,  $T_A = 25^\circ\text{C}$  unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Differential Input Resistance ( $V_{CM} = 0\text{ V}$ )	$R_{in}$	–	> 1.0	–	tera $\Omega$
Differential Input Capacitance ( $V_{CM} = 0\text{ V}$ )	$C_{in}$	–	3.0	–	pF
Equivalent Input Noise Voltage ( $f = 1.0\text{ kHz}$ )	$e_n$	–	100	–	nV/ $\sqrt{\text{Hz}}$
Gain Bandwidth Product ( $f = 100\text{ kHz}$ ) $V_{CC} = 0.45\text{ V}$ , $V_{EE} = -0.45\text{ V}$ $V_{CC} = 1.5\text{ V}$ , $V_{EE} = -1.5\text{ V}$ $V_{CC} = 2.5\text{ V}$ , $V_{EE} = -2.5\text{ V}$	GBW	– – 0.5	1.1 1.3 1.4	– – –	MHz
Gain Margin ( $R_L = 10\text{ k}$ , $C_L = 5.0\text{ pf}$ )	$A_m$	–	6.5	–	dB
Phase Margin ( $R_L = 10\text{ k}$ , $C_L = 5.0\text{ pf}$ )	$\phi_m$	–	60	–	Deg
Power Bandwidth ( $V_O = 4.0\text{ Vpp}$ , $R_L = 2.0\text{ k}$ , THD = 1.0%, $A_V = 1.0$ )	BW <sub>P</sub>	–	80	–	kHz
Total Harmonic Distortion ( $V_O = 4.0\text{ Vpp}$ , $R_L = 2.0\text{ k}$ , $A_V = 1.0$ ) $f = 1.0\text{ kHz}$ $f = 10\text{ kHz}$	THD	– –	0.008 0.08	– –	%
Slew Rate ( $V_S = \pm 2.5\text{ V}$ , $V_O = -2.0\text{ V}$ to $2.0\text{ V}$ , $R_L = 2.0\text{ k}$ , $A_V = 1.0$ ) Positive Slope Negative Slope	SR	1.0 1.0	1.6 1.6	6.0 6.0	V/ $\mu\text{s}$

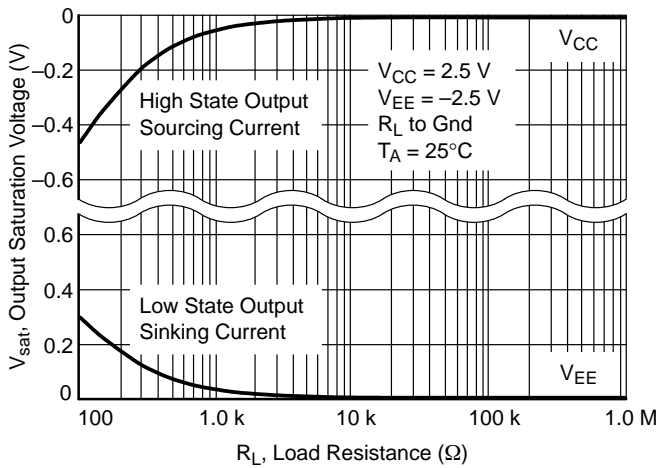


Figure 2. Split Supply Output Saturation vs. Load Resistance

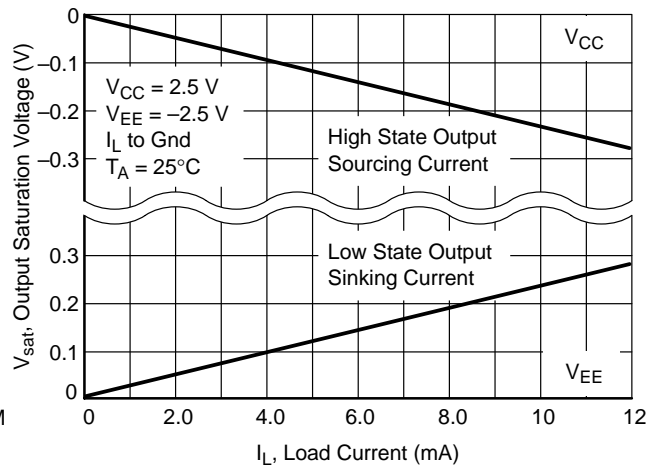


Figure 3. Split Supply Output Saturation vs. Load Current

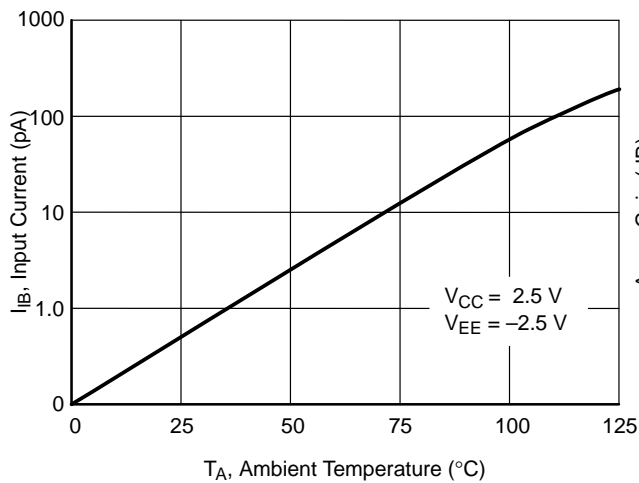


Figure 4. Input Bias Current vs. Temperature

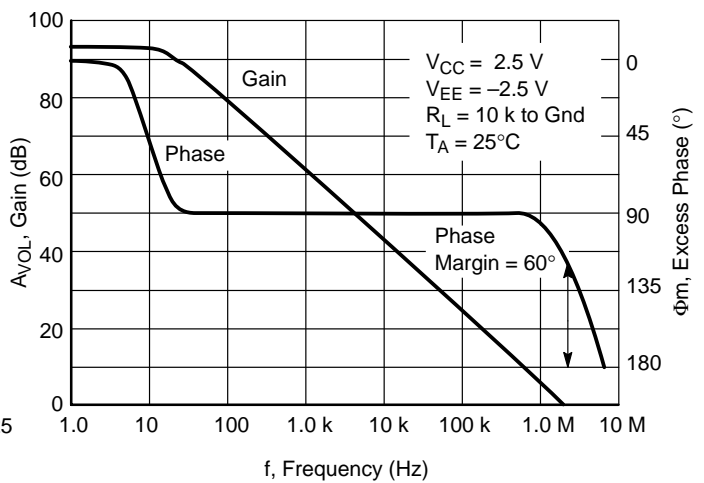


Figure 5. Gain and Phase vs. Frequency

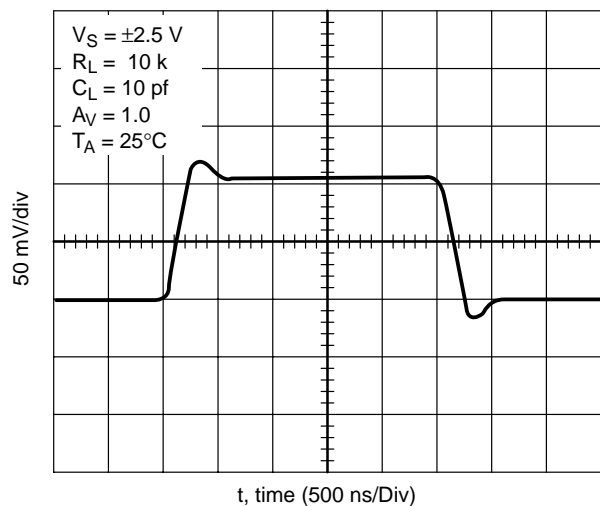


Figure 6. Transient Response

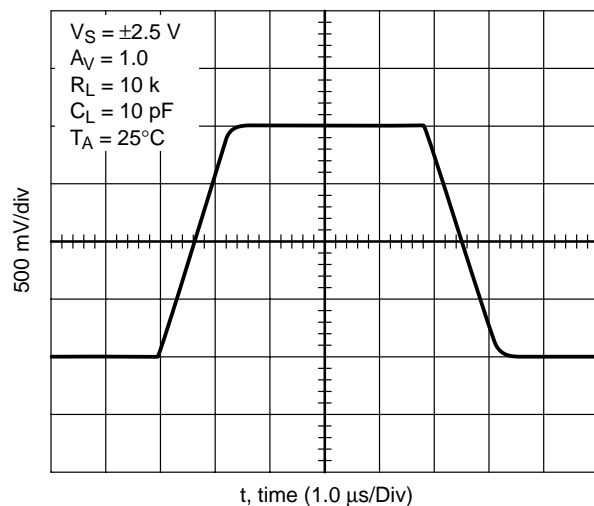


Figure 7. Slew Rate

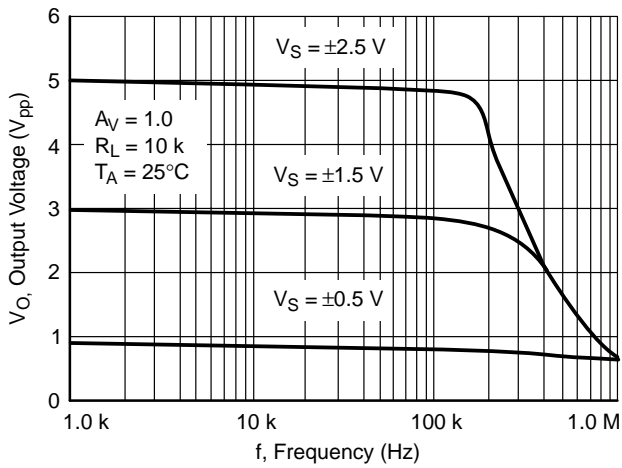


Figure 8. Output Voltage vs. Frequency

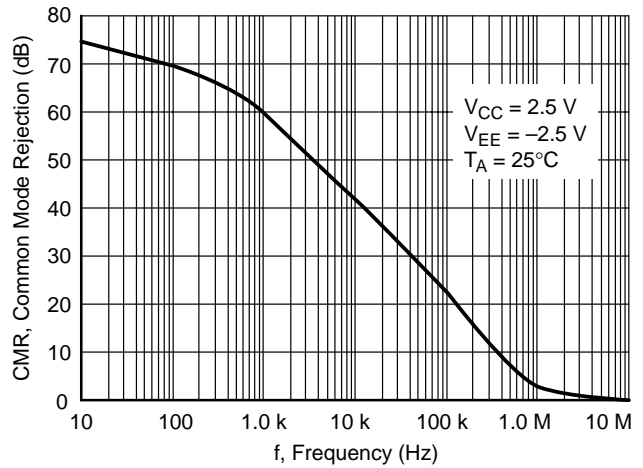


Figure 9. Common Mode Rejection vs. Frequency

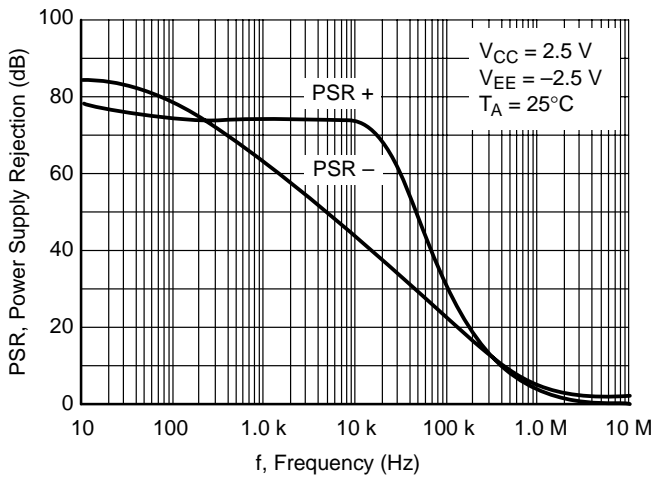


Figure 10. Power Supply Rejection vs. Frequency

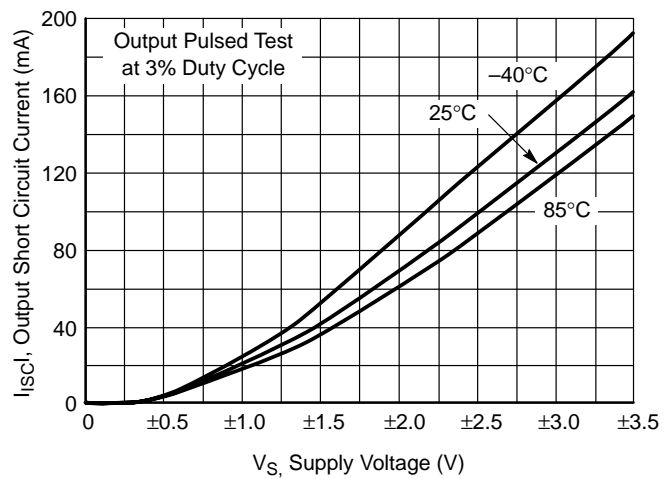


Figure 11. Output Short Circuit Sinking Current vs. Supply Voltage

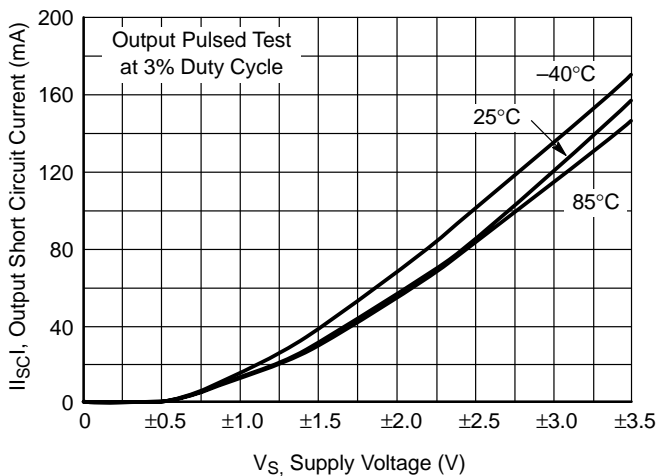


Figure 12. Output Short Circuit Sourcing Current vs. Supply Voltage

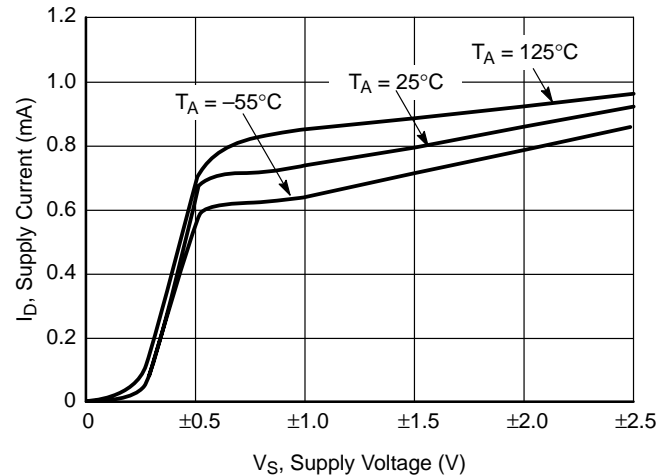


Figure 13. Supply Current vs. Supply Voltage

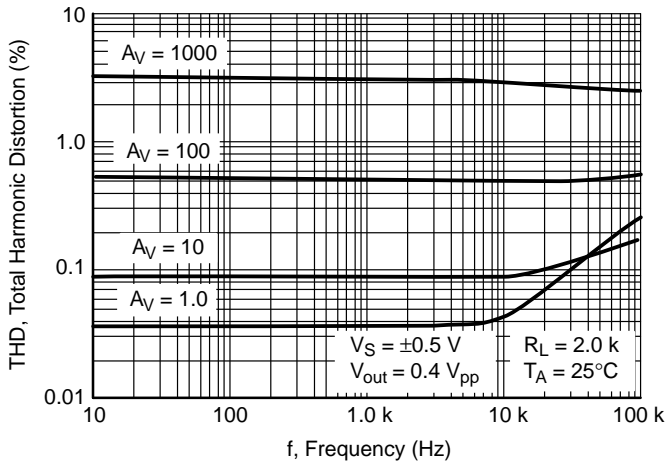


Figure 14. Total Harmonic Distortion vs. Frequency with 1.0 V Supply

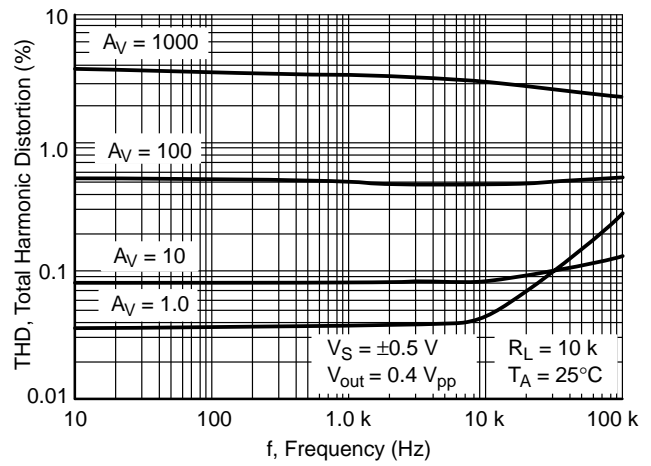


Figure 15. Total Harmonic Distortion vs. Frequency with 1.0 V Supply

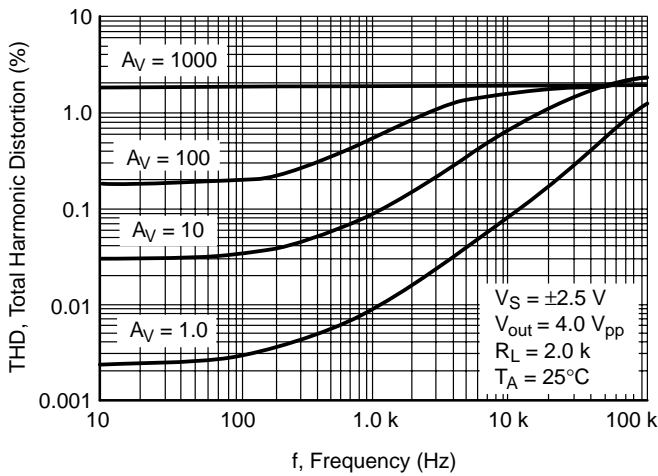


Figure 16. Total Harmonic Distortion vs. Frequency with 5.0 V Supply

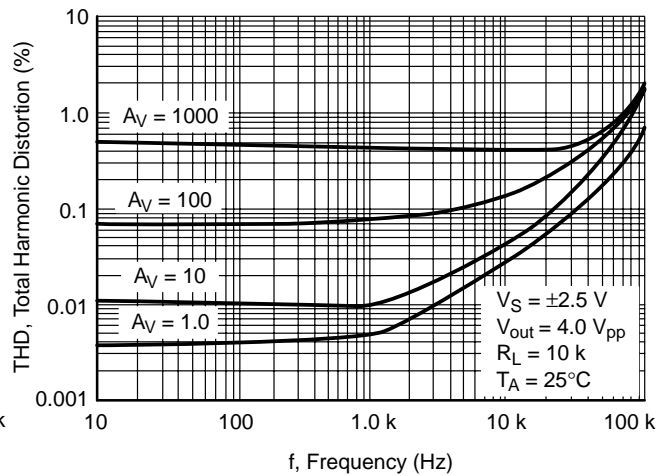


Figure 17. Total Harmonic Distortion vs. Frequency with 5.0 V Supply

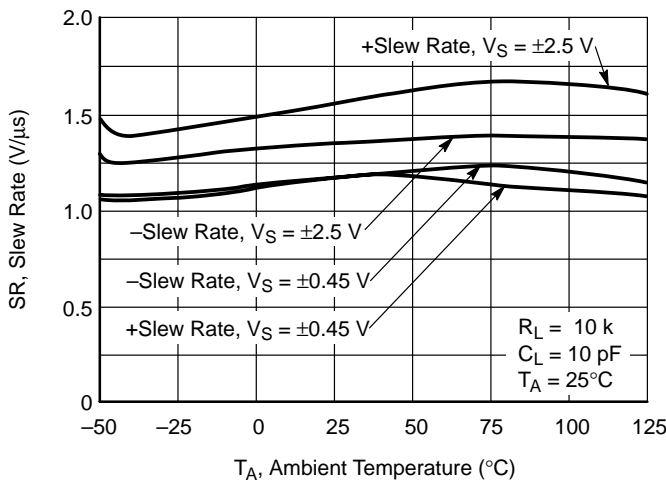


Figure 18. Slew Rate vs. Temperature

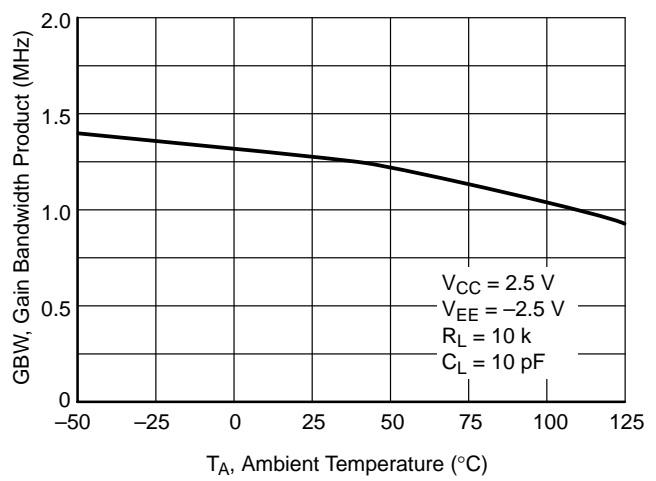


Figure 19. Gain Bandwidth Product vs. Temperature

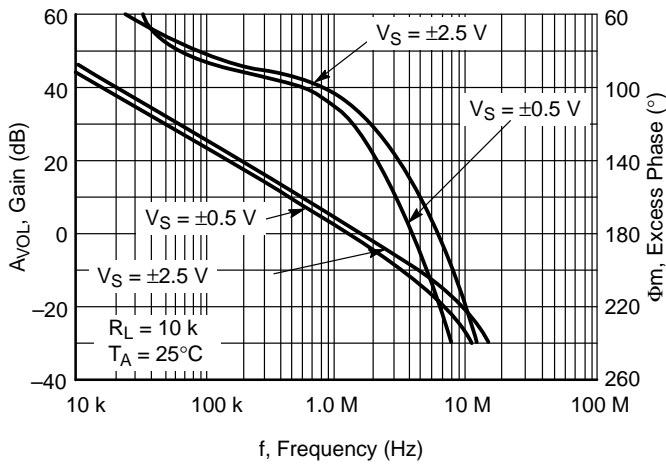


Figure 20. Voltage Gain and Phase vs. Frequency

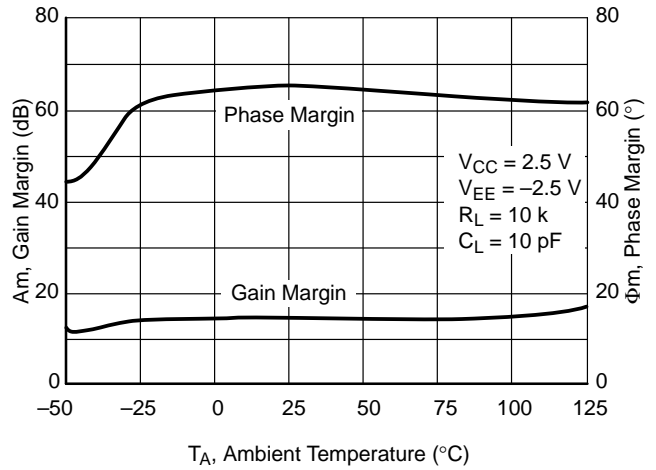


Figure 21. Gain and Phase Margin vs. Temperature

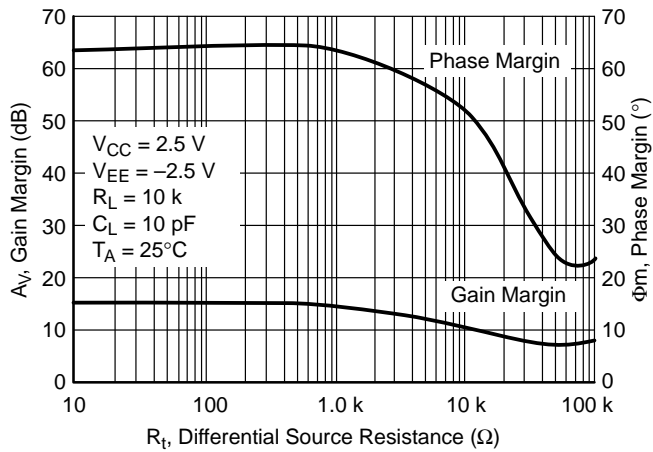


Figure 22. Gain and Phase Margin vs. Differential Source Resistance

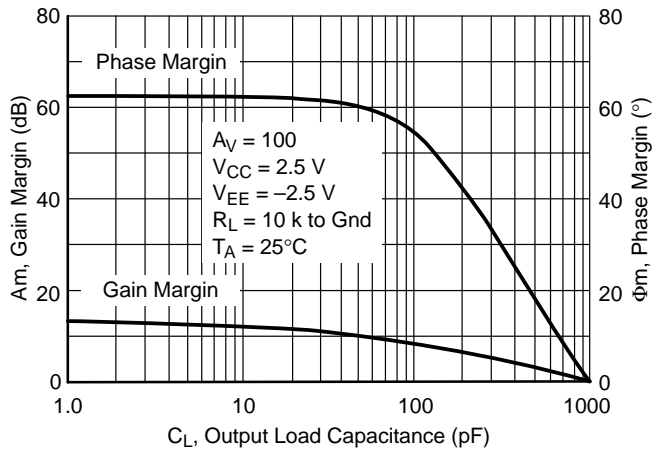


Figure 23. Gain and Phase Margin vs. Output Load Capacitance

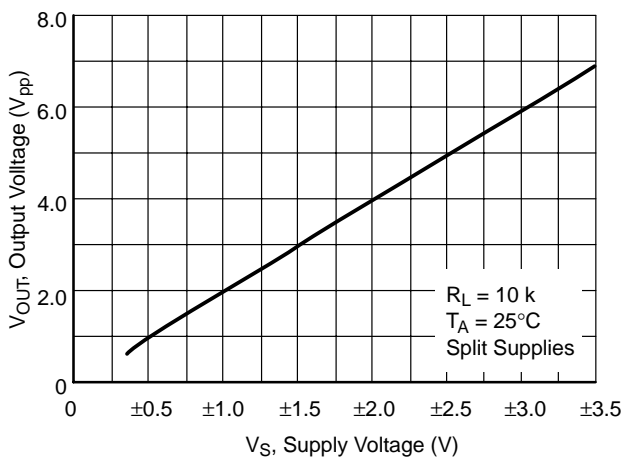


Figure 24. Output Voltage Swing vs. Supply Voltage

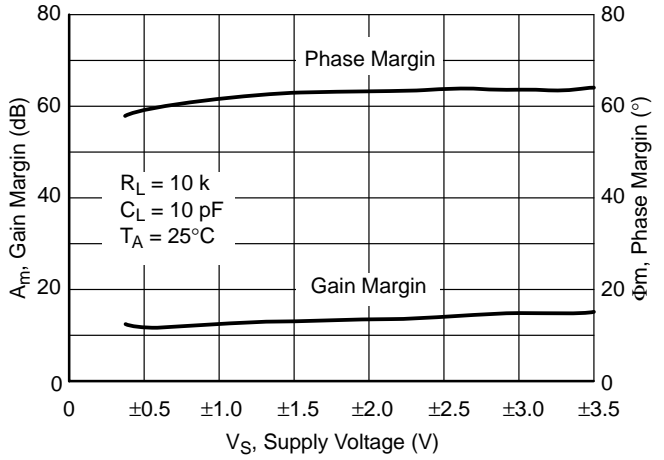


Figure 25. Gain and Phase Margin vs. Supply Voltage



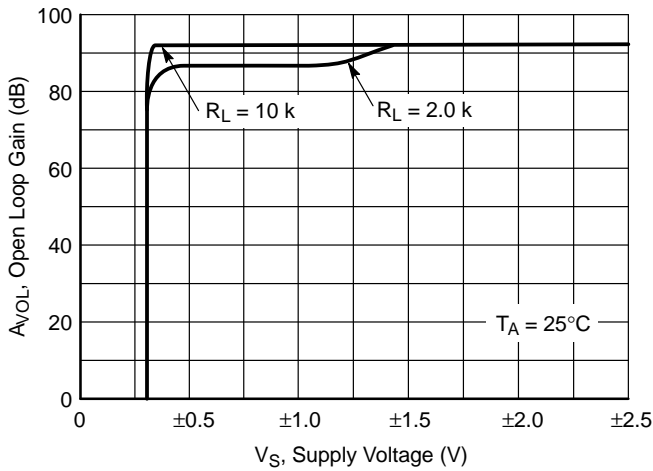


Figure 26. Open Loop Voltage Gain vs. Supply Voltage

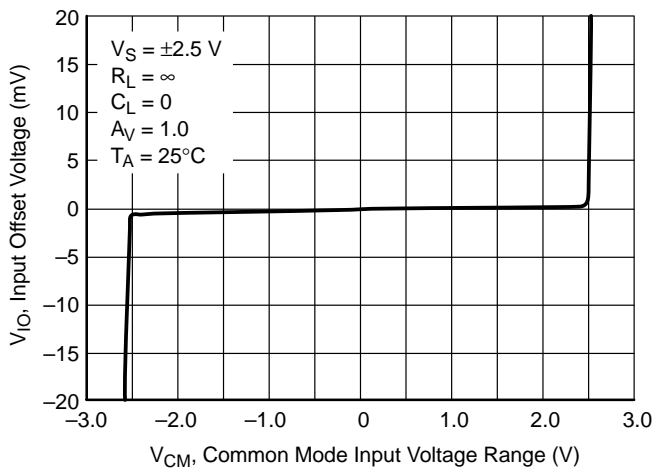


Figure 27. Input Offset Voltage vs. Common Mode Input Voltage Range  $V_S = \pm 2.5$  V

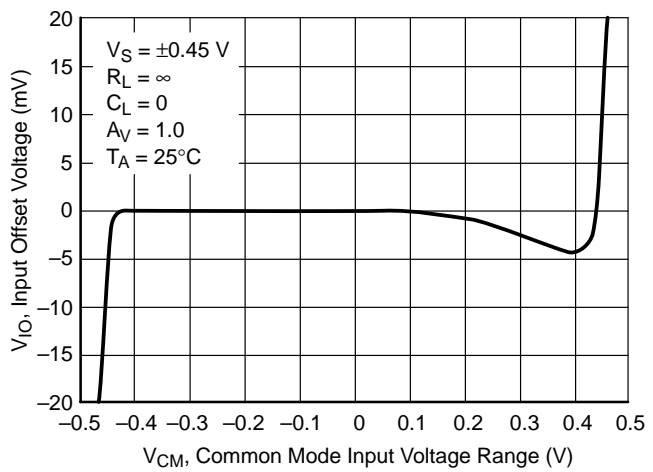


Figure 28. Input Offset Voltage vs. Common Mode Input Voltage Range,  $V_S = \pm 0.45$  V

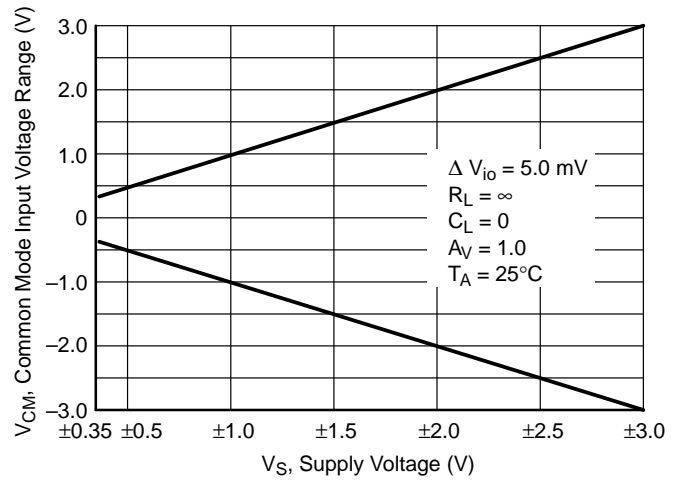


Figure 29. Common-Mode Input Voltage Range vs. Power Supply Voltage

APPLICATION INFORMATION AND OPERATING DESCRIPTION

GENERAL INFORMATION

The NCS2001 is an industry first rail-to-rail input, rail-to-rail output amplifier that features guaranteed sub one volt operation. This unique feature set is achieved with the use of a modified analog CMOS process that allows the implementation of depletion MOSFET devices. The amplifier has a 1.0 MHz gain bandwidth product, 2.2 V/μs slew rate and is operational over a power supply range less than 0.9 V to as high as 7.0 V.

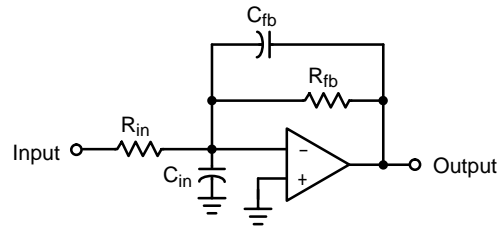
Inputs

The input topology chosen for this device series is unconventional when compared to most low voltage operational amplifiers. It consists of an N-channel depletion mode differential transistor pair that drives a folded cascade stage and current mirror. This configuration extends the input common mode voltage range to encompass the V<sub>EE</sub> and V<sub>CC</sub> power supply rails, even when powered from a combined total of less than 0.9 volts. Figure 27 and 28 show the input common mode voltage range versus power supply voltage.

The differential input stage is laser trimmed in order to minimize offset voltage. The N-channel depletion mode MOSFET input stage exhibits an extremely low input bias current of less than 10 pA. The input bias current versus temperature is shown in Figure 4. Either one or both inputs can be biased as low as V<sub>EE</sub> minus 300 mV to as high as 7.0 V without causing damage to the device. If the input common mode voltage range is exceeded, the output will not display a phase reversal. If the maximum input positive or negative voltage ratings are to be exceeded, a series resistor must be used to limit the input current to less than 2.0 mA.

The ultra low input bias current of the NCS2001 allows the use of extremely high value source and feedback resistor without reducing the amplifier's gain accuracy. These high value resistors, in conjunction with the device input and printed circuit board parasitic capacitances C<sub>in</sub>, will add an additional pole to the single pole amplifier in Figure 30. If low enough in frequency, this additional pole can reduce the phase margin and significantly increase the output settling time. The effects of C<sub>in</sub>, can be canceled by placing a zero into the feedback loop. This is accomplished with the addition of capacitor C<sub>fb</sub>. An approximate value for C<sub>fb</sub> can be calculated by:

$$C_{fb} = \frac{R_{in} \times C_{in}}{R_{fb}}$$



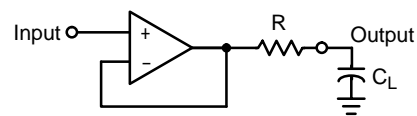
C<sub>in</sub> = Input and printed circuit board capacitance

Figure 30. Input Capacitance Pole Cancellation

Output

The output stage consists of complimentary P and N channel devices connected to provide rail-to-rail output drive. With a 2.0 k load, the output can swing within 50 mV of either rail. It is also capable of supplying over 75 mA when powered from 5.0 V and 1.0 mA when powered from 0.9 V.

When connected as a unity gain follower, the NCS2001 can directly drive capacitive loads in excess of 820 pF at room temperature without oscillating but with significantly reduced phase margin. The unity gain follower configuration exhibits the highest bandwidth and is most prone to oscillations when driving a high value capacitive load. The capacitive load in combination with the amplifier's output impedance, creates a phase lag that can result in an under-damped pulse response or a continuous oscillation. Figure 32 shows the effect of driving a large capacitive load in a voltage follower type of setup. When driving capacitive loads exceeding 820 pF, it is recommended to place a low value isolation resistor between the output of the op amp and the load, as shown in figure 31. The series resistor isolates the capacitive load from the output and enhances the phase margin. Refer to figure 33. Larger values of R will result in a cleaner output waveform but excessively large values will degrade the large signal rise and fall time and reduce the output amplitude. Depending upon the capacitor characteristics, the isolation resistor value will typically be between 50 to 500 ohms. The output drive capability for resistive and capacitive loads is shown in Figures 2, 3, and 23.



Isolation resistor R = 50 to 500

Figure 31. Capacitance Load Isolation

Note that the lowest phase margin is observed at cold temperature and low supply voltage.

# NCS2001

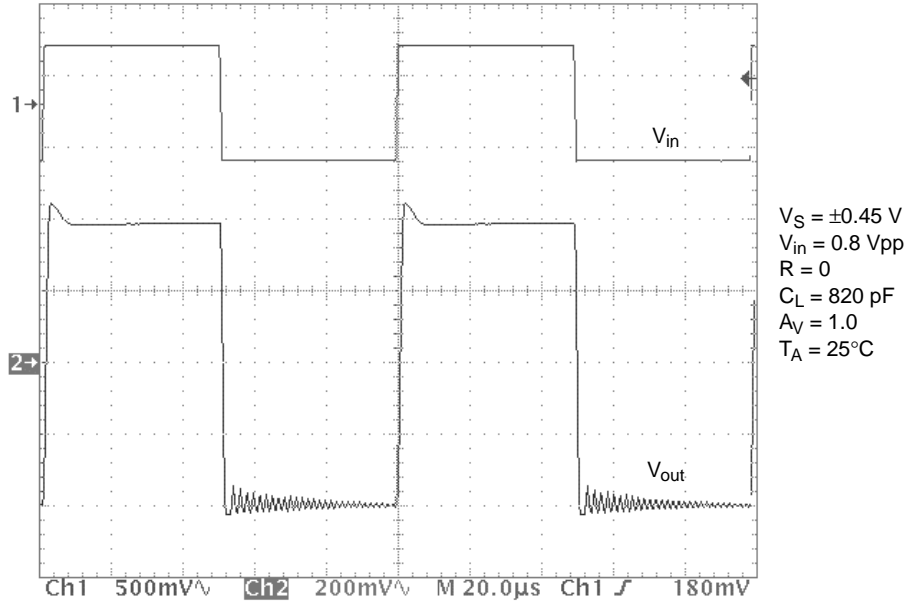


Figure 32. Small Signal Transient Response with Large Capacitive Load

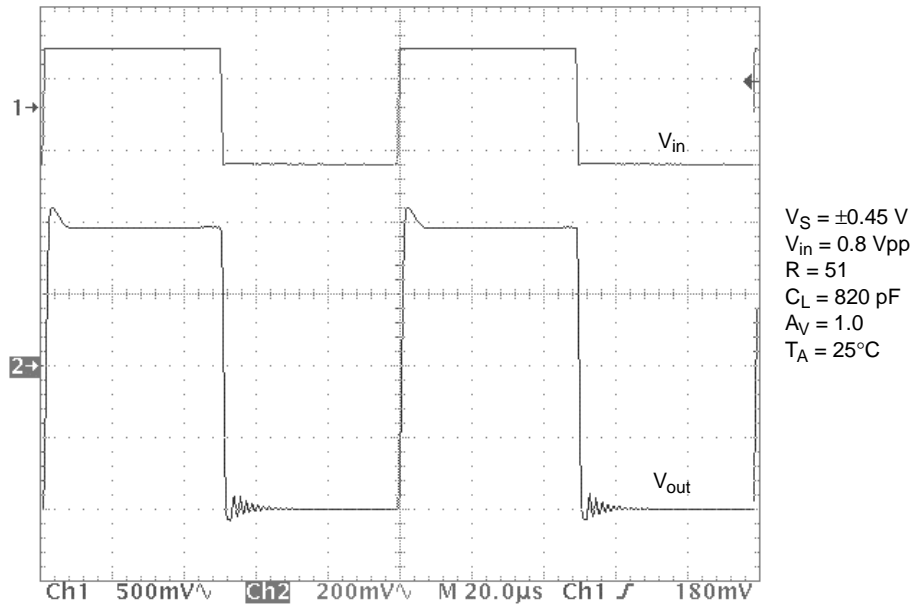


Figure 33. Small Signal Transient Response with Large Capacitive Load and Isolation Resistor.

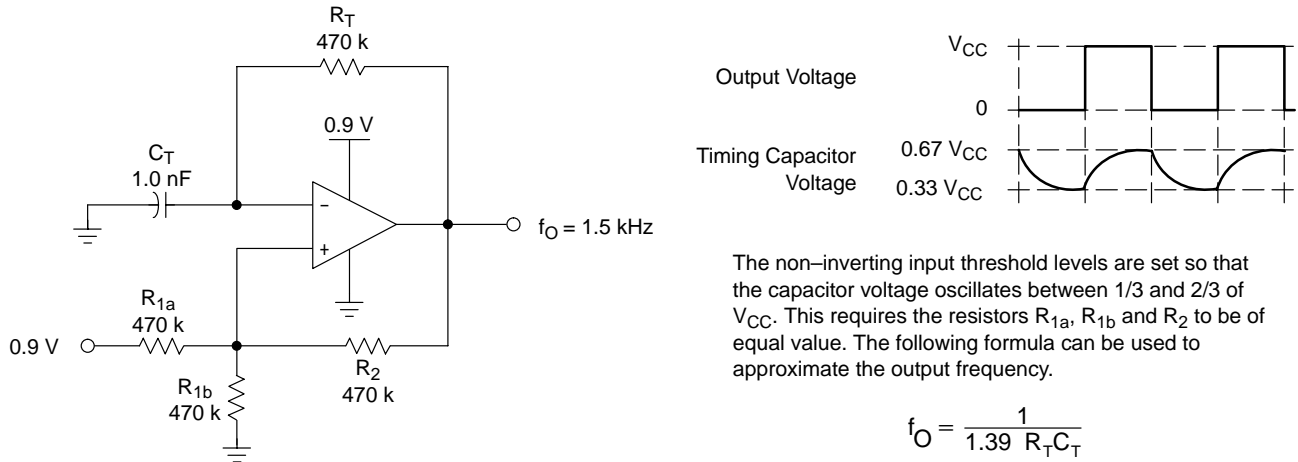


Figure 34. 0.9 V Square Wave Oscillator

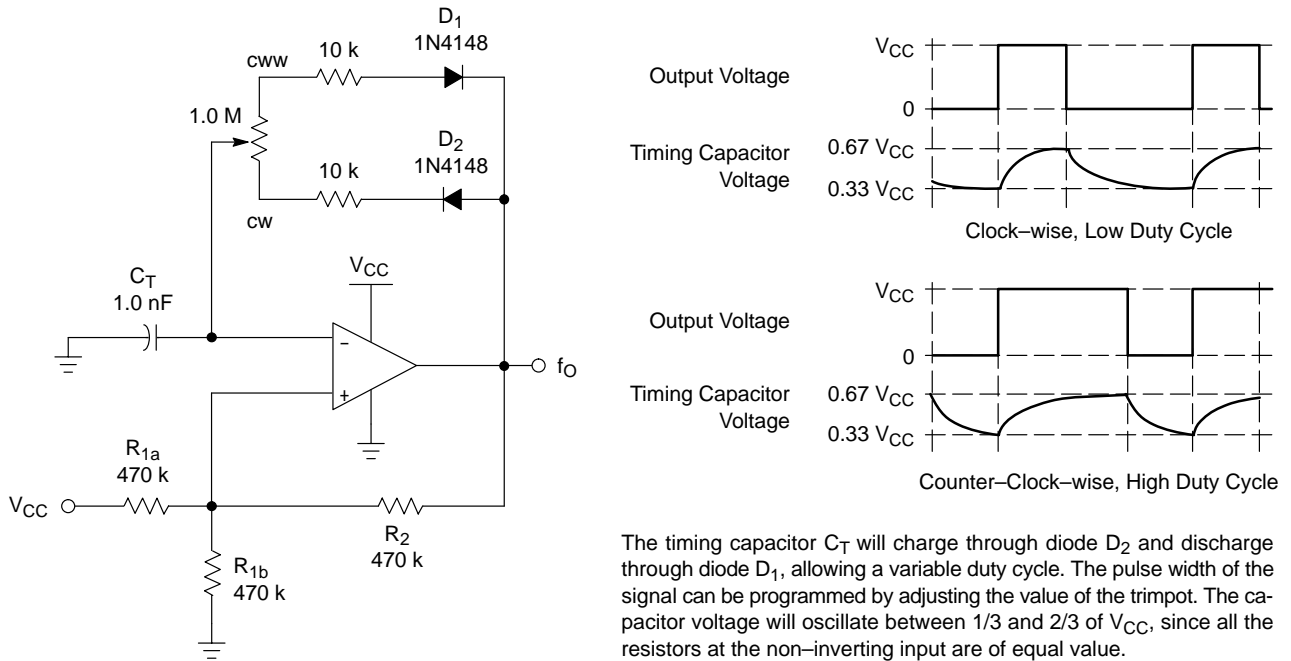


Figure 35. Variable Duty Cycle Pulse Generator

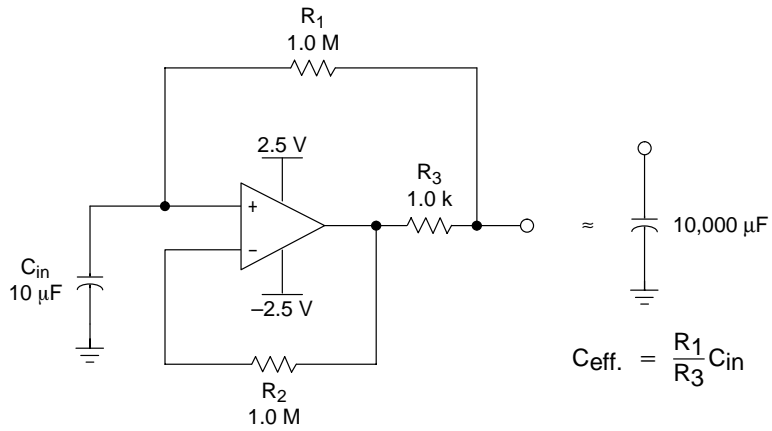


Figure 36. Positive Capacitance Multiplier

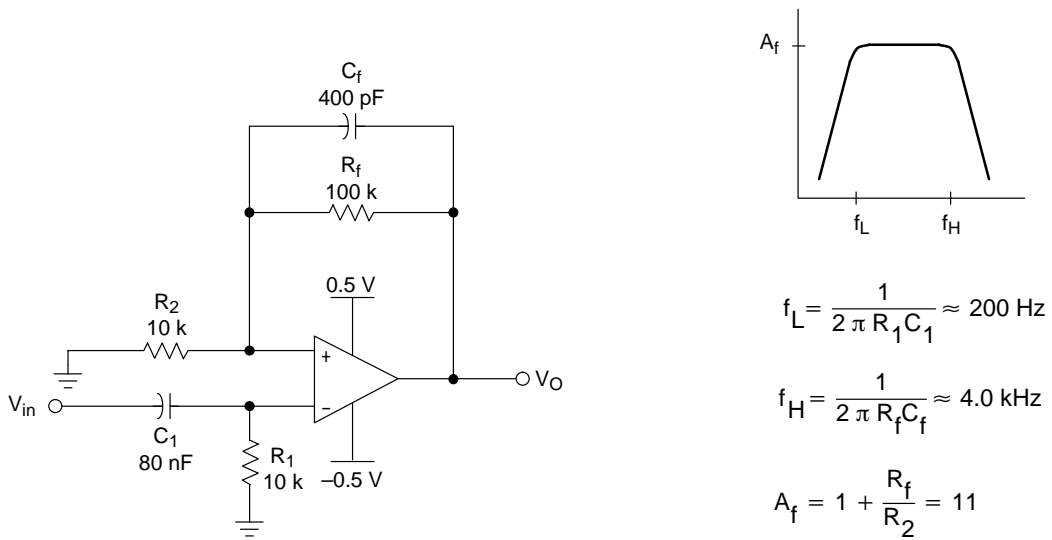


Figure 37. 1.0 V Voiceband Filter

# NCS2001

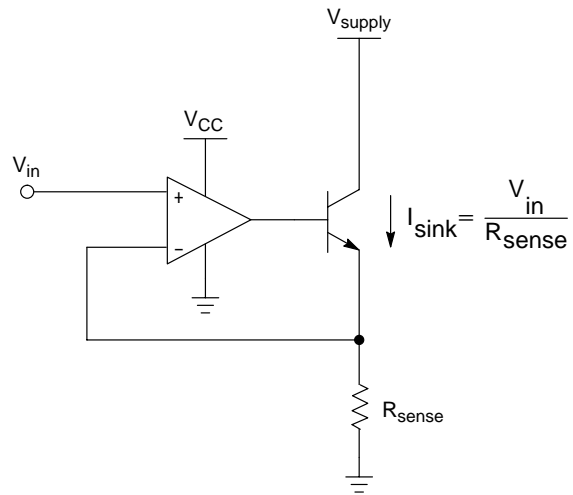
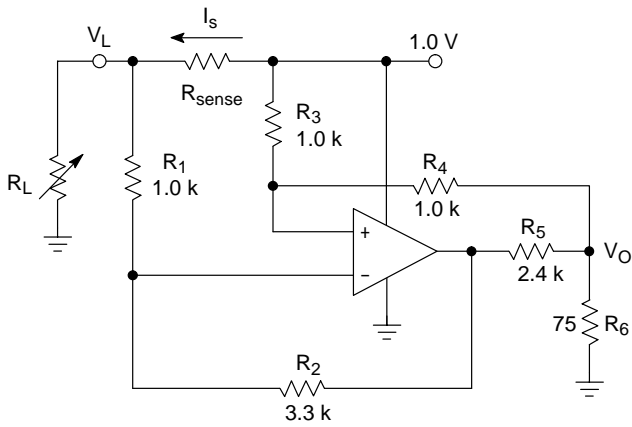


Figure 38. High Compliance Current Sink



$I_s$	$V_O$
435 mA	34.7 mV
212 mA	36.9 mV

For best performance, use low tolerance resistors.

Figure 39. High Side Current Sense

# NCS2001

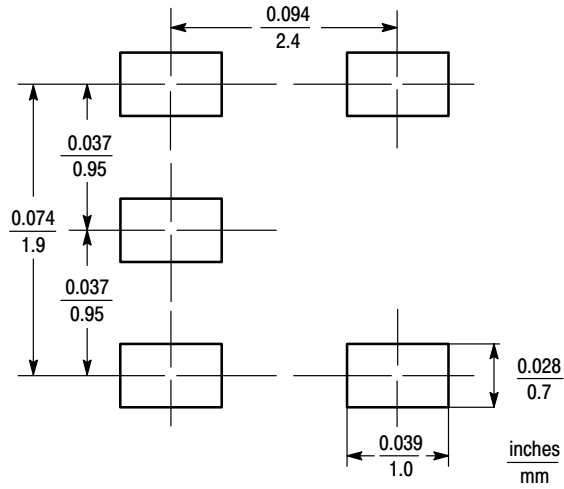
## ORDERING INFORMATION

Device	Package	Shipping*
NCS2001SN1T1	SOT23-5 (TSOP-5/SC59-5)	3000 Units on 7" Reel
NCS2001SN2T1	SOT23-5 (TSOP-5/SC59-5)	3000 Units on 7" Reel
NCS2001SQ1T1	SC70-5 (SC-88A/SOT-353)	3000 Units on 7" Reel
NCS2001SQ2T1	SC70-5 (SC-88A/SOT-353)	3000 Units on 7" Reel

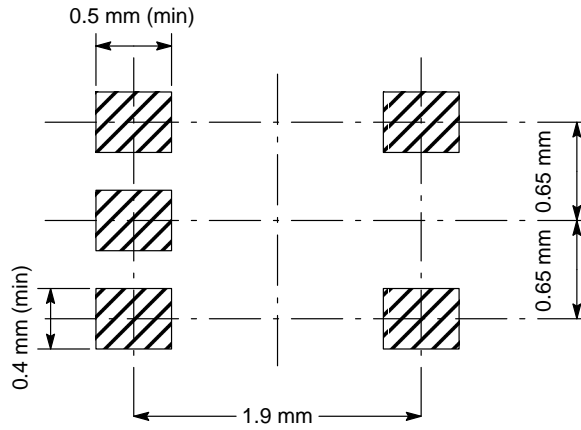
**MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS**

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



**THIN SOT23-5  
(TSOP-5/SC59-5)**



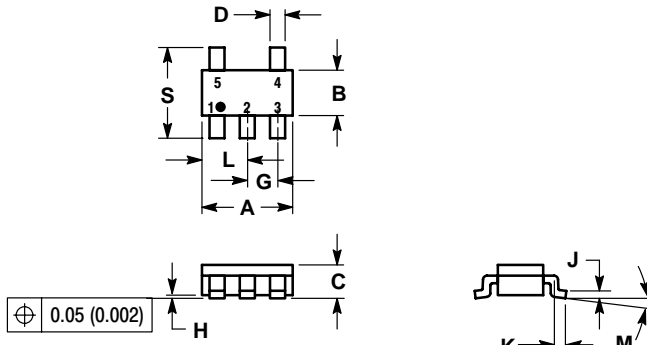
**SC70-5  
(SC-88A/SOT-353)**



# NCS2001

## PACKAGE DIMENSIONS

**SOT23-5**  
**(TSOP-5/SC59-5)**  
**N SUFFIX**  
 PLASTIC PACKAGE  
 CASE 483-01  
 ISSUE B



**NOTES:**

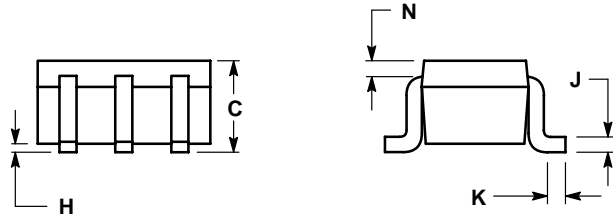
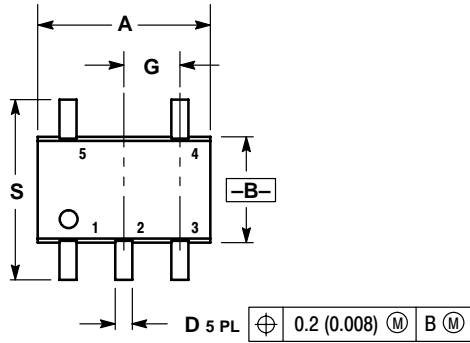
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0°	10°	0°	10°
S	2.50	3.00	0.0985	0.1181

# NCS2001

## PACKAGE DIMENSIONS


SC70-5  
(SC-88A/SOT-353)  
Q SUFFIX  
CASE 419A-02  
ISSUE F



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

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