ARIZONA MICROTEK, INC.

AZ100EP16FE

ECL/PECL High Speed VCSEL Driver with Variable Output Swing or Limiting Amplifier

FEATURES

- Silicon-Germanium for High Speed Operation
- <100ps Typical Rise/Fall Times
- Optimized for 0.622 to 2.5Gbps Fiber Applications
- Available in a 3x3mm MLP Package

PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING
MLP 8	AZ100EP16FEL	AZM16D
MLP 8 T&R	AZ100EP16FELR1	AZM16D
MLP 8 T&R	AZ100EP16FELR2	AZM16D
TSSOP 8	AZ100EP16FET	AZHP16FE
TSSOP 8 T&R	AZ100EP16FETR1	AZHP16FE
TSSOP 8 T&R	AZ100EP16FETR2	AZHP16FE

DESCRIPTION

The AZ100EP16FE is a Silicon–Germanium (SiGe) differential VCSEL driver with variable output swing or limiting post amplifier. The 100EP16FE is optimized for OC-12,OC-24, OC-48, Ethernet, Sonnet, Fiber Channel or related applications at data rates up to 2.5Gbps. An input controls the amplitude of the Q/$\overline{Q}$ outputs, which allows compensation for differing VCSEL characteristics.

The operational range of the 100EP16FE control input, V_{CTRL}, is from V_{REF} (full swing) to V_{CC} (small swing). For post amplifier applications, maximum swing is achieved by leaving the V_{CTRL} pin open or by tying it to the negative supply pin (V_{EE}). Simple control of the output swing can be obtained by a variable resistor between the V_{REF} and V_{CC} pins, with the wiper driving V_{CTRL}. A typical application circuit is described in this Data Sheet.

The 100EP16FE also provides a V_{REF} output which functions as a DC bias for input AC coupling to the device. The V_{REF} pin should be used only as a bias for the 100EP16FE as its current sink/source capability is limited. When used, the V_{REF} pin should be bypassed to ground via a 0.01µF capacitor.

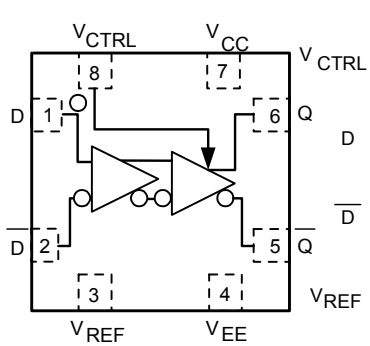
The maximum DC output current should be kept below 16mA. Connecting each output (Q/$\overline{Q}$) to V_{EE} with a 180Ω resistor is typically used. The load is then AC coupled from the output. DC and AC symmetrical loading of the Q/$\overline{Q}$ outputs will provide the best output wave shape.

Under open input conditions for D/$\overline{D}$, the Q/$\overline{Q}$ outputs are not guaranteed.

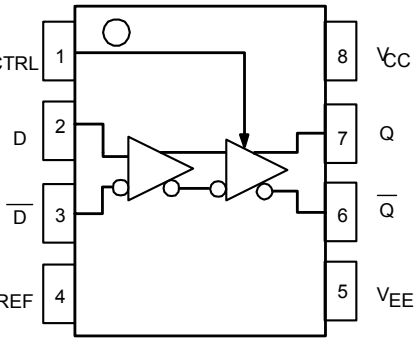
NOTE: Specifications in ECL/PECL tables are valid when thermal equilibrium is established.

PIN DESCRIPTION

PIN	FUNCTION
D, $\overline{D}$	Data Inputs
V_{CTRL}	Output Swing Control
Q, $\overline{Q}$	Data Outputs
V_{REF}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply



8 MLP (TOP VIEW)



8 TSSOP

1630 S. STAPLEY DR., SUITE 125 • MESA, ARIZONA 85204 • USA • (480) 962-5881 • FAX (480) 890-2541
www.azmicrotek.com

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V_{CC}	PECL Power Supply (V_{EE} = 0V)	0 to +4.5	Vdc
V_I	PECL Input Voltage (V_{EE} = 0V)	0 to +4.5	Vdc
V_{EE}	ECL Power Supply (V_{CC} = 0V)	-4.5 to 0	Vdc
V_I	ECL Input Voltage (V_{CC} = 0V)	-4.5 to 0	Vdc
I_{OUT}	Output Current --- Continuous --- Surge	22 44	mA
T_A	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C

100K ECL DC Characteristics (V_{EE} = -3.0V to -3.6V, V_{CC} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	-1095		-890	-1035		-870	-1000	-920	-840	-940		-760	mV
V_{OL}	Output LOW Voltage[1] $V_{CTRL} = V_{REF}$	-1935		-1745	-1905		-1715	-1885	-1790	-1695	-1830		-1640	mV
V_{OL}	Output LOW Voltage[1] $V_{CTRL} = V_{CC}$	-1140		-950	-1120		-930	-1100	-1005	-910	-1055		-865	mV
V_{REF}	Reference Voltage	-1700		-1500	-1700		-1500	-1700		-1500	-1700		-1500	mV
I_{IH}	Input HIGH Current D, $\overline{D}$ V_{CTRL}			80 400			80 400			80 400			80 400	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{EE}	Power Supply Current	20	26	35	21	27	36	21	28	36	22	31	38	mA

1. Each output is terminated through a 180Ω resistor to V_{EE}.

100K LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1,2]	2205		2410	2265		2430	2300	2380	2460	2360		2540	mV
V_{OL}	Output LOW Voltage[2] $V_{CTRL} = V_{REF}$	1365		1555	1395		1585	1415	1510	1605	1470		1660	mV
V_{OL}	Output LOW Voltage[2] $V_{CTRL} = V_{CC}$	2160		2350	2180		2370	2200	2295	2390	2245		2435	mV
V_{REF}	Reference Voltage	1600		1800	1600		1800	1600		1800	1600		1800	mV
I_{IH}	Input HIGH Current D, $\overline{D}$ V_{CTRL}			80 400			80 400			80 400			80 400	µA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			µA
I_{EE}	Power Supply Current	20	26	35	21	27	36	21	28	36	22	31	38	mA

1. For supply voltages other that 3.3V, use the ECL table values and ADD supply voltage value.
2. Each output is terminated through a 180Ω resistor to V_{EE}.

AC Characteristics (V_{EE} = -3.0 to -3.6V, V_{CC} = GND, V_{CTRL}=V_{REF} or V_{EE} = GND, V_{CC} = +3.0V to +3.6V, V_{CTRL}=V_{REF})

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency[5]		>6			>6			>6			>6		GHz
t_{PLH} / t_{PHL}	Input to Output (Diff) Delay (SE)	100	150 155	240	100	150 155	240	100	150 155	240	120	170 175	280	ps
t_{SKEW}	Duty Cycle Skew[1] (Diff)		4	20		4	15		4	15		4	15	ps
V_{pp}	Minimum Input Swing[2]	150			150			150			150			mV
V_{CMR}	Common Mode Range[3]	V_{EE} + 2.0		V_{CC}	V_{EE} + 2.0		V_{CC}	V_{EE} + 2.0		V_{CC}	V_{EE} + 2.0		V_{CC}	V
A_v	Small Signal Gain[4]								28					dB
t_r / t_f	Output Rise/Fall Times Q (20% - 80%)			130			130			130			130	ps

1. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
2. V_{PP} is the minimum peak-to-peak differential input swing for which AC parameters are guaranteed.
3. The V_{CMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}(min) and 1V. The lower end of the V_{CMR} range varies 1:1 with V_{EE} and is equal to V_{EE} + 2V.
4. Differential input, differential output. 180Ω to V_{EE} on Q/$\overline{Q}$ outputs with 50Ω AC coupled load.
5. See Figure 2.

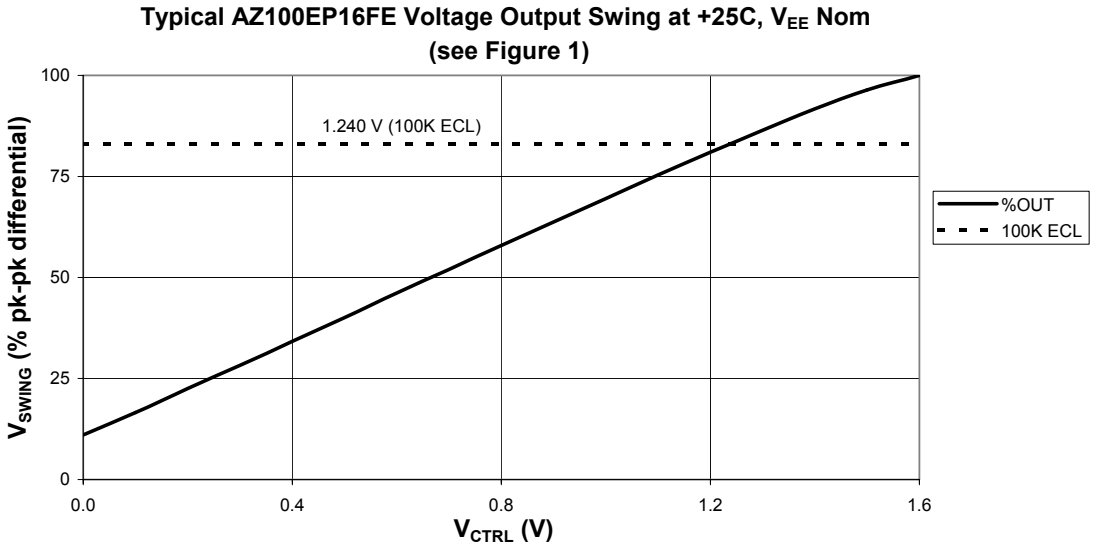


Figure 1: Typical Application

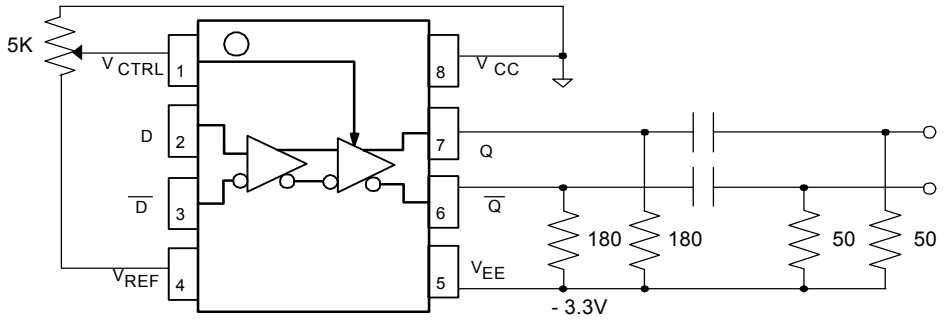
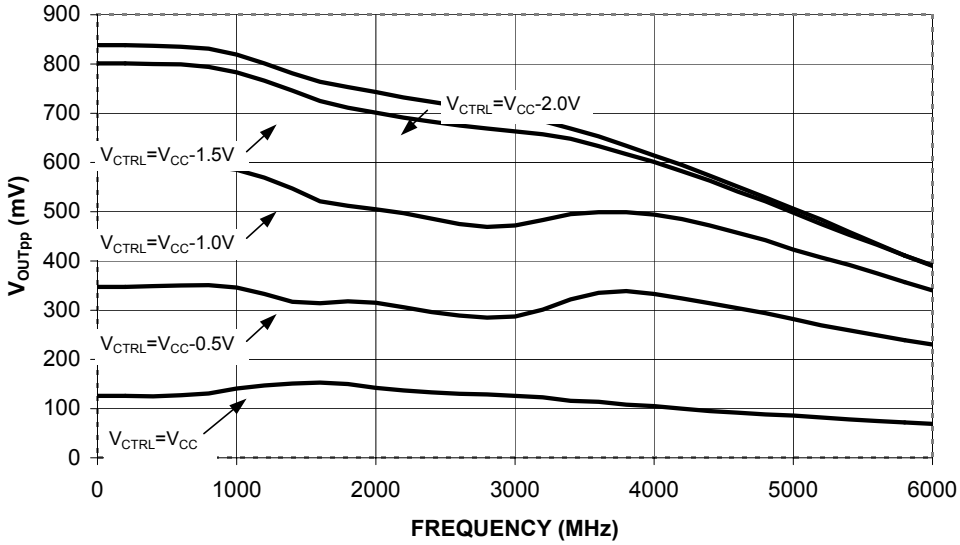
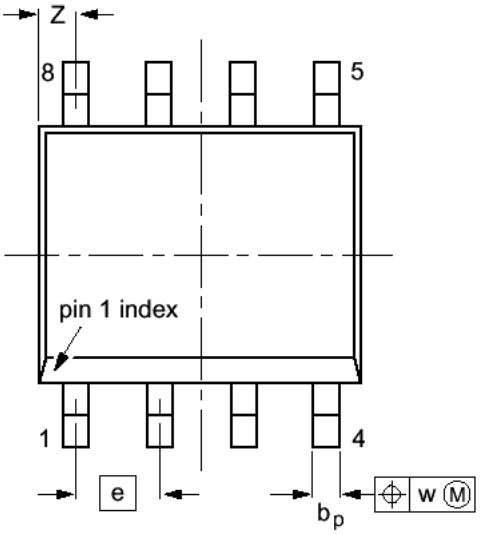


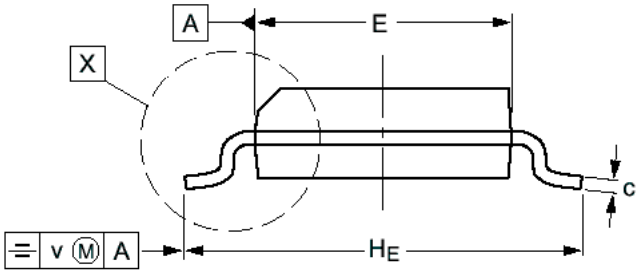
Figure 2: Large Signal Performance*

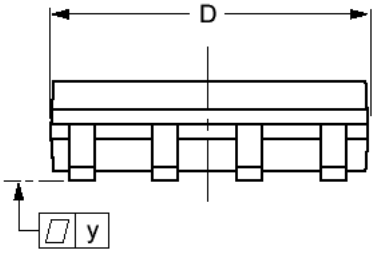


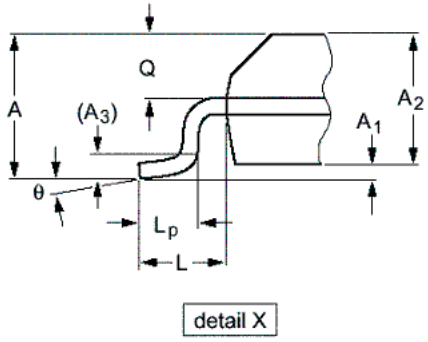
*Measured using a 750mV differential input source at 50% duty cycle.

PACKAGE DIAGRAM
SOIC 8





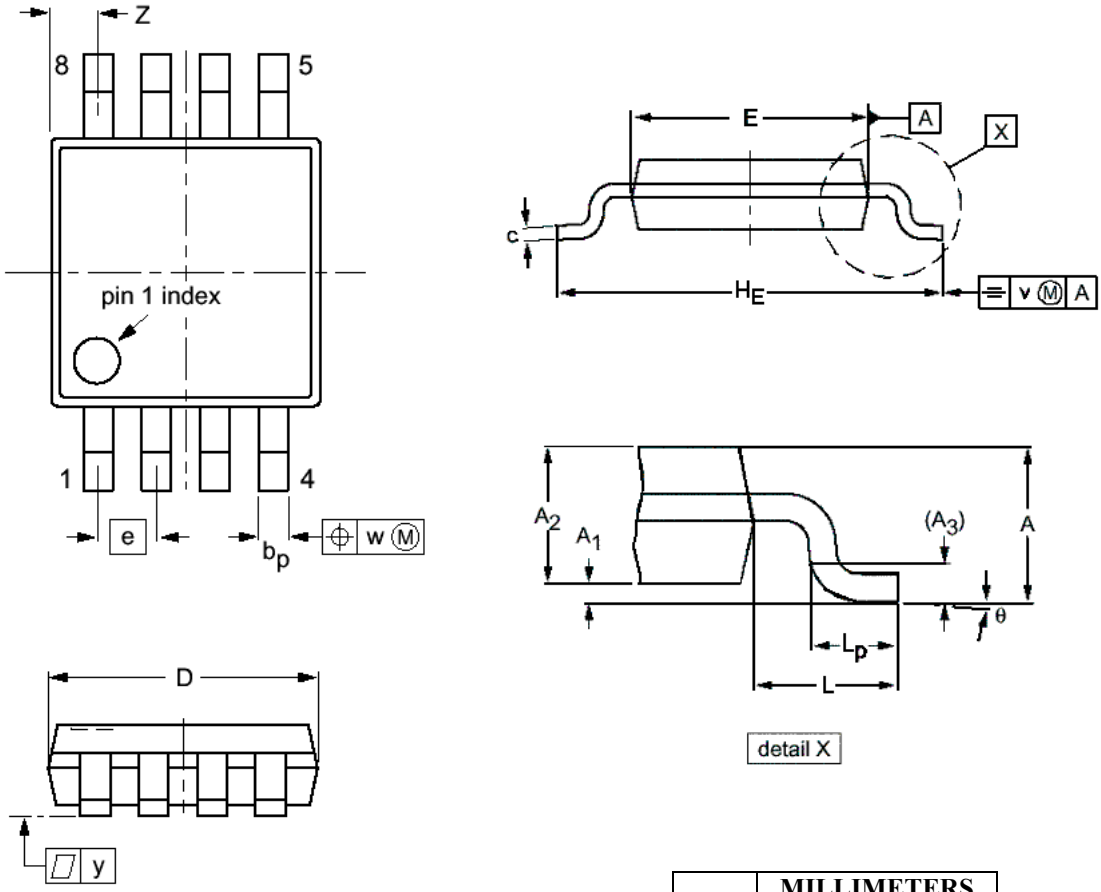




DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
A_2	1.28	1.57	0.050	0.062
A_3	0.25		0.01	
b_p	0.36	0.49	0.014	0.019
c	0.19	0.25	0.0075	0.0100
D	4.80	5.0	0.19	0.20
E	3.80	4.0	0.15	0.16
e	1.27		0.050	
H_E	5.80	6.20	0.228	0.244
L	1.05		0.041	
L_p	0.40	1.27	0.016	0.050
Q	0.60	0.70	0.024	0.028
v	0.25		0.01	
w	0.25		0.01	
y	0.10		0.004	
Z	0.30	0.70	0.012	0.028
θ	0^O	8^O	0^O	8^O

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

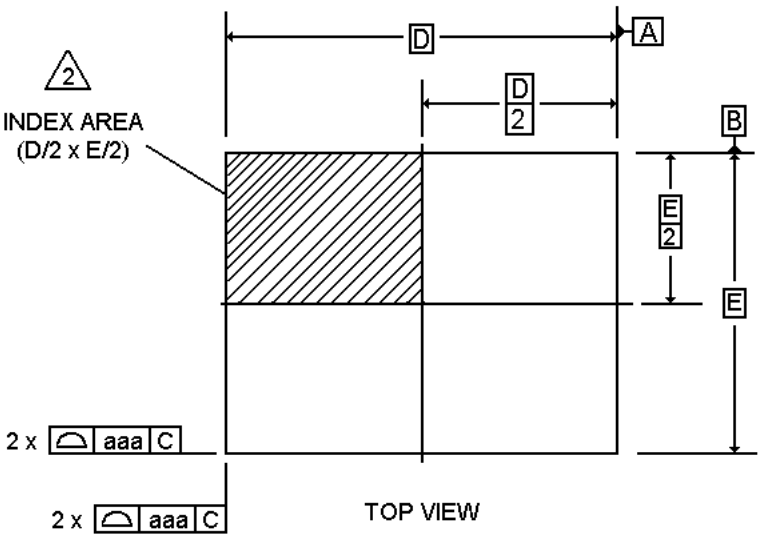
PACKAGE DIAGRAM
TSSOP 8

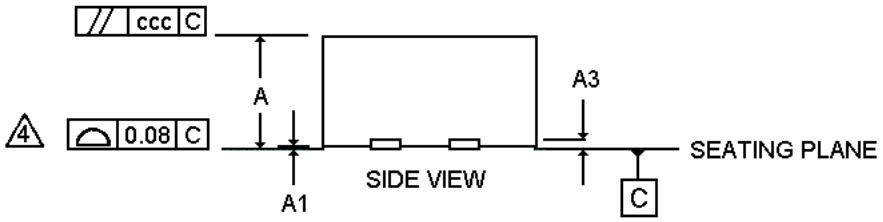


DIM	MILLIMETERS	
	MIN	MAX
A		1.10
A_1	0.05	0.15
A_2	0.75	0.95
A_3	0.25	
b_p	0.22	0.40
c	0.13	0.23
D	2.90	3.10
E	2.90	3.10
e	0.65	
H_E	4.75	5.05
L	0.95	
L_p	0.40	0.70
v	0.10	
w	0.08	
y	0.10	
Z	0.38	0.64
θ	0^O	6^O

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

PACKAGE DIAGRAM
MLP 8





NOTES

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
2. THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
3. DIMENSION b APPLIES TO METALLIZED PAD AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM PAD TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.08	1.00
A1	0.00	0.05
A3	0.25 REF	
b	0.23	0.38
D	2.90	3.10
D2	0.25	1.95
E	2.90	3.10
E2	0.25	1.95
e	0.65 BSC	
L	0.30	0.50
aaa	0.25	
bbb	0.10	
ccc	0.10