New Jersey Semi-Conductor Products, Inc.

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2N6898

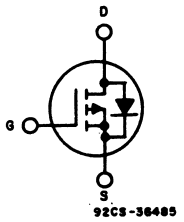
Power MOS Field-Effect Transistors

P-Channel Enhancement-Mode Power MOS Field-Effect Transistors

25 A, −100 V
r_{DS}(on): 0.20 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM

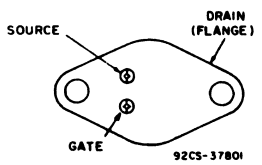


P-CHANNEL ENHANCEMENT MODE

The 2N6898 is a P-channel enhancement-mode silicon-gate power MOS field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This device can be operated directly from an integrated circuit.

The 2N6898 is supplied in the JEDEC TO-204AE steel package.

TERMINAL DESIGNATION



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25°C)

*DRAIN-SOURCE VOLTAGE, V_{DSS}	−100 V
*DRAIN-GATE VOLTAGE (R_{GS} = 1 MΩ), V_{DGR}	−100 V
*GATE-SOURCE VOLTAGE, V_{GS}	±20 V
*DRAIN CURRENT:	
RMS Continuous, I_D	25 A
Pulsed, I_{DM}	60 A
*POWER DISSIPATION, P_T:	
At T_C = 25°C	150 W
Above T_C = 25°C	Derate linearly 1.2 W/°C
*OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	−55 to +150°C
*LEAD TEMPERATURE, T_L:	
At distances ≥ ⅛ in. (3.17 mm) from seating plane for 10 s max.	260°C

*In accordance with JEDEC registration data.

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Standard Power MOSFETs

2N6898

ELECTRICAL CHARACTERISTICS at Case Temperature (T_C) = 25°C unless otherwise specified.

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	-100	—	V
*	Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA	-2	-4	V
*	Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V	—	1	μA
			T_C = 125°C, V_{DS} = -80 V	—	50	
*	Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0	—	100	nA
*	Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 15.8 A, V_{GS} = -10 V	—	3.16	V
			I_D = 25 A, V_{GS} = -10 V	—	-6	
*	Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 15.8 A, V_{GS} = -10 V	—	0.2	Ω
			T_C = 125°C, I_D = 15.8 A, V_{GS} = 10 V	—	0.24	
*	Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V, I_D = 15.8 A	4	16	mho
*	Input Capacitance	C_{iss}	V_{DS} = -25 V	—	3000	pF
*	Output Capacitance	C_{oss}	V_{GS} = 0 V	—	1500	
*	Reverse Transfer Capacitance	C_{rss}	f = 0.1 MHz	—	500	
*	Turn-On Delay Time	$t_d(on)$	V_{DS} = -50 V	—	50	ns
*	Rise Time	t_r	I_D = 12.5 A	—	250	
*	Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 50 Ω	—	400	
*	Fall Time	t_f	V_{GS} = -10 V	—	250	
*	Thermal Resistance Junction-to-Case	$R_{\theta JC}$		—	0.83	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

	CHARACTERISTIC		TEST CONDITIONS	LIMITS Min.	LIMITS Max.	UNITS
*	Diode Forward Voltage	V_{SD}[a]	I_{SD} = 25 A	0.8	1.6	V
	Reverse Recovery Time	t_{rr}	I_F = 4 A, d_{IF}/dt = 100 A/μs	—	750	ns

*In accordance with JEDEC registration data.
[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%

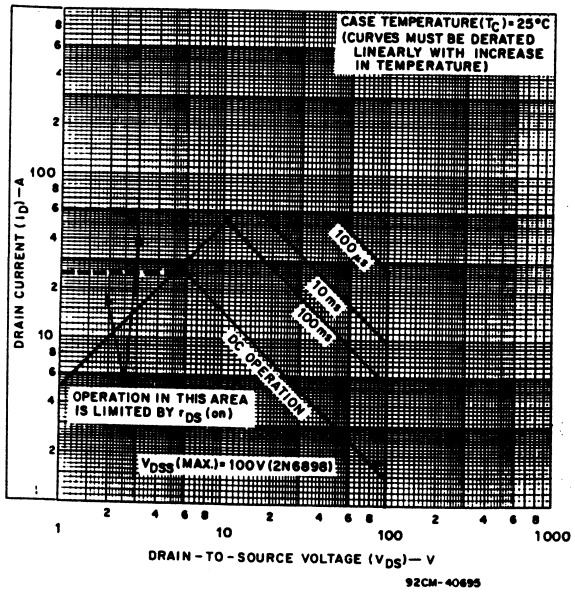

Fig. 1 - Maximum safe operating areas.

Quality Semi-Conductors