

N-channel 30 V, 0.019 Ω typ., 10 A, P-channel 30 V, 0.024 Ω typ., 8 A
 STripFET™ VI Power MOSFET in a PowerFLAT 5x6 d. i. package

Datasheet - production data

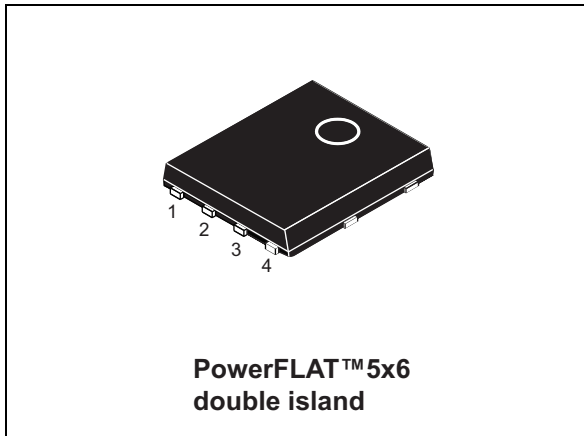
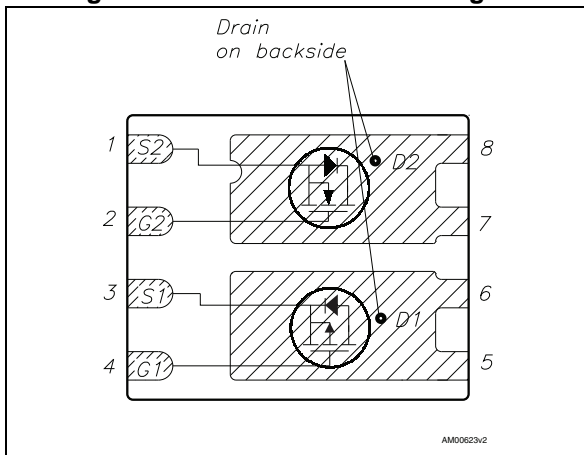


Figure 1. Internal schematic diagram



Features

Order code	Channel	V _{DS}	R _{DS(on)} max	I _D
STL40C30H3LL	N	30 V	0.021 Ω @ 10 V	10 A
	P		0.03 Ω @ 10 V	8 A

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power losses

Applications

- Switching applications

Description

This device is a complementary N-channel and P-channel Power MOSFET developed using STripFET™ V (P-channel) and STripFET™ VI DeepGATE™ (N-channel) technologies. The resulting device exhibits low on-state resistance and an FOM among the lowest in its voltage class.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STL40C30H3LL	40C30H3L	PowerFLAT 5x6 double island	Tape and reel

Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		N-channel	P-channel	
V_{DS}	Drain-source voltage ($v_{gs} = 0$)	30		V
V_{GS}	Gate- source voltage	±20		V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$ single operating	40	30	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$ single operating	25	18.75	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25^\circ\text{C}$ single operating	10	8	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100^\circ\text{C}$ single operating	6.5	5	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	40	32	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25^\circ\text{C}$	60		W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25^\circ\text{C}$	4		W
T_{stg}	Storage temperature	-55 to 150		°C
T_j	Operating junction temperature	150		°C

1. The value is rated according to R_{thj-c}
2. This value is rated according to $R_{thj-pcb}$
3. Pulse width is limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thj-c}	Thermal resistance junction-case	2.08	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb single operation	32.00	°C/W

1. When mounted on 1 inch² FR-4 board, 2 oz. Cu., $t \leq 10$ sec

Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed

2 Electrical characteristics

Table 4. On/off states

Symbol	Parameter	Test conditions	Channel	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	N	30			V
			P				
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 30 V$	N			1	μA
			P				
		$V_{DS}=30 V, T_C=125 \text{ }^\circ C$	N			10	μA
			P				
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 V$	N			± 100	nA
			P				
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	N	1			V
			P				
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10 V, I_D = 4 A$	N		0.019	0.021	Ω
			P		0.024	0.03	Ω
		$V_{GS} = 4.5 V, I_D = 4 A$	N		0.023	0.028	Ω
			P		0.038	0.05	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Channel	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 24 V, f = 1 MHz, V_{GS} = 0$	N	-	475	-	pF
			P	-	1450	-	pF
C_{oss}	Output capacitance		N	-	97	-	pF
			P	-	178	-	pF
C_{rss}	Reverse transfer capacitance		N	-	19	-	pF
			P	-	120	-	pF
Q_g	Total gate charge	$V_{DD}=24 V, I_D=8 A, V_{GS}= 4.5 V$ (see Figure 25)	N	-	4.6	-	nC
			P	-	12	-	nC
Q_{gs}	Gate-source charge		N	-	1.7	-	nC
			P	-	4.4	-	nC
Q_{gd}	Gate-drain charge		N	-	1.9	-	nC
			P	-	5	-	nC

Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed

Table 6. Switching times

Symbol	Parameter	Test conditions	Channel	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 24\text{ V}$, $I_D = 4\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ <i>Figure 24</i>	N	-	4	-	ns
			P	-	15	-	ns
t_r	Rise time		N	-	22	-	ns
			P	-	15	-	ns
$t_{d(off)}$	Turn-off delay time		N	-	13	-	ns
			P	-	24	-	ns
t_f	Fall time		N	-	2.8	-	ns
			P	-	21	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Channel	Min.	Typ.	Max.	Unit	
I_{SD}	Source-drain current	$I_{SD} = 8\text{ A}$, $V_{GS} = 0$	N	-		10	A	
			P	-		8	A	
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		N	-		40	A	
			P	-		32	A	
$V_{SD}^{(2)}$	Forward on voltage		N	-		1.1	V	
			P	-				
t_{rr}	Reverse recovery time		$I_{SD} = 8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 16\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ <i>Figure 26</i>	N	-	16.2		ns
				P	-	15		ns
Q_{rr}	Reverse recovery charge	N		-	8.1		nC	
		P		-	6.5		nC	
I_{RRM}	Reverse recovery current	N		-	1		A	
		P		-	0.9		A	

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Note: For the P-channel MOSFET actual polarity of voltages and current has to be reversed

2.1 Electrical characteristics (curves) for N-channel

Figure 2. Safe operating area

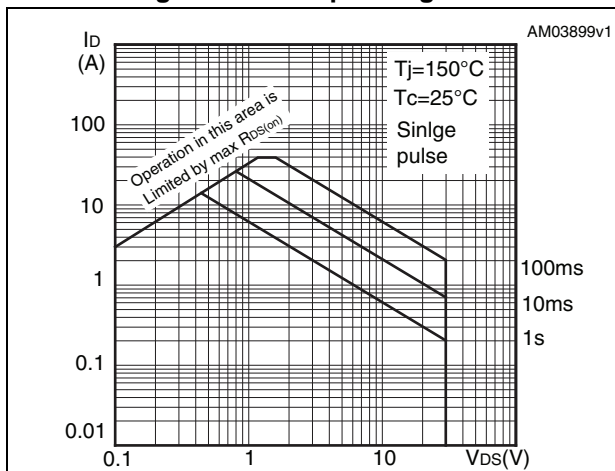


Figure 3. Thermal impedance

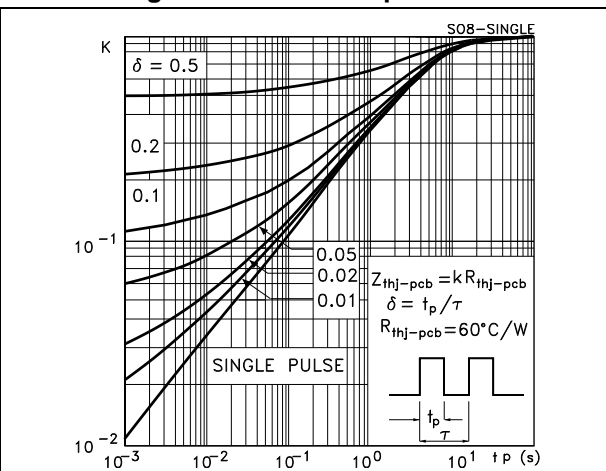


Figure 4. Output characteristics

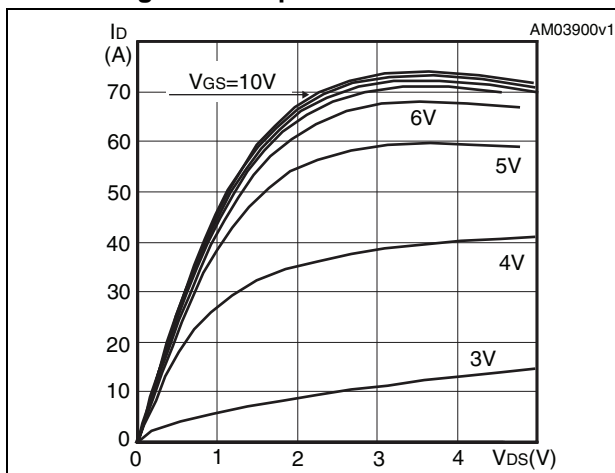


Figure 5. Transfer characteristics

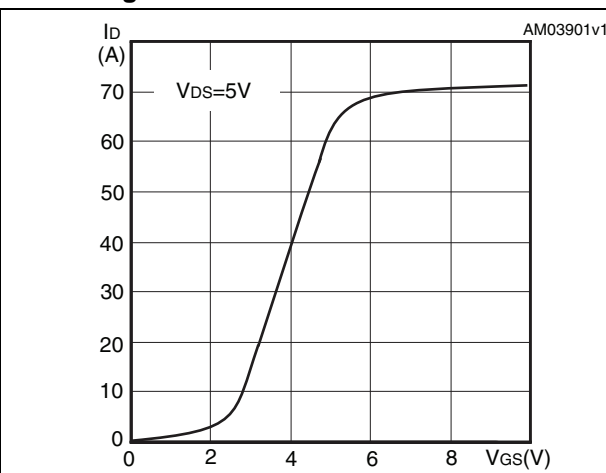


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

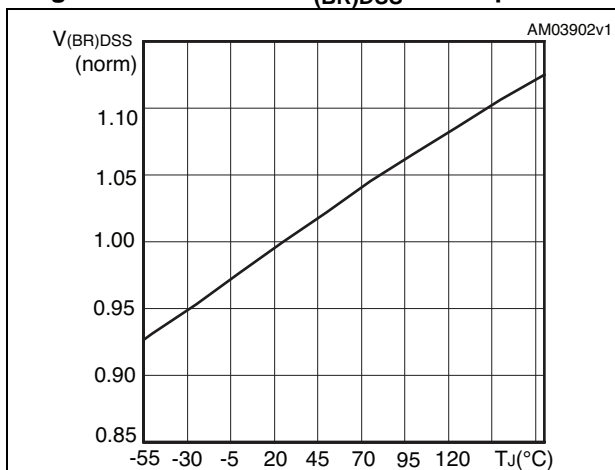


Figure 7. Static drain-source on-resistance

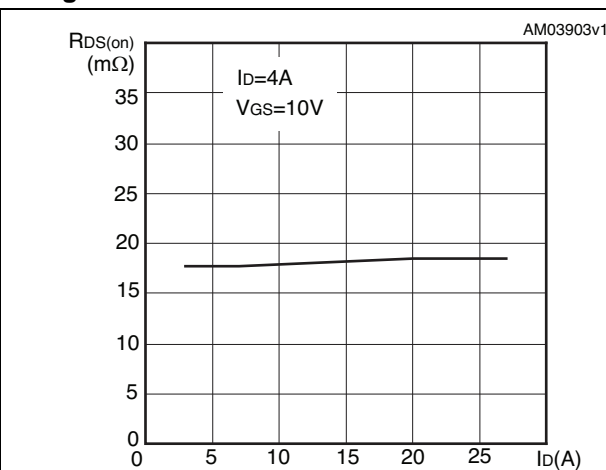


Figure 8. Gate charge vs gate-source voltage

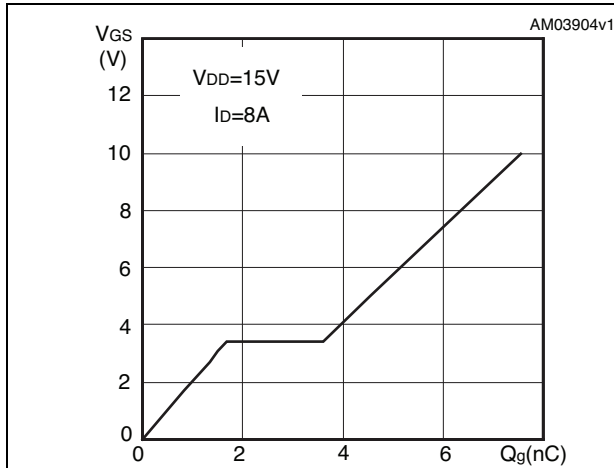


Figure 9. Capacitance variations

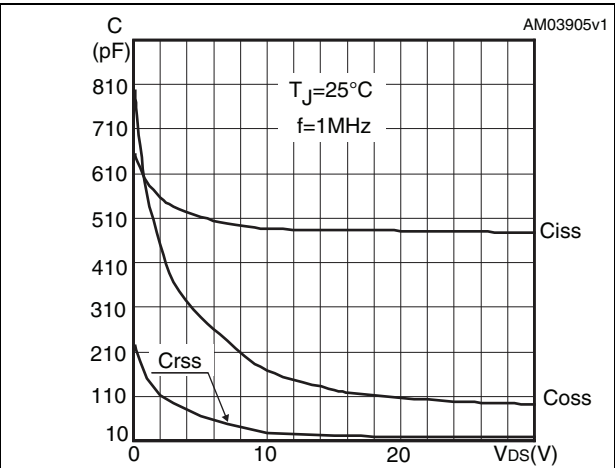


Figure 10. Normalized gate threshold voltage vs temperature

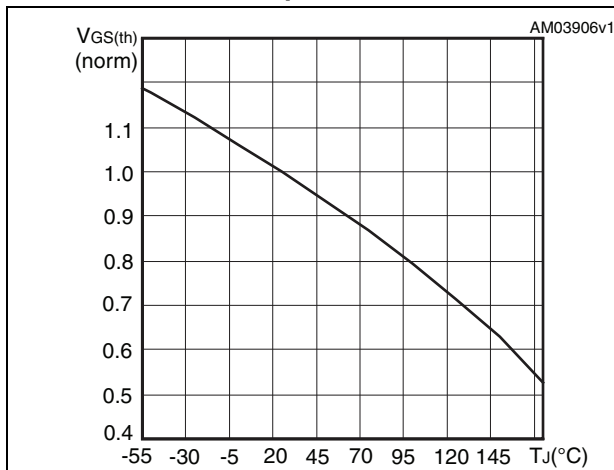


Figure 11. Normalized on-resistance vs temperature

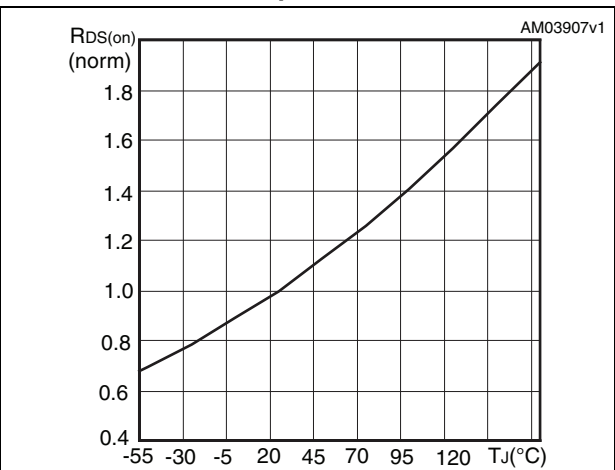
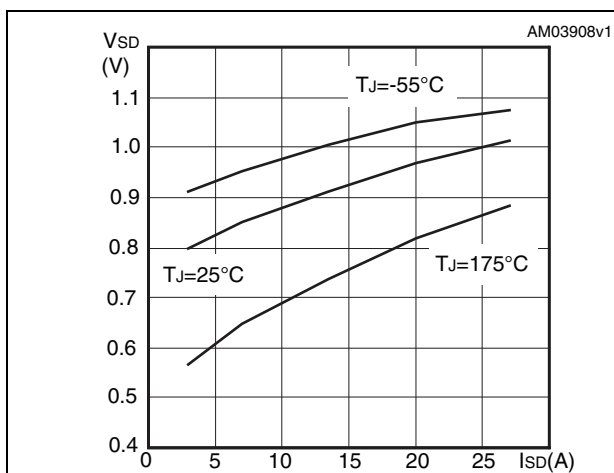


Figure 12. Source-drain diode forward characteristics



2.2 Electrical characteristics (curves) for P-channel

Figure 13. Safe operating area

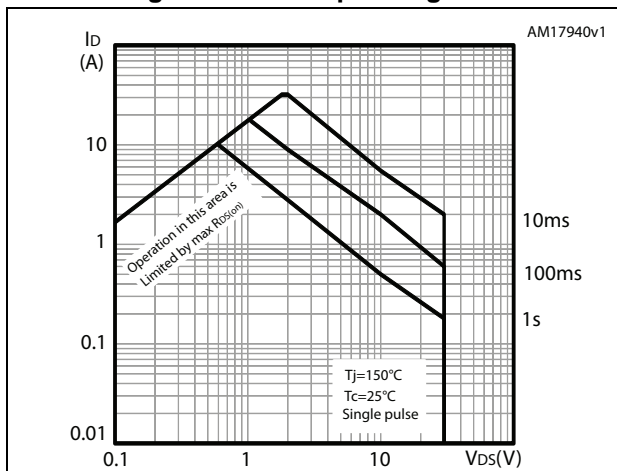


Figure 14. Thermal impedance

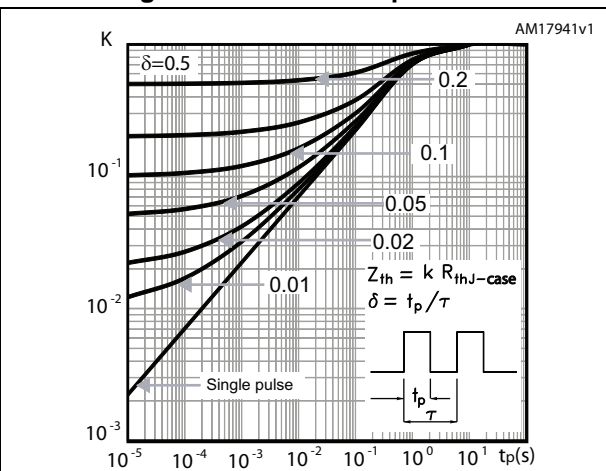


Figure 15. Output characteristics

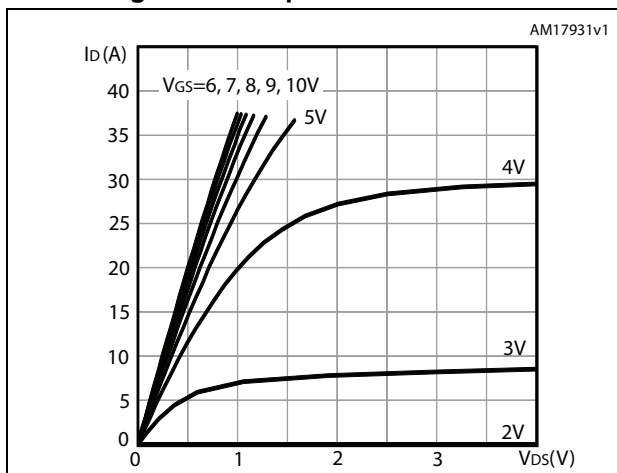


Figure 16. Transfer characteristics

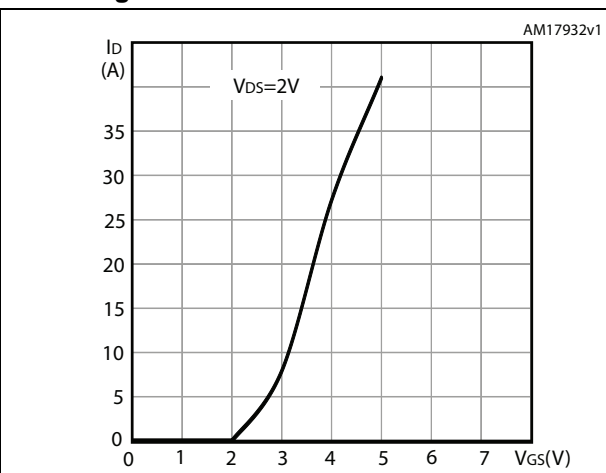


Figure 17. Gate charge vs gate-source voltage

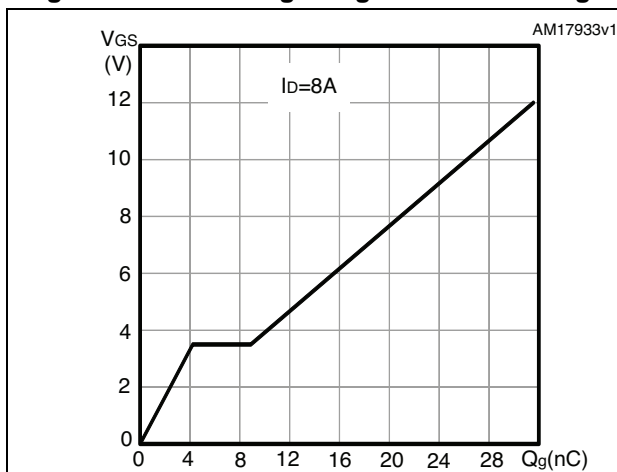


Figure 18. Static drain-source on-resistance

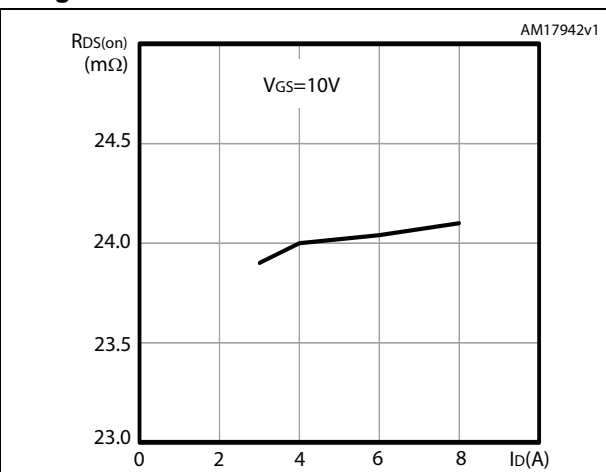


Figure 19. Capacitance variations

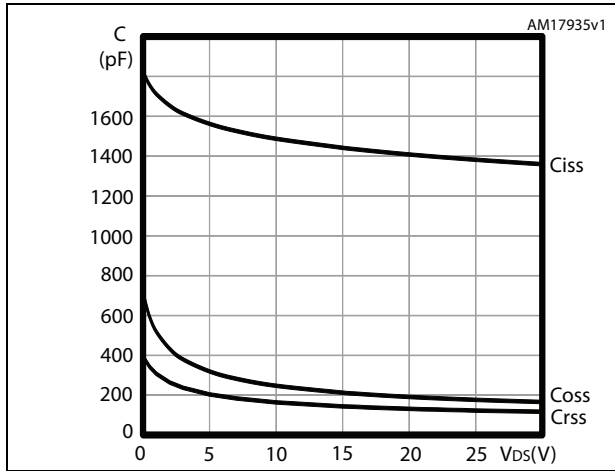


Figure 20. Normalized gate threshold voltage vs temperature

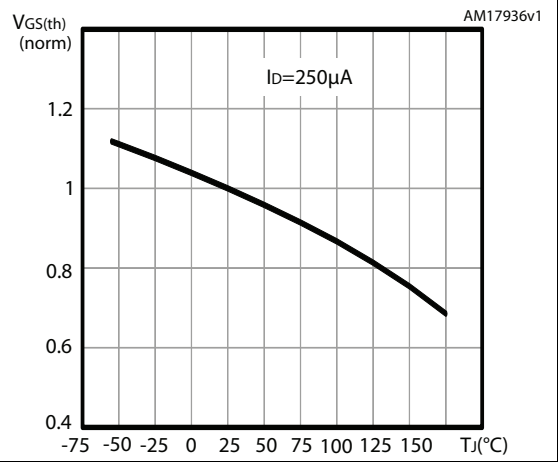


Figure 21. Normalized on-resistance vs temperature

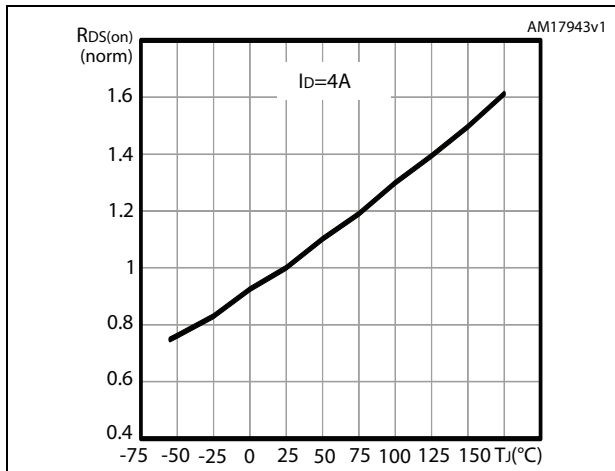


Figure 22. Normalized V(BR)DSS vs temperature

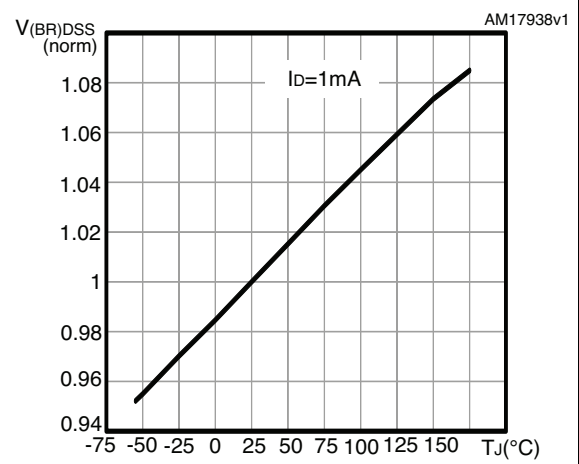
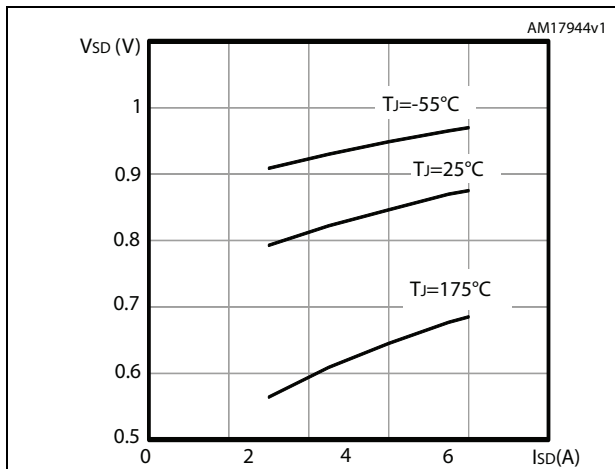
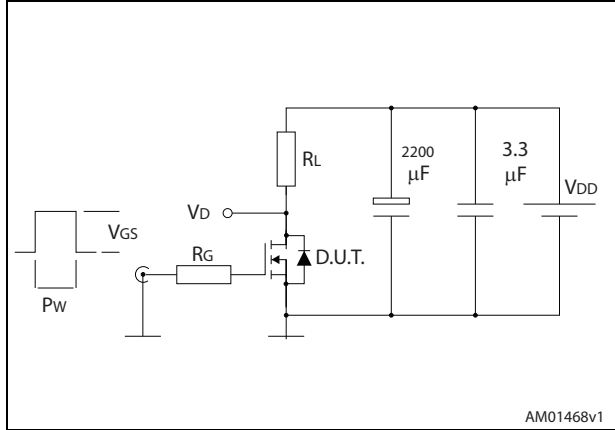


Figure 23. Source-drain diode forward characteristics



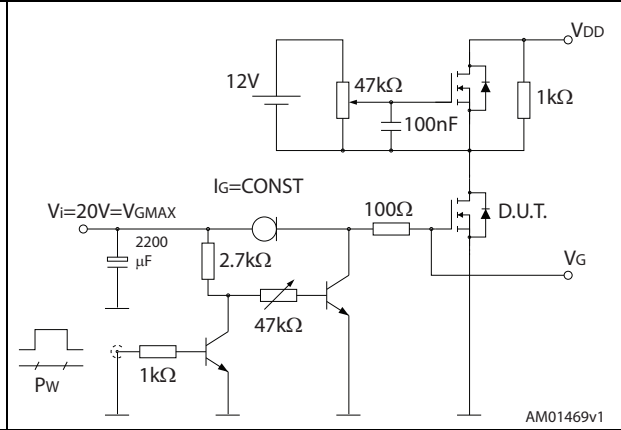
3 Test circuits for N-channel

Figure 24. Switching times test circuit for resistive load



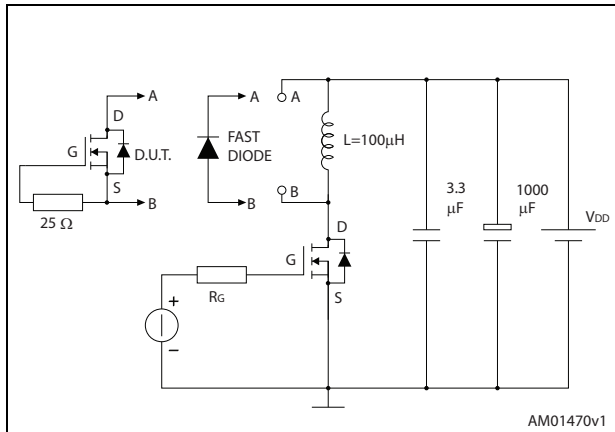
AM01468v1

Figure 25. Gate charge test circuit



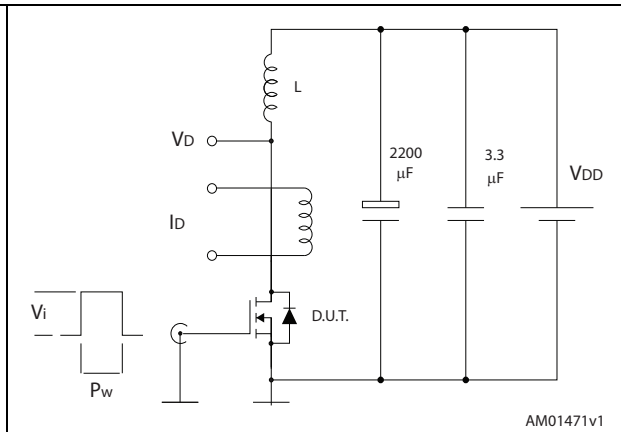
AM01469v1

Figure 26. Test circuit for inductive load switching and diode recovery times



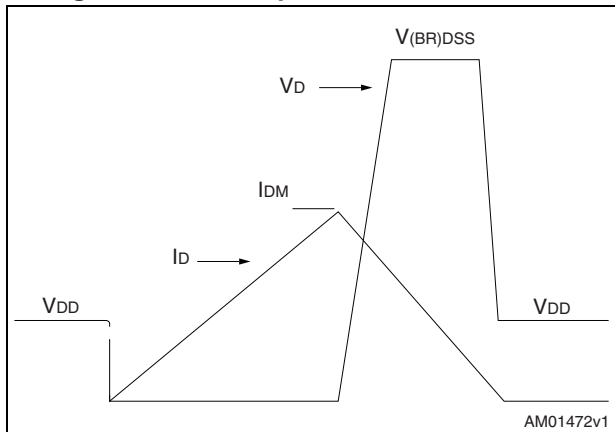
AM01470v1

Figure 27. Unclamped inductive load test circuit



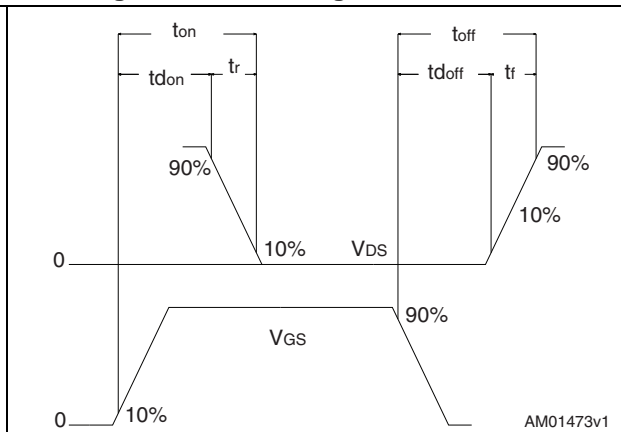
AM01471v1

Figure 28. Unclamped inductive waveform



AM01472v1

Figure 29. Switching time waveform



AM01473v1

4 Test circuits for P-channel

Figure 30. Switching times test circuit for resistive load

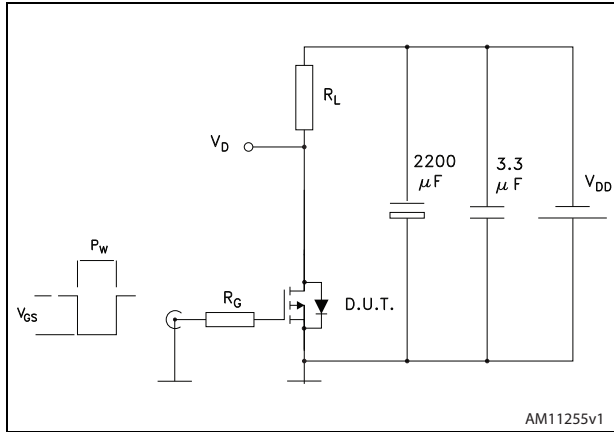


Figure 31. Gate charge test circuit

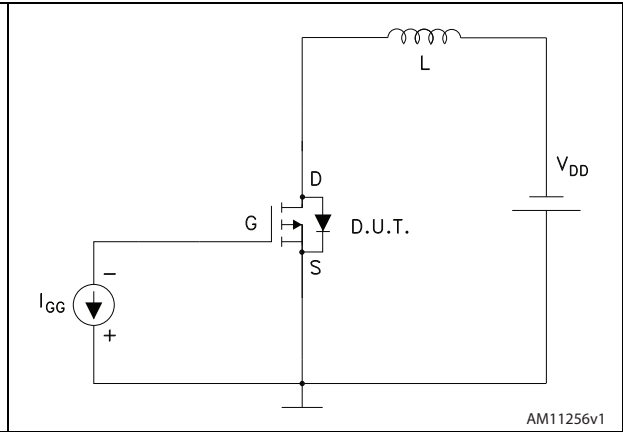
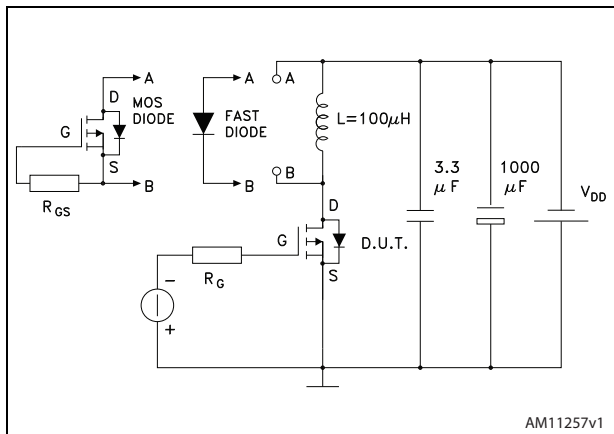


Figure 32. Test circuit for diode recovery behavior



5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 33. PowerFLAT™ 5x6 - double island type R-B drawing

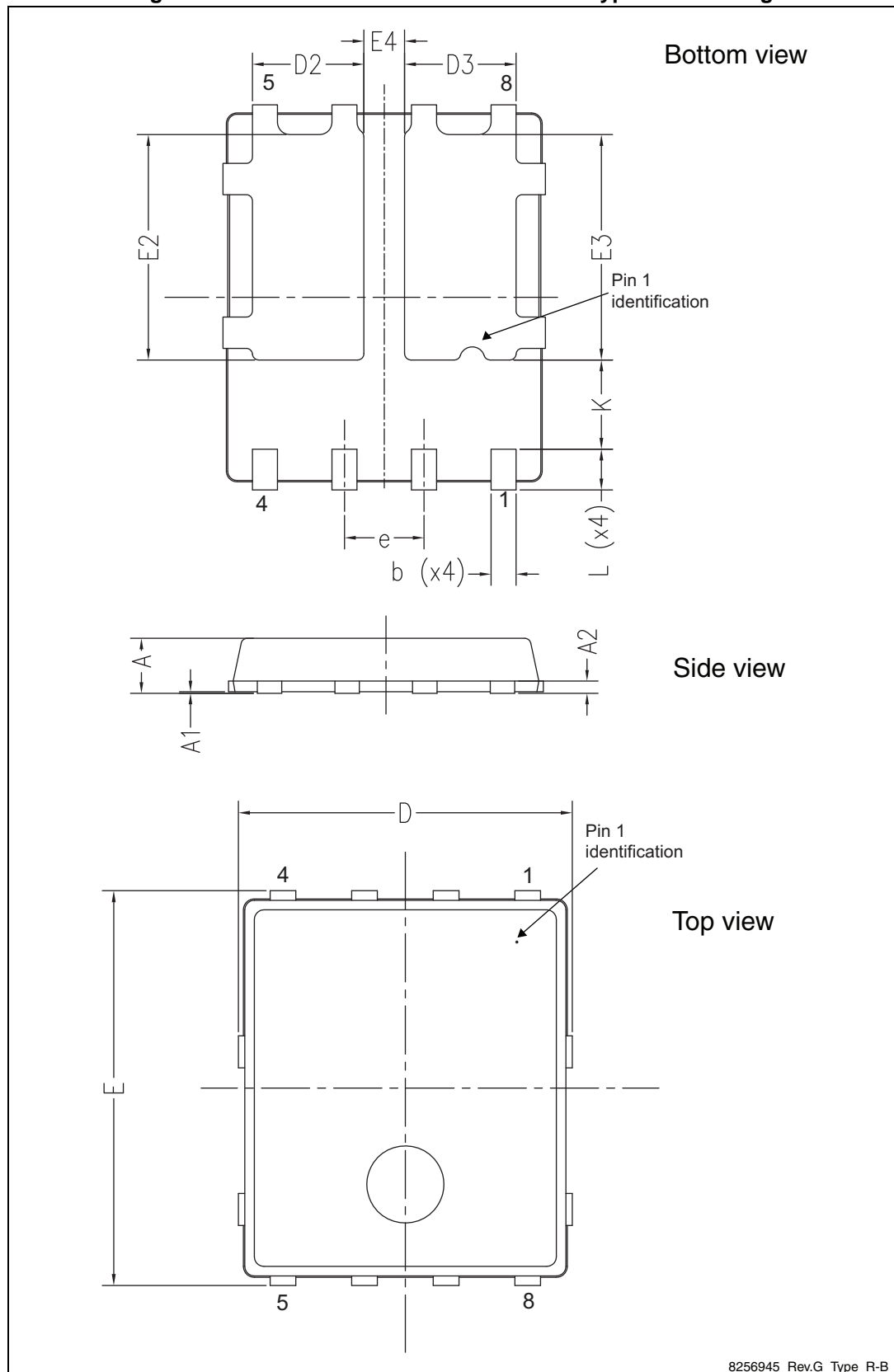


Table 8. PowerFLAT™ 5x6 - double island type R-B mechanical data

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	1.68		1.88
E2	3.50		3.70
D3	1.68		1.88
E3	3.50		3.70
E4	0.55		0.75
e		1.27	
L	0.60		0.80
K	1.275		1.575

6 Packaging mechanical data

Figure 35. PowerFLAT™ 5x6 tape^(a)

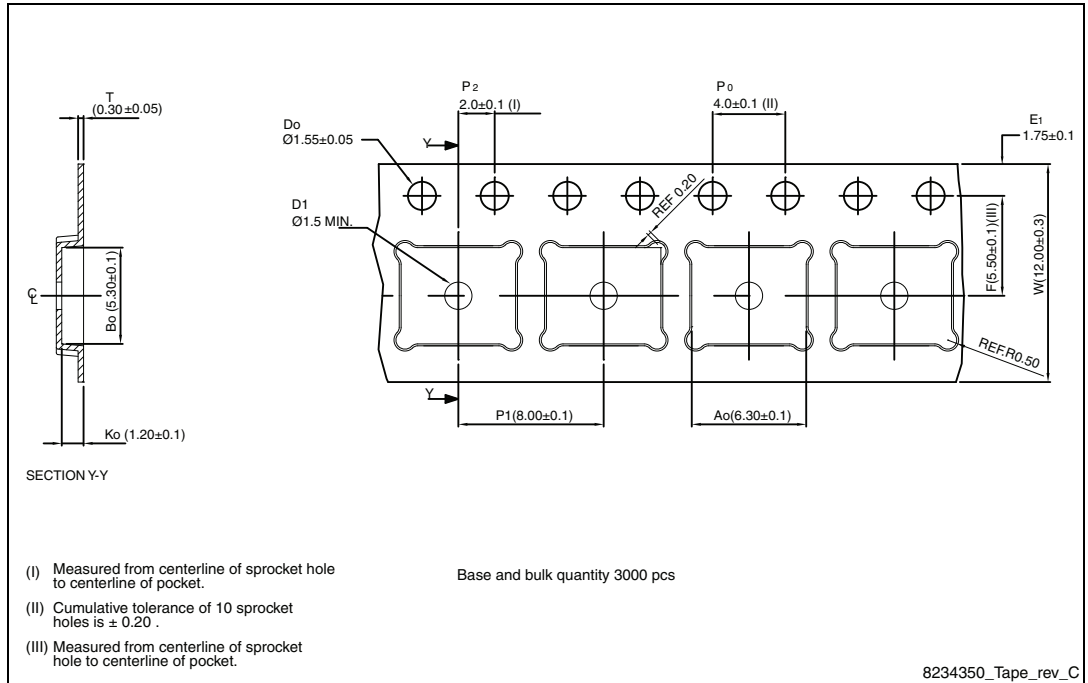
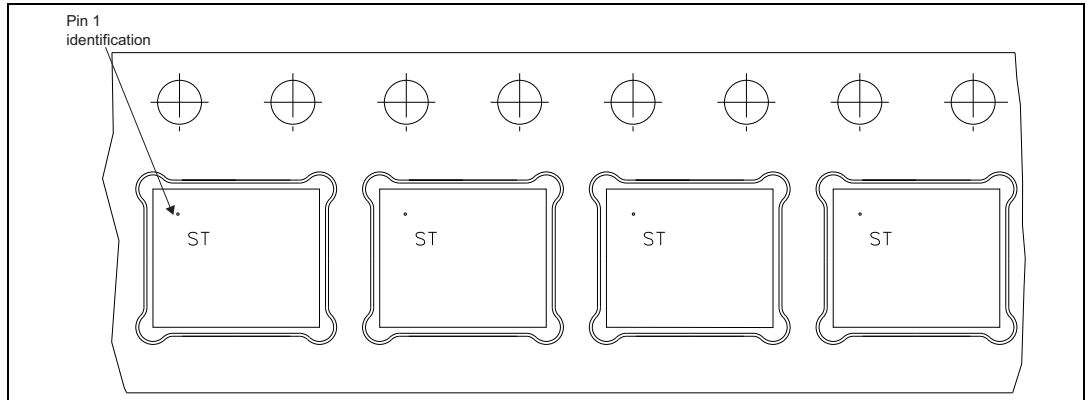
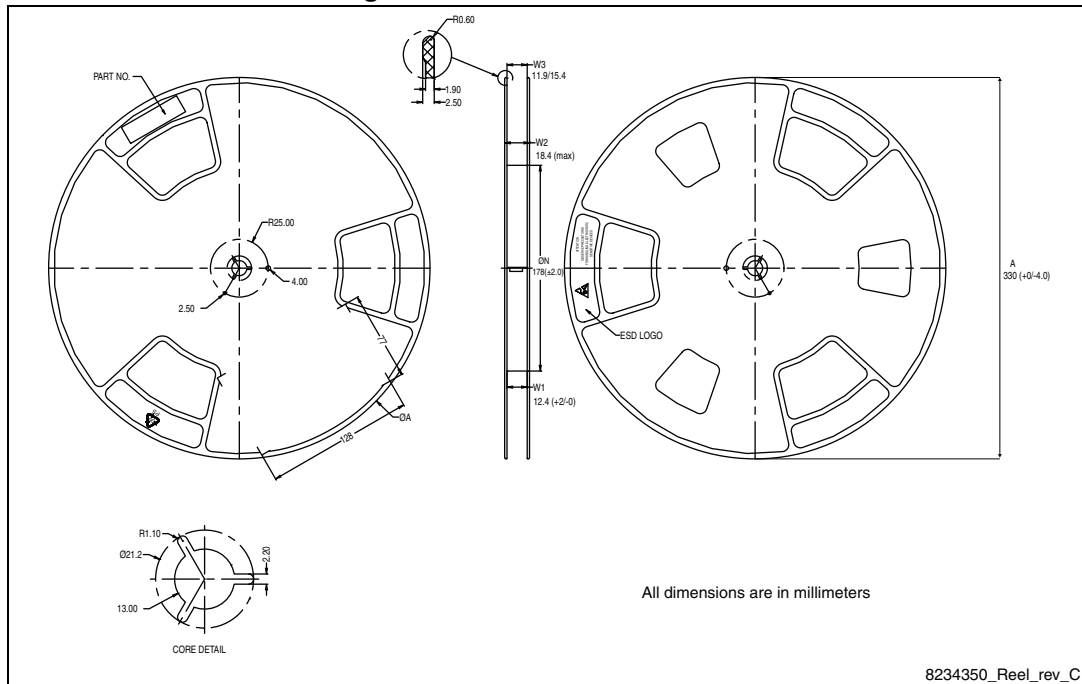


Figure 36. PowerFLAT™ 5x6 package orientation in carrier tape.



a. All dimensions are in millimeters.

Figure 37. PowerFLAT™ 5x6 reel



7 Revision history

Table 9. Revision history

Date	Revision	Changes
31-Oct-2012	1	First revision.
09-Nov-2012	2	<ul style="list-style-type: none"> – Modified: $R_{DS(on)}$ values for N-channel – Changed: Section 5 on page 12
13-Feb-2013	3	<ul style="list-style-type: none"> – Modified: $R_{DS(on)}$ only for P-channel on the title, Features table and Table 4 – Modified: typical values on Table 5, 28, 29, V_{SD} max value on Table 29 (only for P-channel) – Updated: Section 5: Package mechanical data and Section 6: Packaging mechanical data
28-Nov-2013	4	<ul style="list-style-type: none"> – Modified: V_{GS} (for P-channel) value in Table 2 – Modified: I_{GSS} (test conditions values) – Modified: Q_g typical values – Modified: Figure 24, 25, 26, 27, 28, 29, 30 and 31 – Updated: Section 5: Package mechanical data – Minor text changes
03-Apr-2014	5	<ul style="list-style-type: none"> – Added: Section 2.1: Electrical characteristics (curves) for N-channel – Minor text changes

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