凌陽科技
SUNPLUS

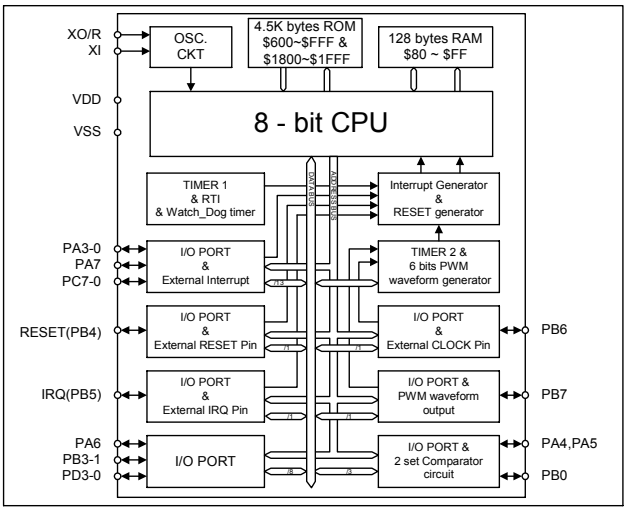
SPMC02A

MICROCONTROLLER

GENERAL DESCRIPTION

SUNPLUS SPMC02A contains a SUNPLUS 8 bit Micro-Controller Units (MCU), 4.5K bytes ROM, 128 bytes SRAM and 2 8-bit Timers. The advanced sub-micron CMOS process technology ensures SPMC02A's high performance, high reliability and advanced functions. In addition, SPMC02A also provides high sink current with slow output transition port pins, multi external interrupt pins, Low Voltage Reset (LVR) function, and multi oscillator options. SPMC02A offers one of the best cost/performance ratios in the industry.

BLOCK DIAGRAM



FEATURES

- Built-in 8-bit Sunplus CPU core and up to 6.0MHz clock operation
- 128 bytes SRAM
- 4.5K bytes ROM for users' program
- On-chip RC oscillator (only one external resistor needed) or crystal input or external clock input
- Up to 14 external interrupt pins.
- 1 I/O can be with RESET input selected by mask option.
- 4 I/Os with Slow output transition Function
- 1 8-bits read-only timer with Real Time Interrupt
- 1 8-bits re-loadable Timer with programmable 8 stage pre-scalar.
- 1 external clock input pin for Timer 2
- 1 6-bit PWM waveform generator
- 1 Watchdog timer
- Built-in two Comparators
- Power-saving STOP & WAIT modes
- Illegal address reset
- Low voltage reset circuit
- Operation Voltage Range: 2.4V - 5.5V
- Provides Chip Form, Package in PDIP or SOIC.

CPU

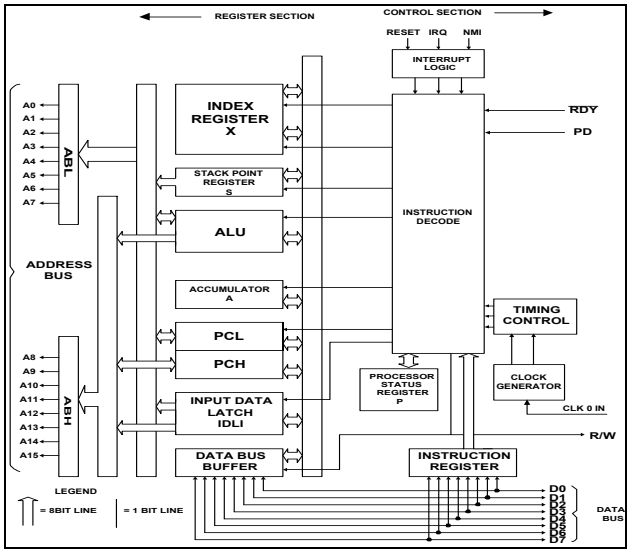
The 8-bit Micro-Controller of SPMC02A is a SUNPLUS proprietary high performance processor equipped with Accumulator, Program Counter, X Register, Stack Pointer and Processor Status Register. (The same as 6502 instruction's structure.) SPMC02A is a fully static CMOS design. The oscillation frequency could be varied from 200KHz up to 6MHz depends on the requirements of applications. The SPMC02A development system includes a SUNPLUS ICE, Evaluation Chip and Engineering Development Board.

1. PROCESSOR STATUS REGISTER

Bit	7	6	5	4	3	2	1	0
flag	N	V	-	B	-	I	Z	C

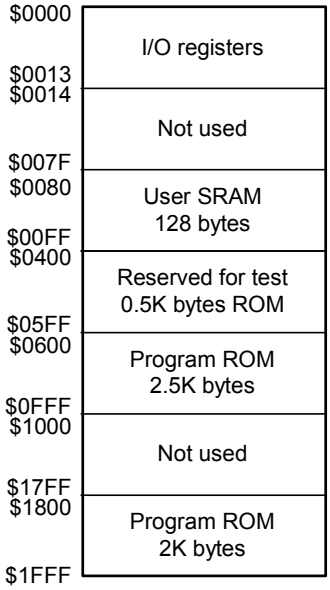
N: negative, V: overflow, B: brk command, I: IRQ disable, Z: Zero, C: Carry

2. BLOCK DIAGRAM OF SUNPLUS CPU



MEMORY

1. MEMORY MAP



2. RAM

Total of 128 bytes of RAM (including the stack) is available from $0080 through $00FF. The stack begins at address $00FF and proceeds down to $0080.

3. ROM

Total of 5120 bytes of on-chip ROM including 4608 (4.5K) bytes of user ROM with 512 bytes of internal test ROM from $400 to $5FF. User's program can only be allocated from $0600 to $0FFF and $1800 to $1FFF.

4. NMI, RESET, IRQ VECTORS

The address of NMI (not provided in this chip), RESET and IRQ are located from $1FFA to $1FFF. That should be specified in the program as following:

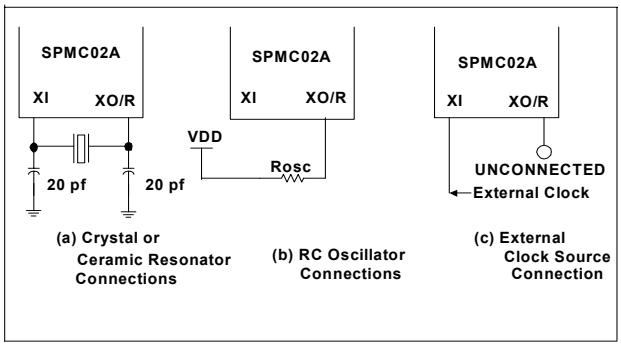
```
ORG  $1FFA              ;define SPMC02A chip
                        ;interrupt vector.
DW   NMI_ROUTINE
DW   RESET
DW   INT_ROUTINE
```

If customer uses Sunplus ICE and Evaluation board, the address $7FFA When using Evaluation board with EPROM (for 27C256), the address of $7FFA must be defined as follows:

```
ORG  $7FFA              ;interrupt vector for
                        ;EPROM with
DW   NMI_ROUTINE        ;Evaluation Board.
DW   RESET
DW   INT_ROUTINE
ORG  $FFFA              ;interrupt vector for
                        ;SUNPLUS ICE.
DW   NMI_ROUTINE
DW   RESET
DW   INT_ROUTINE
```

OSCILLATOR

The SPMC02A supports AT-cut parallel resonant oscillated Crystal /Resonator or RC oscillator or external clock sources by mask option (select one from those three types). The design of application circuit should follow the vendors' specifications or recommendations. The diagrams listed below are typical X'TAL/ROSC circuits for most applications:



MASK OPTIONS

The SPMC02A has the following mask options:

1). Oscillator Select: Crystal / Resonator or External Resistor or External Clock input.
2). PA5 - 0, PB0, PB3, PB6, PB7 & PC7 - 0 Pull-up/down: Pull-down or Pull-up.
3). PA3 - 0 external Interrupt capability: Enable or Disable.
4). External Interrupt Trigger (PA3 - 0 and IRQ): Edge Trigger or Edge-Level Trigger.
5). RESET / PB4 pin: PB4 I/O or I/O with RESET input function.
6). TIMER 1 clock: $f_{CPU}/4$ or $f_{CPU}/1$.
7). Watch - Dog Timer Reset: Enable or Disable.
8). Low Voltage Reset: Reset on Vcc while lower than 2.2V voltage or No detection.

FUNCTION CONTROL REGISTER

All Function register will be set to '0' when a reset is occurred except the RT1 and RT0 will be set to '1' when a reset is occurred.

ADDR	REGISTER	R/W	7	6	5	4	3	2	1	0	ENABLE
$0000	PORT A DATA	R	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	
PA		W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	
$0001	PORT B DATA	R	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	
PB		W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	
$0002	PORT A DATA	R	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	0 = IN
DPA	DIRECTION	W	DPA7	DPA6	DPA5	DPA4	DPA3	DPA2	DPA1	DPA0	1 = OUT
$0003	PORT B DATA	R	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	0 = IN
DPB	DIRECTION	W	DPB7	DPB6	DPB5	DPB4	DPB3	DPB2	DPB1	DPB0	1 = OUT
$0004	TIMER CONTROL	R	TOF(0)	RTIF(0)	TOFE	RTIE	0(0)	0(0)	RT1	RT0	
TCS1	& STATUS	W			(0)	(0)	TOFR	RTIFR	(1)	(1)	1 = SET
$0005	TIMER COUNTER	R	TMR7(0)	TMR6(0)	TMR5(0)	TMR4(0)	TMR3(0)	TMR2(0)	TMR1(0)	TMR0(0)	
TCR1	REGISTER	W									
$0006	IRQ CONTROL &	R	(0)	(0)	IRQF2	IRQE2	IRQF	IRQF1	IRQE1	IRQE	
IRQS	STATUS	W	IRQR1	IRQR	(0)	(0)	(0)	(0)	(0)	(0)	1 = SET
$0007	WATCH DOG	R	CPD1(0)	CPD0(0)	CPIF(0)	(0)	(0)			(0)	1 = CLR
CPWD	TIMER STATUS	W	CPRS1	CPRS0	CPIE	CPIPH	CPE			WDT	/SET
$0008	STOP & WAIT	R									
SNW		W				STOP(0)				WAIT(0)	1 = SET
$0009	PORTA PULLUP /	R	(0)		(0)	(0)	(0)	(0)	(0)	(0)	
RPA	DOWN REGISTER.	W	SLE		RPA5	RPA4	RPA3	RPA2	RPA1	RPA0	0 = EN
$000A	PORTB PULLUP /	R	(0)	(0)		(0)	(0)	(0)	(0)	(0)	
RPB	DOWN REGISTER.	W	RPB7	RPB6		RPB4	RPB3	RPB2	RPB1	RPB0	0 = EN
$000B	PORT C PULL-UP/	R	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	
RPC	DOWN REGISTER.	W	RPC7	RPC6	RPC5	RPC4	RPC3	RPC2	RPC1	RPC0	0 = EN
$000C	PORT C DATA	R	C7	C6	C5	C4	C3	C2	C1	C0	
PC		W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	
$000D	PORT C DATA	R	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	0 = IN
DPC	DIRECTION	W	DPC7	DPC6	DPC5	DPC4	DPC3	DPC2	DPC1	DPC0	1 = OUT
$000E	TIMER CONTROL	R	PS2	PS1	PS0	CKS	(0)	(0)	TOF2	(0)	
TCS2	& STATUS 2	W	(0)	(0)	(0)	(0)	TM2E	TOFR2	(0)	TOFE2	1 = SET
$000F	TIMER COUNTER	R	TM2R7	TM2R6	TM2R5	TM2R4	TM2R3	TM2R2	TM2R1	TM2R0	
TCR2	REGISTER 2	W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	
$0010	PWM WAVEFORM	R	(0)	(0)	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0	
PWMC	CONTROL	W	PWMS	PWME	(0)	(0)	(0)	(0)	(0)	(0)	1 = SET
$0011	PORT D DATA	R					(0)	(0)	(0)	(0)	0 = IN
DPD	DIRECTION	W					DPD3	DPD2	DPD1	DPD0	1 = OUT
$0012	PORT D DATA	R					D3	D2	D1	D0	
PD		W					(0)	(0)	(0)	(0)	
$0013	PORT D PULL-UP	R					(0)	(0)	(0)	(0)	
RPD	REGISTER	W					RPD3	RPD2	RPD1	RPD0	

The value of bracket () is power-on default value.

The gray block is reserved.

I/O AND CONTROL REGISTER
- see Appendix A, ~ G (I/O Diagram)

Total of 28 I/Os (grouped into four ports PA, PB, PC, and PD) are provided. The descriptions are as follows:

1). The 8 I/Os are normal I/O ports: PA6, Port B (PB3 - 0) and Port D (PD3 - 0).

2). There are 13 I/Os used for I/O or I/O with external interrupt.
- The PA3 - 0 can be mask-option for I/O or I/O with external interrupt.
- The PA7 & PC7 - 0 can be programmed as I/O or I/O with external interrupt.

3). There are 3 I/Os used to comparator function.
- The PA4 and PA5 are comparator input pins.
- The PB0 is reference voltage input pin for comparator.

4). The PB4 can be mask option to I/O or I/O with RESET pin.

5). The PB5 can be programmed as I/O or I/O with IRQ pin.

6). The PB6 can be programmed as I/O or I/O with external clock input pin.

7). The PB7 can be programmed as I/O or I/O with PWM waveform output pin.

1. PORT A (PA7 - 0): (see Appendix A, B, C)

ADDR	REGISTER		7	6	5	4	3	2	1	0
$0000	PORT A DATA		DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
$0002	DIRECTION	0	In	In	In	In	In	In	In	In
		1	Out	Out	Out	Out	Out	Out	Out	Out
$0009	Pull-Up/Down	0	Always*	Always	Enable	Enable	Enable	Enable	Enable	Enable
		1	Pull-Up	Pull-Up	Disable	Disable	Disable	Disable	Disable	Disable
	Up/Down resistor		5KΩ	5KΩ	100KΩ	100KΩ	100KΩ	100KΩ	100KΩ	100KΩ
	Source/sink current		-/8mA	-/8mA	-8/8mA	-8/8mA	-8/8mA	-8/8mA	-8/8mA	-8/8mA
	Special Function		Ext. INT	-	Comparator	Comparator	Ext. INT	Ext. INT	Ext. INT	Ext. INT

Note: This bit is defined as SLE bit. Please refer to SLOW TRANSITION ENABLE for more detail.

2. PORT A DATA REGISTER ($0000 PA)

PortA's output data will be determined by $0000 PA Data Register when PortA is programmed as output. Any read of PortA Data Register will return the logical state of the I/O pin when PortA is programmed as input. The PA Data Register is set to '0' when a RESET is occurred.

3. PORT A DATA DIRECTION REGISTER ($0002 DPA)

The PortA can be programmed as input or output by $0002 DPA Register. When DPA = '1', the corresponding pin(s) is (are) programmed as output. When DPA = '0', the corresponding pin(s) is (are) programmed as input. The DPA is set to '0' (input) when a RESET is occurred.

4. PORT A PULL-UP/DOWN CONTROL REGISTER ($0009 RPA)

PA5 - 0 pull-up/down resistors can be mask option to pull-up or pull-down, but PA6, PA7 are always pull-up. The register, RPA, is used to enable or disable the pull-up/down resistors on PA5 - 0. **When RPA = '0'**, it will **enable** pull-up/down resistor of corresponding pins (PA5 - 0) at Input mode. **When RPA = '1'**, it will **disable** the corresponding pull-up/down resistors at input mode only. No pull-up/down resistor is available at output mode. The RPA will be set to '0' (enabling mode) by RESET.

5. PORT B (PB7 - 0): (see Appendix A, B, D, E, and F)

ADDR	REGISTER		7	6	5	4	3	2	1	0
$0001	PORT B DATA		DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
$0003	DIRECTION	0	In	In	In	In	In	In	In	In
		1	Out	Out	Out	Out	Out	Out	Out	Out
$000A	Pull-Up/Down	0	Enable	Enable	-	Pull-Up	Enable	Pull-Up	Pull-Up	Enable
		1	Disable	Disable	-	Disable	Disable	Disable	Disable	Disable
	Up/Down resistor		100KΩ	100KΩ	-	100KΩ	100KΩ	100KΩ	100KΩ	100KΩ
	Source/sink current		-8/8mA	-8/8mA	-/8mA	-8/8mA	-8/8mA	-/25mA	-/25mA	-8/8mA
	Special Function		PWM(O)	Ext. Clock	IRQ	RESET	-	-	-	VRef*

Note*: VRef is reference voltage for comparator.

6. PORT B DATA REGISTER ($0001 PB)

Port B's output data are determined by $0001 PB data register when PortB is programmed as output. Any read of the Port B Data Register will return the Logic State of the I/O pin when PortB is programmed as input. Notice that data register is set to 0 when RESET is occurred.

7. PORT B DATA DIRECTION REGISTER ($0003 DPB)

The Port B can be programmed as inputs or outputs by $0003 DPB register. When DPB = '1', the corresponding pin(s) is (are) programmed as output. When DPB = '0', the corresponding pin(s) is (are) programmed as input. The DPB is set to '0' (input mode) when a RESET is occurred.

8. PORT B PULL-UP/DOWN CONTROL REGISTER ($000A RPB)

PB0, PB3, PB6, PB7 pull-up/down resistor can be controlled by user's program through mask option. PB1, PB2, PB4 have pull-up resistor through program control. PB5 does not have pull-up or pull-down resistor; it is an open-drain output only. The register, RPB, is used to enable or disable the pull-up/down resistors. When **RPB = '0'**, it will **enable** pull-up/down resistor of corresponding pins (PB0, PB3, PB6, PB7) and enable pull-up resistor of corresponding pins (PB1, PB2, PB4) at Input mode. When **RPB = '1'**, it will **disable** the corresponding pull-up/down resistors at input mode only. No pulled up/down resistor is available during output mode. The RPB will be set to '0' (enabling mode) by RESET.

9. RESET / PB4: (see Appendix E)

The RESET/PB4 pin can be selected as I/O or I/O with RESET function by Mask option. The RESET pin is the only external source of a reset when RESET function is selected. This pin is connected to a Schmitt trigger input gate, pull-up 100KΩ by RPB (set $000A b4 = 0) & low active. PB4 pin is a normal I/O function when I/O function is selected.

10. IRQ / PB5: (see Appendix F)

The IRQ/PB5 pin can be selected as I/O or I/O with IRQ function by program.

1). When IRQ function is selected, the IRQ pin is the main external source of an interrupt with active-low polarity. This pin is connected to a Schmitt trigger input. It is an open-drain mode and therefore it needs to be pulled-up externally.

2). When I/O function is selected, the PB5 pin is normal I/O function and open-drain always. Thus, it needs add a resistor externally.

11. PORT C (PC7 - 0): (see Appendix A)

ADDR	REGISTER		7	6	5	4	3	2	1	0
$000C	PORT C DATA		DATA	DATA	DATA	DATA	DATA	DATA	DATA	DATA
$000D	DIRECTION	0	In	In	In	In	In	In	In	In
		1	Out	Out	Out	Out	Out	Out	Out	Out
$000B	Pull-Up/Down	0	Enable	Enable	Enable	Enable	Enable	Enable	Enable	Enable
		1	Disable	Disable	Disable	Disable	Disable	Disable	Disable	Disable
	Up/Down resistor		100KΩ	100KΩ	100KΩ	100KΩ	100KΩ	100KΩ	100KΩ	100KΩ
	Source/sink current		-8/8mA	-8/8mA	-8/8mA	-8/8mA	-8/8mA	-8/8mA	-8/8mA	-8/8mA
	Special Function		Ext. INT	Ext. INT	Ext. INT	Ext. INT	Ext. INT	Ext. INT	Ext. INT	Ext. INT

12. PORT C DATA REGISTER ($000C PC)

When Port C is programmed as output, PortC's data is determined by $000C (PC Data Register). Any read of the Port C Data Register will return the Logic State of the I/O pin when PortC is programmed as input. The PC data register is set to '0' when a RESET is occurred.

13. PORT C DATA DIRECTION REGISTER ($000D DPC)

Port C can be programmed as input or output by $000D DPC Register. When DPC = '1', the corresponding pin(s) is (are) programmed as output. The corresponding pin(s) is (are) programmed as input when DPC = '0'. The DPC is set to '0' (input mode) when a RESET is occurred.

14. PORT C PULL-UP/DOWN CONTROL REGISTER ($000B RPC)

PC7 - 0 pull-up/down resistors can be mask option to pull-up or pull-down. The register, RPC, is used to enable or disable the pull-up/down resistors on PC7-0. When RPC = '0', it will enable pull-up/down resistor of corresponding pins (PC7 - 0) at Input mode. When RPC = '1', it will disable pull-up/down resistor of corresponding pins (PC7 - 0) at input mode only. No pulled up/down resistor is available during output mode. The RPC will be set to '0' (enabling mode) by RESET.

15. PORT D (PD3 - 0): (see Appendix G)

ADDR	REGISTER		7	6	5	4	3	2	1	0
$0012	PORT D DATA						DATA	DATA	DATA	DATA
$0011	DIRECTION	0					In	In	In	In
		1					Out	Out	Out	Out
$0013	Pull-Up/Down	0					Pull-Up	Pull-Up	Pull-Up	Pull-Up
		1					Disable	Disable	Disable	Disable
	Up/Down resistor						100KΩ	100KΩ	100KΩ	100KΩ
	Source/sink current						-8/8mA	-8/8mA	-8/8mA	-8/8mA

16. PORT D DATA REGISTER ($0012 PD)

PortD's output data is determined by $0012 (PD Data Register) when PortD is programmed as output. Any read of the Port D Data Register will return the Logic State of the I/O pin when PortD is programmed as input. The PD data register is set to '0' when a RESET is occurred.

17. PORT D DATA DIRECTION REGISTER ($0011 DPD)

Port D can be programmed as input or output by $0011 DPD register. The corresponding pin(s) is (are) programmed as output when DPD = '1'. The corresponding pin(s) is (are) programmed as input when DPD = '0'. The DPD is set to '0' (input mode) when a RESET is occurred.

18. PORT D PULL-UP CONTROL REGISTER ($0013 RPD)

PD3 - 0 pull-up resistors can be programmed as enabled (0) or disabled (1) by $0013 RPD Register. When **RPD = '0'**, it will **enable** pull-up resistor of corresponding pin (PD3 - 0) at Input mode. When **RPD = '1'**, it will **disable** the corresponding pull-up resistor at input mode. No pull-up resistor is available during output mode. The RPD will be set to '0' (enable mode) by RESET.

19. HIGH SINK CURRENT PORT: (see Appendix D)

Both of PB1 & PB2's output current is able to sink 25mA. If connecting PB1 and PB2 together, 50mA of sink current will be generated. Output sink current setting methods are as follows (DPB2 = DPB1 = 1):

1). The single sink current is 25mA when PB1 = 0 & PB2 = 1, or PB1 = 1 & PB2 = 0.
2). The PB1, PB2 single sink current is 25mA when PB1 = PB2 = 0.
3). The 50mA sink current can be created when PB1 and PB2 are set to '0' and both are short together.

Example: PB0, PB7 - 3 set as input. PB1, PB2 as output.

```
        LDA  #%00000110      ;0 as input, 1 as
                             ;output.
        STA  DPB             ;DPB EQU $0003.
        LDA  #%11111001      ;
        STA  RPB             ;
        LDA  #%00000100
        STA  PB              ;PB2 out "low" & sink
current as 25mA.
        LDA  #%00000010
        STA  PB              ;PB1 out "low" & sink
current as 25mA.
        LDA  #%00000000
        STA  PB              ;PB1, PB2 out "low" &
                             ;sink 25mA when
                             ;single output Or
                             ;sink 50mA when PB1,
                             ;PB2 short and
                             ;together output.
```

20. EXTERNAL INTERRUPT INPUT PORTS: (see Appendix A, C, I)

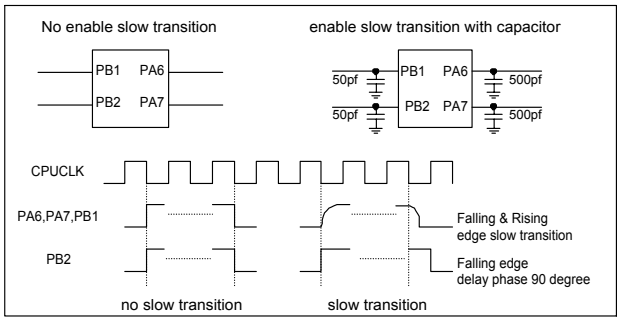
The PA3 - 0, PA7, PB5, and PC7 - 0 can be used as I/O or I/O with external Interrupt sources. For external interrupt sources, PA3 - 0 interrupt are enabled or disabled by mask option and controlled by IRQE ($0006). PA7 is enabled or disabled by IRQE1 ($0006). PB5 is enabled or disabled by IRQE ($0006). PC7 - 0 is enable or disable by register IRQE2 ($0006). For more details on interrupt statements, please see INTERRUPT section.

21. SLOW TRANSITION ENABLE (SLE) - $0009 (RPA) bit7 (see Appendix D)

PA6, PA7, PB1 and PB2 pin have Slow Transition signal output function (SLE). If this function is enabled ($0009 bit7 = 1), the transition time of outputs is 250ns ± 20% with 50pf (PB), 500pf (PA) load at 2.0MHz. When SLE ($0009 bit7) = 0, the slow transition output is disabled.

Example: PA6, PA7 & PB1, PB2 set as output and have slow transition function.

```
        LDA  #%11000000
        STA  DPA             ;DPA $0002, set PA6,
                             ;PA7 as output
        LDA  #%00000110
        STA  DPB             ;DPB $0003, set PB1,
                             ;PB2 as output
        LDA  #%1XXXXXXX      ;X = user-define
        STA  RPA             ;and set SLE as "1" for
                             ;enable slow
                             ;transition.
        LDA  #FFh
        STA  TEMP            ;TEMP = a register of
                             ;$80h~FFh
Loop1:  LDA  TEMP
        EOR  #C6h            ;cross-change B6, B7
                             ;& B1, B2
        STA  TEMP
        STA  PA              ;PA6, PA7 output
                             ;pulse.
        STA  PB              ;PB1, PB2 output
                             ;pulse
        LDX  #00h            ;delay
Loop2:  DEX
        BNE  Loop2
        JMP  Loop1           ;repeat output of
                             ; PA6, PA7, PB1.
```



RESET - see Appendix E (Reset Block Diagram)

1. EXTERNAL RESET (RESET pin) (see Appendix E, H)

The RESET/PB4 pin can be selected to I/O or I/O with RESET function by Mask option. When RESET is selected through Mask option, the RESET pin is the only external reset source with active-low polarity. This pin is connected to a Schmitt trigger input gate & low active.

Note*: When using RESET function, the DPB b4 must be set to input mode (b4 = 0), and RPB b4 set to pull-up resistor (b4 = 0)

2. POWER ON RESET (see Appendix H)

This reset is an internal reset. The Power-On-Reset will generate the reset signal that will reset the CPU until oscillator stabilized. To confirm the Power on Reset is generated properly, the system power should be held at a zero potential with respect to ground. Improper initial setting of the power might cause the system can not work properly. The CPU will become active after 4096 clock cycles.

3. WATCH DOG TIMER RESET ($0007 bit0 WDT) (see Appendix H, J)

The Watch-Dog Timer can be disabled or enabled through mask option. The internal reset of Watch-Dog is generated by a time-out of the Watch-Dog Timer automatically when Watch-Dog is enabled. It is implemented on this device by using the output of the RTI circuit and further dividing it by eight (RT1, RT0 timing times 8). This time-out generates reset if the WDT register is not cleared. An internal reset is generated and reset vector is fetched. Preventing a WDT time-out reset is done by writing a '1' to WDT ($0007 b0) within a specific time.

The minimum WDT reset time is listed in (RT1, RT0) & WDT Interrupt Frequency Table.

ADDR	REGISTER	R/W	7	6	5	4	3	2	1	0	ENABLE
$0007	WATCH DOG	R	CPD1(0)	CPD0(0)	CPIF(0)	(0)	(0)				
WDT	TIMER STATUS	W	CPRS1	CPRS0	CPIE	CPIPH	CPE			WDT(0)	1 = CLR

Example: clear Watch-Dog Timer

```
MainLoop:   JSR  Clear_WDT
            ....              ;Long program will
                              ;over Watch-Dog
                              ;Timer
            JSR  Clear_WDT    ;so need call clear
                              ;WDT subroutine
                              ;again.
            ....              ;some work.
            JMP  MainLoop
Clear_WDT:  LDA  CPWD_STU
            ORA  #01h         ;only set b0 = 1.
            STA  CPWD         ;WDT ($0007), clear
                              ;$0007 b0 WDT
                              ;register.
            RTS
```

4. ILLEGAL ADDRESS RESET (IAR) (see Appendix H)

The internal reset of IAR is generated when an instruction op-code fetch occurs from an address that is not implemented in the RAM ($0080-$00FF) nor ROM ($0400-$17FF). The IAR will generate the reset signal that will reset the CPU and other peripherals.

5. LOW VOLTAGE RESET (LVR) (see Appendix H)

The internal LVR reset is generated when VDD falls below the specified LVR trigger voltage (herein, 2.2V) for at least one CPU clock cycle.

INTERRUPT - see Appendix A, C, F, I (Interrupt Diagram)

1. SOFTWARE INTERRUPT (BRK)

The BRK is an executable instruction interrupt since it is executed regardless of the state of the I-bit in the processor status register flag (inside CPU). When BRK is occurred, it jumps to IRQ_routine.

2. EXTERNAL INTERRUPT

The external interrupt sources include IRQ/PB5 pin, PA3 - 0, PA7 and PC7 - 0. The PA3 - 0 can be mask option as I/O or I/O with an external interrupt function. The IRQ/PB5 pin provides an interrupt to the CPU by program control (see I/O Port B section). PA7 and PC7 - 0 can also be programmed as an external interrupt (see I/O Port A section and I/O Port C section). The PA7 and IRQ/PB5 pin are designed with Schmitt Trigger input and low active, but PA3 - 0 and PC7 - 0 are high active.

ADDR	REGISTER	R/W	7	6	5	4	3	2	1	0	ENABLE
$0006	IRQ CONTROL &	R	0(0)	0(0)	IRQF2	IRQE2	IRQF(0)	IRQF1(0)	IRQE1	IRQE	
IRQS	STATUS	W	IRQR1	IRQR	(0)	(0)			(0)	(0)	1 = SET

1). The b0 IRQE is PA3 - 0 & IRQ pin interrupt enabling control. (1 as enable, 0 as disable).
2). The b1 IRQE1 is PA7 interrupt enabling control. (1 as enable, 0 as disable).
3). The b2 IRQF1 is PA7 IRQ flag. When b2 = 1, it indicates PA7 generates interrupt. When b2 = 0, no interrupt is generated. It is read-only.
4). The b3 IRQF is PA3 - 0 & IRQ pin IRQ flag. When b3 = 1, it indicates PA3 - 0 & IRQ pin generate interrupt. When b3 = 0, no interrupt is generated. It is read-only.
5). The b4 IRQE2 is PC7 - 0 interrupt control bit. (B4 = 1 as enable interrupt, b4 = 0 as disable).
6). The b5 IRQF2 is PC7 - 0 IRQ flag. (B5 = 1 has interrupt generated. B5 = 0, no interrupt). It is read-only.
7). The b6 IRQR is a write-only bit for clearing IRQF flag. (1 as clear active, 0 as no clear).
8). The b7 IRQR1 is a write-only bit for clearing IRQF1 flag. (1 as clear active, 0 as no clear)

3. IRQ, PA3 - 0 INTERRUPT (see Appendix A, F, I)

The IRQ/PB5 pin can be selected as I/O or I/O with IRQ function by program. When IRQ function is selected, the IRQ pin is the main external source of an interrupt with active-low polarity. This pin is connected to a Schmitt trigger input. It is an open-drain mode and therefore an external pull-up resistor is required. When PB5 I/O function is selected, the PB5 pin is normal I/O with open-drain always. When IRQE1 is disabled, the IRQF will be cleared during creating interruption. However, if IRQE1 is enabled, the IRQF will not be cleared by interrupt. This interrupt source can be either " Edge-Trigger" or "Level-Trigger". It is selected by mask option. If mask option is set to 'Edge-Trigger' mode, the following conditions will generate IRQ interrupt:

1). Falling edge on the IRQ pin.
2). Rising edge on any of PA3 - 0 pin.
(During PA3 - 0 mask option enabled.)

If mask option is set to “Edge-Level Trigger” mode, the following conditions will generate IRQ interrupt:

1). Falling edge and Low level trigger on the IRQ pin.
2). Rising edge and High level on any of PA3 - 0 pins.
(PA3 - 0 mask option enabled.)

When IRQ pin or PA3 - 0 pins generate an interrupt (CPU will set IRQF ($0006 bit3) = 1), the IRQE (if $0006 bit0 = 1,enabled) controls whether the interrupt request being sent to CPU. The IRQR ($0006 bit6) is the IRQ pin and PA3 - 0 pin interrupt acknowledge. When IRQR = 1, it clears the interrupt flag IRQF ($0006 bit3 = 0).

4. PA7 INTERRUPT (see Appendix C, I)

The PA7 interrupt input is falling-edge trigger. It is controlled by IRQE1 ($0006 bit1). When PA7 interrupt occurred, the IRQF1 ($0006 bit2) will be set. The IRQR1 ($0006 bit7) is the PA7 pin interrupt acknowledge. When IRQR1 = 1, it will clear the PA7 interrupt flag IRQF1 ($0006 bit2 = 0).

5. PC7 - 0 INTERRUPT (see Appendix A, I)

The PC7 - 0 interrupt inputs are rising edge trigger. It is controlled by IRQE2 ($0006 bit4). When PC7 - 0 interrupt occurred, the IRQF2 ($0006 bit5) will be set. To clear IRQF2, disable IRQE2 first and then set IRQE2 again. As stated above, IRQF2 will be cleared to '0'.

Example: use IRQ pin, PA3 - 0, PA7 and PC7 - 0 as interrupt.

```
            LDA  #00
            STA  DPA           ;set PA, PC port to
                               ;input
            STA  DPC
            LDA  #%11010011    ;enable IRQ, PA3 - 0,
                               ;PA7, PC7 - 0 IRQ and
                               ;clear INT Flag
            STA  IRQS          ;IRQS = $0006
            ....               ;other working
IRQVacter:  LDA  IRQS          ;Interrupt
                               ;subroutine
            STA  IRQS_STU      ;IRQ status register
            AND  #%00000100    ;check interrupt of
                               ;PA7
            BNE  PA7_IRQ
            LDA  IRQS_STU
            AND  #%00100000    ;check interrupt
                                PC7 - 0
            BNE  PC_IRQ
PA03_IRQ:   LDA  IRQS_STU
            AND  #%00001000    ;check interrupt of
                               ;PA3 - 0
            BEQ  IRQ_END       ;no PA3 - 0, PA7,
                               ;PC7 - 0 & external IRQ
                               ;pin
            LDA  PA
            AND  #%00001111    ;check PA3 - 0 create
                               ;IRQ
            BNE  PA03_In
IRQP_In:    ....               ;IRQ pin interrupt
                               ;works something.
            JMP  PA03_END
PA03_In:    ....               ;PA3 - 0 interrupt
                               ;work something.
PA03_END:   LDA  #%01010011    ;set PA3 - 0, PA7,
                               ;PC7 - 0 clear
                               ;PA3 - 0 Flag. Don't
            JMP  IRQ_END       ;clear PA7, PC7 - 0
                               ;Flag for next IRQ of
                               ;PA7, PC7 - 0.
PA7_IRQ:    ....               ;PA7 interrupt works
                               ;something.
            LDA  #%10010011    ;set PA3 - 0, PA7,
                               ;PC7 - 0 & clear PA7
                               ;Flag, Don't
            JMP  IRQ_END       ;clear PA3 - 0, PC Flag
                               ;for next IRQ of
                               ;PA3 - 0, PC
PC_IRQ:     ....               ;PC7 - 0 interrupt
                               ;work something.
            LDA  IRQS_STU
            AND  #%11001111    ;clear PC7 - 0 IRQ Flag
            STA  IRQS
            ORA  #%00010011    ;set PA3 - 0, PA7,
                               ;PC7 - 0 & clear PC
                               ;Flag, Don't clear
                               ;PA3 - 0, PA7 Flag for
                               ;next IRQ
 IRQ_END:   STA  IRQS
            RTI
```

6. TIMER INTERRUPT (TIMER) (see Appendix J, K)

The TIMER INTERRUPT is generated when Timer1 or Timer2 overflows or a real time interrupt has occurred. The timer interrupt flags (TOF1, TOF2, RTIF), enable bits (TOFE1, TOFE2, RTIE) and timer interrupt acknowledge bits (TOFR1, TOFR2, and RTIFR) are designed for the timer interrupt. There are located in the Timer Control & Status Register 1 (TCS1) (address at $0004) and Timer Control & Status Register 2 (TCS2) (address at $000E). The I-bit in the Processor Status Flag (inside CPU) must be cleared to '0' for enabling interrupt (use CLI instruction). For more details on settings of the Timer Control & Status Register (TCS), please see the MULTI-FUNCTION TIMER section.

7. COMPARATOR INTERRUPT (see Appendix B)

The comparator generates the COMPARATOR INTERRUPT. It can compare external input (PA4 or PA5) (set CPWD $0007 b3 CPE & b5 CPIE for enabling) voltage with internal reference voltage 1.2V or external reference voltage on PB0 (selected by CPWD $0007 b6 CPRS0 and b7 CPRS1). It is controlled by CPIPH (CPWD $0007 b4) that whether the input voltage is higher (lower) than reference voltage. When $0007 b5 (CPIE) is enabled (=1) for comparison, it needs to be disabled (set to '0') when sleep. Without disable CPIE, it may consume current while sleeping.

ADDR	REGISTER	R/W	7	6	5	4	3	2	1	0	ENABLE
$0007	WATCH DOG	R	CPD1(0)	CPD0(0)	CPIF(0)	(0)	(0)			(0)	1 = CLR
CPWD	TIMER STATUS	W	CPRS1	CPRS0	CPIE	CPIPH	CPE			WDT	/SET

1). The WDT is a Watch-Dog Timer clear register. See WATCH DOG TIMER RESET section.
2). The b3 CPE is a control bit to enable or disable comparator function. It is a write-only bit.
3). The b4 CPIPH controls less or over than VREF. It is a write-only bit.
4). The CPIE is a comparator IRQ enabling bit (1: enable, 0: disable). It's available in write mode. The CPIF is IRQ flag for program check (1 indicates interrupt, 0 indicates no interrupt). It is available in read mode.
5). The CPRS0 selects comparator 0(PA4) reference voltage VREF, using internal default 1.2V or external reference from PB0 input (1 as choose PB0, 0 as choose 1.2V). It's is available in write mode. The CPD0 is the flag for compare result (0 as happen, 1 as no happen). It is available in read mode.
6). The CPRS1 selects comparator 1(PA5) reference voltage, using internal default 1.2V or external reference from PB0 input. (1 as choose PB0, 0 as chooses 1.2V). It is available in write mode. The CPD1 is the flag for compare result. (0 as happen, 1 as not happen). It is available in read mode.

The comparator programming method can be accomplished as follows:

1). Check CPIF through IRQ routine, then check CPD0 and CPD1 to identify which one is generated.
2). Use polling method. Check CPD0 and CPD1 to identify that is generated occasionally.

Example: use IRQ routine to acknowledge comparator result

```
                LDA  #%10101001    ;enable comparator &
                                   ;IRQ, PA4 VREF = 1.2V,
                STA  CPWD          ;PA5 VREF = PB0,
                                   ;CPWD = $0007.
                ....
                CLI
IRQVacter:      LDA  CPWD
                STA  CPWD_STU      ;comparator status
                                   ;register.
                AND  #%00100000    ;only check CPIF.
                BEQ  IRQ_END       ;PA4, PA5 is not
                                   ;bigger then VREF. So
                                   ;no IRQ flag.
                LDA  CPWD_STU
                AND  #%01000000    ;check PA4
                                   ;comparator 0.
                BNE  PA5_COM       ;no CPD0 happen.
PA4_COM:        ....               ;VINPA4 > 1.2V so
                                   ;working some thing.
                JMP  IRQ_END
PA5_COM:        LDA  CPWD_STU
                AND  #%10000000    ;check PA5
                                   ;comparator 1.
                BNE  IRQ_END       ;no CPD1 happen.
                ....               ;VINPA5 > VREFPB0 so
                                   ;working some thing.
IRQ_END:        LDA  #%00000001    ;clear CPIF and WDT.
                STA  CPWD
                LDA  #%00101001
                STA  CPWD          ;set comparator
                                   ;again.
                RTI
```

Example: use polling method to acknowledge comparator result

```
            LDA  #%10011001    ;PA4 VREF = 1.2V, PA5
                               ;VREF = PB0, enable
                               ;CPE
            STA  CPWD          ;don't use IRQ,
                               ;compare less then
                               ;VREF.
            ....               ;some thing works.
            JSR  CP_PGM
            ....               ;Some thing works.
            JSR  CP_PGM
            ....               ;Some thing works.
CP_PGM:     LDA  CPWD
            STA  CPWD_STU
            AND  #%01000000
            BNE  PA5_COM       ;no CPD0 happen.
PA4_COM:    ....               ;VINPA4 < 1.2V so
                               ;working some thing.
            JMP  CP_END
PA5_COM:    LDA  CPWD_STU
            AND  #%10000000    ;check PA5
                               ;comparator.
            BNE  CP_END        ;no CPD1 happen.
            ....               ;VINPA5 < VREFPB0 so
                               ;working some thing.
CP_END:     LDA  #%00000001    ;clear CPIF and WDT.
            STA  CPWD
            LDA  #%00101001
            STA  CPWD         ;set comparator
                               ;again.
            RTS
```

MULTI-FUNCTION TIMER

Two types of timers are supported in SPMC02A. Description is as follows:

The timer1 for this device is a 15-bit multi-function ripple up-counter. The feature functions include Timer Overflow, Real Time Interrupt (RTI), Power on Reset and Watch-Dog Timer Reset (WDT).

When the Timer Counter Register 1 (TCR1 $0005) overflows, the Timer Overflow Flag (TOF1) will be set. TOF1 = 1 will generate an interrupt request to CPU in case of Timer Overflow Enable being set (TOFE1 = 1). Whenever TOFR1 is set to '1', the TOF1 flag bit will be cleared.

The Real Time Interrupt Flag (RTIF) will be set when 1 of 4 selections (RT1, RT0) is active. RTIF = 1 will generate an interrupt request to CPU if Real Time Interrupt Enable is set (RTIE = 1). Whenever RTIFR = 1, it will clear the RTIF flag bit. When a RESET is occurred, RT1 and RT0 of TCS1 are set as '1' and rest of the bits on TCS are set as '0'.

When the Timer Counter Register 2 (TCR2 $000F) overflows, the Timer Overflow Flag (TOF2) will be set. And TOF2 = 1 will produce an interrupt request to CPU when Timer Overflow Enable is set (TOFE2 = 1). Whenever TOFR2 is set to '1', the TOF2 flag bit will be cleared.

The Timer2's content can be loaded by program, and re-loaded the same content by itself when interrupt occurs. The Timer 1 cannot be loaded and re-loaded any data; it is an auto-counter.

1. TIMER 1 - see Appendix J (Timer 1 Block Diagram)

The Timer1 input clock can be mask option to be divided by 4 or original Timer1 input clock. Therefore, frequency of Timer1 is $f_{CPU}/2^{10}$ or $f_{CPU}/2^{8}$. Frequency of Timer2 is $f_{CPU}/2^{14}$~2^{17} or $f_{CPU}/2^{12}$~2^{15}.

The 15-Stage timer contains two registers: Timer Counter Register 1 & Timer Control/Status Register 1.

■ TIMER COUNTER REGISTER 1 (TCR1) - $0005

The timer counter register 1 is a read-only register that contains 8-bit content at the beginning of the timer chain. The content of each bit of the TCR1 is shown in the following table. The register is cleared by reset.

ADDR	REGISTER	R/W	7	6	5	4	3	2	1	0	ENABLE
$0005	TIMER COUNTER	R	TMR7(0)	TMR6(0)	TMR5(0)	TMR4(0)	TMR3(0)	TMR2(0)	TMR1(0)	TMR0(0)	
TCR1	REGISTER	W									

Timer Counter Register 1 (TCR1)

■ TIMER CONTROL/STATUS REGISTER 1 (TCS1)- $0004

The TCS1 contains the timer interrupt flag (TOF1, RTIF), the timer interrupt enable (TOFE1, RTIE), timer interrupt acknowledge (TOFR1, RTIFR) and the real timer interrupt rate selection bits (RT1, RT0). Bit 2 and bit 3 are write-only bits that will be read as logical zeros. The following table shows the content of each bit in the TCS. RT1 and RT0 of TCS are set as '1' and rest of the bits on TCS are set as '0' by reset initially.

ADDR	REGISTER	R/W	7	6	5	4	3	2	1	0	ENABLE
$0004	TIMER CONTROL	R	TOF(0)	RTIF(0)	TOFE	RTIE	0(0)	0(0)	RT1	RT0	
TCS1	& STATUS	W			(0)	(0)	TOFR	RTIFR	(1)	(1)	1 = SET

Timer Control/Status Register 1 (TCS1)

2. TOF1 - Timer 1 Overflow Flag (The TOF1 is a read-only flag bit.)

1 = Set when the 8-bit ripple counter rolls over from $FF change to $00. A timer interrupt request will be generated if TOFE1 is also set.

0 = Reset by writing a logical one to the TOF1 acknowledgment bit, TOFR1.

3. RTIF - Real Time Interrupt Flag (The RTIF is a read-only flag bit.)

1 = Set when the output of the chosen Real Time Interrupt stage goes active. A timer interrupt request will be generated if RTIE is also set.

0 = Reset by writing a logical '1' to the RTIF acknowledgment bit, RTIFR.

4. TOFE1 - Timer 1 Overflow Enable

The TOFE1 is an enable bit that allows generating timer interrupt upon overflow of the Timer Counter Register 1.

1 = When set, the timer interrupt is generated when the TOF1 flag bit is set.

0 = When cleared, there is no timer interrupt being generated for TOF1 flag.

5. RTIE - Real Time Interrupt Enable

The RTIE is an enable bit that allows generation of a timer interrupt by the RTIF bit.

1 = When set, the timer interrupt is generated when the RTIF flag bit is set.

0 = When cleared, there is no timer interrupt being generated even though RTIF flag is set.

6. TOFR1 - Timer 1 Overflow Acknowledge

The TOFR1 is an acknowledge bit that resets TOF1 flag. Reading the TOFR1 will always return a logical zero.

1 = Clears the TOF1 flag bit.

0 = Does not clear the TOF1 flag bit.

7. RTIFR - Real Time Interrupt acknowledge

The RTIFR is an acknowledge bit that resets the RTIF flag. Reading the RTIFR will always return a logical zero.

1 = Clears the RTIF flag bit.

0 = Does not clear the RTIF flag bit.

8. RT1: RT0 - Real Time Interrupt Rate Select

The RT0 & RT1 control bits select one of four types to let the Real Time Interrupt circuit run. The following table shows the available interrupt rates for two frequency values of timer 1 clock selected by mask option.

Example: CPU Clock f_{CPU} = 1.0MHz (Oscillation Frequency = 2.0MHz) with two options for Timer 1 clock						
	RTI RATES			MIN. WDT RESET (=RTI/8)		
RT1:RT0	Divider	option $f_{CPU}/4$	option $f_{CPU}/1$	Divider	option $f_{CPU}/4$	option $f_{CPU}/1$
00	2048	8.192ms	2.048ms	16384	65.536ms	16.384ms
01	4096	16.384ms	4.096ms	32768	131ms	32.768ms
10	8192	32.768ms	8.192ms	65536	262ms	66ms
11	16384	65.536ms	16.384ms	131072	524ms	131ms

(RT1, RT0) & WDT Interrupt Frequency Table at f_{CPU} = 1.0MHz

Example: enable Timer Counter 1 & RTI (RT1 = 1, RT0 = 0), use 2.0MHZ Rosc.

```
                LDA  #%00111110    ;TCS1 $0004 set
                                   ;TOFE1, RTIE, RT1,
                                   ;RT0 = 10,
                STA  TCS1          ;& clear
                                   ;interrupt Flag
                ....               ;other
                                   ;instruction for
                                   ;initialized or
                                   ;work
                CLI                ;software enable
                                   ;interrupt
IRQ_Vacter:     LDA  TCS1          ;Interrupt
                                   ;subroutine.
                AND  #%10000000    ;check Timer
                                   ;Overflow
                                   ;interrupt flag.
                BNE  TO1_IRQ
RTI_IRQ:        LDA  TCS1
                AND  #%01000000    ;check Real Time
Interrupt
                BEQ  IRQ_END
                ....               ;working for used
                                   ;RTI
                LDA  #%00110110    ;enable RTI, TO
                                   ;again, only
                                   ;clear RTIF
                JMP  IRQ_END
TO1_IRQ:        ....               ;working for used
                                   ;Timer1 Overflow
                LDA  #%00111010    ;enable RTI, TO
                                   ;again, only
                                   ;clear TOF
IRQ_END:        STA  TCS1
                RTI
```

9. TIMER 2 - see Appendix K (Timer 2 Block Diagram)

The Timer2 clock source can select to f_{CPU} or External clock input (PB6) by program. It also can be divided with the scale defined by PS2-0 (TCS2 $000F b7-5), and it has a re-loadable timer counter register, so Timer 2 frequency is f_{CPU} ~ $f_{CPU}/2^{16}$ (f_{PB6} ~ $f_{PB6}/2^{16}$).

The timer2 contain two registers: Timer Counter Register 2 & Timer Control/Status Register 2.

■ TIMER COUNTER REGISTER 2 (TCR2) - $000F

The timer counter register 2 is re-loadable register. It can initialize data and re-load it data by itself when occur interrupt. The value of each bit of the TCR2 is shown in following table. The register is cleared by reset.

ADDR	REGISTER	R/W	7	6	5	4	3	2	1	0	ENABLE
$000F	TIMER COUNTER	R	TM2R7	TM2R6	TM2R5	TM2R4	TM2R3	TM2R2	TM2R1	TM2R0	
TCR2	REGISTER 2	W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	

Timer Counter Register 2 (TCR2)

■ TIMER CONTROL/STATUS REGISTER 2 (TCS2)- $000E

The TCS2 contains the timer interrupt flag (TOF2), the timer interrupt enable (TOFE2), the timer interrupt acknowledge (TOFR2), clock source (CKS) and pre-scale selector (PS2 - 0). Bit 2 is write-only bit that will be read as logical zeros. Bit 1 is read-only whose data is not being cared in the write mode. The following table shows the content of each bit in the TCS2, which is set to 0 by reset.

ADDR	REGISTER	R/W	7	6	5	4	3	2	1	0	ENABLE
$000E	TIMER CONTROL	R	PS2	PS1	PS0	CKS	(0)	(0)	TOF2	(0)	
TCS2	& STATUS 2	W	(0)	(0)	(0)	(0)	TM2E	TOFR2	(0)	TOFE2	1 = SET

Timer Control/Status Register 2 (TCS2)

10. PS2 - 0 - Pre-scale selector

These 3 bits can be selected to eight types of pre-scale status. The 000 as 2^0, 001 as 2^1, ... 110 as 2^7, 111 as 2^8.

11. CKS - Timer 2 clock source selector

The CKS is a selected bit for Timer 2 counter clock source.

1 = Select external clock source input from PB6

0 = Select internal clock source from f_{CPU}.

12. TM2E - Timer 2 counter clock enable flag

The TM2E is a control bit for counter clock. TOFE2 is ineffective when this bit is 0. TOFE2 is able to control whether Timer 2 interrupt is generated or not during this bit is set to 1.

1 = Enable Timer 2 counter clock input.

0 = Disable Timer 2 counter clock input.

13. TOFR2 - Timer 2 Overflow Acknowledge (The TOFR2 is a write-only bit.)

The TOFR2 is an acknowledgment bit that resets TOF2 flag. Reading TOFR2 will always return a logical zero.

1 = Clears the TOF2 flag bit.

0 = Does not clear the TOF2 flag bit.

14. TOF2 - Timer 2 Overflow Flag (The TOF2 is a read-only flag bit.)

1 = Set when the 8-bit ripple counter rolls over from $FF change to $00. A timer interrupt request will be generated if TOFE2 is also set.

0 = Reset by writing a logical one to the TOF2 acknowledge bit, TOFR2.

15. TOFE2 - Timer 2 Overflow Enable

The TOFE2 is an enable bit that allows generating timer interrupt upon overflow of the Timer Counter Register 2. This bit is ineffective when TM2E is disable (0).

1 = When set, the timer interrupt is generated when the TOF2 flag bit is set.

0 = When cleared, no timer interrupt is generated even though TOF2 is set.

Example: enable Timer 2 & pre-scale 2^4 & load data #30h and use internal clock

```
            LDA  #30h           ;initial TCR2 data.
            STA  TCR2           ;TCR2 = $000F.
            LDA  #%10001101     ;TCS2 = $000E,
                                ;pre-scale 2^4,
            STA  TCS2           ;enable TM2E, TOFE2,
                                ;clear TOFR2.
            ....                ;other working.
            CLI
IRQ_Vacter: LDA  TCS2           ;interrupt
                                ;subroutine
            AND  #%00000010     ;check Timer
                                ;Overflow interrupt
                                ;flag.
            BEQ  IRQ_END
TM2_IRQ:    ....                ;working for used
                                ;Timer 2 Overflow.
                                ;The TCR2 will
                                ;re-load #30h again.
IRQ_END:    LDA  #%10001101     ; re-set TCS2 again &
                                ;clear TOFR2.
            STA  TCS2
            RTI
```

16. PWM - see Appendix L (PWM GENERATOR Block Diagram)

The clock source of PWM generator is obtained from Timer 2 circuit. The Timer 2 counter value is generated by 3 duty cycles wave generator or 64 duty cycles wave generator which are selected by PWMS ($0010 b7) and then sent to PWM pulse output PB7 by PWME $0010 b6 controlled. The duty cycle of wave generator can be divided from (1/64high, 63/64 low) to (63/64 high, 1/64 low) with step 1/64 by PWM5 - 0 selected. The content of each bit in the PWMC is shown in following table, which is set to 0 by reset.

ADDR	REGISTER	R/W	7	6	5	4	3	2	1	0	ENABLE
$0010	PWM WAVEFORM	R	(0)	(0)	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0	
PWMC	CONTROL	W	PWMS	PWME	(0)	(0)	(0)	(0)	(0)	(0)	1 = SET

PWM Waveform Control Register (PWMC)

17. PWMS - 3 duty cycle or 64 duty cycle generator selector

The PWMS is selected as 3-duty cycles generator or as 64-duty cycles by programming.

1 = selecting 64-duty cycles wave generator. Duty value is controlled through bits PWM5 - 0. It can output high wave from 1/64 duty to 63/64 duty.

0 = selecting 3-duty cycles wave generator. It is fixed output 1/3 high & 2/3 low duty cycle.

18. PWME - PWM wave output enable flag

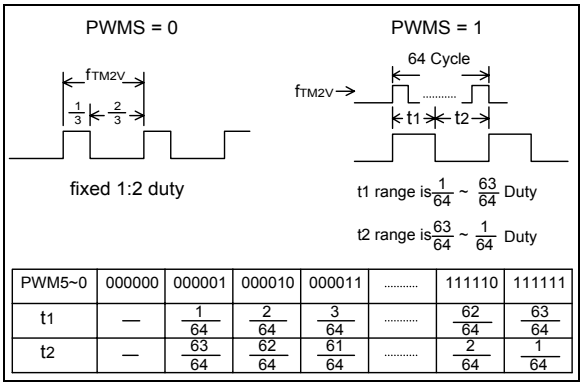
The PWME is responsible for controlling PWM wave output to PB7.

1 = enabling PB7 output PWM wave; It will close PB7 I/O function for use of PWM pulse output only.

0 = disabling PWM output.

19. PWM5 - 0 - 6 bits PWM wave duty cycle controller

The PWM5 - 0 are selected for PWM wave duty cycle. The value of selection is shown as follows:



PWM5~0	000000	000001	000010	000011	.....	111110	111111
t1	—	1/64	2/64	3/64	.....	62/64	63/64
t2	—	63/64	62/64	61/64	.....	2/64	1/64

Example: enable TM2 & PWM output.

```
LDA  #30h          ;initial TCR2 data.
STA  TCR2          ;TCR2 = $000F.
LDA  #%10001100    ;TCS2 = $000E, pre-scale
                   ;2^4, enable TM2E,
STA  TCS2          ;clear TOFR2 for PWM
                   ;only.
LDA  #%11000111    ;enable PB7 output,
                   ;select 64 duty,
STA  PWMC          ;& set 7/64 high, 56/64
                   ;low, PWMC = $0010
....               ;other working.
```

*You can measure the waveform with 7/64 duty high, 56/64 duty low at PB7.

WAIT / STOP MODE

The WAIT mode function will set CPU clock disabled and Timer counter enabled if WAIT $0008 bit0 = 1 be set. The TOF, RTI, or external interrupt will make CPU recovered normally from wait mode interrupt point next address. The STOP mode function will set CPU and Timer counter disabled if STOP $0008 bit4 = 1. Only the EXTERNAL INTERRUPT will make CPU and TIMER COUNTER being recovered normally from STOP MODE INTERRUPT POINT next address.

ADDR	REGISTER	R/W	7	6	5	4	3	2	1	0	ENABLE
$0008	STOP & WAIT	R									
SNW		W				STOP(0)				WAIT(0)	1 = SET

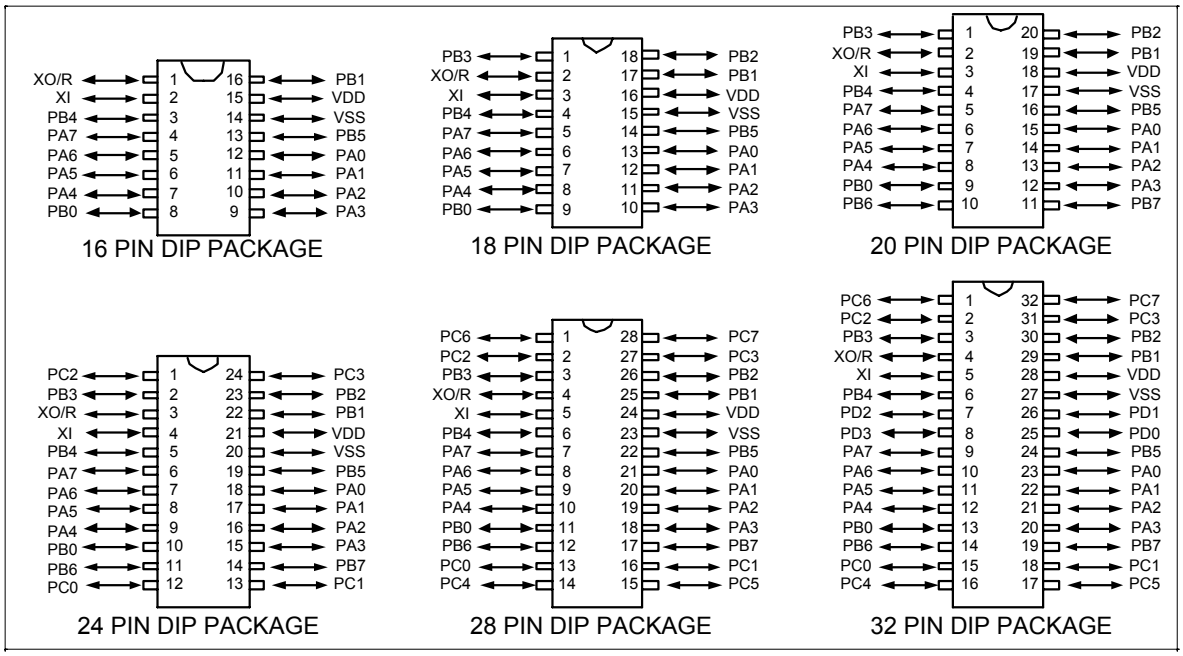
```
Example:    ....                ; normal working.
Wait_Set:   LDA  #%00000001     ;STPWAT $0008, set
                                ;Wait mode enable.
            STA  STPWAT         ;enter the WAIT mode.
            NOP                 ;*
            NOP                 ;
            JMP  MainPGMLoop

Stop_Set:   LDA  #%00010000     ;set Stop mode
                                ;enable.
            STA  STPWAT         ;enter the STOP mode.
            NOP                 ;*
            NOP                 ;
            JMP  MainPGMLoop
```

Note*: To add two more NOPs to ensure proper wake up is preferred.

PIN DESCRIPTION

Mnemonic	PIN No.	Description		Pull-Up/Down Register	Source/Sink
		Normal Function	External input port		
VDD	28	I	(Power)		
VSS	27	I	(Ground)		
XO/R	4	I	(Crystal in or resistor)		
XI	5	O	(Crystal out or Ext. Clock in)		
PA3 - 0	20 - 23	Normal I/O	Ext. INT (Edge/Level High)	Up, Down (100K)	-8/8mA
PA4	12	Normal I/O	Comparator 0 input	Up, Down (100K)	-8/8mA
PA5	11	Normal I/O	Comparator 1 input	Up, Down (100K)	-8/8mA
PA6	10	I/O (open-drain O)	Slow transition output	Up (5K)	-/8mA
PA7	9	I/O (open-drain O)	Ext. INT (Edge low) / Slow transition output	Up (5K)	-/8mA
PB0	13	Normal I/O	Comparator reference input	Up, Down (100K)	-8/8mA
PB1, PB2	29, 30	I/O (open-drain O)	Slow transition output	Up (100K)	-/25mA
PB3	3	Normal I/O		Up, Down (100K)	-8/8mA
RESET/PB4	6	Normal I/O	Ext. RESET	Up (100K)	-8/8mA
IRQ/PB5	24	I/O (open-drain)	Ext. IRQ (Edge/Level low)	(Pull-up resistor on outside)	-/8mA
PB6	14	Normal I/O	External clock	Up, Down (100K)	-8/8mA
PB7	19	Normal I/O	PWM waveform output	Up, Down (100K)	-8/8mA
PC7 PC6 PC5 - 4 PC3 PC2 PC1 PC0	32 1 17 - 16 31 2 18 15	Normal I/O	External INT (Edge High)	Up, Down (100K)	-8/8mA
PD3 - 2 PD1 - 0	8 - 7 26 - 25	Normal I/O		Up (100K)	-/8mA

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATING

Power Supply Voltage	VDD = +2.4V to + 5.5V
Input Voltage	V_{IN} = - 0.3V to VDD+0.3V
Output Voltage	V_{OUT} = 0V to VDD
CPU clock	From 200KHz to 6.0MHz
Operating Ambient Temperature	T_{OPR} = - 0°C to +70°C
Storage Temperature	T_{STR} = -20°C to +70°C

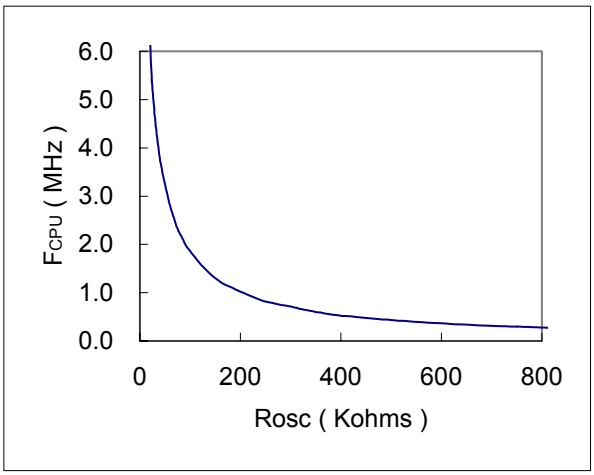
Note: Stresses beyond those given in the Absolute Maximum Ratings table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS (25°C, VDD = 5.0V)

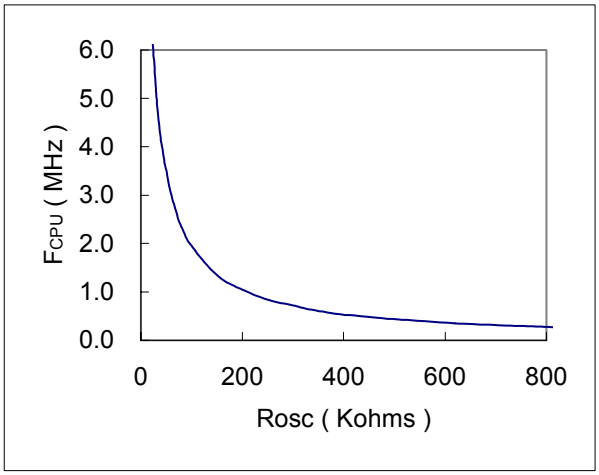
Characteristic	Condition	Symbol	Min.	Typ.	Max.	Unit
Output high voltage PA5-0, PB7-6, PB4-3, PB0, PC7-0, PD3-0	I_{OH} = -8mA	V_{OH}	2.4	-	-	V
Output low voltage PA7-0, PB7-3, PB0, PC7-0, PD3-0	I_{OL} = 8mA	V_{OL}	-	-	0.4	V
Output low voltage PB1, PB2	I_{OL} = 25mA	V_{OL}	-	-	0.5	V
Input high voltage PA5-0, PB7, PB6, PB3-0, PC7-0, PD3-0	VDD = 5.0V	V_{IH}	3.5	-	-	V
Input low voltage PA5-0, PB7-6, PB3-0, PC7-0, PD3-0	VDD = 5.0V	V_{IL}	-	-	1.4	V
Positive-going input threshold voltage PA6, PA7, IRQ/PB4, RESET/PB5	VDD = 5.0V	V_{IH}	-	2.0	-	V
Negative-going input threshold voltage PA6, PA7, IRQ/PB4, RESET/PB5	VDD = 5.0V	V_{IL}	-	0.8	-	V
Pull-Up/Down resistance PA5-0, PB7, PB6, PB3, PB0, PC7-0	V_{IN} = 5.0V /V_{IN} = 0V	R_{PUDWN} /R_{PULLUP}	-	100	-	KΩ
Pull-up resistance PA6, PA7	Pull-up always V_{IN} = 0V	R_{PULLUP}	-	5.0	-	KΩ
Pull-up resistance PB1, PB2, PB4, PD3-0	V_{IN} = 0V	R_{PULLUP}	-	100	-	KΩ
I/O port Hi-Z leakage PA5 - 0, PB7 - 0, PC7 - 0, PD3 - 0	Pull-Down/up inactivated	I_{IZ}	-	-	10	μA
Power consumption		I_{CC}	-	TBD	-	mA
Stand by current		I_{STB}	-	5.0	-	μA
LVR trigger voltage		V_{LVR}	-	2.2	-	V

THE RELATIONSHIP BETWEEN THE R_{osc} AND THE F_{osc}

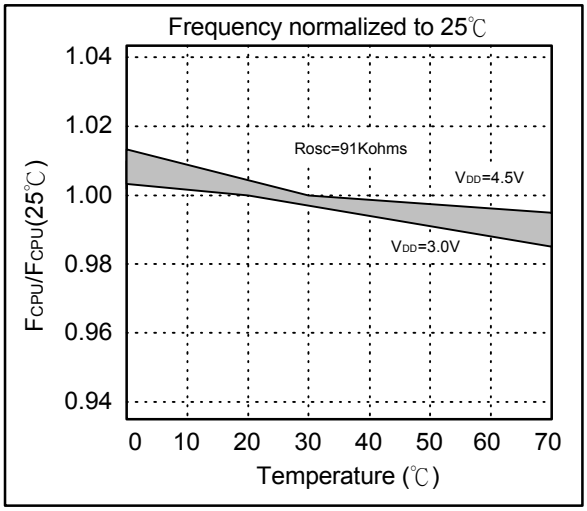
1. VDD = 3.0V , T_A = 25℃



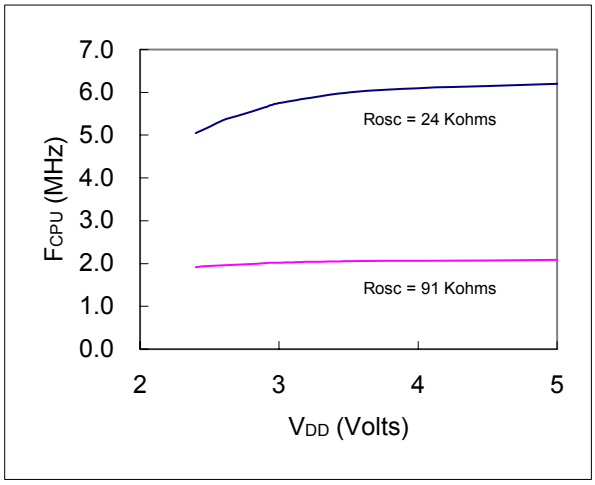
2. VDD = 5.0V , T_A = 25℃



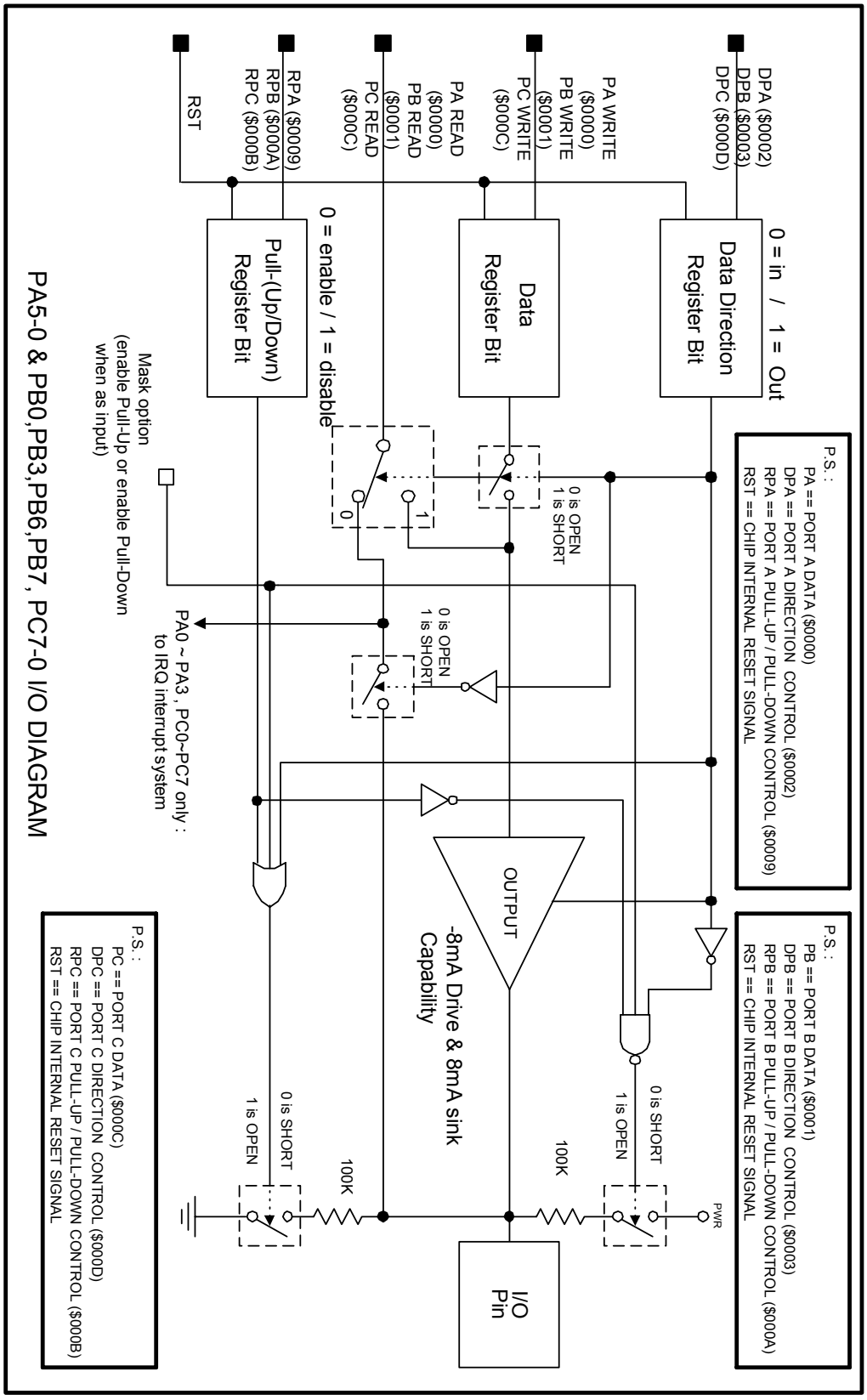
3. FREQUENCY vs. TEMPERATURE



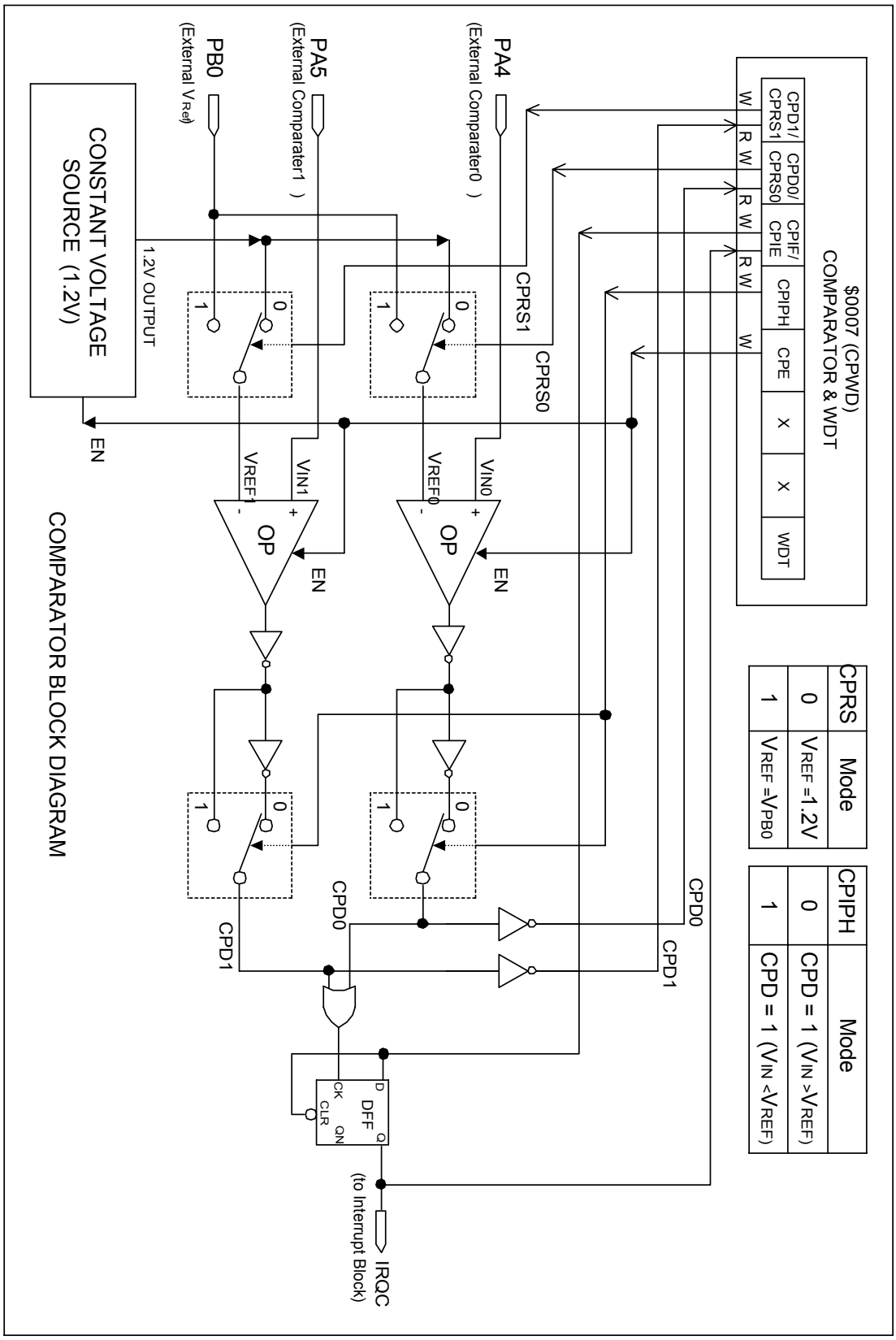
4. FREQUENCY vs. VDD



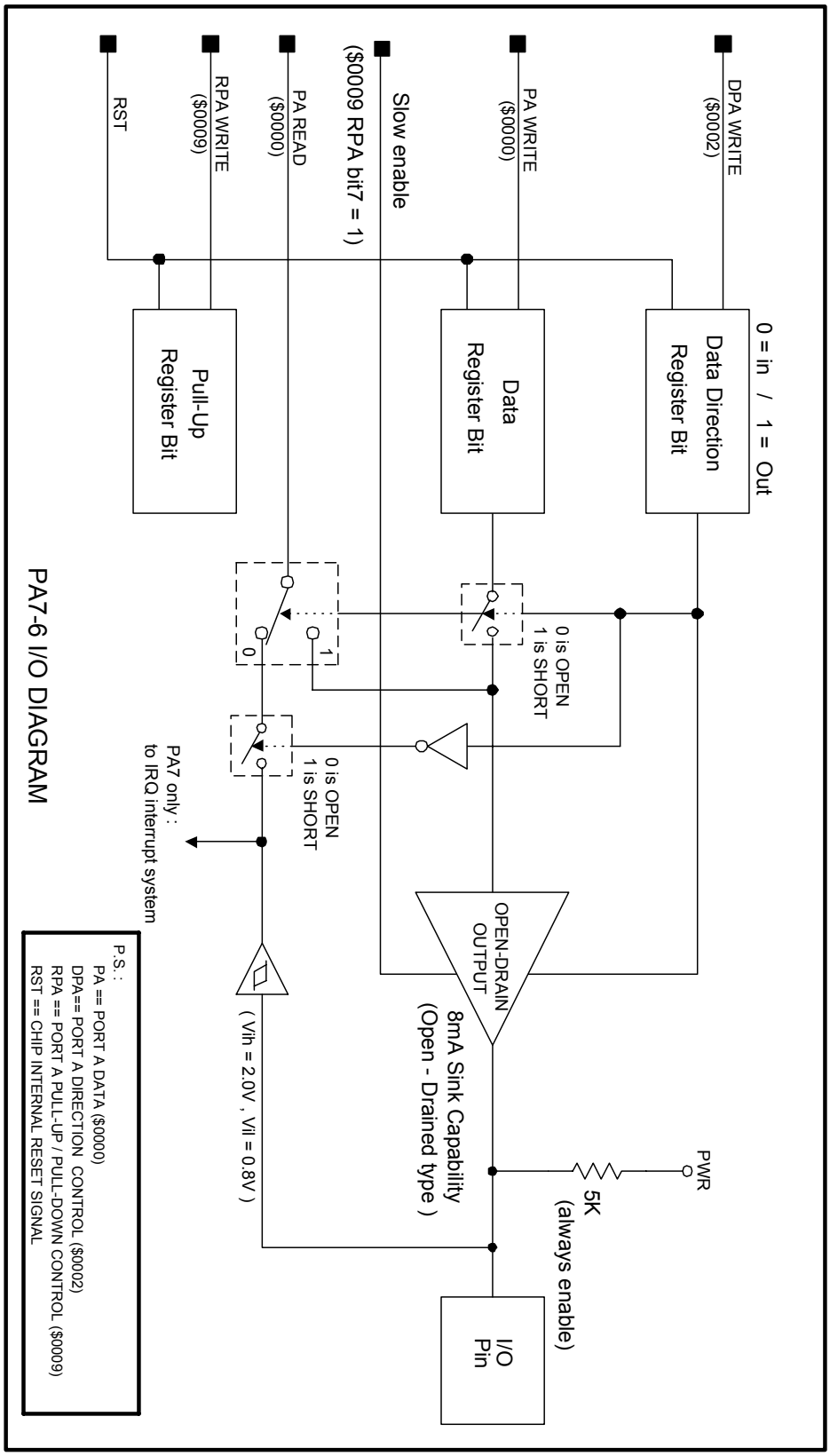
APPENDIX A: PA5 - 0, PB0, PB3, PB6, PB7, & PC7 - 0 I/O DIAGRAM



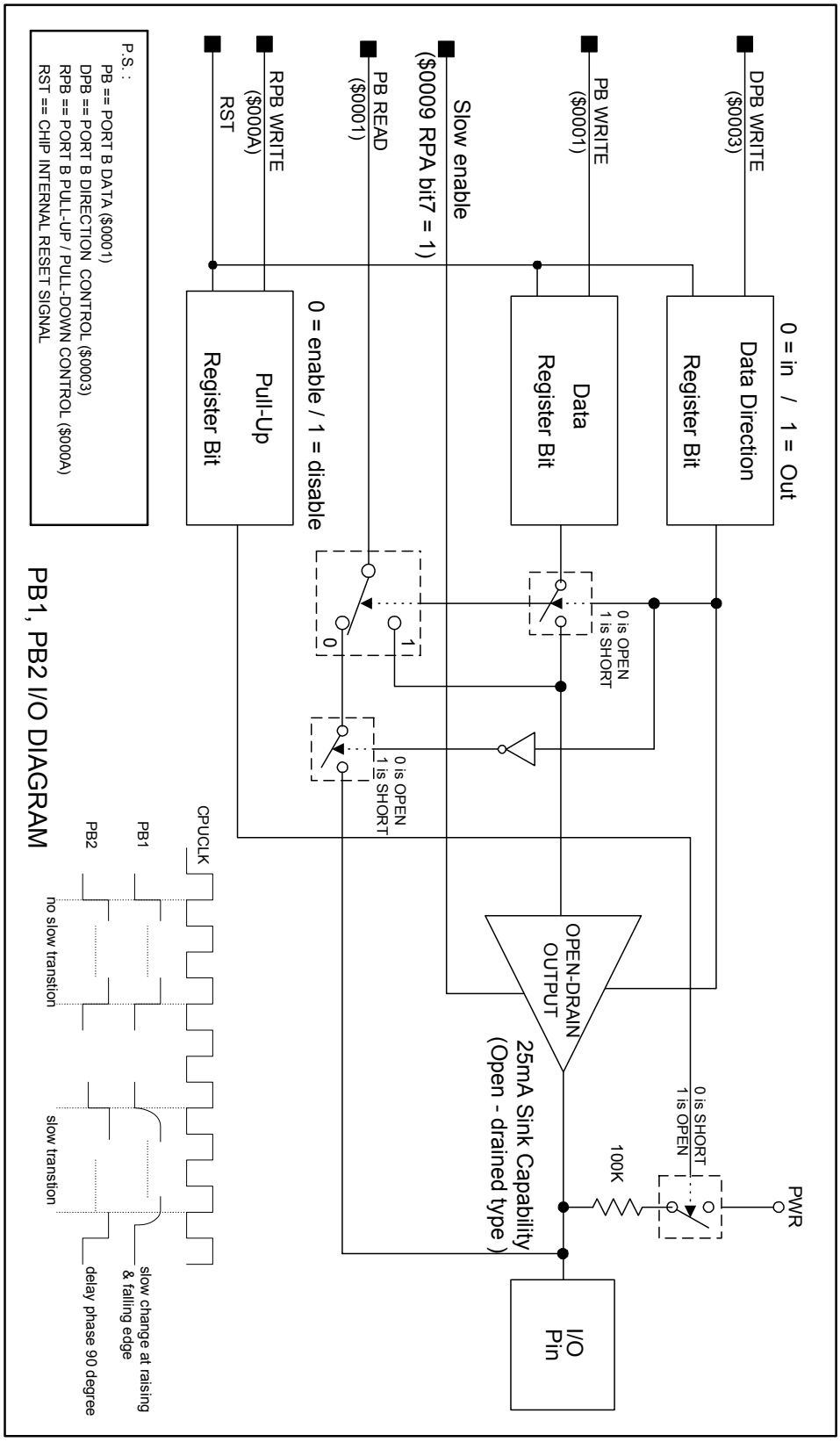
APPENDIX B: COMPARATOR BLOCK DIAGRAM



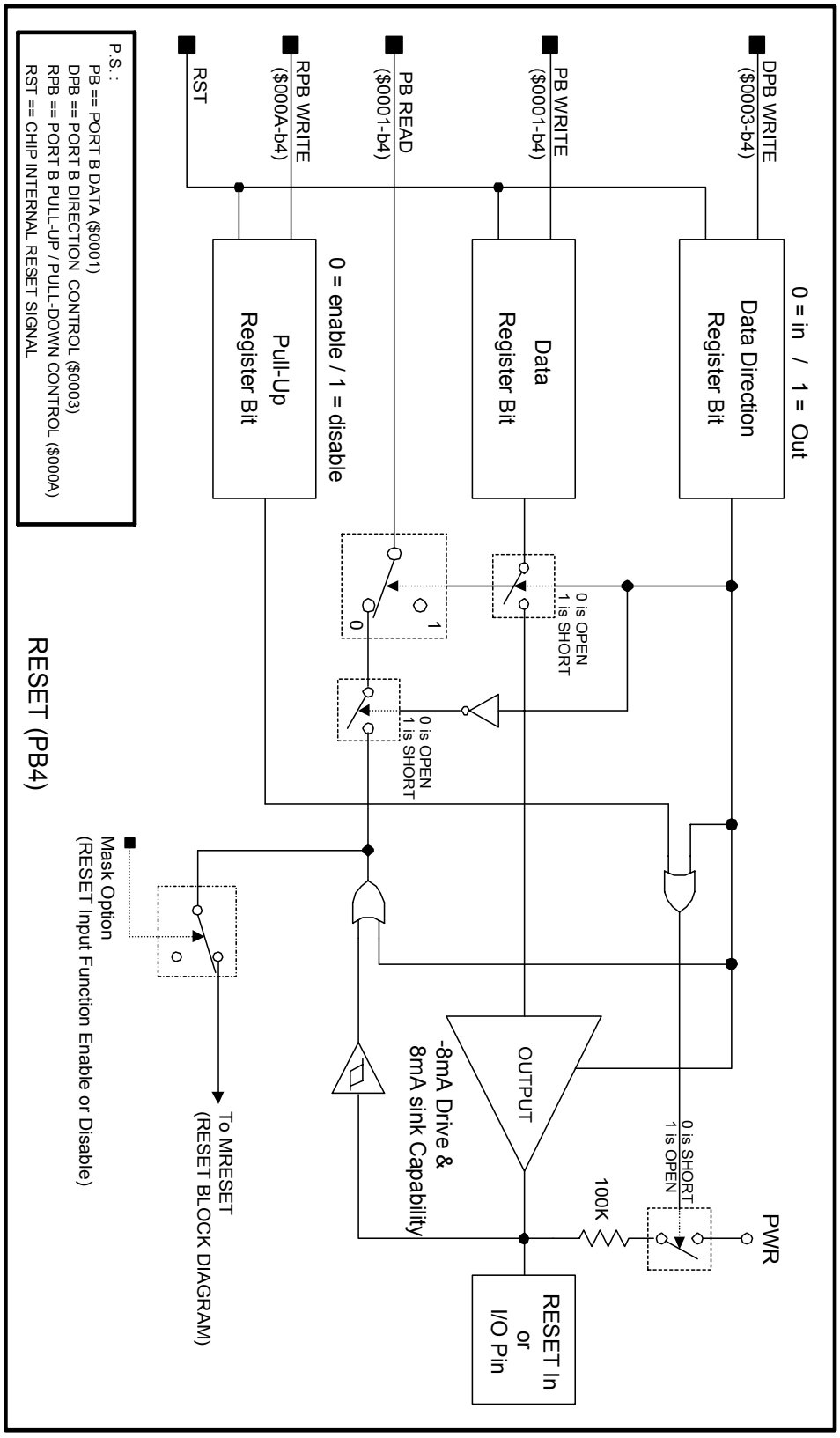
APPENDIX C: PA6, PA7 I/O DIAGRAM



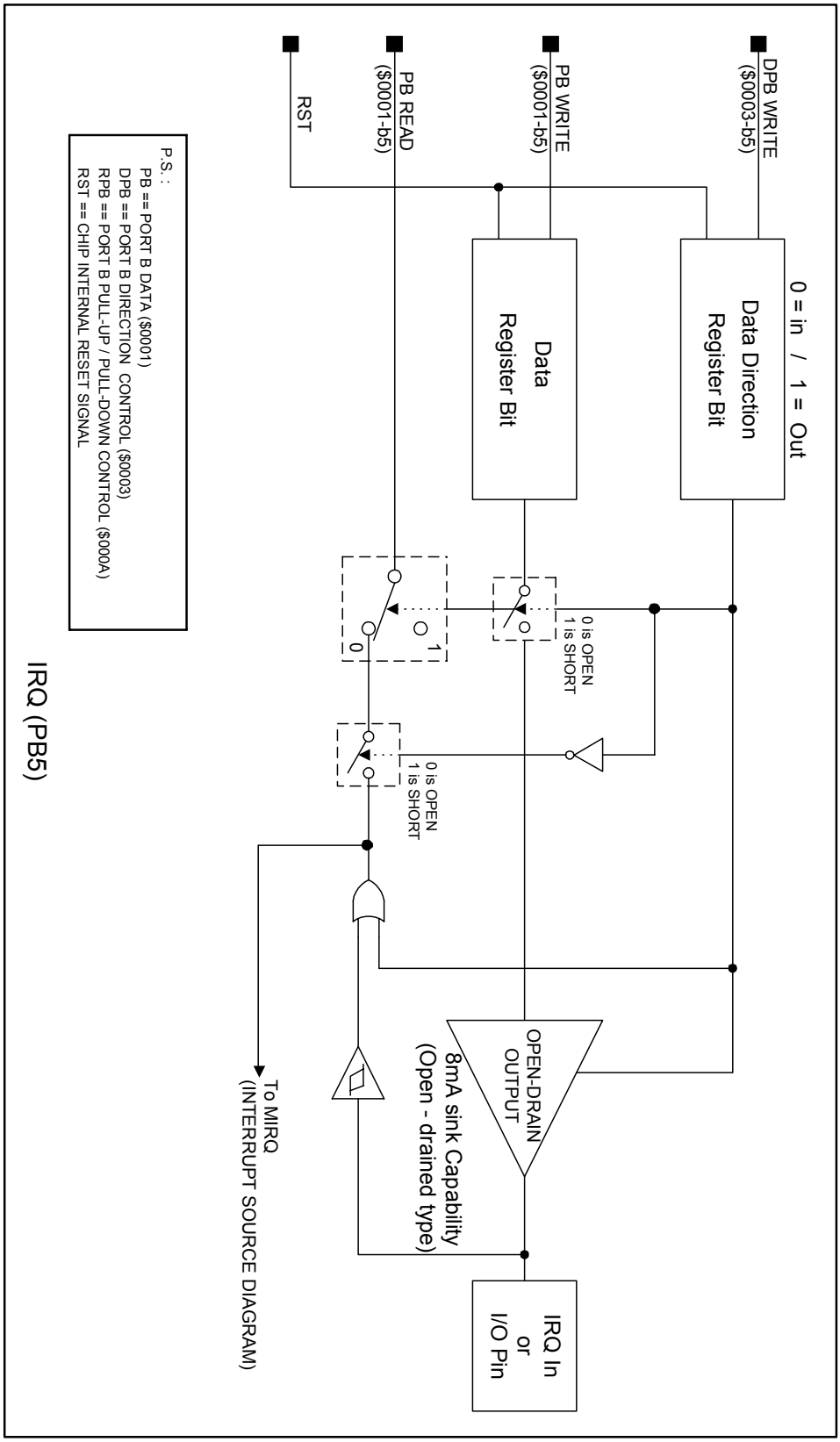
APPENDIX D: PB1, PB2 I/O DIAGRAM



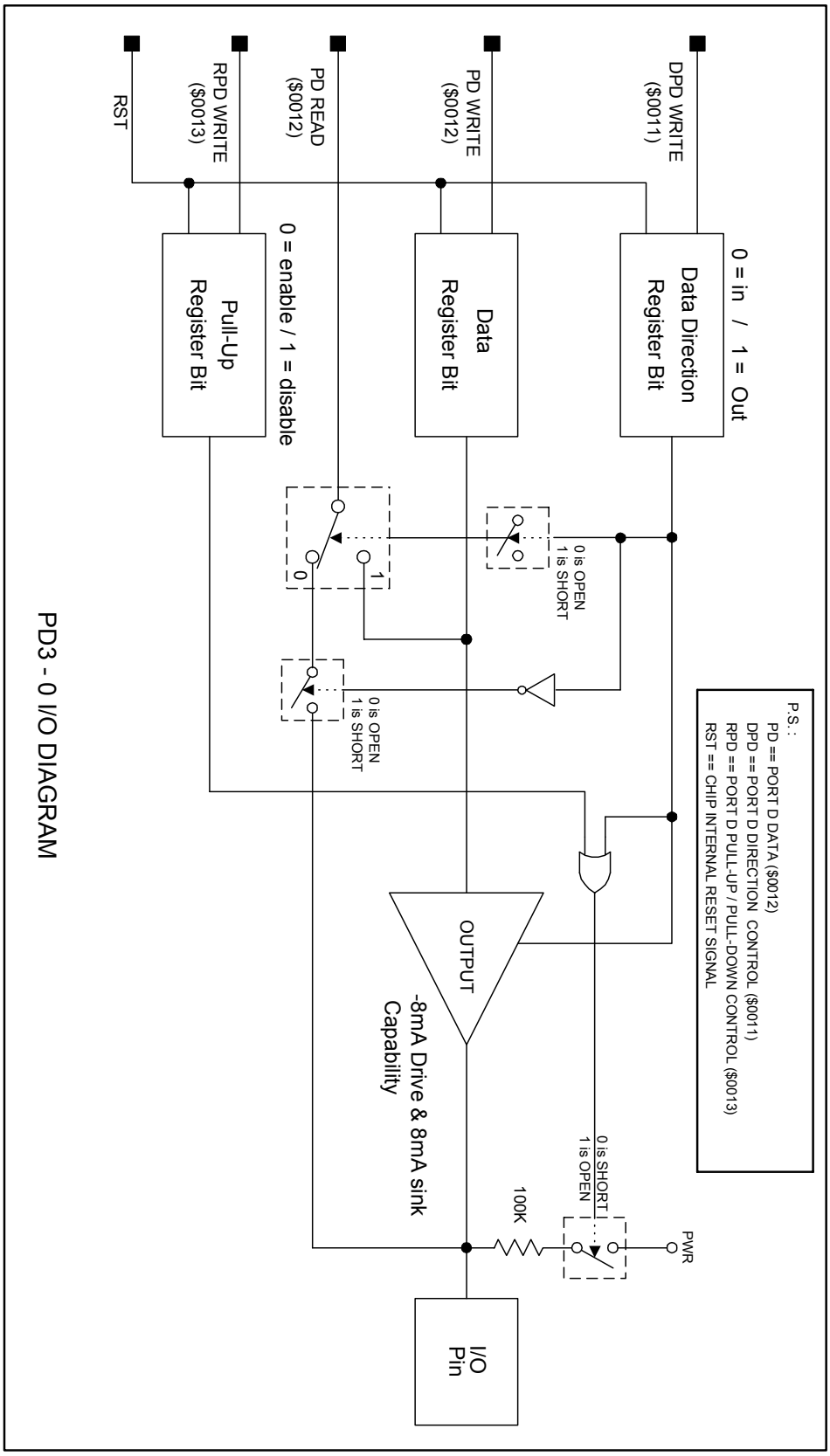
APPENDIX E: RESET & PB4 I/O DIAGRAM



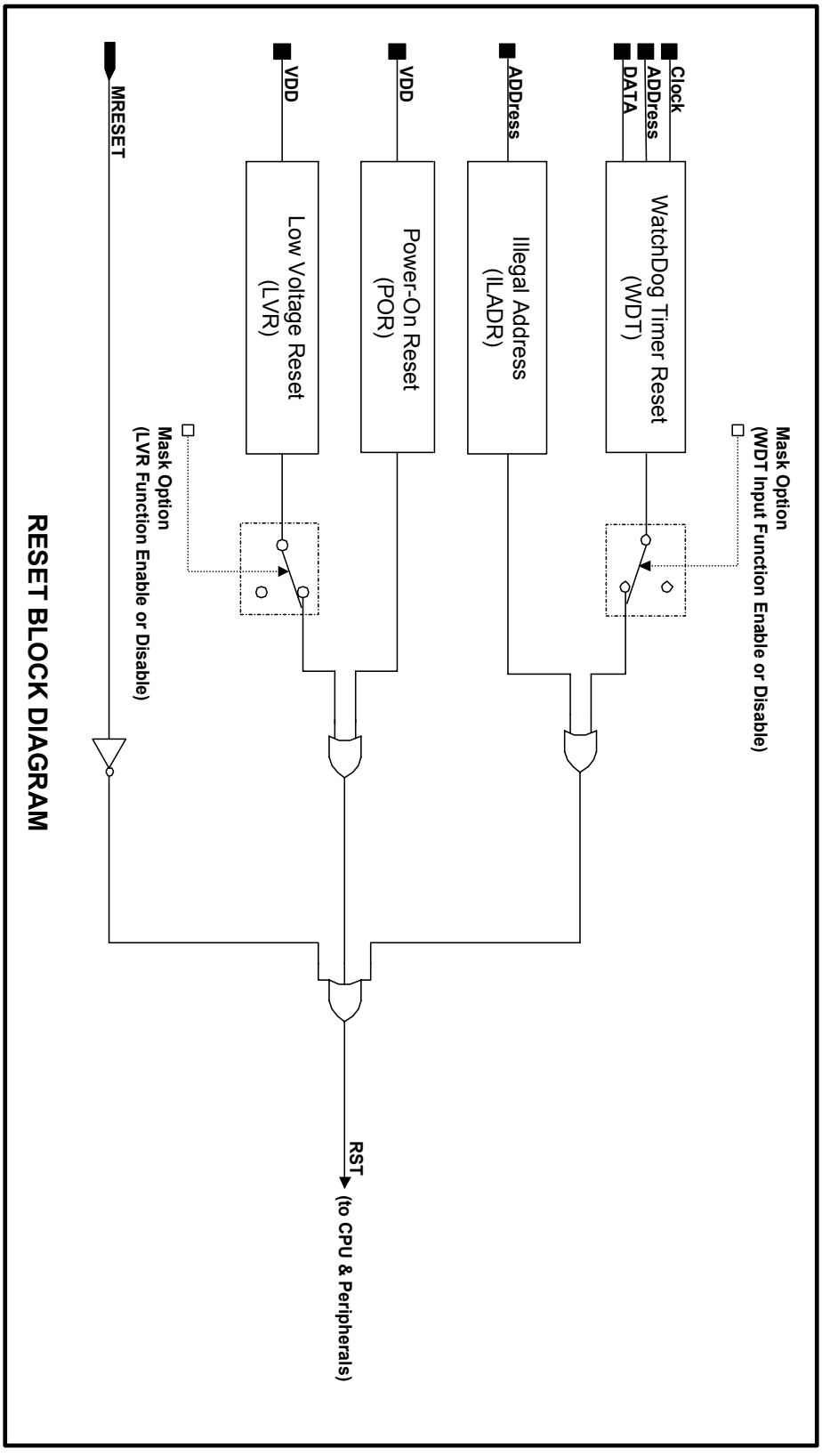
APPENDIX F: IRQ & PB5 I/O DIAGRAM



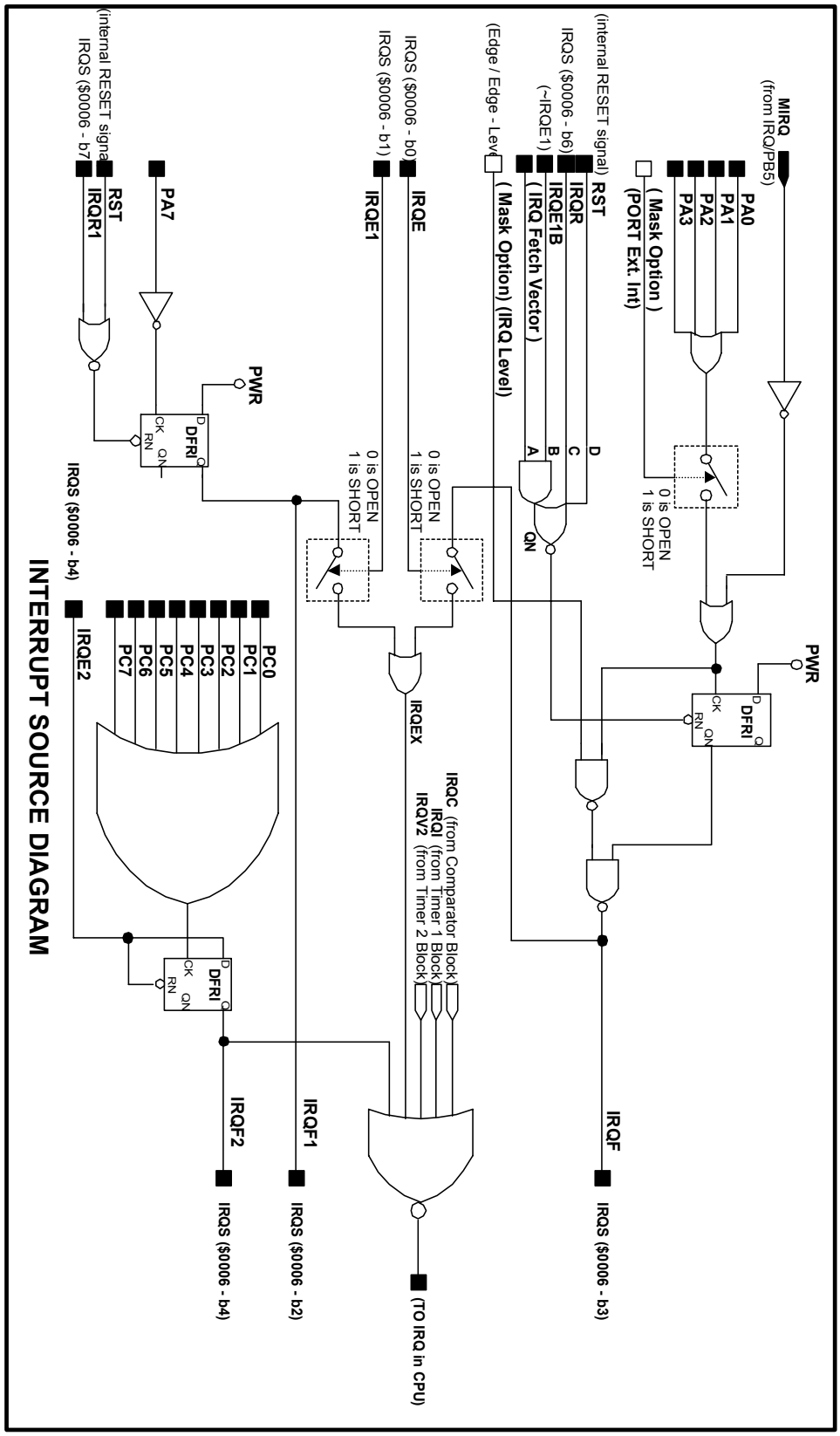
APPENDIX G: PD3 - 0 I/O DIAGRAM



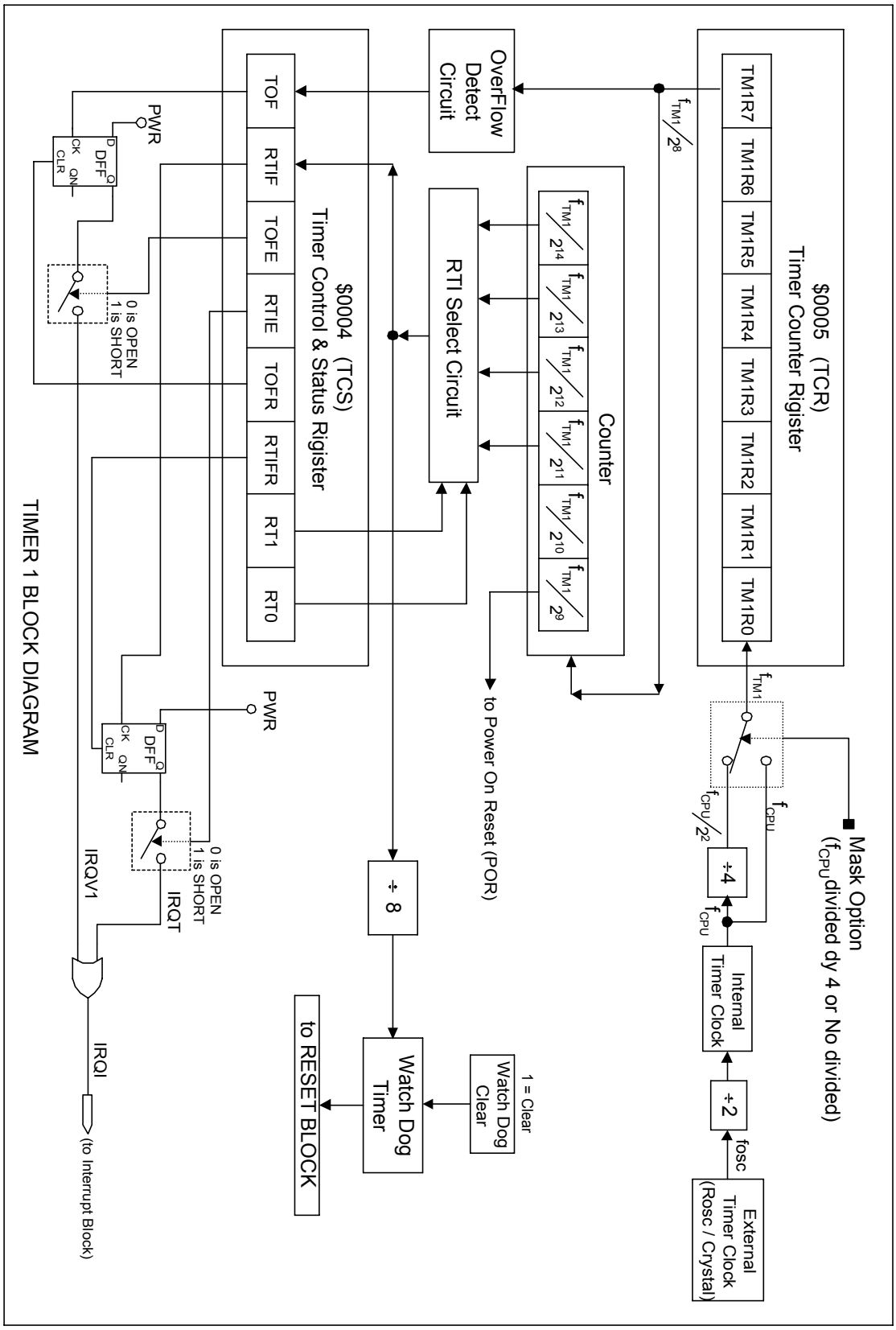
APPENDIX H: RESET BLOCK DIAGRAM



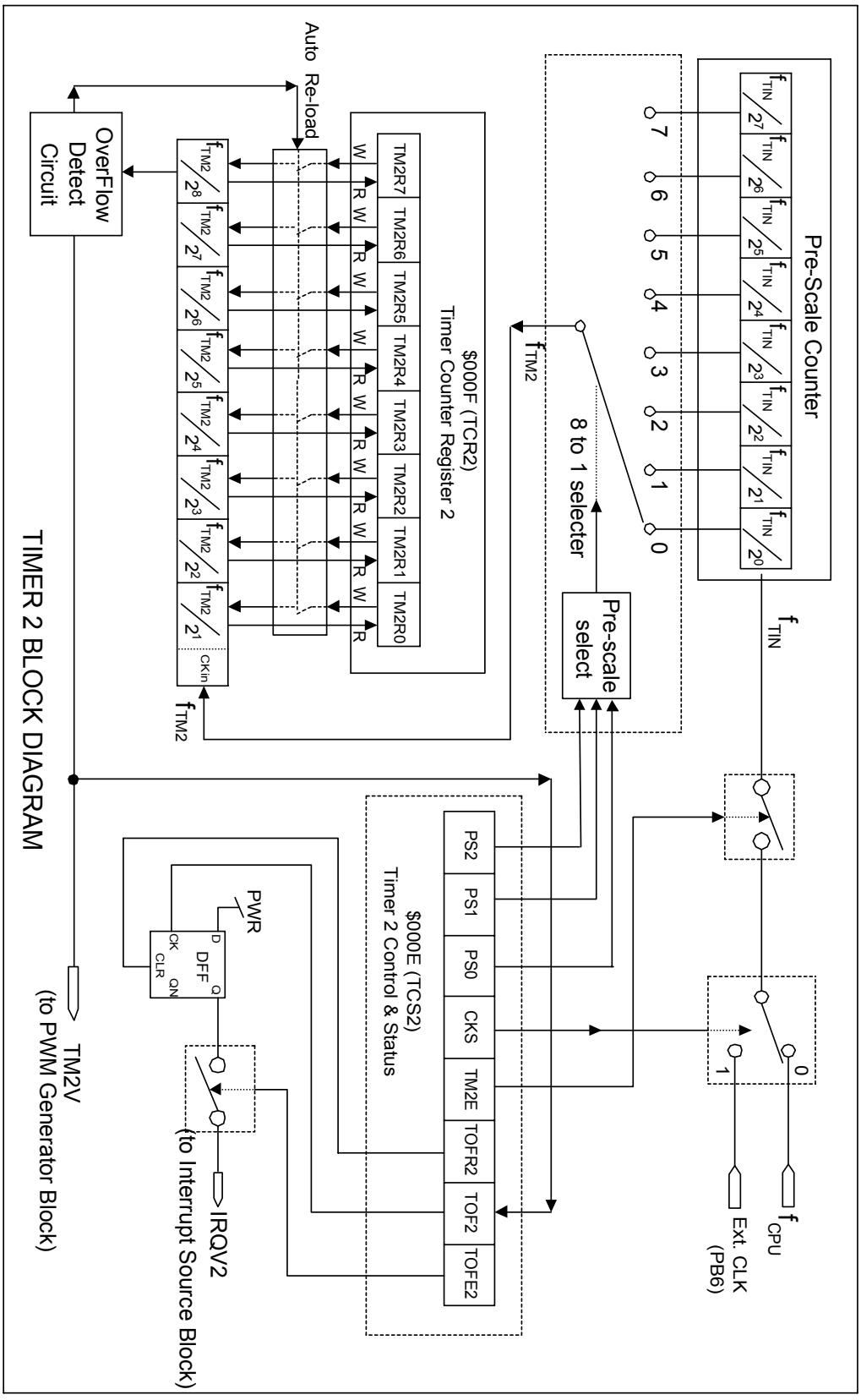
APPENDIX I: INTERRUPT SOURCE DIAGRAM



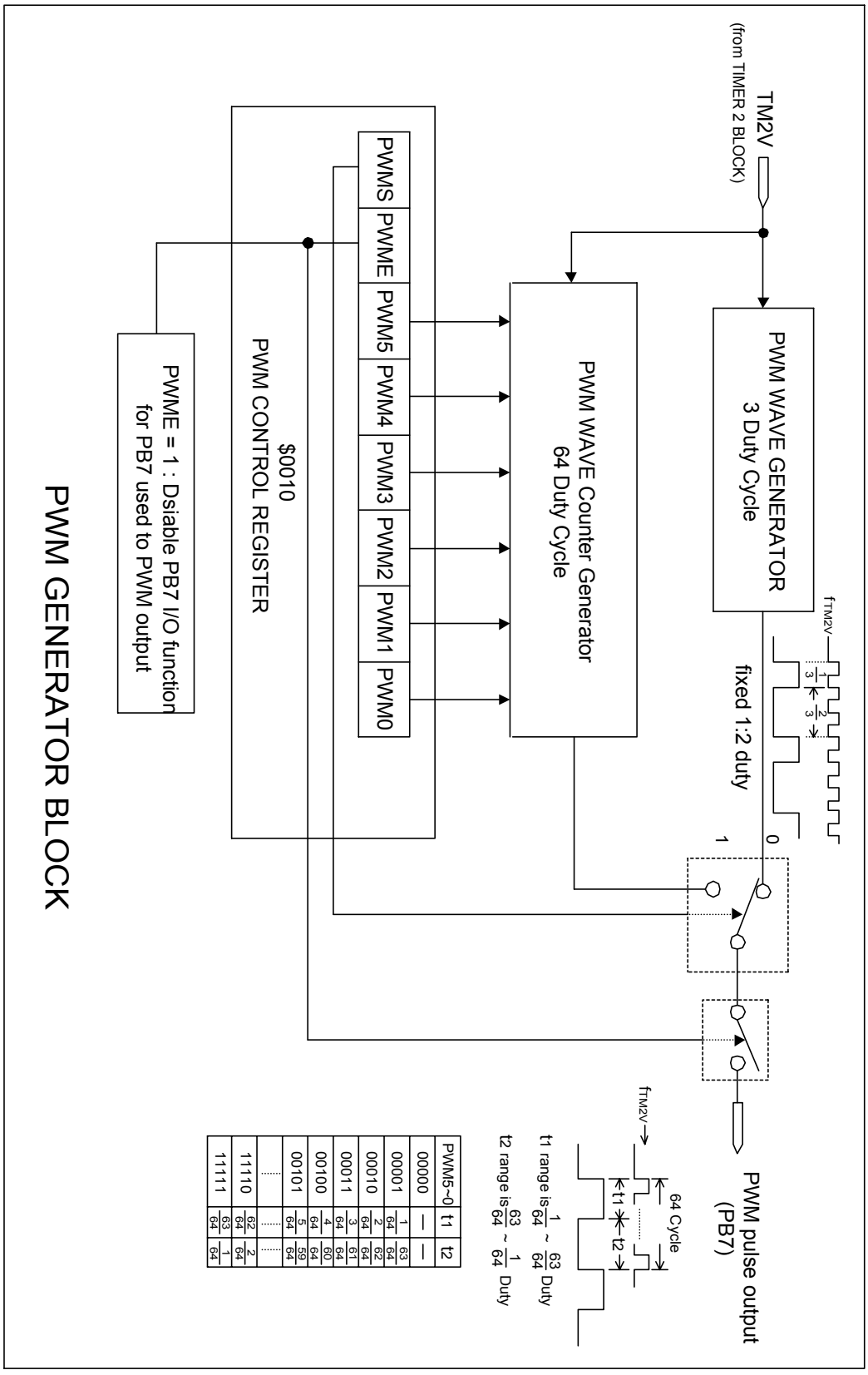
APPENDIX J: TIMER 1 BLOCK DIAGRAM



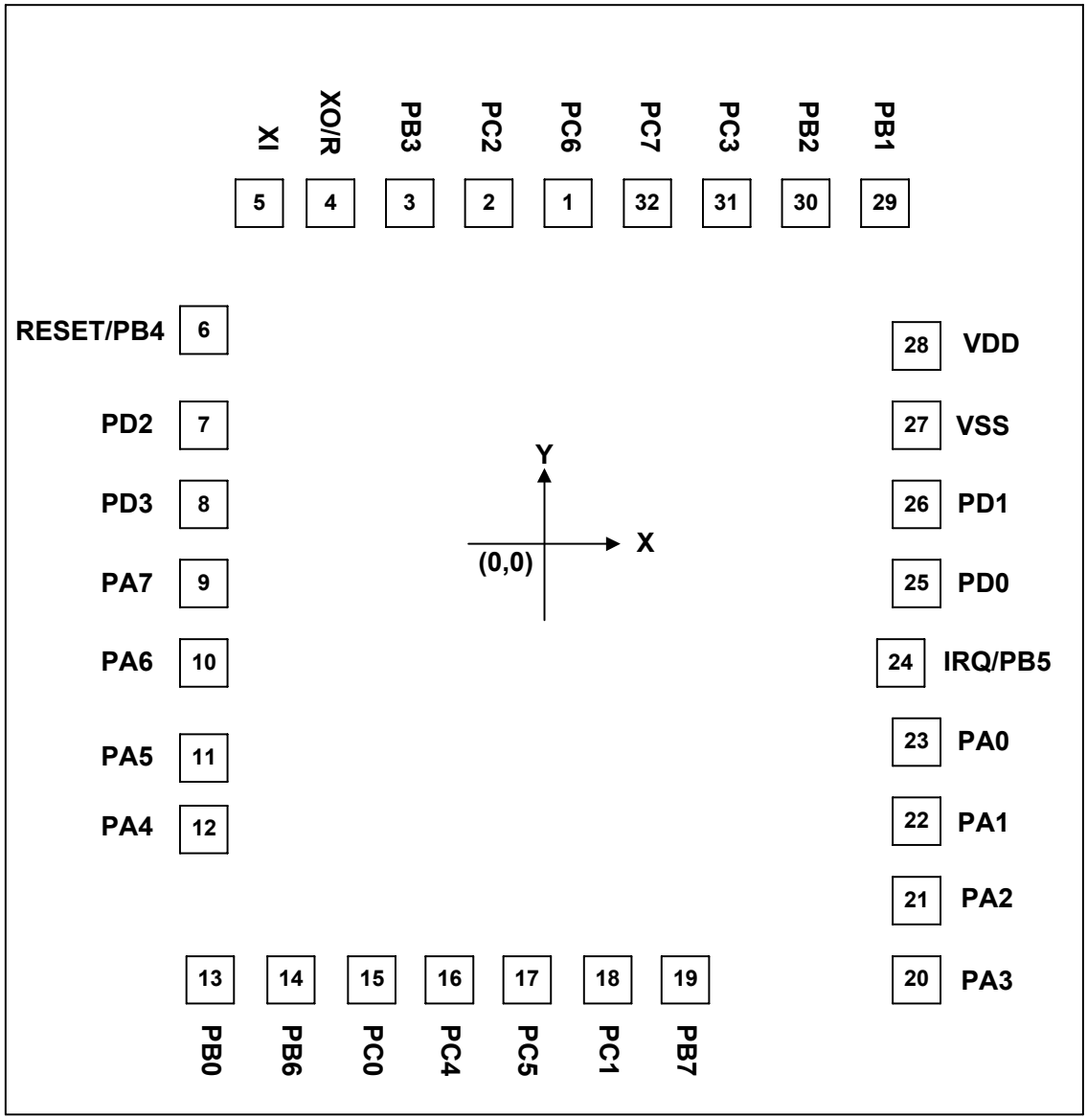
APPENDIX K: TIMER 2 BLOCK DIAGRAM



APPENDIX L: PWM GENERATOR BLOCK DIAGRAM



APPENDIX M: BONDING DIAGRAM



Chip Size: 1900μm x 1970μm

The IC substrate should be connected to VSS

Note: 0.1μF capacitor between VDD and VSS should be placed to IC as close as passible.

BONDING COORDINATE

Pad No	Pad Name	X	Y
1	PC6	54	786
2	PC2	-107	786
3	PB3	-277	786
4	XO/R	-439	767
5	XI	-605	767
6	RESET / PB4	-749	532
7	PD2	-749	367
8	PD3	-749	216
9	PA7	-749	47
10	PA6	-749	-121
11	PA5	-749	-290
12	PA4	-749	-451
13	PB0	-741	-784
14	PB6	-579	-784
15	PC0	-410	-784
16	PC4	-249	-784
17	PC5	-80	-784
18	PC1	82	-784
19	PB7	251	-784
20	PA3	749	-778
21	PA2	749	-609
22	PA1	749	-447
23	PA0	749	-278
24	IRQ / PB5	722	-117
25	PD0	749	48
26	PD1	749	199
27	VSS	749	358
28	VDD	749	508
29	PB1	715	786
30	PB2	554	786
31	PC3	385	786
32	PC7	223	786

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REVISION HISTORY

Date	Revision #	Description	Page
NOV. 04, 1997	0.1	Original	
SEP. 17, 1997	0.2	1. Modify "*BLOCK DIAGRAM*" 2. Modify grammar	
JAN. 09, 1998	0.3	1. Add Operation Voltage Range: 2.4V - 6.0V in "*FEATURES*" and "*DC ELECTRICAL CHARACTERISTICS"* 2. Chang font: "Arial" 3. Add "*EMULATION BOARD*" and "*PIGGY BACK BOARD*" User Guide	
MAR. 02, 1998	1.0	Delete "*PRELIMINARY*"	
MAR. 21, 1998	1.1	1. Change Voltage Range value: 2.4V - 6.0V to 2.4V - 5.5V 2. Change footer font: "Times New Roman"	1, 28, 29
JUN. 04, 1998	1.2	1. Add "*FREQUENCY vs. VDD, TEMPERATURE*" 2. Revise the pin naming in "*BLOCK DIAGRAM*", "*PIN ASSIGMENT*", "*BONDING DIAGRAM*", "*BONDING CORRDINATE*": OSC2 -> XO, OSC1 -> XI	
DEC. 13, 1999	1.3	1. Add PIN No. in "*PIN ASSIGNMENT*" 2. Add "*DISCLAIMER*" 3. Renew to a new document format	
FEB. 22, 2000	1.4	1. Modify: $1800~$FFFF -> $1800~$1FFF in the "*BLOCK DIAGRAM*" 2. Modify: Table port A, B, C and D	6 - 9
NOV. 07, 2000	1.5	1. Wording improvement 2. To revise the CPU low bound clock range from 1KHz to 200KHz. 3. To correct the I/O block diagrams on Appendix D: PB1 I/O Diagram and Appendix G: PB5 & IRQ I/O Diagram. 4. To remove Appendix E: I-V Curve of PB1, Appendix K: the Emulation Board and the Jumper Setting, and Appendix L: Piggyback Board. 5. Add "Note: The 0.1uF capacitor between VDD and VSS…" 6. Add "*REVISION HISTORY*" 7. Renew to a new document format	 34 37