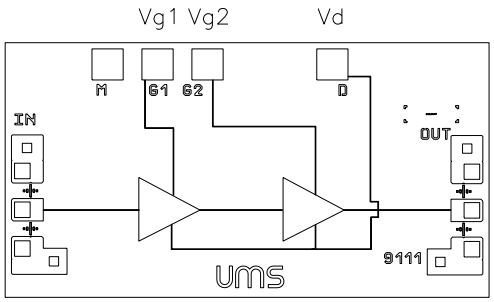
9-18GHz Frequency Multiplier

GaAs Monolithic Microwave IC

Description

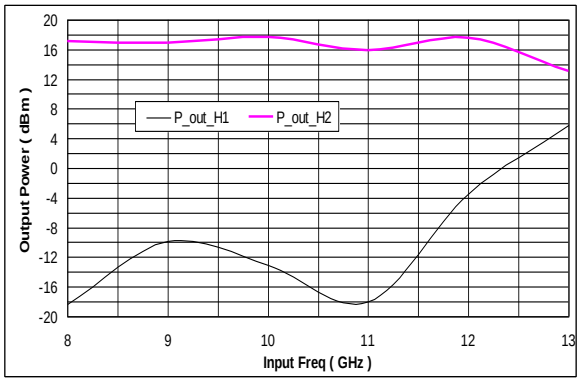
The CHX2089-99F is a cascadable times 2 frequency multiplier monolithic circuit.
It is designed for a wide range of applications, from ISM to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.



Main Features

- Broadband performances: 8-11.5GHz
- Pout(H2) = 15dBm @ Pin = 12dBm
- DC bias: Vd = 3.5Volt @ Id = 60mA
- Chip size: 1.62 x 0.89 x 0.10mm



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	8	9	11.5	GHz
Fout	Output frequency range	16	18	23	GHz
Pin	Input power		12	15	dBm
Pout	Output power for +12dBm input power	11	15		dBm

United Monolithic Semiconductors S.A.S.
Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34

Electrical Characteristics

Tamb = +25°C, Vd = 3.5V, Vg1 = -0.9V, Vg2 adjusted for Id=50 mA, no RF (Vg2 typ.= -0.3V).

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	8	9	11.5	GHz
Fout	Output frequency range	16	18	23	GHz
Pin	Input power		12	15	dBm
Pout	Output power for +12dBm input power	11	15		dBm
Is/Fo	Fin rejection at the output	15	20		dBc
VSWRin	Input VSWR			2.0:1	
VSWRout	Output VSWR			2.5:1	
Id	Bias current without RF		50	70	mA
Id_RF	Bias current with RF (Pin=12 dBm)		60	85	mA

These values are representative of on-wafer measurements that are made without bonding wires at the RF ports.

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4	V
Id	Drain bias current	90	mA
Vg	Gate bias voltage	-2 to +0.4	V
Pin	Input power	20	dBm
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +155	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vd	D	Positive Drain voltage	3.5	V
Vg1	G1	Negative multiplier stage gate voltage	-0.9	V
Vg2	G2	Negative buffer stage gate voltage	(-0.3)	V

Vg2 should be adjusted to achieve Id = 50mA while no RF applied at the input.

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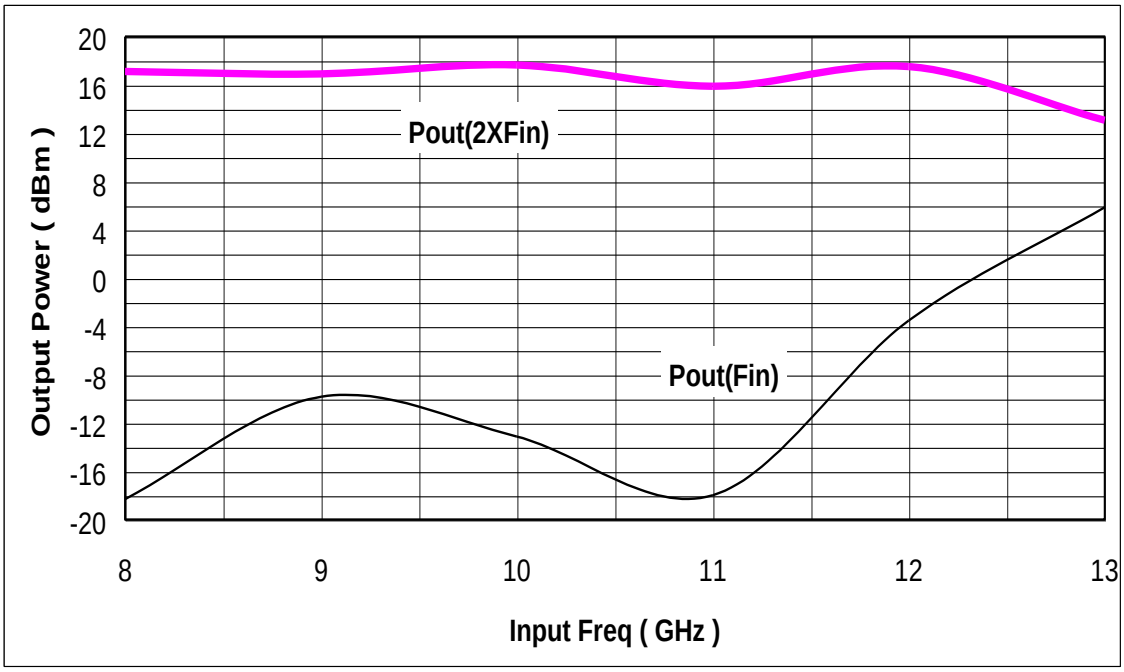
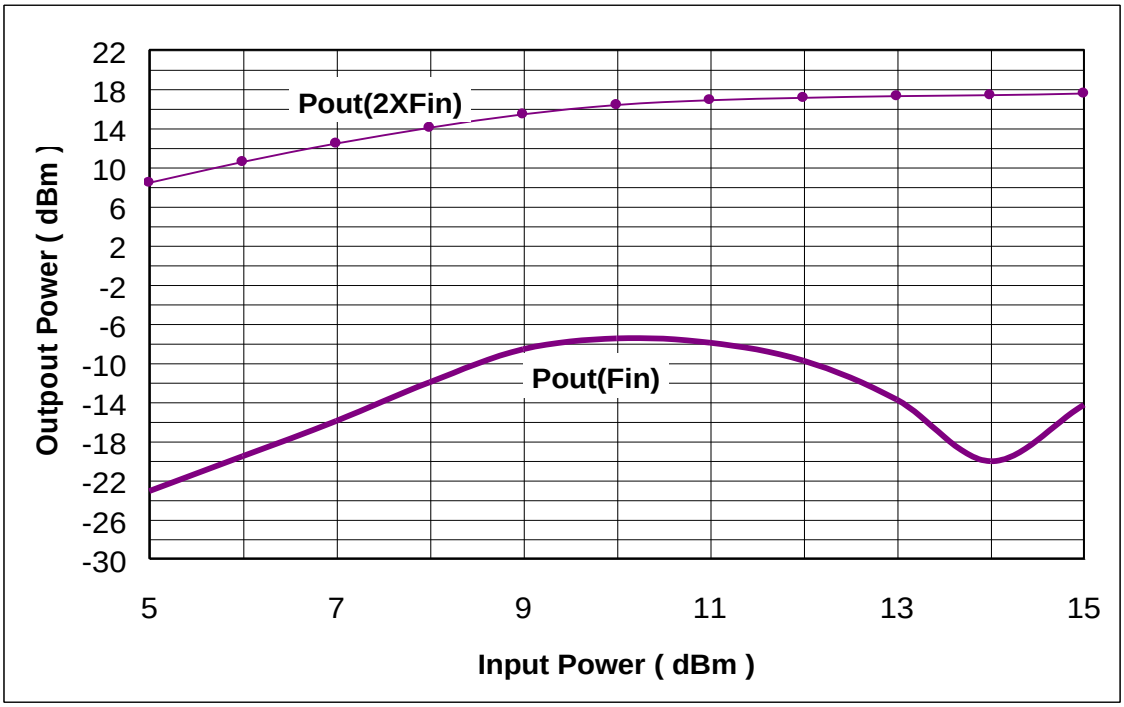
Typical on wafer Measurements

Tamb.= +25°C, Vd = 3.5V, Vg1 = -0.9V, Vg2 = -0.3V.

Pout = f(Fin) for Pin=12 dBm



Pout = f(Pin) for Fin = 9 GHz



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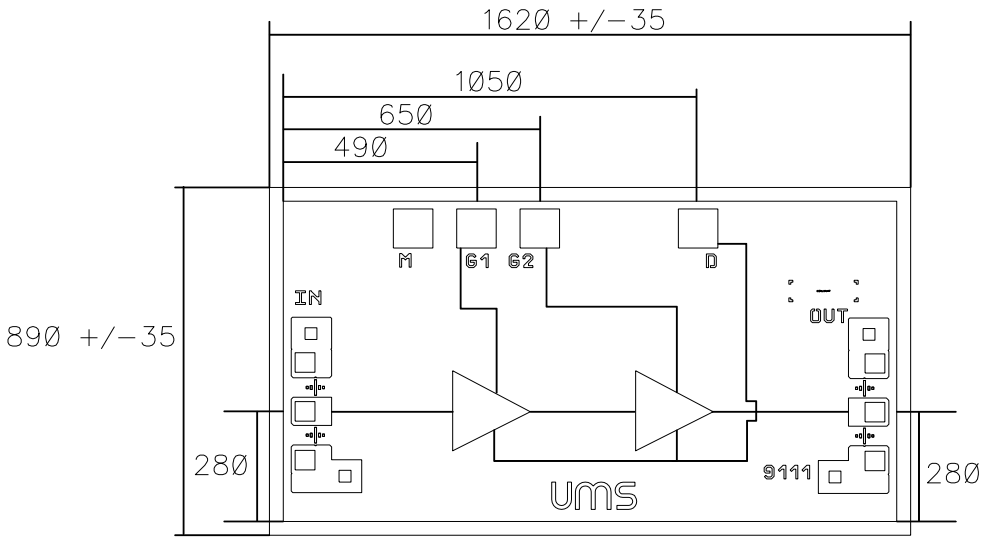
Mechanical data



Chip thickness: 100µm.
Chip size: 890x1620 ±35µm
All dimensions are in micrometers

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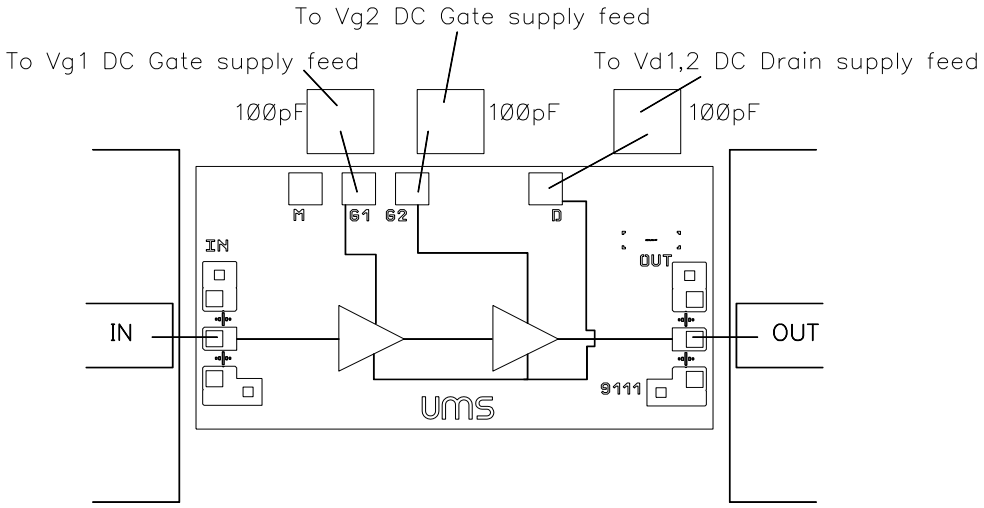
Recommended assembly plan



Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Recommended circuit bonding table

Label	Type	Decoupling	Comment
D	Vd	100pF	Drain Supply
G1	Vg1	100pF	Multiplier Gate Supply
G2	Vg2	100pF	Buffer amplifier Gate Supply
M	GND	NC	No connection required

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Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Ordering Information

Chip form:	CHX2089-99F/00

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