OKI semiconductor
MSM6434

HIGH-SPEED 4-BIT SINGLE CHIP MICROCONTROLLER WITH A/D CONVERTER

GENERAL DESCRIPTION

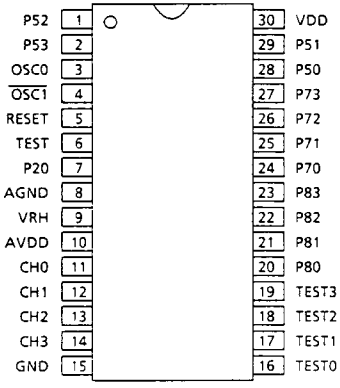
The OKI MSM6434 microcontroller is a low power, high-performance single-chip device implemented in complementary metal oxide semiconductor technology. 32K bits of mask program ROM, 1024 bits of data RAM, 13 Input/Output lines, a programmable timer/event-counter, 8 bit A/D converter, and oscillator are integrated onto one chip. Program memory is byte wide and data-paths are organized in 4 bit nibbles. RAM and I/O lines are bit addressable. 113 instructions include binary, BCD operations; bit set, reset, test; relative jumps; multi functional instructional (increment, modify, skip) 8 bit wide table output; subroutine call and return.

FEATURES

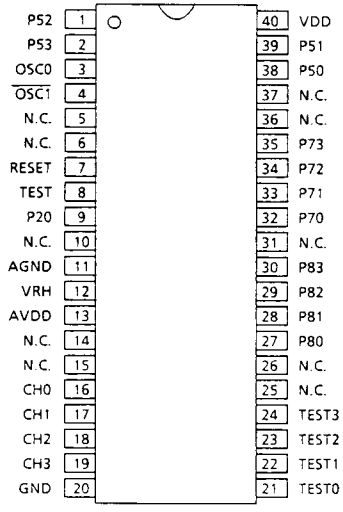
- 4000 x 8 MASK ROM
  An evaluation board is available for up to 8k x 8.
- 256 x 4 RAM (including the stack area)
- 3 x 4, 1 x 1 ports, 13 I/O lines
  1 lines for input ports having a latch, and the other 12 lines for bit operation are available.
- Three built-in counters
  12-bit time-base counter
  12-bit programmable timer
  8-bit high-speed programmable time/event counter
- 4 interrupts with four priority levels (3 internal, 1 external)
- 32 stack levels (in RAM)
- LED direct drive available (8 mA x 3 ports at the same time)
- Power down features
- Instruction execution time
  952 ns 4.2 MHz clock
- Instruction systems suitable for control
- 113 instructions
- 8 bit A/D converter (4 channel)
- Full static operation
- Low power consumption
  TYP 0.4μW at V_{DD} = 2V
  TYP 5μW at V_{DD} = 5V 0Hz clock
- 5V single power supply
- Package:
  30 pin plastic shrink DIP (SDIP30-P-600)
  40 pin plastic DIP (DIP40-P-400)
  44 pin PLCC (QFJ44-P-S650)

PIN CONFIGURATION

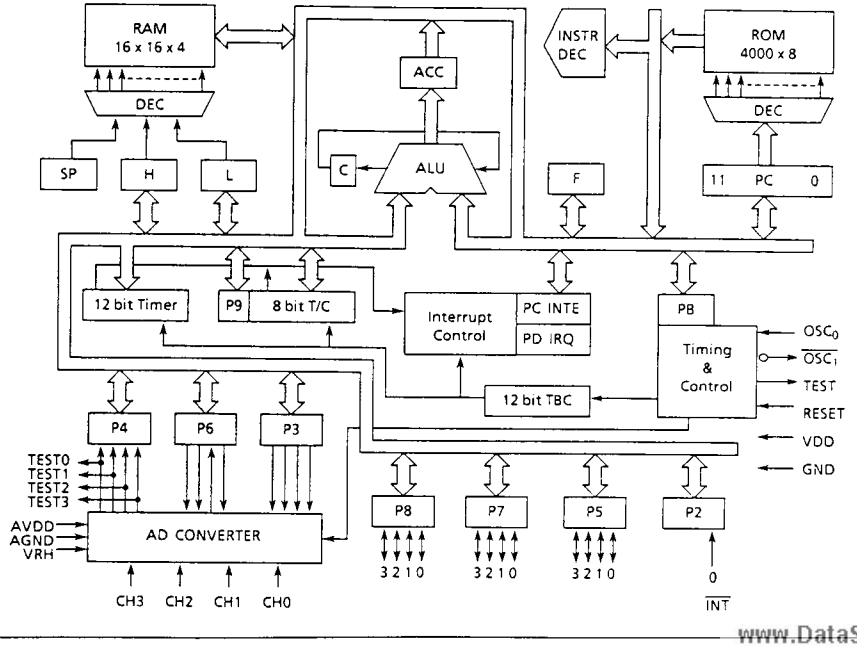
(Top View) 30-Lead Plastic Shrink DIP



(Top View) 40-pin Plastic DIP



BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Input/Output	Function	When Reset
P20/$\overline{INT}$	Input	Input port with a latch. P20 is shared with INT input. (Fall trigger input). Built-in pull up register	The latch is reset
P50 - 53	Input/Output	4-bit input/output port	"0"
P70 - 73	Input/Output	4-bit input/output port	"0"
P80 - 83	Input/Output	4-bit input/output port	"0"
$\overline{OSC0}$ $\overline{OSC1}$	Input/Output	X'tal connection terminal for system clock oscillation	Oscillation wave
TEST	Output	(Test terminal for Maker)	Pulse output
TEST0 - 3	Output		Hi-z
RESET	Input	System reset input terminal	
CH0 - 3	Input	Analog voltage input pin	
VRH		Reference voltage input pin for A/D converter	
AVDD AGND		A/D converter power supply	
VDD GND		System power supply	

INSTRUCTION LIST

	Mnemonic	Description	Code	Byte	Cycle
Load, Push, Pop	LAI n	A←n	9n	1	1
	LLI n	L←n	8n	1	1
	LHLI nn	HL←nn	15nn	2	2
	LMI nn	M(w)←nn	14nn	2	2
	LAL	A←L	21	1	1
	LLA	L←A	2D	1	1
	LAH	A←H	22	1	1
	LHA	H←A	2E	1	1
	LAM	A←M	38	1	1
	LMA	M←A	2F	1	1
	LAM +	A←M, L←L + 1, Skip if L = 0	24	1	1

INSTRUCTION LIST (Continued)

	Mnemonic	Description	Code	Byte	Cycle
Load, Push, Pop	LAM –	A←M, L←L – 1, Skip if L = F	25	1	1
	LMA +	M←A, L←L + 1, Skip if L = 0	26	1	1
	LMA –	M←A, L←L – 1, Skip if L = F	27	1	1
	LAMM n_2	A←M, H←H∀n_2	39-3B	1	1
	LAMD mm	A←Md	10mm	2	2
	LMAD mm	Md←A	11mm	2	2
	LMTD mm	Md(w)←T(M(w), A), T = ROM table	19mm	2	3
	LMCT	M(w)←CT	3E59	2	2
	LCTM	CT←M(w)	3E51	2	2
	LTMM	TM←(M(w), A)	3E50	2	2
	PUSH	ST←C, A, H, L, SP←SP – 4	1C	1	3
	POP	C, A, H, L←ST SP←SP + 4	1D	1	3
Exchange	X	A↔M	28	1	1
	XM n_2	A↔M, H←H∀n_2	29-2B	1	1
	X +	A↔M, L←L + 1, Skip if L = 0	3C	1	1
	X –	A↔M, L←L – 1, Skip if L = F	2C	1	1
Increment/ Decrement	INA	A←A + 1, Skip if A = 0	30	1	1
	INM	M←M + 1, Skip if M = 0	33	1	1
	INL	L←L + 1, Skip if L = 0	31	1	1
	INH	H←H + 1, Skip if M = 0	32	1	1
	INMD mm	Md←Md + 1, Skip if Md = 0	12mm	2	2
	DCA	A←A – 1, Skip if A = F	34	1	1
	DCM	M←M – 1, Skip if M = F	37	1	1
	DCL	L←L – 1, Skip if L = F	35	1	1
	DCH	H←H – 1, Skip if H = F	36	1	1
	DCMD mm	Md←Md – 1, Skip if Md = F	13mm	2	2
Arithmetic	ADS	A←A + M, Skip if Cy = 1	02	1	1
	ADCS	A, C←A + M + C, Skip if Cy = 1	01	1	1
	ADC	A, C←A + M + C	03	1	1
	AIS n	A←A + n, Skip if Cy = 1	3E4n	2	2
	DAA	A←A + 6	06	1	1
	DAS	A←A + 10	0A	1	1

INSTRUCTION LIST (Continued)

	Mnemonic		Description	Code	Byte	Cycle
Arithmetic	AND		A←A ∧ M	0D	1	1
	OR		A←A∨M	05	1	1
	EOR		A←A∀M	04	1	1
	CMA		A←$\overline{A}$	0B	1	1
	CIA		A←$\overline{A}$ + 1	0C	1	1
	RAL		Rotate Left with C	0E	1	1
	RAR		Rotate Right with C	0F	1	1
	TC		Skip if C = 1	09	1	1
	SC		C←1	07	1	1
	RC		C←0	08	1	1
Compare	CAI	n	Skip if A = n	3E0n	2	2
	CLI	n	Skip if L = n	3E2n	2	2
	CPI	p, n	Skip if Pp = n	17pn	2	2
	CMI	n	Skip if M = n	3E1n	2	2
	CAM		Skip if A = M	16	1	1
Bit operation	TAB	n_2	Skip if A bit (n_2) = 1	54-57	1	1
	RAB	n_2	A bit (n_2)←0	64-67	1	1
	SAB	n_2	A bit (n_2)←1	74-77	1	1
	TMB	n_2	Skip if M bit (n_2) = 1	58-5B	1	1
	RMB	n_2	M bit (n_2)←0	68-6B	1	1
	SMB	n_2	M bit (n_2)←1	78-7B	1	1
	TFB	n_2	Skip if F bit (n_2) = 1	5C-5F	1	1
	RFB	n_2	F bit (n2)←0	6C-6F	1	1
	SFB	n_2	F bit (n_2)←1	7C-7F	1	1
	TPB	n_2	Skip if P bit (n_2) = 1	50-53	1	1
	RPB	n_2	P bit (n_2)←0	60-63	1	1
	SPB	n_2	P bit (n_2)←1	70-73	1	1
	TPBD	pn_2	Skip if Pp bit (n_2) = 1	3D $p_{0\sim3}$	2	2
	RPBD	pn_2	Pp bit (n_2)←0	3D $p_{4\sim7}$	2	2
	SPBD	pn_2	Pp bit (n_2)←1	3D $p_{8\sim B}$	2	2

INSTRUCTION LIST (Continued)

	Mnemonic	Description	Code	Byte	Cycle
Interrupt	MEI	MEIF←1	3E60	2	2
	MDI	MEIF←0	3E61	2	2
	EITB	EITBF←1	3DC9	2	2
	EITM	EITMF←1	3DCA	2	2
	EICT	EICTF←1	3DCB	2	2
	EIEX	EIEXF←1	3DC8	2	2
	DITB	EITBF←0	3DC5	2	2
	DITM	EITMF←0	3DC6	2	2
	DICT	EICTF←0	3DC7	2	2
	DIEX	EIEXF←0	3DC4	2	2
	TITB	Skip if EITBF = 1	3DC1	2	2
	TITM	Skip if EITMF = 1	3DC2	2	2
	TICT	Skip if EICTF = 1	3DC3	2	2
	TIEX	Skip if EIEXF = 1	3DC0	2	2
	TQEX	Skip if IRQEX = 1	3D20	2	2
	TQTB	Skip if IRQTB = 1	3DD0	2	2
	TQTM	Skip if IRQTM = 1	3DD1	2	2
	TQCT	Skip if IRQCT = 1	3DD2	2	2
	RQEX	IRQEX←0	3D24	2	2
	RQTB	IRQTB←0	3DD4	2	2
	RQTM	IRQTM←0	3DD5	2	2
	RQCT	IRQCT←0	3DD6	2	2
Counter	ECT	CTF←1 (start)	3DBB	2	2
	DCT	CTF←0 (stop)	3DB7	2	2
	TCT	Skip if CTF = 1	3DB3	2	2
Branch	JCP a_6	PC←a_6	C0~FF	1	1
	JP a_{12}	PC←a_{12}	$4a_{12}$	2	2
	CZP a	ST←PC + 1, PC←2a, SP←SP − 4	Ba	1	4
	CAL a_{12}	ST←PC + 2, PC←a_{12}, SP←SP − 4	Aa_{12}	2	4
	RT	PC←ST, SP←SP + 4	IE	1	4

INSTRUCTION LIST (Continued)

	Mnemonic	Description	Code	Byte	Cycle
Branch	RTS	PC←ST, SP←SP + 4, Skip unconditional	IF	1	4
	JA	PC←(PC←A) + 1	IA	1	1
	JM	PC←(M(w), A)	IB	1	2
Input/ Output	IP	A←P	20	1	1
	IPD p	A←Pp	3DpD	2	2
	OP	P←A	23	1	1
	OPD p	Pp←A	3DpC	2	2
CPU control	NOP	No Operation	00	1	1
	HALT	Halt CPU	3DB8	2	2
	STOP	Stop Clock	3DB9	2	2

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	Ta = 25°C	− 0.3 to 7	V
	AV_{DD}		− 0.3 to 7 $AV_{DD} = V_{DD}$	V
	VRH		− 0.3 to V_{DD}	V
Input Voltage	V_I		− 0.3 toV_{DD}	V
Output Voltage	V_O		− 0.3 toV_{DD}	V
Power Dissipation	P_D	Ta = 25°C per package	200 max.	mW
		Ta = 25°C per out	50 max.	mW
Storage Temperature	T_{STG}	−	− 55 to + 150	°C

OPERATING RANGE

Item	Symbol	Conditions	Limits	Unit
Supply Voltage	V_{DD}	$f_{(OSC)} \leqq 1$ MHz	3 to 6	V
		$f_{(OSC)} \leqq 4.2$ MHz	4.5 to 5.5	V
Data-Hold Voltage	V_{DDH}	$f_{(OSC)} = 0$ Hz	2 to 6	V
Operating Temperature	T_{OP}	–	– 40 to + 85	°C
Fan Out	N	MOS Load	15	–
		TTL Load	1	

DC CHARACTERISTICS

($V_{DD} = AV_{DD} = 5V \pm 10\%$, Ta = – 40 to + 85°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
"H" Input voltage *1 *2	V_{IH}	–	2.4	–	V_{DD}	V
"H" Input voltage *3 *4	V_{IH}	–	3.6	–	V_{DD}	V
"L" Input voltage	V_{IL}	–	– 0.3	–	0.8	V
"H" Output Voltage *1 *5	V_{OH}	$I_O = -15\mu A$	4.2	–	–	V
"L" Output voltage *1	V_{OL}	$I_O = 1.6$mA	–	–	0.4	V
"L" Output voltage *5	V_{OL}	$I_O = 15\mu A$	–	–	0.4	V
"L" Output voltage *6	V_{OL}	$I_O = 8$mA	–	1	2	V
Input Current *3	I_{IH}/I_{IL}	$V_I = V_{DD}/0V$	–	–	15/ – 15	μA
Input Current *2 *4	I_{IH}/I_{IL}	$V_I = V_{DD}/0V$	–	–	1/ – 30	μA
"H" Output Current *1	I_{OH}	$V_O = 2.4V$	– 0.1	–	–	mA
"H" Output Current *1	I_{OH}	$V_O = 0.4V$	–	–	– 1.2	mA
Input Capacity	C_I	f = 1MHz, Ta = 25°C	–	5	–	pF
Output Capacity	C_O		–	7	–	

DC CHARACTERISTICS (Continued)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Current Dissipation (when stop condition)	I_{DDS}	V_{DD} = 2V, no load Ta = 25°C	–	0.2	5	μA
		No load	–	1	100	μA
Current Dissipation	I_{DD}	Quarts oscillation f = 4.19MHz, no load	–	–	20	mA

*1 Applied to P5, P7 and P8
*2 Applied to P2
*3 Applied to OSC_0
*4 Applied to RESET
*5 Applied to $\overline{OSC_1}$
*6 In using LED, total output current should be within the limit of Power dissipatation in "Absolute Maximum Rating."

AC CHARACTERISTICS

($V_{DD} = AV_{DD} = 5V \pm 10\%$, Ta = − 40 to + 85°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Clock Pulse Width Clock (OSC)	$t_{\phi W}$	–	119	–	–	ns
Cycle Time	t_{CY}	–	952	–	–	ns
Input Data Setup Time	t_{DS}	–	120	–	–	ns
Input Data Hold Time	t_{DH}	–	120	–	–	ns
Data Delay Time	t_{DR}	C_L = 15pF	–	–	t_{CY} + 300	ns
INT Invalid Time	t_{IINH}	–	1/8 t_{CY}	–	–	ns

A/D CONVERSION CHARACTERISTICS

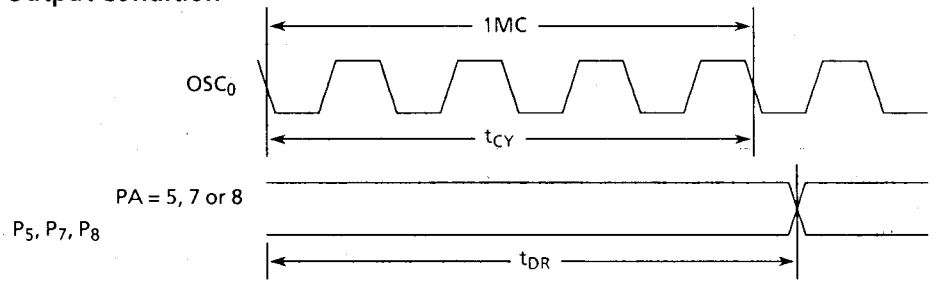
($V_{DD} = AV_{DD} = V_{RH} = 5V \pm 10\%$, GND = AGND = 0V, 1MHz ≦ f(osc) ≦ 4.2MHz, Ta = − 40 to + 85°C)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Resolution	–	–	8	–	–	Bits
Absolute Accuracy	–	–	–	–	± 1.5	LSB
Conversion Speed	t_{CON}	SPEED = "0"	60t cy	–	–	ns
		SPEED = "1"	120t cy	–	–	ns
Analog channel Input Voltage	VI	–	AGND	–	VRH	V
Analog channel Input Current	ILI	VI ≧ AGND VI ≦ VRH	–	–	± 1	μA
VRH Input Current	I REF	–	–	0.5	1.0	mA

(Note: t cy = 952ns (f(osc) = 4.2MHz))

TIMING CHARTS

Output Condition



Input Condition