MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ CE

500V CoolMOS™ CE Power Transistor
IPA50R650CE

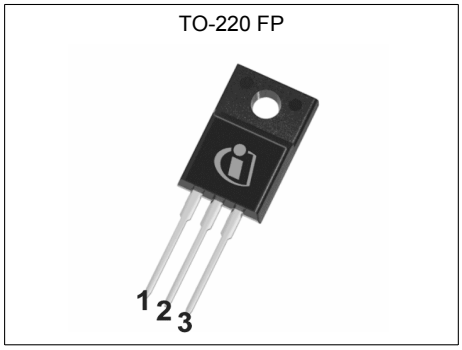
Data Sheet

Rev. 2.1
Final

Power Management & Multimarket

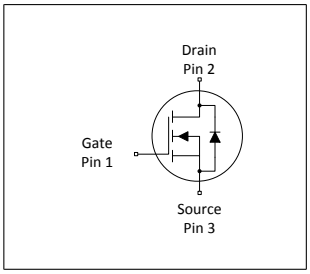
1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE series combines the experience of the leading SJ MOSFET supplier with high class innovation while representing a cost appealing alternative compared to standard MOSFET in target applications. The resulting devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter and cooler.



Features

- Extremely low losses due to very low FOM Rdson*Qg and Eoss
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for consumer grade applications according to JEDEC (J-STD20 and JESD22)



Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages for e.g. PC Silverbox, Adapter, LCD & PDP TV and Lighting.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or seperate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	550	V
$R_{DS(on),max}$	0.65	Ω
$Q_{g,typ}$	15	nC
$I_{D,pulse}$	19	A
E_{oss} @ 400V	1.69	µJ
Body diode di/dt	500	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPA50R650CE	PG-TO 220 FullPAK	5R650CE	see Appendix A

Table of Contents

2 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - -	- - -	6.1 4.6 2.9	A	T_C = 25°C; TO-220 T_C = 25°C; TO-220 FullPAK T_C = 100°C; TO-220 FullPAK
Pulsed drain current[2]	$I_{D,pulse}$	-	-	19	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	102	mJ	I_D =2.3A; V_{DD} = 50V
Avalanche energy, repetitive	E_{AR}	-	-	0.15	mJ	I_D =2.3A; V_{DD} = 50V
Avalanche current, repetitive	I_{AR}	-	-	2.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	V_{DS} =0...400V
Gate source voltage	V_{GS}	-20 -30	- -	20 30	V	static; AC (f>1 Hz)
Power disspiation	P_{tot}	-	-	27.2	W	T_C=25°C
Operating and storage temperature	T_j, T_{stg}	-40	-	150	°C	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	I_S	-	-	4.0	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	19.0	A	T_C = 25°C
Reverse diode dv/dt[3]	dv/dt	-	-	15	V/ns	V_{DS} =0...400V, I_{SD}<=I_S, T_j=25°C
Maximum diode commutation speed[3]	di_f/dt	-	-	500	A/µs	V_{DS} =0...400V, I_{SD}<=I_S, T_j=25°C
Insulation withstand voltage for TO-220 FullPAK	V_{ISO}	-	-	2500	V	V_{rms}, T_C=25°C, t=1min

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.6	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

[1] Limited by $T_{j\,max}$. Maximum duty cycle D=0.75
[2] Pulse width t_p limited by $T_{j,max}$
[3] V_{DClink}=400V; $V_{DS,peak}$<$V_{(BR)DSS}$; identical low side and high side switch with identical R_G

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	2.50	3	3.50	V	V_{DS}=V_{GS}, I_D=0.15mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=500V, V_{GS}=0V, T_j=25°C V_{DS}=500V, V_{GS}=0V, T_j=150°C
Gate-source leakage curent	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.59 1.52	0.65 -	Ω	V_{GS}=13V, I_D=1.8A, T_j=25°C V_{GS}=13V, I_D=1.8A, T_j=150°C
Gate resistance	R_G	-	3	-	Ω	f=1 MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	342	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Output capacitance	C_{oss}	-	26	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Effective output capacitance, energy related[1)]	$C_{o(er)}$	-	21	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[2)]	$C_{o(tr)}$	-	80	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	6	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.3A, R_G=5.3Ω
Rise time	t_r	-	5	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.3A, R_G=5.3Ω
Turn-off delay time	$t_{d(off)}$	-	27	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.3A, R_G=5.3Ω
Fall time	t_f	-	13	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=2.3A, R_G=5.3Ω

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	1.8	-	nC	V_{DD}=400V, I_D=2.3A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	8.1	-	nC	V_{DD}=400V, I_D=2.3A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	15	-	nC	V_{DD}=400V, I_D=2.3A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.3	-	V	V_{DD}=400V, I_D=2.3A, V_{GS}=0 to 10V

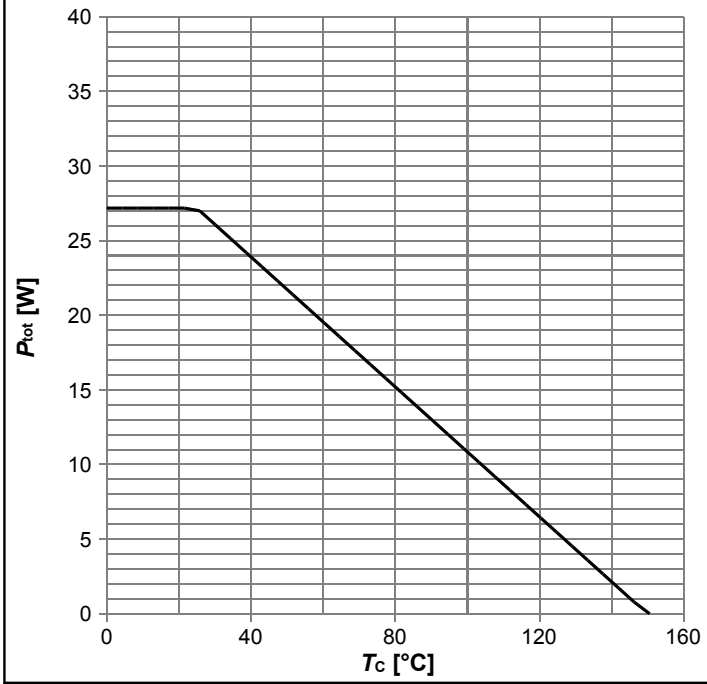
[1)] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2)] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.84	-	V	V_{GS}=0V, I_F=2.3A, T_j=25°C
Reverse recovery time	t_{rr}	-	162	-	ns	V_R=400V, I_F=2.3A, di_F/dt=100A/µs
Reverse recovery charge	Q_{rr}	-	1	-	µC	V_R=400V, I_F=2.3A, di_F/dt=100A/µs
Peak reverse recovery current	I_{rrm}	-	11.1	-	A	V_R=400V, I_F=2.3A, di_F/dt=100A/µs

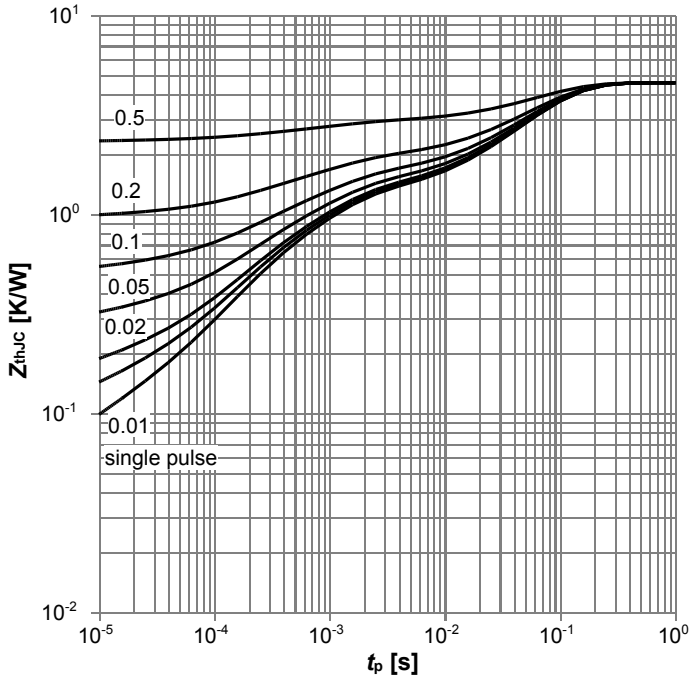
5 Electrical characteristics diagrams

Power dissipation (FullPAK)



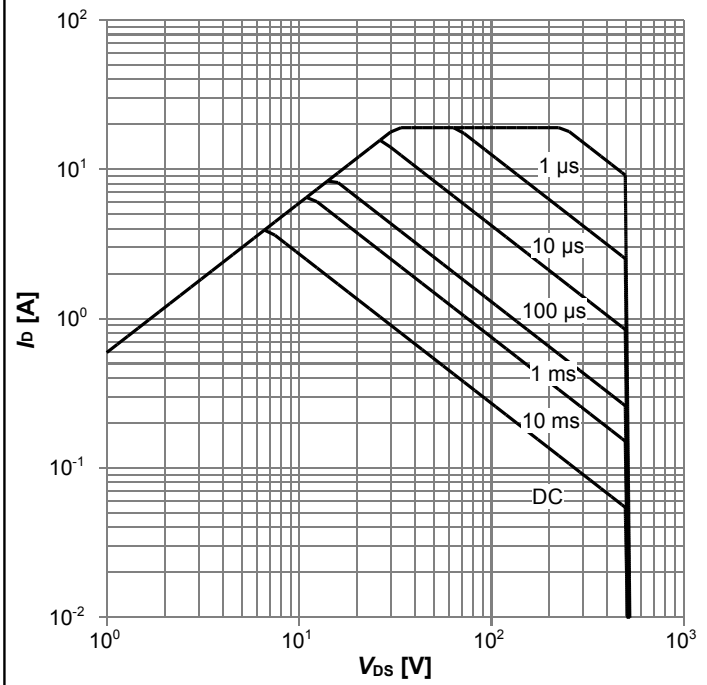
$P_{tot}=f(T_C)$

Max. transient thermal impedance (FullPAK)



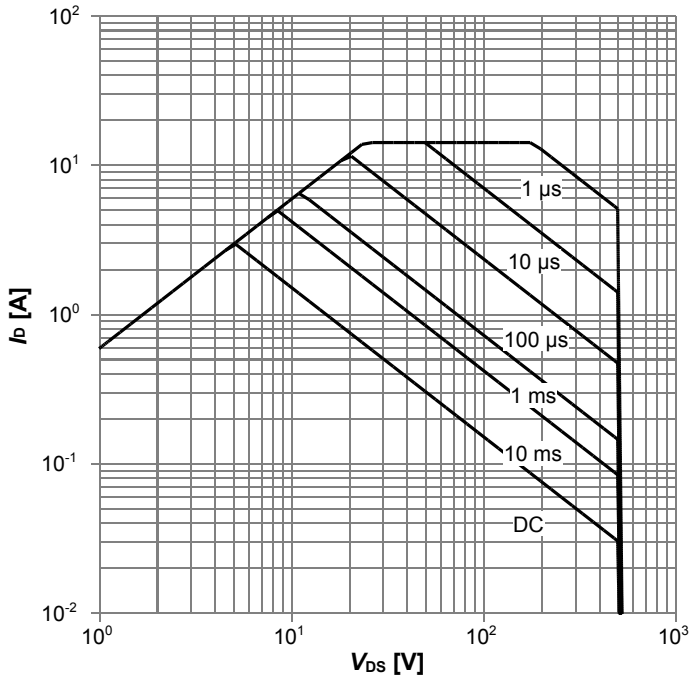
$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$

Safe operating area (FullPAK) Tj=25°C



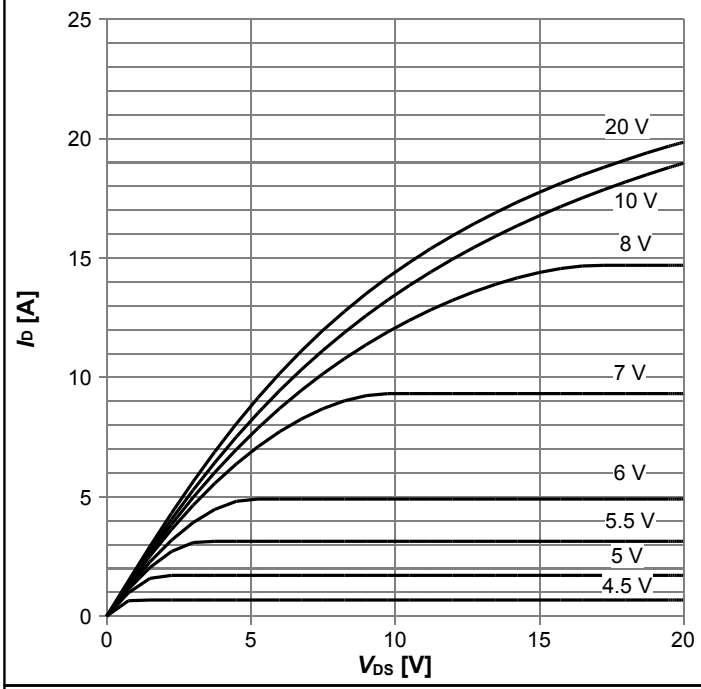
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Safe operating area (FullPAK) Tj=80°C



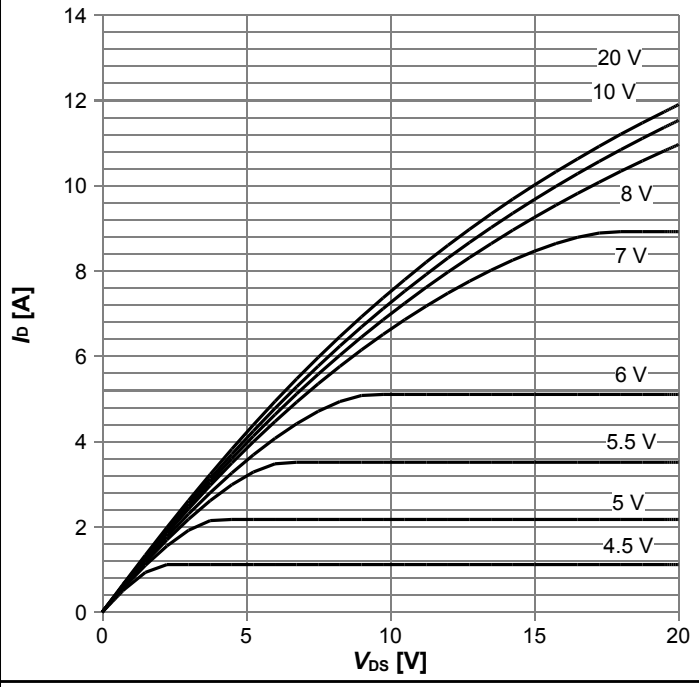
$I_D=f(V_{DS})$; T_C=80 °C; D=0; parameter: t_p

Typ. output characteristics Tj=25°C



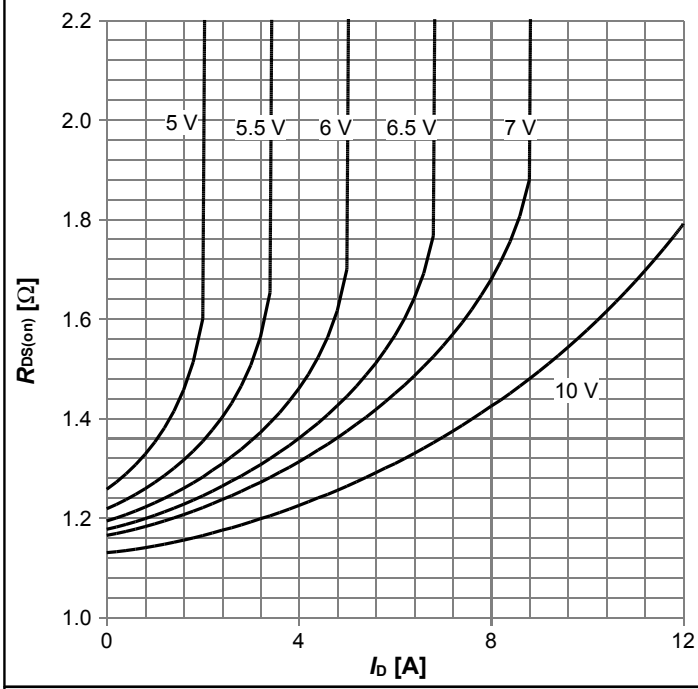
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Typ. output characteristics Tj=125°C



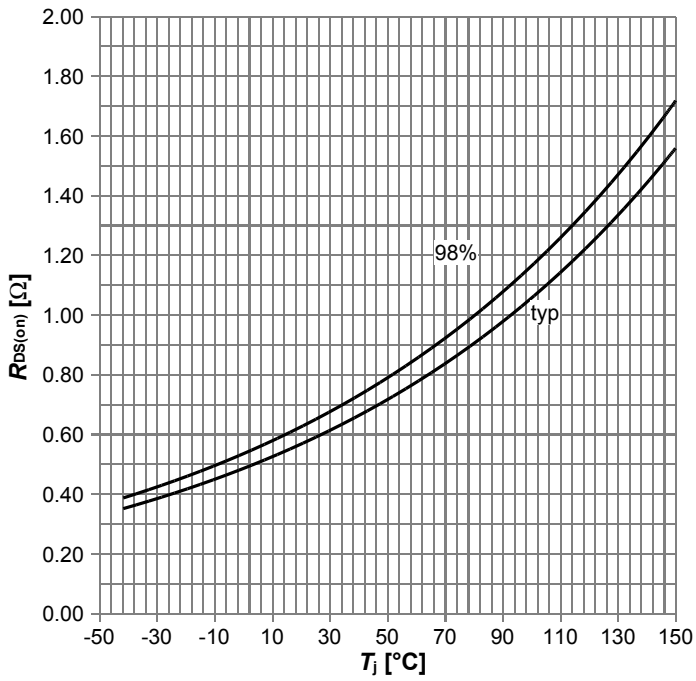
$I_D=f(V_{DS})$; $T_j=125$ °C; parameter: V_{GS}

Typ. drain-source on-state resistance



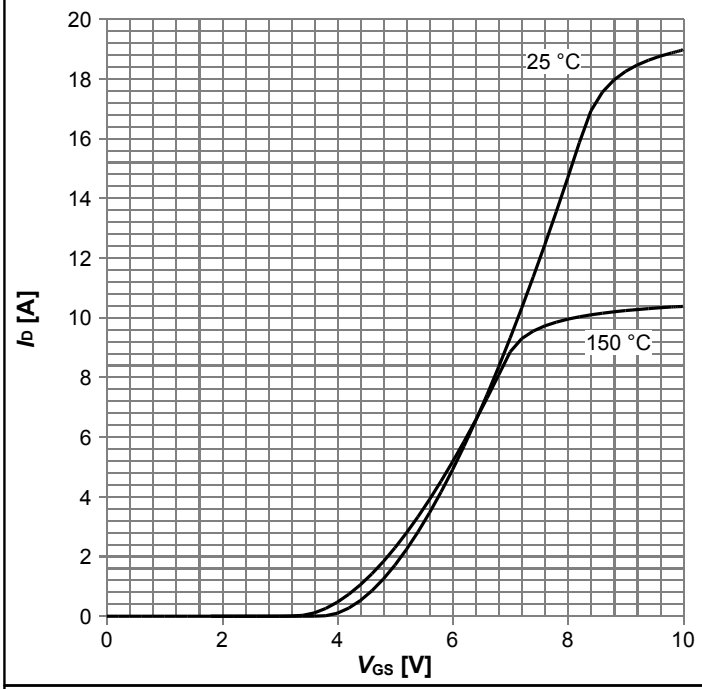
$R_{DS(on)}=f(I_D)$; $T_j=125$ °C; parameter: V_{GS}

Drain-source on-state resistance



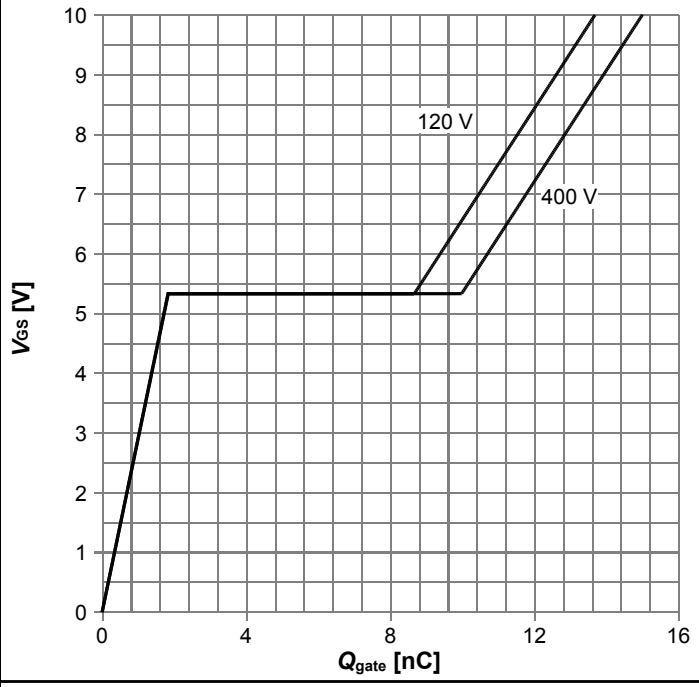
$R_{DS(on)}=f(T_j)$; $I_D=1.8$ A; $V_{GS}=13$ V

Typ. transfer characteristics



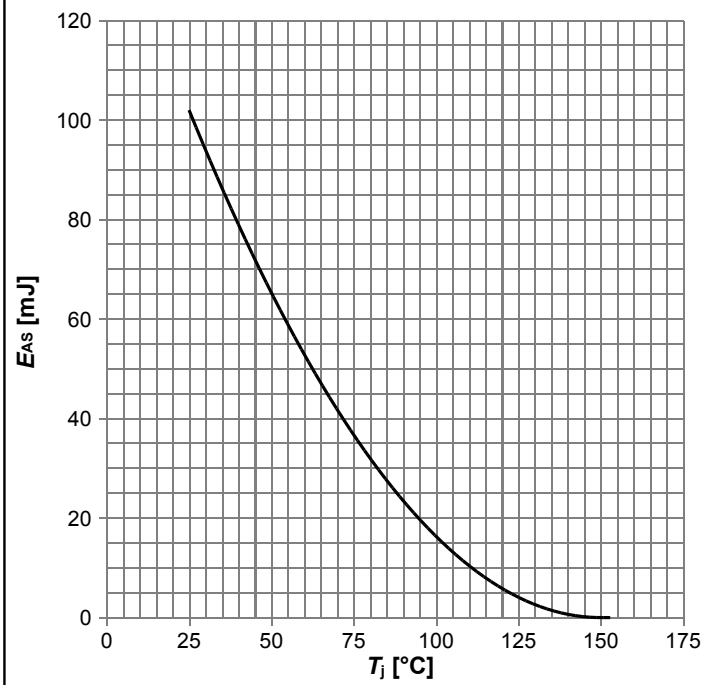
$I_D=f(V_{GS})$; V_{DS}=20V; parameter: T_j

Typ. gate charge



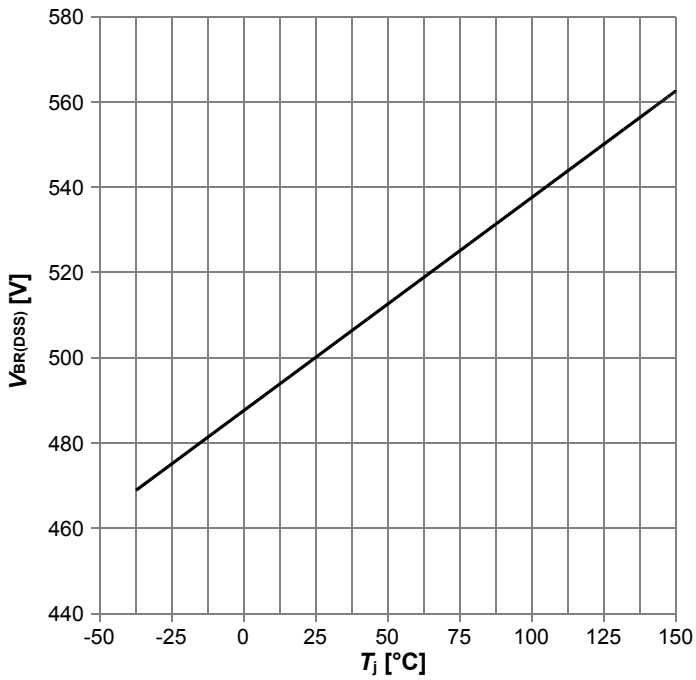
$V_{GS}=f(Q_{gate})$; I_D=2.3 A pulsed; parameter: V_{DD}

Avalanche energy



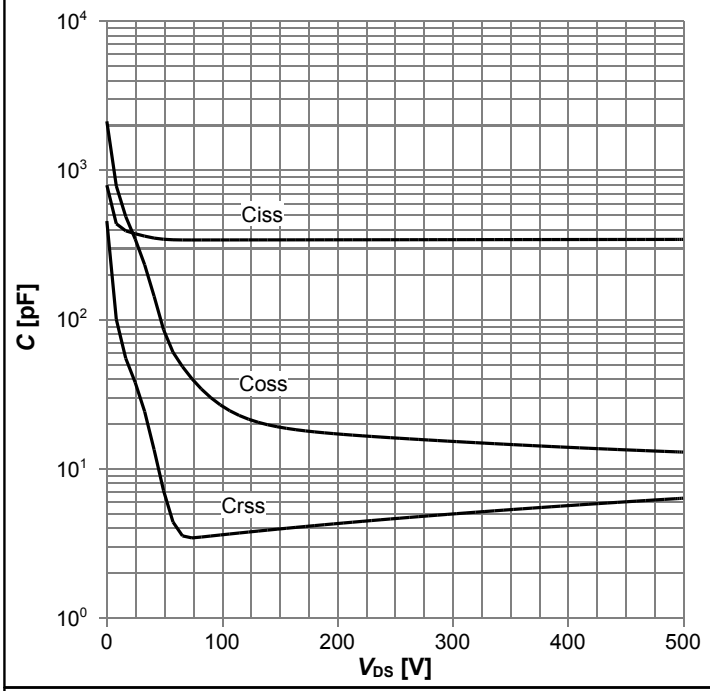
$E_{AS}=f(T_j)$; I_D=2.3 A; V_{DD}=50 V

Drain-source breakdown voltage



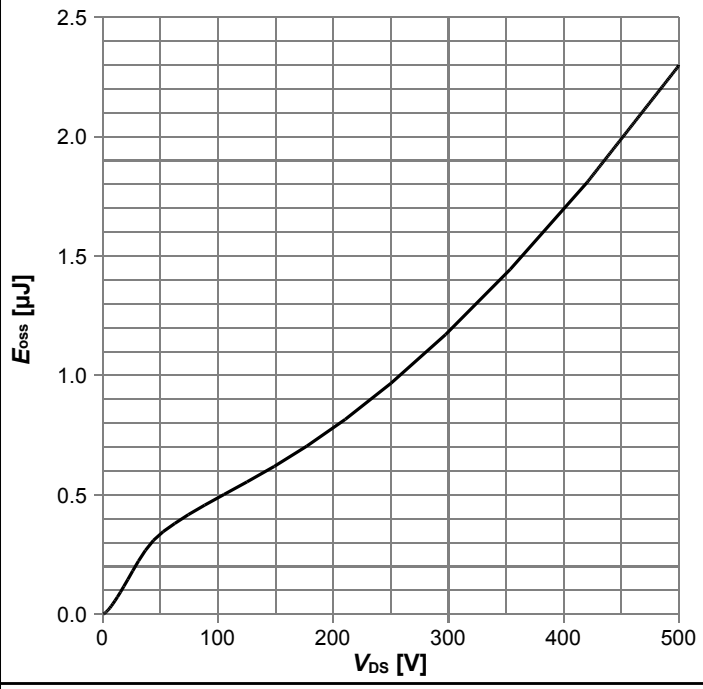
$V_{BR(DSS)}=f(T_j)$; I_D=1 mA

Typ. capacitances



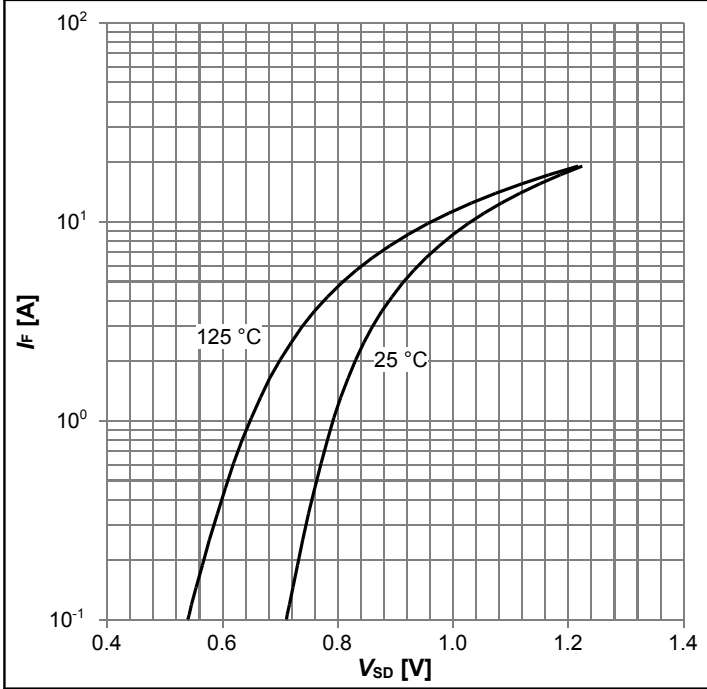
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Typ. Coss stored energy



E_{oss}=f(V_{DS})

Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

6 Test Circuits

Table 8 Diode characteristics

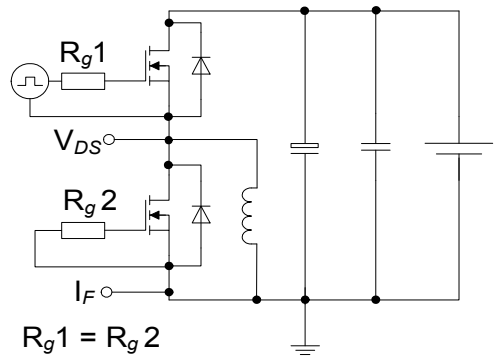
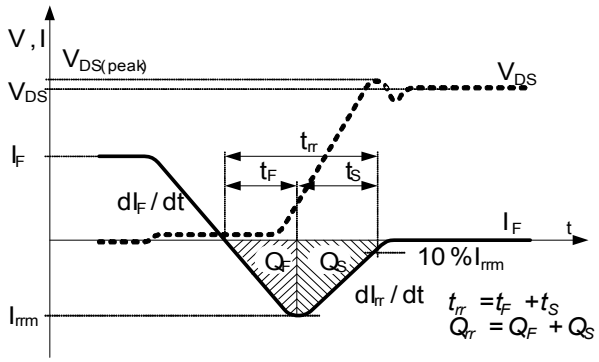
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

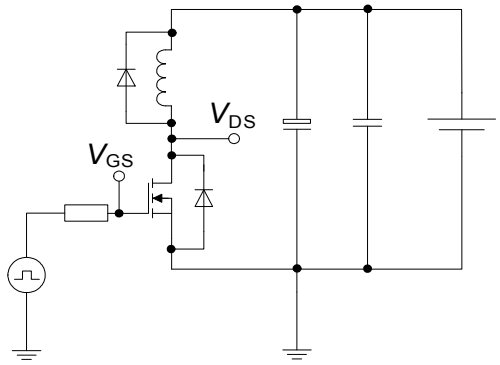
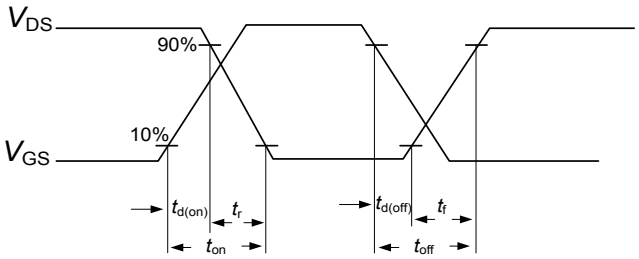
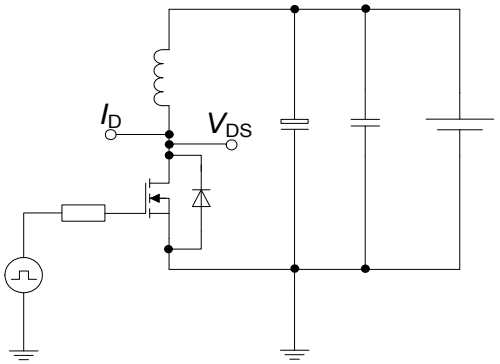
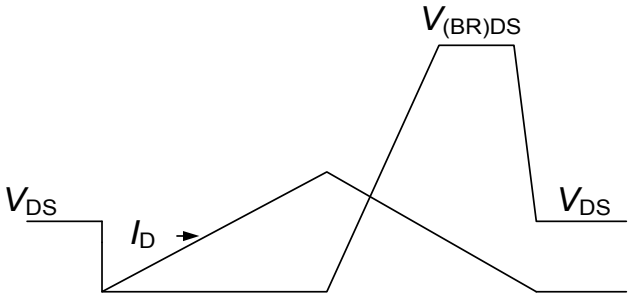
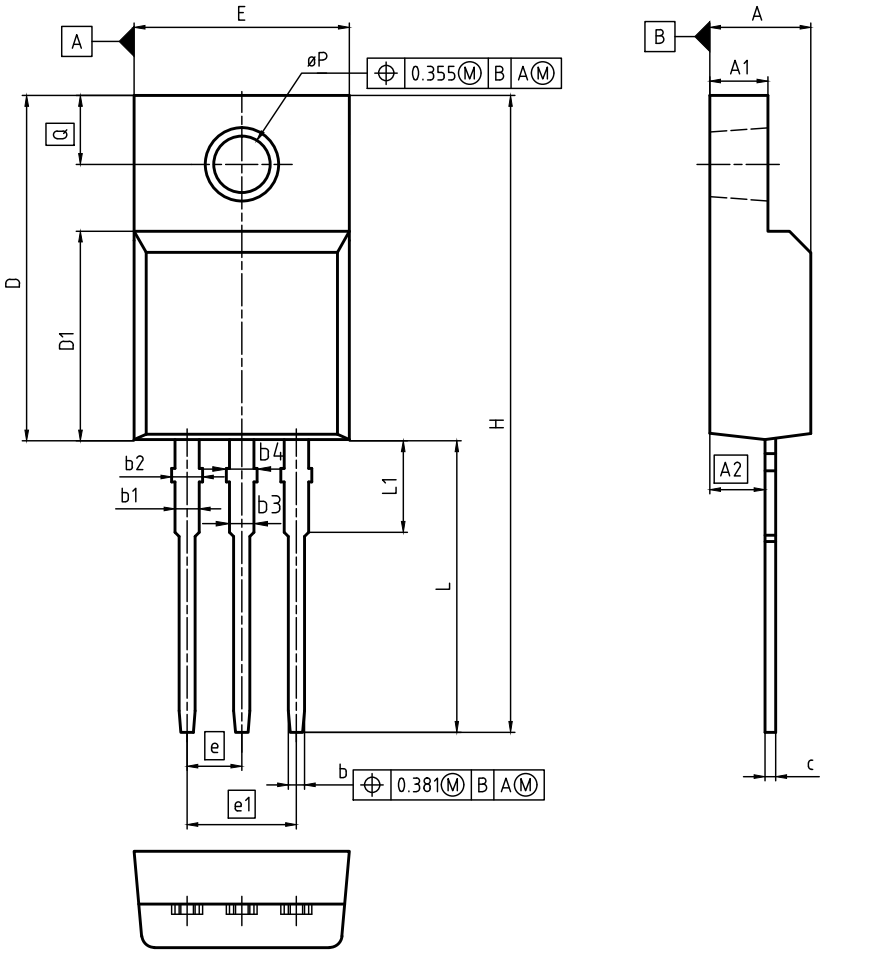
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.85	0.092	0.112
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	0.95	1.51	0.037	0.059
b3	0.65	1.38	0.026	0.054
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
øP	2.95	3.38	0.116	0.133
Q	3.15	3.50	0.124	0.138

DOCUMENT NO.
Z8B00003319

SCALE
0 2.5 0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
05-05-2014

REVISION
04

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

8 Appendix A

Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPA50R650CE

Revision: 2014-06-12, Rev. 2.1

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2012-08-24	Release of final version
2.1	2014-06-12	Release of final datasheet

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