



# Data Book

**AU6362**

**USB 2.0 Multiple Slots  
Flash Memory Card Reader  
Technical Reference Manual**

**Product Specification**

**Initial Release**

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### Data sheet status

Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.

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# 1.0 Introduction

## 1.1 Description

This AU6362 is a highly integrated single chip USB 9-in-1 flash memory card reader controller. It supports USB v2.0 high-speed transmission to all of the popular storage media interface on one chip, such as Compact Flash (CF), Micro Drive (MD), Smart Media Card (SMC), Secure Digital (SD), Multi Media Card (MMC), Memory Stick (MS, MS Pro, MS Duo) and Digital photo (xD),

The AU6362 supports USB v2.0 and USB v1.0 Storage Class specification. It can read digital contents stored on memory card designed to cover a wide area of applications such as digital cameras, PDAs, MP3 players and smart phones...etc. With the AU6362, users can transfer digital data between flash memory card and PC or these electronic devices.

The integration of various mixed mode makes component AU6362 is the most powerful and most effective solution for multi-slot flash memory readers.

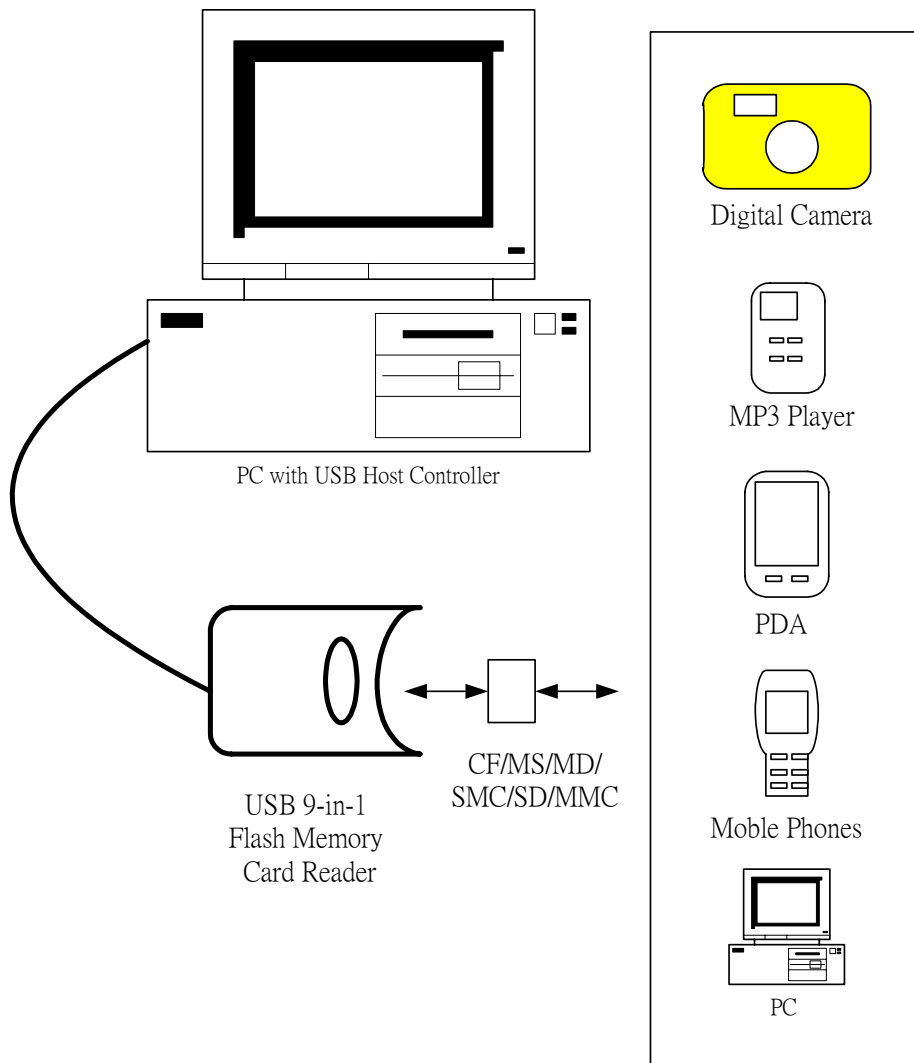
## 1.2 Features

- Support USB v2.0 specification and USB Device Class Definition for Mass Storage, Bulk-Transport v1.0
- Integrated USB 2.0 Transceiver Macrocell Interface (UTMI) transceiver and Serial interface Engine
- Support CF/MD, SD/MMC, MS/MS PRO/MS ROM/MS Duo AND xD/SMC specification
- Support 1 piece NAND type flash memory up to 2Gbit capacity.
- Work with default driver from Windows ME, Windows XP, and Mac OS X. Windows 98, Windows 2000 are supported by vendor AP (The AP included both win98 and 2000 driver) from Alcor.
- Ping-pong FIFO implementation for concurrent bus operation
- Support multiple sectors transfer optimize performance
- Support optional external EEPROM for USB VID, PID and string customization
- Support slot-to-slot read/write operation.
- Support auto-detecting slot with card inserted on Win 2000 without driver.
- Capable of handing 4 sets of built-in PID, VID and strings to minimize inventory control and improve lead production lead-time.
- Support LED for bus activity indication.
- Each slot can be enables/disabled by 5 independent pins to fit all the different card readers' combination requirement.
- Runs at 30MHz, built-in 480 MHz PLL
- Built-in 3.3V to 2.5V regulator

## 2.0 Application Block Diagram

Following is the application diagram of a typical card reader product with AU6362. By connecting the card reader to a desktop or notebook PC through USB bus, AU6362 is implemented as a bus-powered, full speed USB card reader, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

### 2.1 Block Diagram

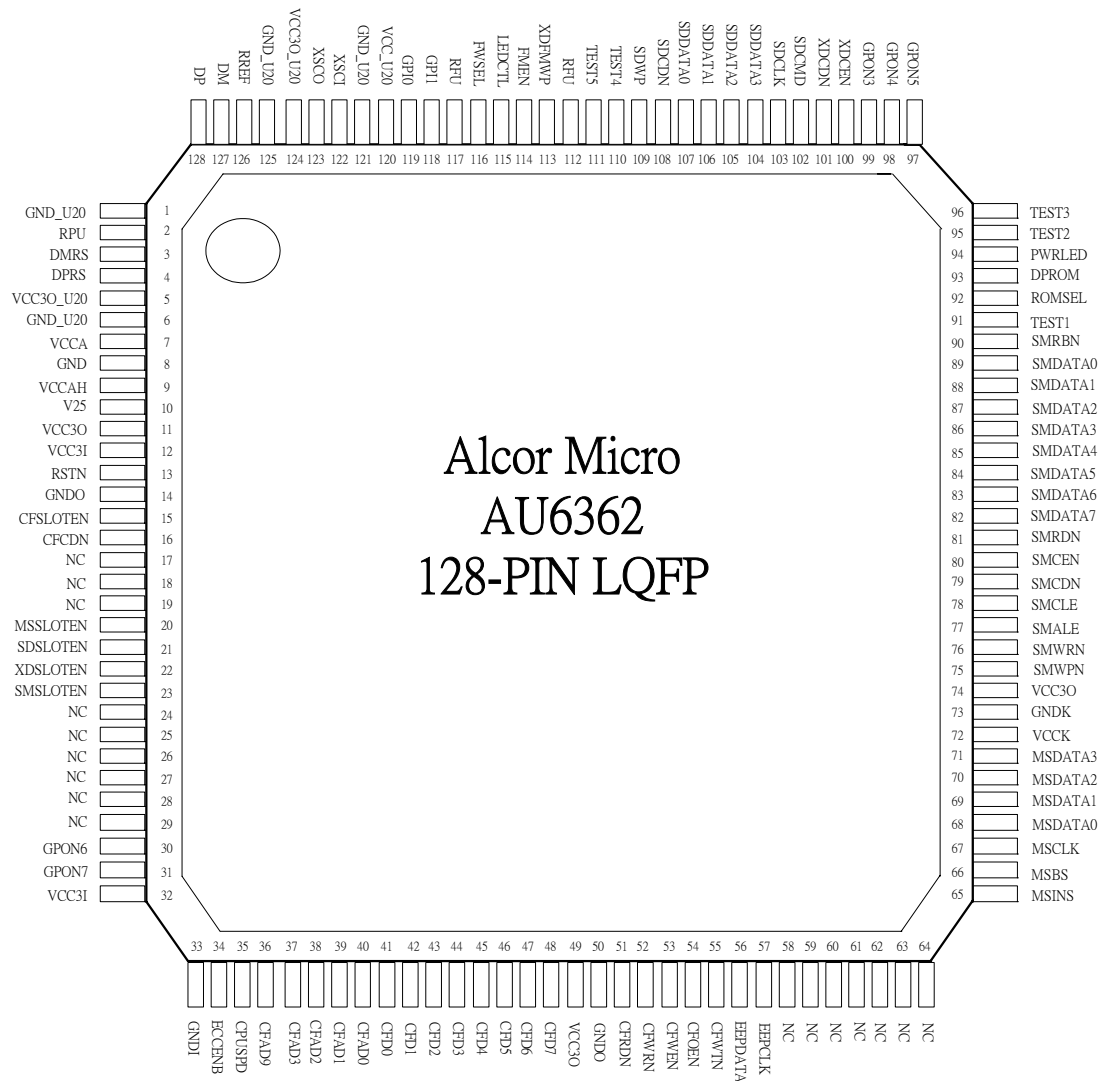




# 3.0 Pin Assignment

The AU6362 is packed in 128pin-LQFP-form factor. The following figure shows signal name for each pin and the table in the following page describes each pin in detail.

Figure 3.1 Pin Assignment Diagram







**Table 3.1 Pin Descriptions**

Pin #	Pin Name	I/O	Description
1	GND_U20	PWR	USB 2.0 Ground supply
2	RPU	I	Connects external resistor (1.5k $\Omega$ $\pm$ 5%) to analog GND.
3	DMRS	I/O	USB 1.1 data positive pin terminal
4	DPRS	I/O	USB 1.1 data negative pin terminal
5	VCC30_U20	PWR	USB IO pad power supply 3.3V
6	GND_U20	PWR	USB 2.0 Ground
7	VCCA	PWR	Power supply 3.3v
8	GND	PWR	Ground
9	VCCA_H	PWR	Power supply 3.3v
10	V25	O	Regulator Voltage output 2.5v
11	VCC30		Pad power supply 3.3v
12	VCC3I		Pad power supply 3.3v
13	RSTN	I	Reset (low active to reset the whole chip), must be pull up with RC.
14	GNDO		IO pad Ground Supply
15	CFSLOTEN	I	CF slot enable. ("1": disable, "0":enable)
16	CFCDN	I	CF card detect. ("1": undetected,"0": detect)
17	NC		
18	NC		
19	NC		
20	MSSLOTEN	I	MS slot enable. ("1": disable, "0": enable)
21	SDSLOTEN	I	SD slot enable. ("1": disable, "0": enable)
22	XDSLOTEN	I	XD slot enable. ("1": disable, "0": enable)
23	SMSLOTEN	I	SMC slot enable. ("1": disable, "0": enable)
24	NC		
25	NC		
26	NC		
27	NC		
28	NC		
29	NC		
30	GPON6	O	General Purpose Output.
31	GPON7	O	General Purpose Output.
32	VCC3I		IO pad Power supply 3.3v
33	GNDI		IO pad Ground
34	ECCENB	I	Selection ECC. (default:'1'; Disable:'0', Enable:'1')
35	CPUSPD	I	Selection CPU Speed. (default:'0'; 30MHz:'0', 15MHz:'1')
36	CFAD9	O	CF Addr9.
37	CFAD3	O	CF Addr3.
38	CFAD2	O	CF Addr2.
39	CFAD1	O	CF Addr1.
40	CFAD0	O	CF Addr0.
41	CFD0	I/O	CF Data0.
42	CFD1	I/O	CF Data1..
43	CFD2	I/O	CF Data2.
44	CFD3	I/O	CF Data3.
45	CFD4	I/O	CF Data4.
46	CFD5	I/O	CF Data5.
47	CFD6	I/O	CF Data6.
48	CFD7	I/O	CF Data7.
49	VCC30		IO pad Power supply 3.3v
50	GNDO		Ground
51	CFRDN	O	CF IORDN. ("1": disable, "0": enable)
52	CFWRN	O	CF IOWRN. ("1": disable, "0": enable)
53	CFWEN	O	CF WEN. ("1": disable, "0": enable)



54	CFOEN	O	CF OEN. ("1": disable, "0": enable)
55	CFWTN	I	CF WAITN. External pull up with 100K to CFPWR. (low true for card busy)
56	EEPDATA	I/O	EEPROM for PID, VID customization. External pull up with 1K to 3.3V.
57	EEPCLK	O	EEPROM serial clock.
58	NC		
59	NC		
60	NC		
61	NC		
62	NC		
63	NC		
64	NC		
65	MSINS	I	MS stick insertion/extraction detect.
66	MSBS	O	MS protocol bus state.
67	MSCLK	O	MS serial protocol clock.
68	MSDATA0	I/O	MS Data0.
69	MSDATA1	I/O	MS Data1.
70	MSDATA2	I/O	MS Data2.
71	MSDATA3	I/O	MS Data3.
72	VCK		Core Power supply 2.5v
73	GNDK		Core ground
74	VCC30		IO power supply 3.3v
75	SMWPN	I	SMC write protect. External pull up with 47K to SMPWR. (Low true for protect)
76	SMWRN	O	SMC write control enable. ("1": disable, "0": enable)
77	SMALE	O	SMC Address Latch Enable. ("1": enable, "0": disable)
78	SMCLE	O	SMC Command Latch Enable. ("1": enable, "0": disable)
79	SMCDN	I	SMC card detect. ("1": undetected, "0": detected)
80	SMCEN	O	SMC card enable. ("1": disable, "0": enable)
81	SMRDN	O	SMC read control enable. ("1": disable, "0": enable)
82	SMDATA7	I/O	SMC Data7.
83	SMDATA6	I/O	SMC Data6.
84	SMDATA5	I/O	SMC Data5.
85	SMDATA4	I/O	SMC Data4.
86	SMDATA3	I/O	SMC Data3.
87	SMDATA2	I/O	SMC Data2.
88	SMDATA1	I/O	SMC Data1.
89	SMDATA0	I/O	SMC Data0.
90	SMRBN	I	SMC read/busy. External pull up with 470K to 3.3V.
91	TEST1	I	Test pin must be "0"
92	ROMSEL	I	Selection ROM. (ExternalROM:"1", InternalROM:"0")
93	DPROM	I	Dump internal ROM. ("1": enable,"0": default)
94	PWRLED	O	General Purpose Output.
95	TEST2	I	Internal pull up leave on open
96	TEST3	O	Test pin
97	GPON5	O	General Purpose Output
98	GPON4	O	General Purpose Output
99	GPON3	O	General Purpose Output
100	XDCEN	O	xD card enable. ("1": disable, "0": enable)
101	XDCDN	I	xD card detect. ("1": undetected, "0": detected)
102	SDCMD	I/O	SD CMD.
103	SDCLK	O	SD clock.
104	SDDATA3	I/O	SD Data3.
105	SDDATA2	I/O	SD Data2.
106	SDDATA1	I/O	SD Data1.

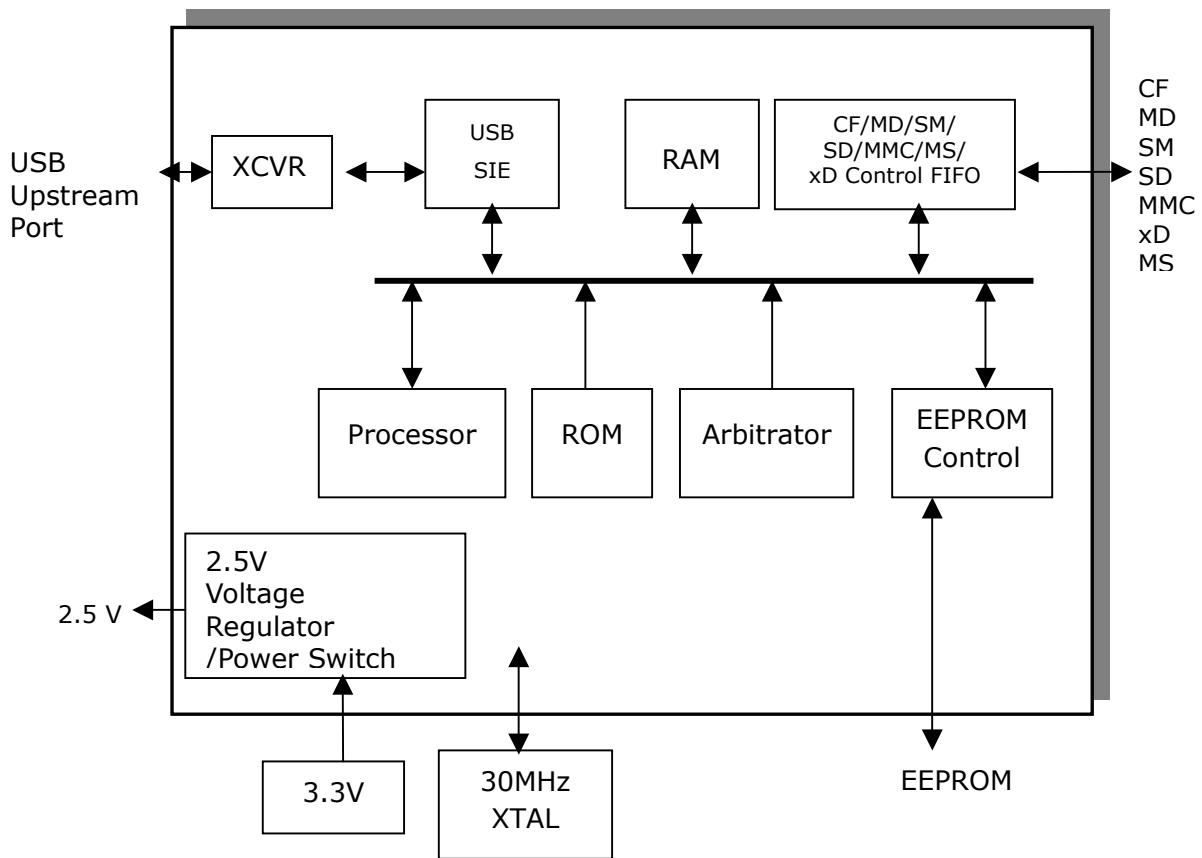


107	SDDATA0	I/O	SD Data0.
108	SDCDN	I	SD card detect. ("1": undetected, "0": detected)
109	SDWP	I	SD write protect. ("1": protected, "0": unprotected)
110	TEST4		Test pin must be "0"
111	TEST5		Test pin must be "0"
112	RFU	I	Reserved for future use
113	XDFMWP	I	xD/Flash memory write protect. ('0':default, "1": protected, "0": unprotected)
114	FMEN	I	Flash memory enable. (Default:'0'; "1": disable, "0": enable)
115	LEDCTL	I	Led mode. Have to pull down
116	FWSEL	I	Firmware mode. (Default:'0'; normal mode:'0', test mode:'1')
117	RFU	I	Reserved for future use
118	GPI1	I	(GPI0, GPI1)=(VIDPID1, VIDPID0)
119	GPI0	I	operation mode: (0,0): reserved (0,1): 4.5 slot mode (1,0): 2 slot mode (1,1): reserved
120	VCC_U20	PWR	USB power supply 3.3V
121	GND_U20	PWR	USB 2.0 Ground
122	XSCI	I	30 MHz crystal input.
123	XSCO	O	30 MHz crystal output.
124	VCC30_U20	PWR	Analog supply voltage for HS receiver (3.3V)
125	GND_U20	PWR	Usb ground.
126	RREF	I	Connects external reference resistor (12.1k $\Omega$ $\pm$ 1%) to analog GND.
127	DM	I/O	USB2.0 data in data negative pin terminal
128	DP	I/O	USB2.0 data in data positive pin terminal

# 4.0 System Architecture and Reference Design

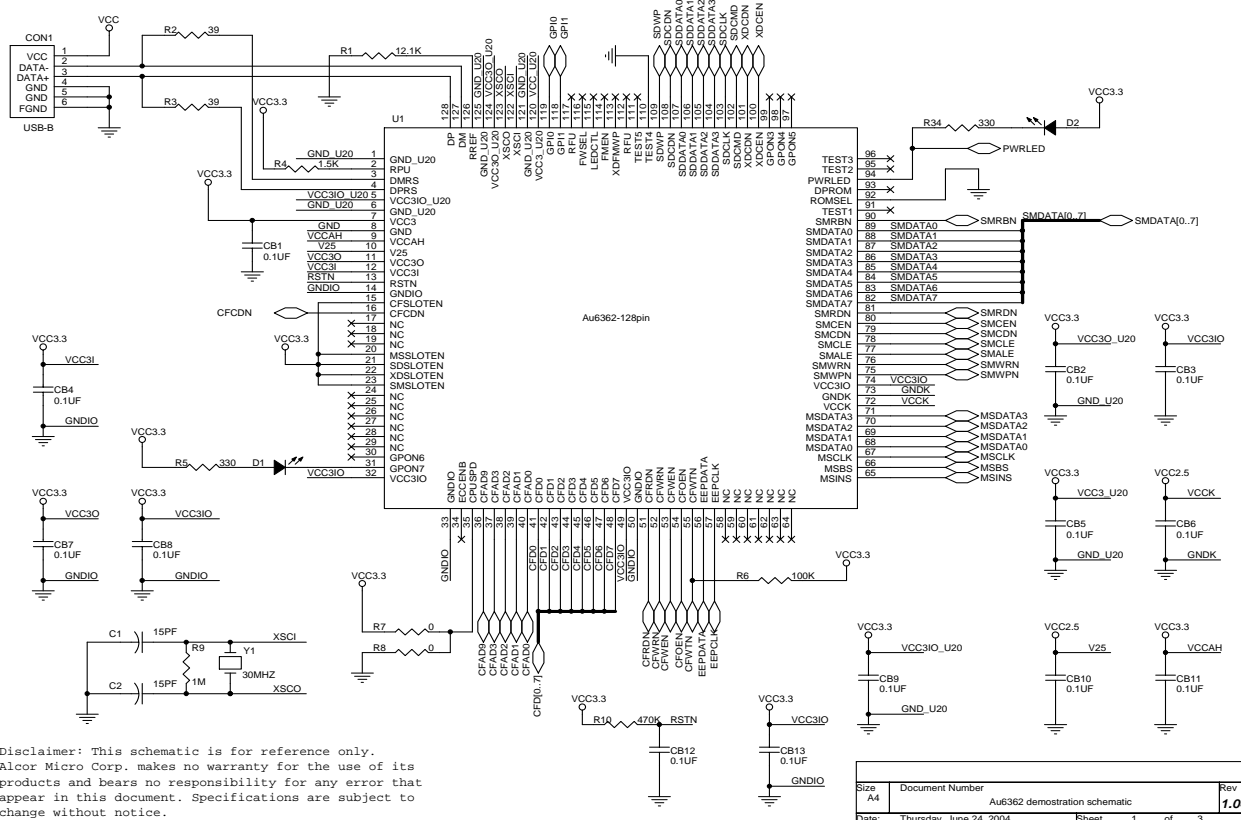
## 4.1 AU6362 Block Diagram

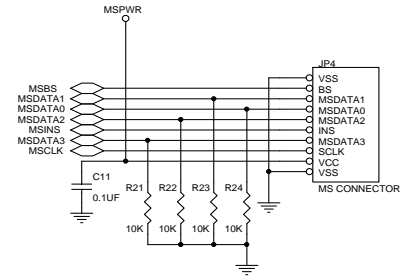
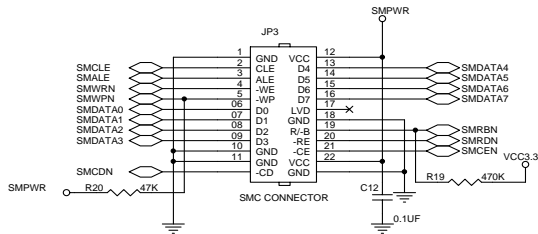
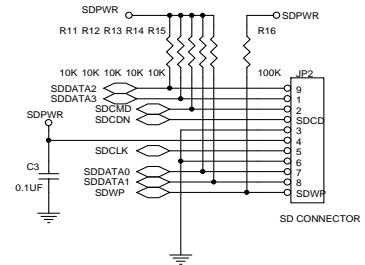
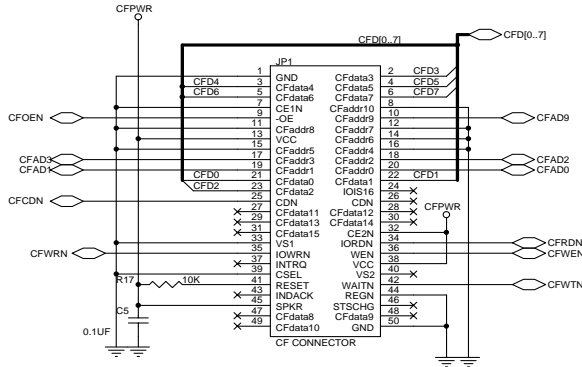
Figure 4.1 AU6362 Block Diagram





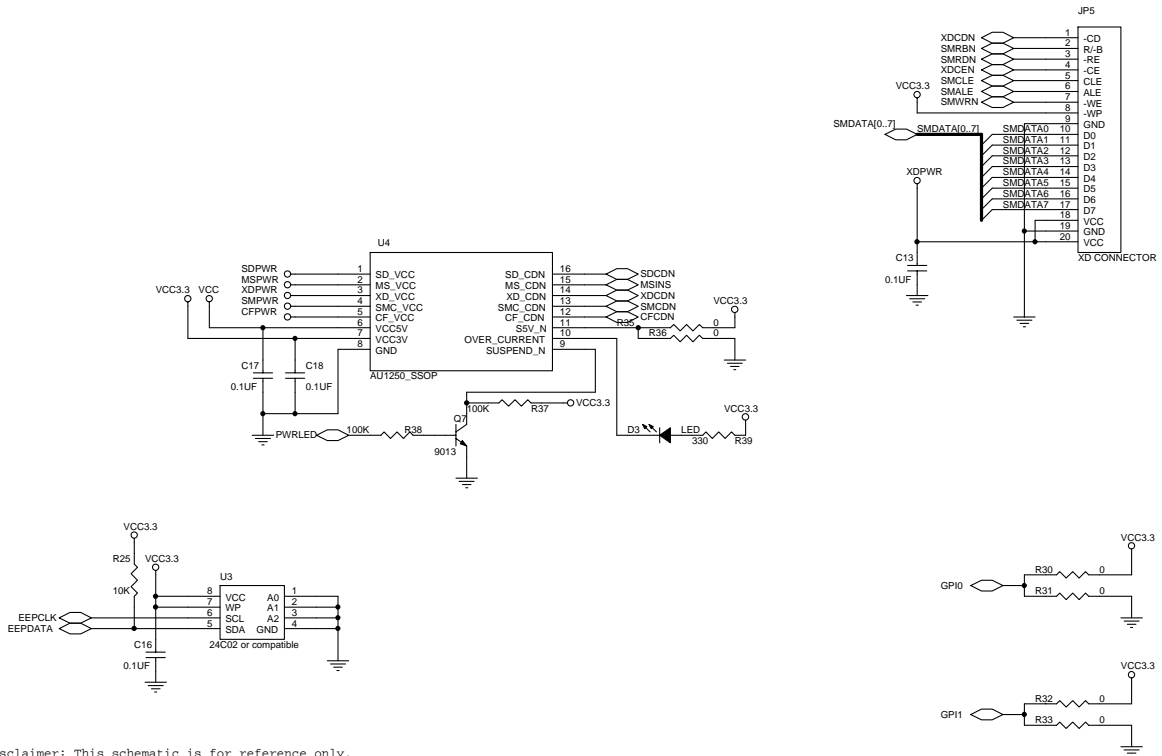
### 4.2. Sample Schematics





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Size A4	Document Number Au6362 demonstration schematics	Rev 1.04
Date: Thursday, June 24, 2004	Sheet 2	of 3



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Size	Document Number	Rev
A4	Au6362 demonstration schematics	1.04
Date:	Thursday, June 24, 2004	Sheet 3 of 3



## 5.0 Electrical Characteristics

### 5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V <sub>CC</sub>	Power Supply	-0.3 to V <sub>CC</sub> +0.3	V
V <sub>IN</sub>	Input Voltage	-0.3 to 3.3	V
V <sub>OUT</sub>	Output Voltage	-0.3 to V <sub>CC</sub> +0.3	V
T <sub>STG</sub>	Storage Temperature	-40 to 150	°C

### 5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V <sub>CC</sub>	Power Supply	3.0	3.3	3.6	V
V <sub>IN</sub>	Input Voltage	0	3.3	5.2	V
T <sub>OPR</sub>	Operating Temperature	-40		115	°C

### 5.3 Leakage Current and Capacitance

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I <sub>IN</sub>	Input current	no pull-up or pull-down	-10	±1	10	μA
I <sub>OZ</sub>	Tri-state leakage current		-10	±1	10	μA
C <sub>IN</sub>	Input capacitance	Pad Limit		2.8		ρF
C <sub>OUT</sub>	Output capacitance	Pad Limit		2.8		ρF
C <sub>BID</sub>	Bi-directional buffer capacitance	Pad Limit		2.8		ρF





## 5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V <sub>CC</sub>	Power supply	3.3V I/O	3.0	3.3	3.6	V
V <sub>il</sub>	Input low voltage	LVTTTL			0.8	V
V <sub>ih</sub>	Input high voltage		2.0			V
V <sub>ol</sub>	Output low voltage	I <sub>ol</sub>   = 2~16mA			0.4	V
V <sub>oh</sub>	Output high voltage	I <sub>oh</sub>   = 2~16mA	2.4			V
R <sub>pu</sub>	Input pull-up resistance	PU=high, PD=low	40	75	190	KΩ
R <sub>pd</sub>	Input pull-down resistance	PU=low, PD=high	40	75	190	KΩ
I <sub>in</sub>	Input leakage current	V <sub>in</sub> = V <sub>CC</sub> or 0	-10	±1	10	μA
I <sub>oz</sub>	Tri-state output leakage current		-10	±1	10	μA



### 5.5 USB Transceiver Characteristics

**Table 5.5 Electrical characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AVCC	Analog supply current		3.0	3.3	3.6	V
VCC	Digital supply current		2.25	2.5	2.75	V
I <sub>CC</sub>	Operating supply current	High speed operating at 480 MHz			73	mA
I <sub>CC(susp)</sub>	Suspend supply current	In suspend mode, current with 1.5kΩ pull-up resistor on pin RPU disconnected			120	μA

**Table 5.6 Static characteristic : Digital pin**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V <sub>IL</sub>	Low-level input voltage				0.8	V
V <sub>IH</sub>	High-level input voltage		2.0			V
Output levels						
V <sub>OL</sub>	Low-level output voltage				0.2	V
V <sub>OH</sub>	High-level output voltage		VCC-0.2			V



AVCC=3.0V~3.6V ; VCC=2.25V~2.75V ; Temp=0°C~115°C

**Table 5.7 Static characteristic : Analog I/O pins (DP/DM)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver (HS)						
Input Levels ( differential receiver )						
$V_{HSDIFF}$	High speed differential input sensitivity	$ V_{I(DP)} - V_{I(DM)} $ measured at the connection as application circuit	300			mV
$V_{HSCM}$	High speed data signaling common mode voltage range		-50		500	mV
$V_{HSSQ}$	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
$V_{HSDSC}$	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
$V_{HSOI}$	High speed idle level output voltage(differential)		-10		10	mV
$V_{HSOL}$	High speed low level output voltage(differential)		-10		10	mV
$V_{HSOH}$	High speed high level output voltage(differential)		-360		400	mV
$V_{CHIRPJ}$	Chirp-J output voltage (differential)		700		1100	mV
$V_{CHIRPK}$	Chirp-K output voltage (differential)		-900		-500	mV
Resistance						
$R_{DRV}$	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	$\Omega$
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
$V_{TERM}$	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver (FS/LS)						
Input Levels ( differential receiver )						
$V_{DI}$	Differential input sensitivity	$ V_{I(DP)} - V_{I(DM)} $	0.2			V
$V_{CM}$	Differential common mode voltage		0.8		2.5	V



Input Levels (single-ended receivers)						
$V_{SE}$	Single ended receiver threshold		0.8		2.0	V
Output levels						
$V_{OL}$	Low-level output voltage		0		0.3	V
$V_{OH}$	High-level output voltage		2.8		3.6	V

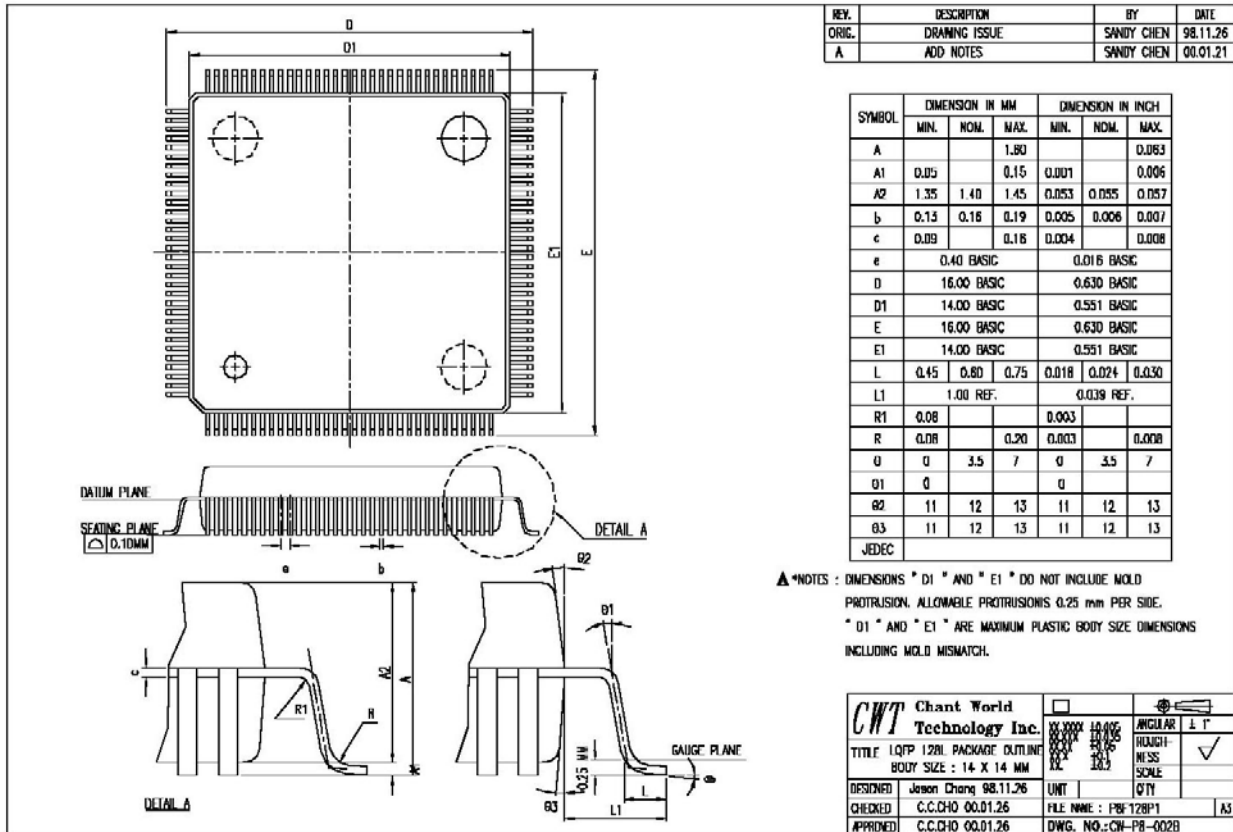
**AVCC=3.0V~3.6V ; VCC=2.25V~2.75V ; Temp=0°C~115°C**

**Table 5.8 Dynamic characteristic : Analog I/O pins (DP/DM)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
$t_{HSR}$	High-speed differential rise time		500			ps
$t_{HSF}$	High-speed differential fall time		500			ps
Full-Speed Mode						
$t_{FR}$	Rise time	CL=50pF ; 10 to 90% of $ V_{OH}-V_{OL} $ ;	4		20	ns
$t_{FF}$	Fall time	CL=50pF ; 90 to 10% of $ V_{OH}-V_{OL} $ ;	4		20	ns
$t_{FRMA}$	Differential rise/fall time matching ( $t_{FR} / t_{FF}$ )	Excluding the first transition from idle mode	90		110	%
$V_{CRS}$	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						
$t_{LR}$	Rise time	CL=200pF-600pF ; 10 to 90% of $ V_{OH}-V_{OL} $ ;	75		300	ns
$t_{LF}$	Fall time	CL=200pF-600pF ; 90 to 10% of $ V_{OH}-V_{OL} $ ;	75		300	ns
$t_{LRMA}$	Differential rise/fall time matching ( $t_{LR} / t_{LF}$ )	Excluding the first transition from idle mode	80		125	%
$V_{CRS}$	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
$V_{OH}$	High-level output voltage		2.8		3.6	V

# 6.0 Mechanical Information

Figure 6.1 Mechanical Information Diagram





## 7.0 Abbreviations

This chapter lists and defines terms and abbreviations used throughout this specification.

<b>SIE</b>	Serial Interface Engine
<b>CF</b>	Compact Flash
<b>MD</b>	Micro Drive
<b>SMC</b>	SmartMedia Card
<b>MS</b>	Memory Stick
<b>SD</b>	Secure Digital
<b>MMC</b>	Multimedia Card
<b>UTMI</b>	USB Transceiver Macrocell Interface



**【MEMO】**

### **About Alcor Micro, Corp**

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