

Phase Control Thyristor



DS5830-4 August 2014 (LN31837)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V _{DRM} and V _{RRM} V	Conditions
DCR690G52* DCR690G50 DCR690G48	5200 5000 4800	$\begin{split} T_{vj} &= \text{-}40 ^{\circ}\text{C to 125} ^{\circ}\text{C}, \\ I_{DRM} &= I_{RRM} = 100 \text{mA}, \\ V_{DRM}, V_{RRM} t_p &= 10 \text{ms}, \\ V_{DSM} \& V_{RSM} &= \\ V_{DRM} \& V_{RRM} + 100 V \\ respectively \end{split}$

Lower voltage grades available. * 5000V @ -40^o C, 5200V @ 0^o C

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR690G52

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

V_{DRM}	5200V
$I_{T(AV)}$	690A
I _{TSM}	9450A
dV/dt*	1500V/µs
dI/dt	300A/us

* Higher dV/dt selections available

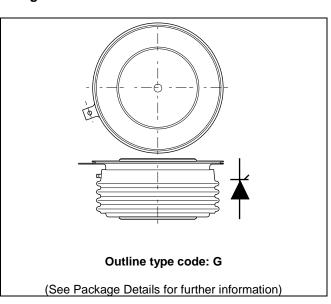


Fig. 1 Package outline



CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Si	de Cooled			
I _{T(AV)}	Mean on-state current	Half wave resistive load	690	А
I _{T(RMS)}	RMS value	-	1084	А
I _T	Continuous (direct) on-state current	-	1050	А

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I _{TSM}	Surge (non-repetitive) on-state current 10ms half sine, T _{case} = 125°C		9.45	kA
l ² t	I ² t for fusing	$V_R = 0$	0.45	MA ² s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
R _{th(j-c)}	Thermal resistance – junction to case	Double side cooled	DC	-	0.0268	°C/W
		Single side cooled	Anode DC	-	0.0527	°C/W
			Cathode DC	-	0.0652	°C/W
R _{th(c-h)}	Thermal resistance – case to heatsink	Clamping force 11.5kN	Double side	-	0.0072	°C/W
		(with mounting compound)	Single side	-	.0144	°C/W
T _{vj}	Virtual junction temperature	Blocking V _{DRM} / _{VRRM}		-	125	°C
T _{stg}	Storage temperature range			-55	125	°C
F _m	Clamping force			10	13	kN





DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I _{RRM} /I _{DRM}	Peak reverse and off-state current	At V _{RRM} /V _{DRM} , T _{case} = 125°C		-	100	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V _{DRM} , T _j = 125°C, ga	ate open	-	1500	V/µs
dl/dt	Rate of rise of on-state current	From 67% V _{DRM} to 2x I _{T(AV)}	Repetitive 50Hz	-	150	A/µs
		Gate source 30V, 10Ω,	Non-repetitive	-	300	A/µs
		$t_r < 0.5 \mu s, T_j = 125 ^{\circ} C$				
$V_{T(TO)}$	Threshold voltage – Low level	100A to 380A at T _{case} = 125°	C	-	.9	V
	Threshold voltage – High level	380A to 3000A at T _{case} = 125°C		-	1.075	V
r _T	On-state slope resistance – Low level	100A to 380A at T _{case} = 125°C		-	1.618	mΩ
	On-state slope resistance – High level	380A to 3000A at T _{case} = 125°C		-	1.125	mΩ
t _{gd}	Delay time	$V_D = 67\% V_{DRM}$, gate source 30V, 10Ω		-	3	μs
		$t_r = 0.5 \mu s, T_j = 25^{\circ}C$				
tq	Turn-off time	$T_j = 125^{\circ}C$, $V_R = 200V$, $dI/dt = 5A/\mu s$,		400	800	μs
		dV _{DR} /dt = 20V/µs linear				
Qs	Stored charge	$I_T = 2000A$, $T_j = 125$ °C, $dI/dt = 5A/\mu s$,		1200	2400	μC
lι	Latching current	$T_{j} = 25^{\circ}C, V_{D} = 5V$		-	3	А
I _H	Holding current	$T_j = 25$ °C, $R_{G-K} = \infty$, $I_{TM} = 500$ A, $I_T = 5$ A		-	300	mA



GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V _{DRM} = 5V, T _{case} = 25°C	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% V _{DRM} , T _{case} = 125°C	0.4	V
I _{GT}	Gate trigger current	$V_{DRM} = 5V$, $T_{case} = 25$ °C	350	mA
I _{GD}	Gate non-trigger current	At 50% V _{DRM} , T _{case} = 125°C	10	mA

CURVES

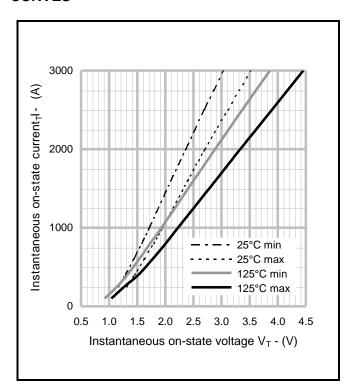
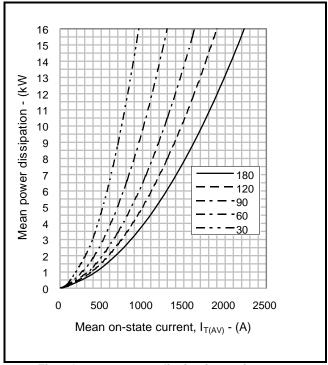


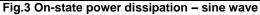
Fig.2 Maximum & minimum on-state characteristics

 $\begin{array}{lll} \textbf{V}_{\text{TM}} \; \textbf{EQUATION} & \text{Where} & A = 0.246536 \\ B = 0.166331 \\ V_{\text{TM}} = A + B \text{In} \; (I_{\text{T}}) + C.I_{\text{T}} + D. \sqrt{I_{\text{T}}} & C = 0.001110 \\ D = -0.008349 \end{array}$

these values are valid for $T_j = 125$ °C for $I_T 50A$ to 3000A







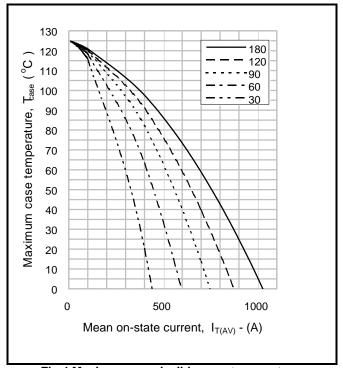


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

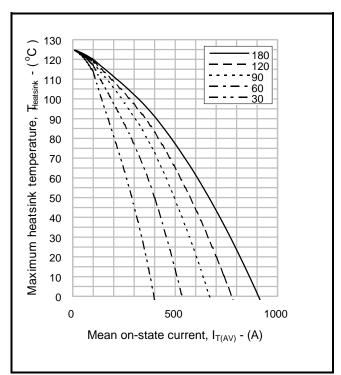


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

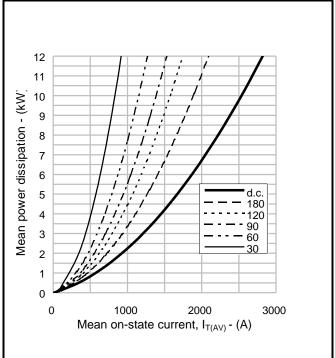


Fig.6 On-state power dissipation - rectangular wave



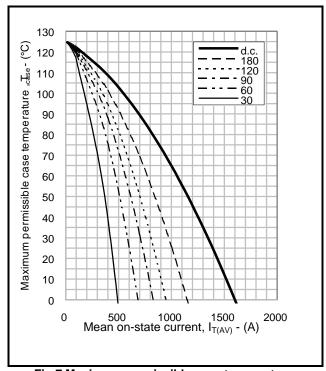


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

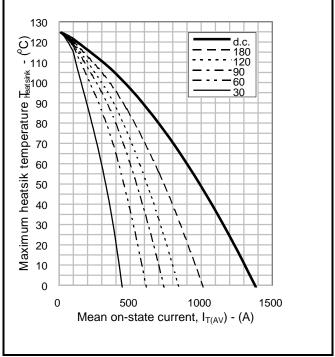


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave

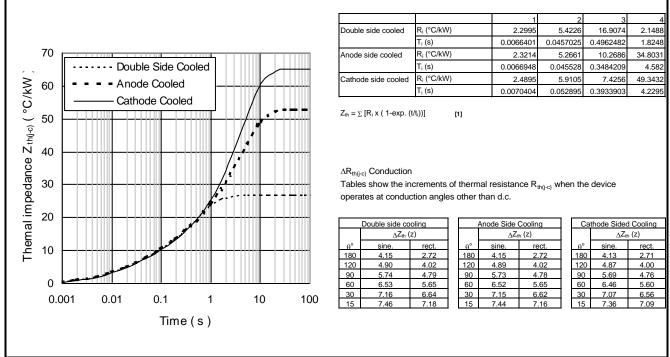
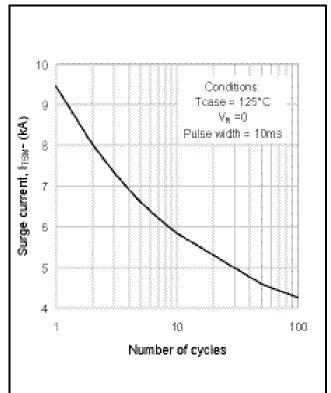


Fig.9 Maximum (limit) transient thermal impedance - junction to case (°C/kW)





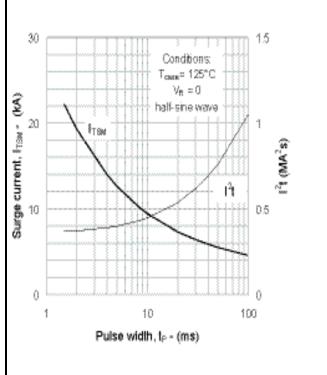
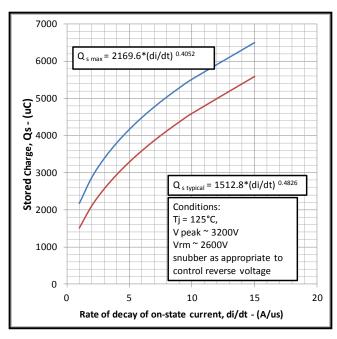
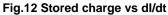


Fig.10 Multi-cycle surge current

Fig.11 Single-cycle surge current





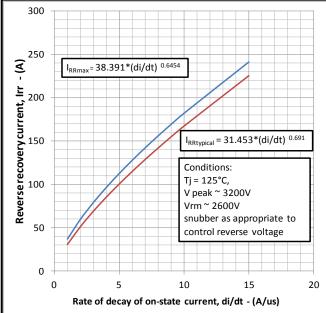


Fig.13 Reverse recovery current vs dl/dt

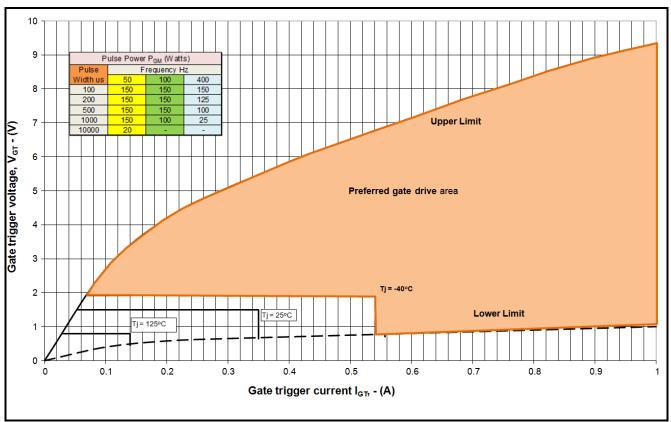


Fig14 Gate Characteristics

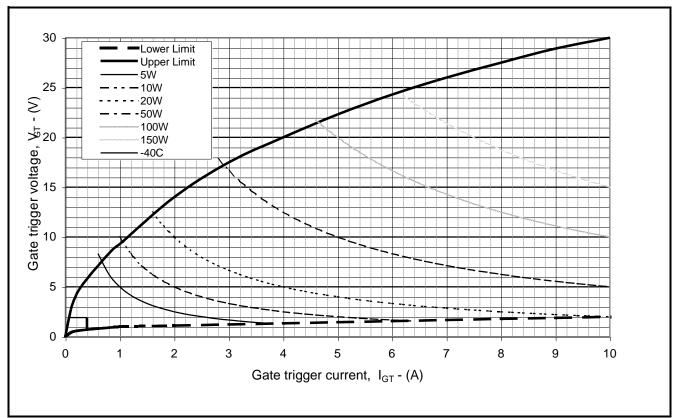


Fig. 15 Gate characteristics



PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

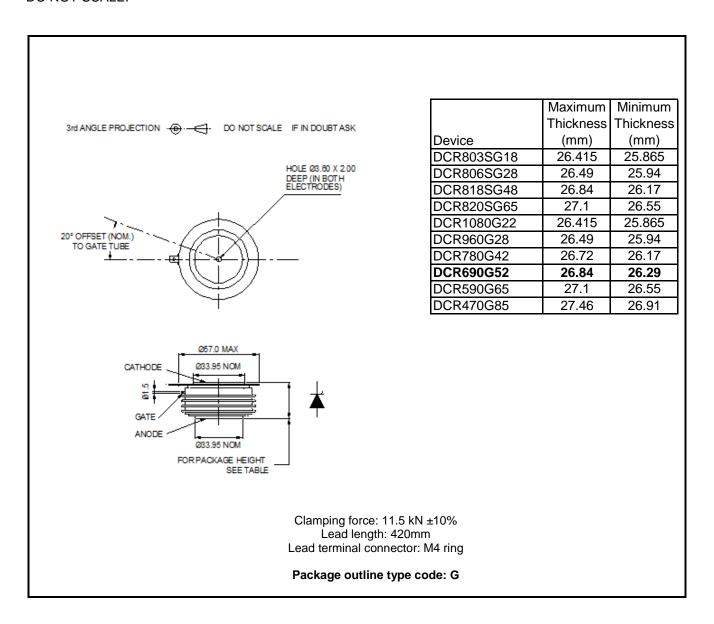


Fig.16 Package outline





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