

FEATURES

- **V_{CC} Current (Commercial/Industrial)**
 - Operating: 70mA/85mA
 - CMOS Standby: 100µA/100µA
- **Access Times**
 - 55/70/85
- **Wide Range Power Supply: 2.7V to 3.6V**
- **Easy Memory Expansion Using \overline{CE} and \overline{OE} Inputs**
- **Common Data I/O**
- **Three-State Outputs**
- **Fully TTL Compatible Inputs and Outputs**
- **Advanced CMOS Technology**
- **Automatic Power Down**
- **Packages**
 - 28-Pin 600 mil DIP
 - 28-Pin 330 mil SOP
 - 28-Pin TSOP



DESCRIPTION

The P3C1256L is a 262,144-bit low power CMOS static RAM organized as 32Kx8. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates with a wide range power supply (2.7V to 3.6V).

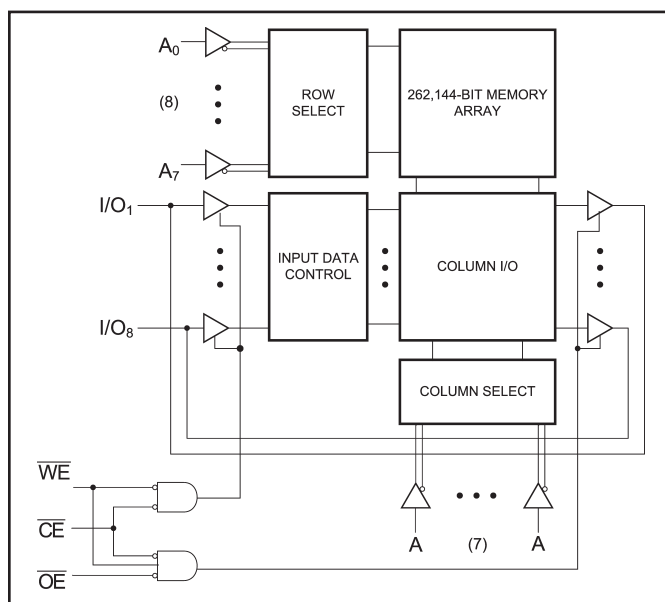
Access times of 55 ns and 70 ns are available. CMOS is utilized to reduce power consumption to a low level.

The P3C1256L device provides asynchronous operation

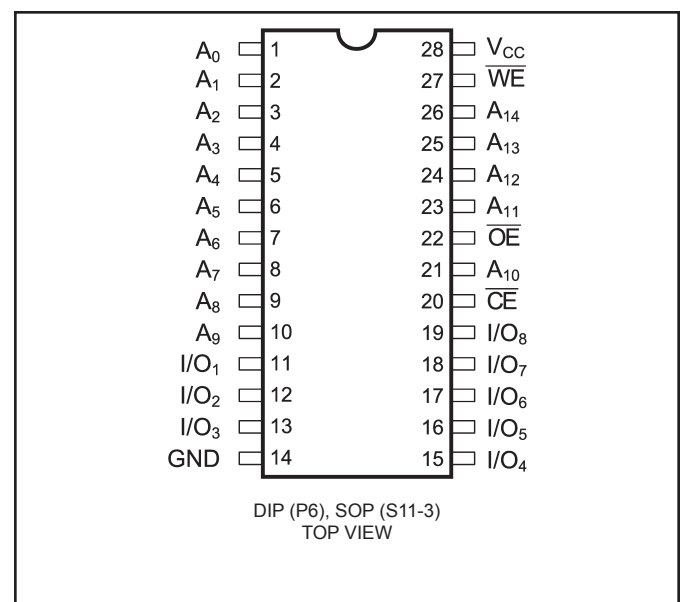
with matching access and cycle times. Memory locations are specified on address pins A_0 to A_{14} . Reading is accomplished by device selection (\overline{CE} and output enabling (\overline{OE}) while write enable (\overline{WE}) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either \overline{CE} or \overline{OE} is HIGH or \overline{WE} is LOW.



FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS





RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Temperature Range (Ambient) | Supply Voltage |
|-----------------------------|------------------------------|
| Commercial (0°C to 70°C) | $2.7V \leq V_{CC} \leq 3.6V$ |
| Industrial (-40°C to 85°C) | $2.7V \leq V_{CC} \leq 3.6V$ |
| Military (-55°C to 125°C) | $2.7V \leq V_{CC} \leq 3.6V$ |

MAXIMUM RATINGS⁽¹⁾

| Sym | Parameter | Min | Max | Unit |
|------------|---|-------|----------------|------|
| V_{CC} | Supply Voltage with Respect to GND | -0.5 | 7.0 | V |
| V_{TERM} | Terminal Voltage with Respect to GND (up to 7.0V) | -0.5 | $V_{CC} + 0.5$ | V |
| T_A | Operating Ambient Temperature | -55 | 125 | °C |
| S_{TG} | Storage Temperature | -65 | 150 | °C |
| I_{OUT} | Output Current into Low Outputs | | 25 | mA |
| I_{LAT} | Latch-up Current | > 200 | | mA |

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)⁽²⁾

| Sym | Parameter | Test Conditions | Min | Max | Unit | |
|-----------|---|---|---------------------|----------------|---------|---------|
| V_{OH} | Output High Voltage ($I/O_0 - I/O_7$) | $I_{OH} = -1mA, V_{CC} = 3.0V$ | 2.4 | | V | |
| V_{OL} | Output Low Voltage ($I/O_0 - I/O_7$) | $I_{OL} = 2.1mA$ | | 0.4 | V | |
| V_{IH} | Input High Voltage | | 2.2 | $V_{CC} + 0.3$ | V | |
| V_{IL} | Input Low Voltage | | -0.5 ⁽³⁾ | 0.8 | V | |
| I_{LI} | Input Leakage Current | $GND \leq V_{IN} \leq V_{CC}$ | Com | -2 | +2 | μA |
| | | | Ind | -5 | +5 | |
| | | | Mil | | | |
| I_{LO} | Output Leakage Current | $GND \leq V_{OUT} \leq V_{CC}$ $\overline{CE} = V_{IH}$ | Com | -2 | +2 | μA |
| | | | Ind | -5 | +5 | |
| | | | Mil | | | |
| I_{SB} | V_{CC} Current TTL Standby Current (TTL Input Levels) | $V_{CC} = 3.6V, I_{OUT} = 0 mA$ $\overline{CE} = V_{IH}$ | | 3 | mA | |
| I_{SB1} | V_{CC} Current CMOS Standby Current (CMOS Input Levels) | $V_{CC} = 3.6V, I_{OUT} = 0 mA$ $\overline{CE} \geq V_{CC} - 0.2V$ | | 100 | μA | |

N/A = Not applicable

**CAPACITANCES⁽⁴⁾** $(V_{CC} = 3.3V, T_A = 25^{\circ}C, f = 1.0MHz)$

| Symbol | Parameter | Test Conditions | Max | Unit |
|-----------|--------------------|-----------------|-----|------|
| C_{IN} | Input Capacitance | $V_{IN}=0V$ | 7 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT}=0V$ | 9 | pF |

POWER DISSIPATION CHARACTERISTICS VS. SPEED

| Sym | Parameter | Temperature Range | * | | | ** | | | Unit |
|----------|----------------------------|-------------------|-----|-----|-----|-----|-----|-----|------|
| | | | -55 | -70 | -85 | -55 | -70 | -85 | |
| I_{CC} | Dynamic Operating Current* | Commercial | 70 | 70 | 70 | 15 | 15 | 15 | mA |
| | | Industrial | 85 | 85 | 85 | 25 | 25 | 25 | mA |
| | | Military | 100 | 100 | 100 | 35 | 35 | 35 | mA |

* Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously enabled for writing, i.e. \overline{CE} and $\overline{WE} \leq V_{IL}(\text{max})$, \overline{OE} is high. Switching inputs are 0V and 3V.

** As above but @ $f=1$ MHz and $V_{IL}/V_{IH} = 0V/V_{CC}$.

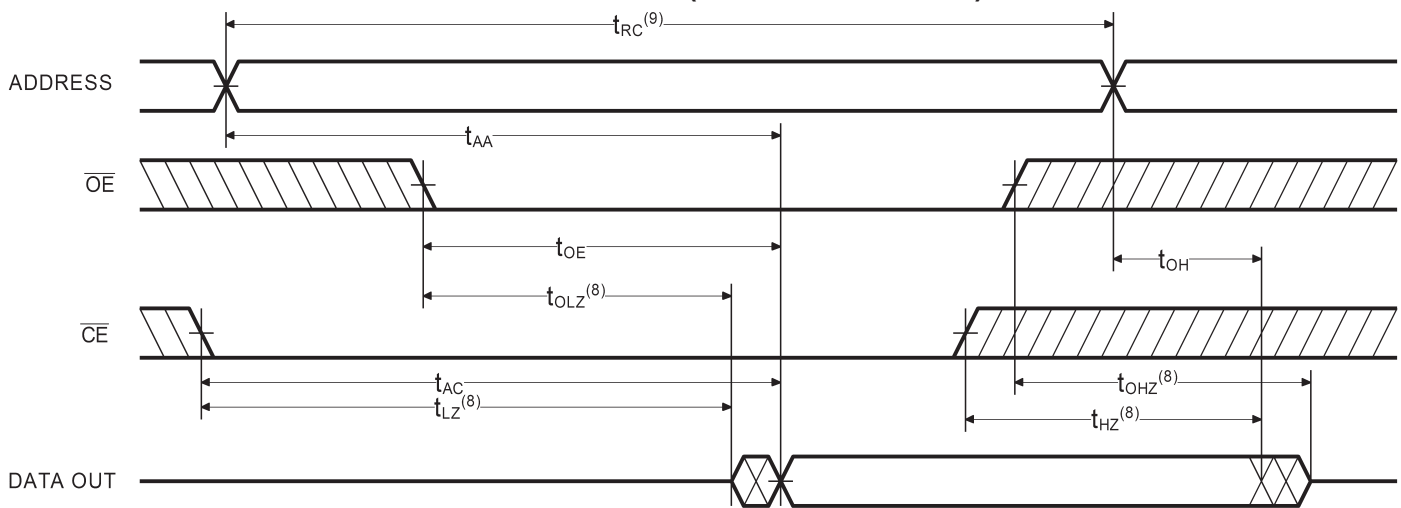
AC ELECTRICAL CHARACTERISTICS—READ CYCLE

(Over Recommended Operating Temperature & Supply Voltage)

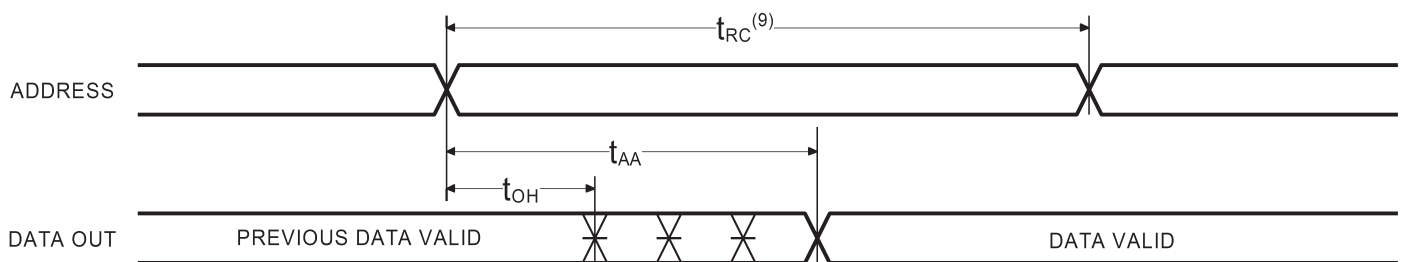
| Sym | Parameter | -55 | | -70 | | -85 | | Unit |
|-----------|----------------------------------|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| t_{RC} | Read Cycle Time | 55 | | 70 | | 85 | | ns |
| t_{AA} | Address Access Time | | 55 | | 70 | | 85 | ns |
| t_{AC} | Chip Enable Access Time | | 55 | | 70 | | 85 | ns |
| t_{OH} | Output Hold from Address Change | 5 | | 5 | | 5 | | ns |
| t_{LZ} | Chip Enable to Output in Low Z | 5 | | 5 | | 5 | | ns |
| t_{HZ} | Chip Disable to Output in High Z | | 20 | | 25 | | 30 | ns |
| t_{OE} | Output Enable Low to Data Valid | | 30 | | 35 | | 40 | ns |
| t_{OLZ} | Output Enable Low to Low Z | 5 | | 5 | | 5 | | ns |
| t_{OHZ} | Output Enable High to High Z | | 20 | | 25 | | 30 | ns |
| t_{PU} | Chip Enable to Power Up Time | 0 | | 0 | | 0 | | ns |
| t_{PD} | Chip Disable to Power Down Time | | 55 | | 70 | | 85 | ns |



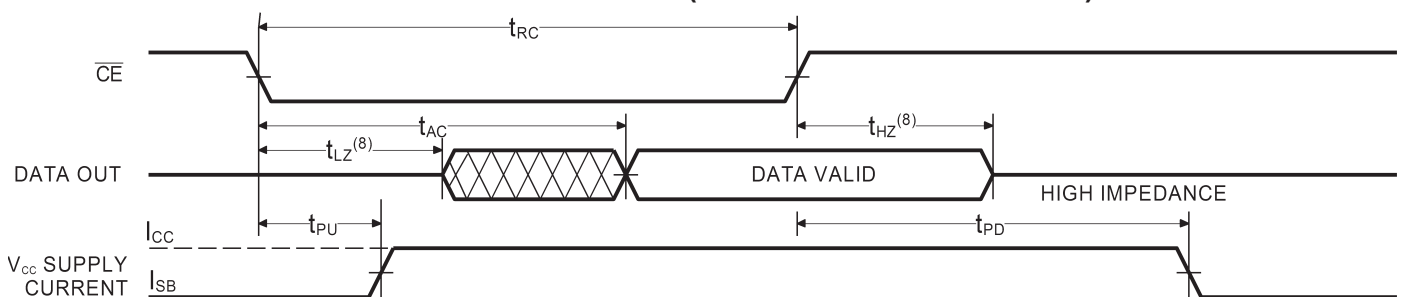
TIMING WAVEFORM OF READ CYCLE NO. 1 (\overline{OE} CONTROLLED)⁽⁵⁾



TIMING WAVEFORM OF READ CYCLE NO. 2 (ADDRESS CONTROLLED)^(5,6)



TIMING WAVEFORM OF READ CYCLE NO. 3 (ADDRESS CONTROLLED)^(5,7)



Notes:

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- Transient inputs with V_{IL} and I_{IL} not more negative than $-3.0V$ and $-100mA$, respectively, are permissible for pulse widths up to 20ns.
- This parameter is sampled and not 100% tested.
- \overline{WE} is HIGH for READ cycle.
- \overline{CE} is LOW and \overline{OE} is LOW for READ cycle.
- ADDRESS must be valid prior to, or coincident with \overline{CE} transition LOW.
- Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
- Read Cycle Time is measured from the last valid address to the first transitioning address.

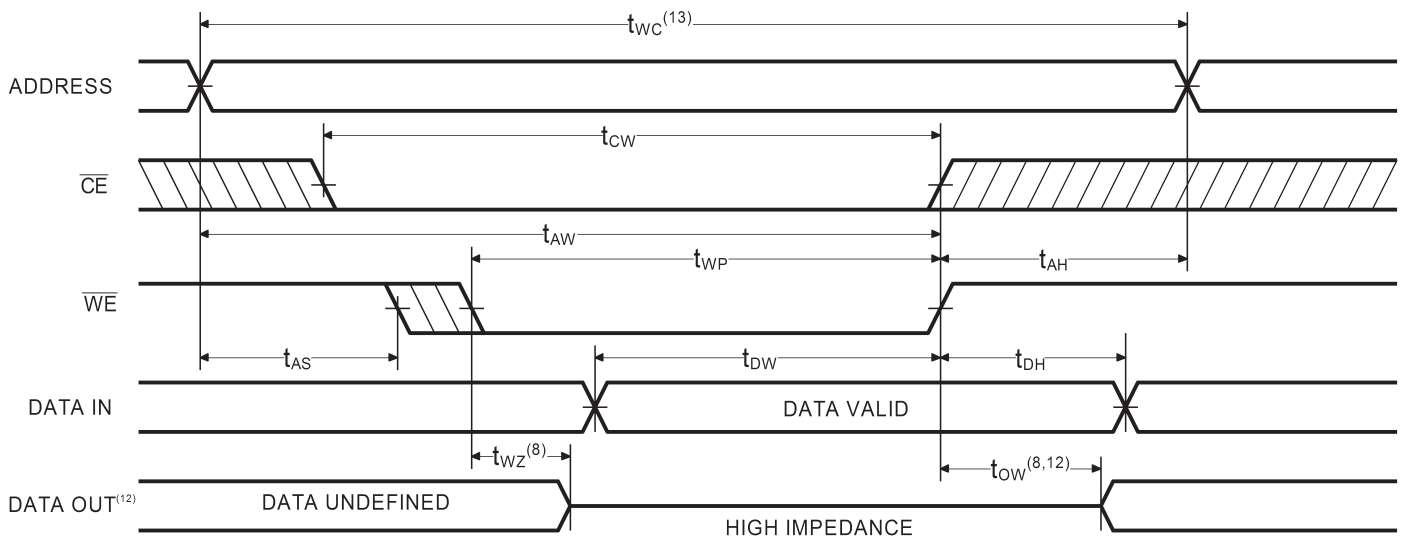


AC CHARACTERISTICS—WRITE CYCLE

(Over Recommended Operating Temperature & Supply Voltage)

| Symbol | Parameter | -55 | | -70 | | -85 | | Unit |
|----------|----------------------------------|-----|-----|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| t_{WC} | Write Cycle Time | 55 | | 70 | | 85 | | ns |
| t_{CW} | Chip Enable Time to End of Write | 50 | | 60 | | 75 | | ns |
| t_{AW} | Address Valid to End of Write | 50 | | 60 | | 75 | | ns |
| t_{AS} | Address Setup Time | 0 | | 0 | | 0 | | ns |
| t_{WP} | Write Pulse Width | 40 | | 50 | | 60 | | ns |
| t_{AH} | Address Hold Time | 0 | | 0 | | 0 | | ns |
| t_{DW} | Data Valid to End of Write | 25 | | 30 | | 35 | | ns |
| t_{DH} | Data Hold Time | 0 | | 0 | | 0 | | ns |
| t_{WZ} | Write Enable to Output in High Z | | 25 | | 30 | | 35 | ns |
| t_{OW} | Output Active from End of Write | 5 | | 5 | | 5 | | ns |

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED)^(10,11)



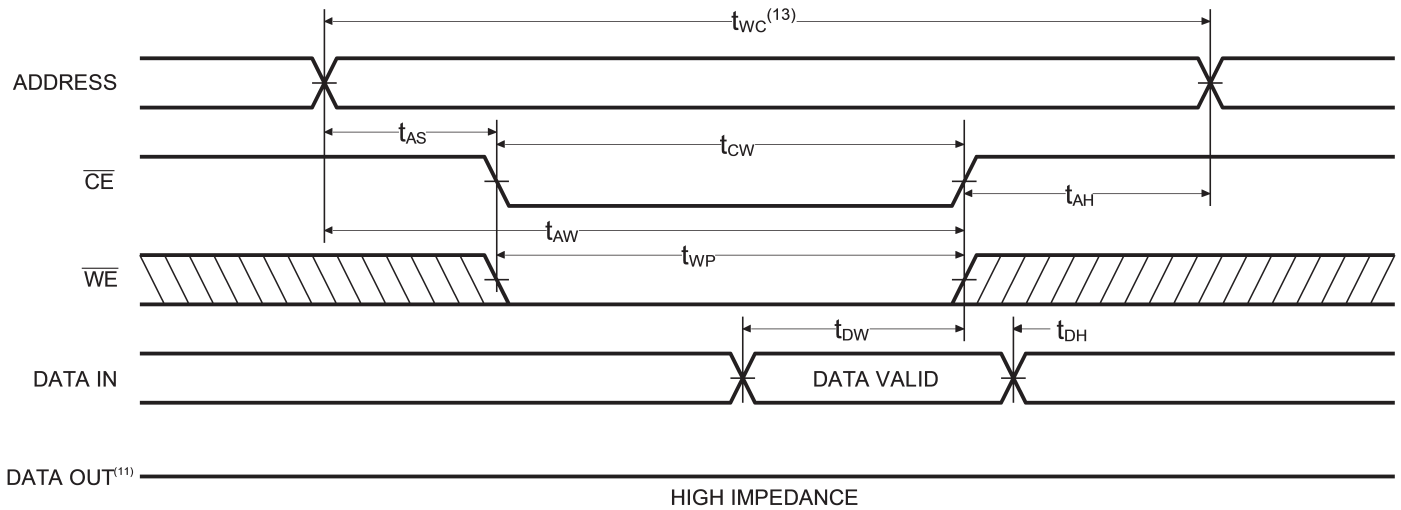
Notes:

10. \overline{CE} and \overline{WE} must be LOW for WRITE cycle.
11. \overline{OE} is LOW for this WRITE cycle to show t_{WZ} and t_{OW} .
12. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high impedance state.

13. Write Cycle Time is measured from the last valid address to the first transitioning address.



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CE} CONTROLLED)⁽¹⁰⁾



AC TEST CONDITIONS

| | |
|-------------------------------|---------------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Times | 3ns |
| Input Timing Reference Level | 1.5V |
| Output Timing Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

TRUTH TABLE

| Mode | \overline{CE} | \overline{OE} | \overline{WE} | I/O | Power |
|--------------------|-----------------|-----------------|-----------------|-----------|---------|
| Standby | H | X | X | High Z | Standby |
| Standby | X | X | X | High Z | Standby |
| D_{OUT} Disabled | L | H | H | High Z | Active |
| Read | L | L | H | D_{OUT} | Active |
| Write | L | X | L | High Z | Active |

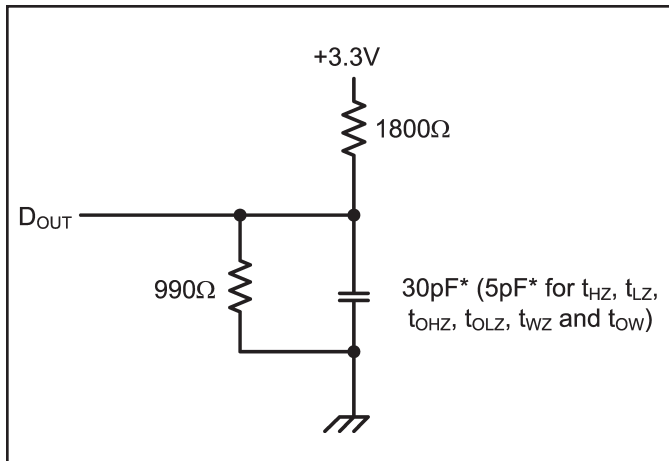


Figure 1. Output Load

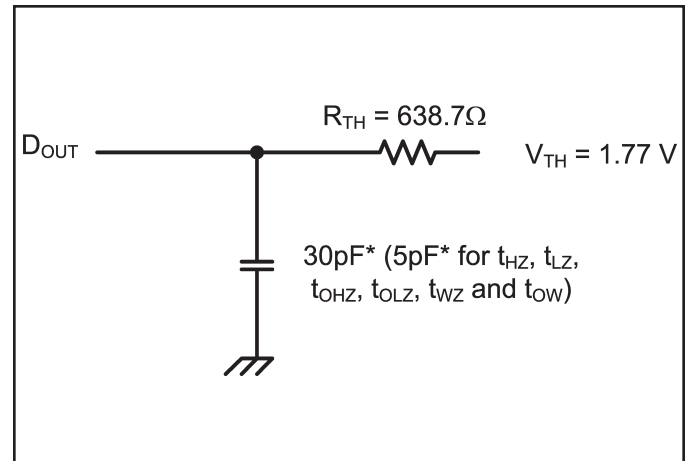


Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:

Because of the high speed of the P3C1256L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 μ F high frequency capacitor

is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50 Ω test environment should be terminated into a 50 Ω load with 1.77V (Thevenin Voltage) at the comparator input, and a 589 Ω resistor must be used in series with D_{OUT} to match 639 Ω (Thevenin Resistance).



DATA RETENTION CHARACTERISTICS

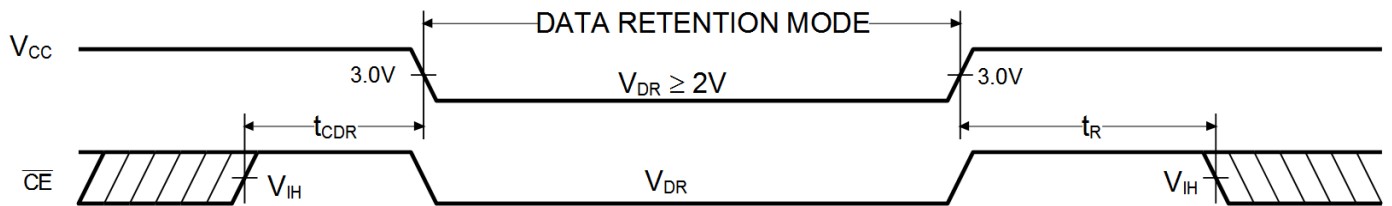
| Sym | Parameter | Test Conditions | Min | Typ.* $V_{CC} =$ | | Max $V_{CC} =$ | | Unit |
|---------------|--------------------------------------|---|-------------|---------------------|------|-------------------|------|---------|
| | | | | 2.0V | 3.0V | 2.0V | 3.0V | |
| V_{DR} | V_{CC} for Data Retention | | 2.0 | | | | | V |
| I_{CCDR} | Data Retention Current | $\overline{CE} \geq V_{CC} - 0.2V,$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | | 10 | 15 | 80 | 120 | μA |
| t_{CDR} | Chip Deselect to Data Retention Time | | 0 | | | | | ns |
| t_R^\dagger | Operation Recovery Time | | t_{RC}^\S | | | | | ns |

* $T_A = +25^\circ C$

t_{RC}^\S = Read Cycle Time

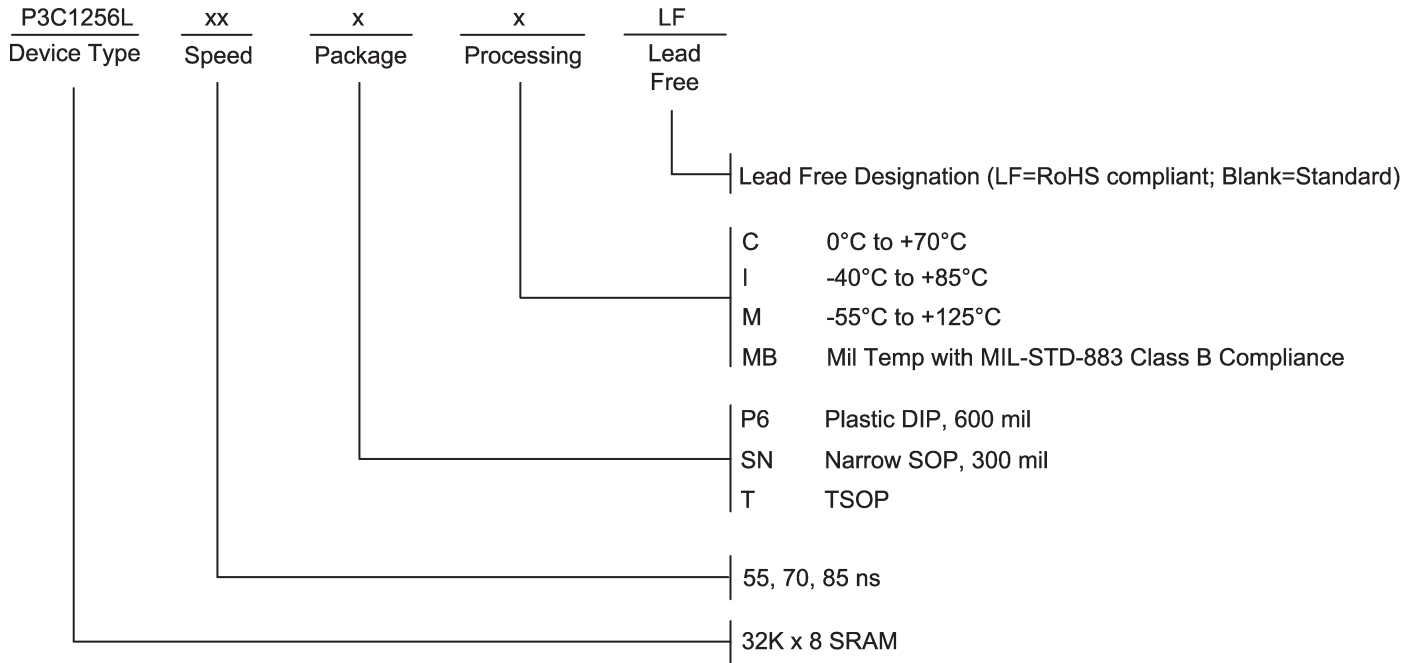
\dagger = This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM





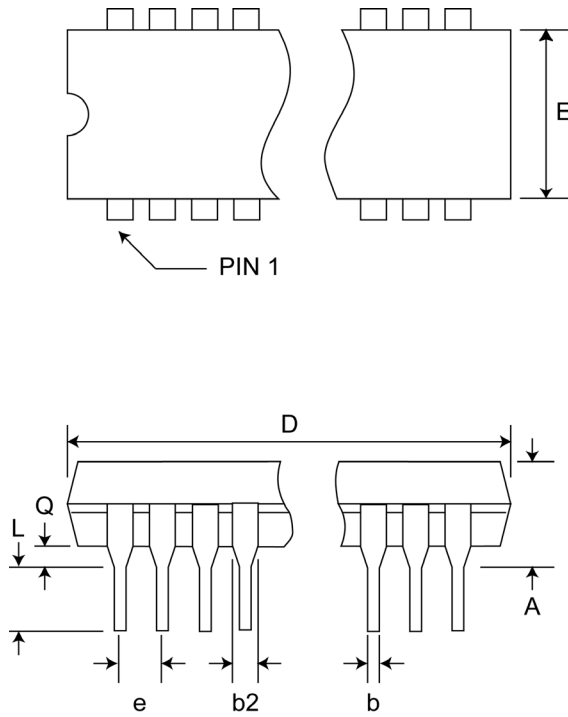
ORDERING INFORMATION





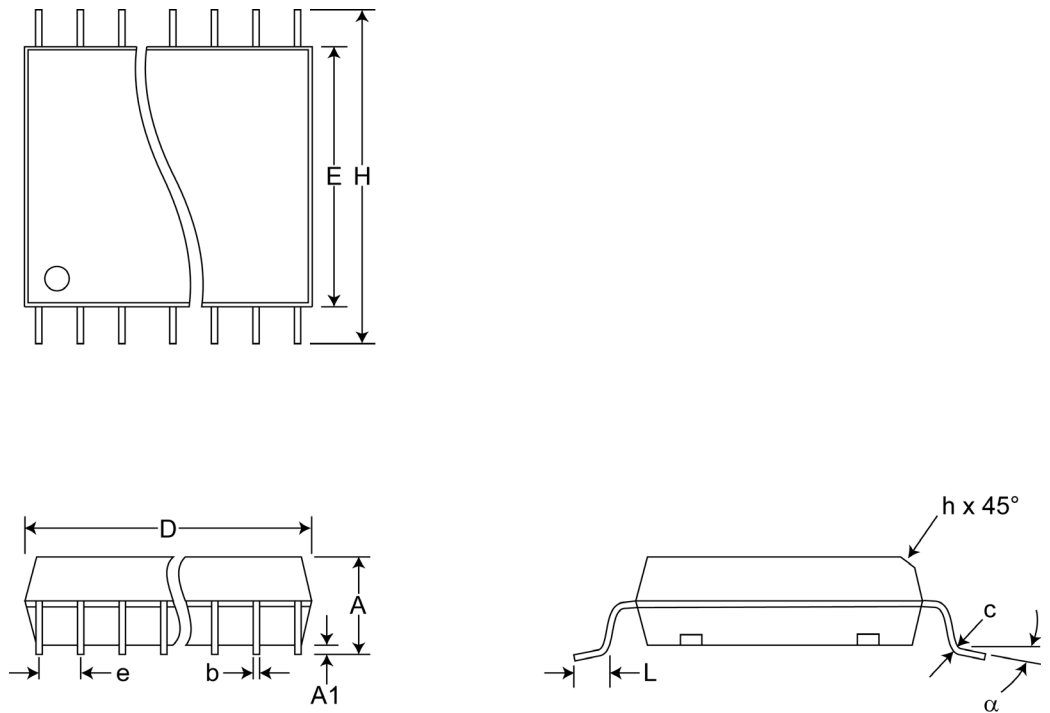
| | | |
|--------|--------------|------------|
| Pkg # | P6 | |
| # Pins | 28 (600 mil) | |
| Symbol | Min | Max |
| A | 0.090 | 0.200 |
| A1 | 0.000 | 0.070 |
| b | 0.014 | 0.020 |
| b2 | 0.015 | 0.065 |
| C | 0.008 | 0.012 |
| D | 1.380 | 1.430 |
| E | 0.485 | 0.550 |
| E1 | 0.600 | 0.625 |
| e | 0.100 BSC | |
| eB | 0.600 TYP | |
| L | 0.100 | 0.180 |
| | 0° | 15° |

PLASTIC DUAL IN-LINE PACKAGE



| | | |
|--------|--------------|------------|
| Pkg # | S11-3 | |
| # Pins | 28 (330 Mil) | |
| Symbol | Min | Max |
| A | 0.094 | 0.120 |
| A1 | 0.002 | 0.014 |
| B | 0.014 | 0.020 |
| C | 0.008 | 0.012 |
| D | 0.702 | 0.728 |
| e | 0.050 BSC | |
| E | 0.291 | 0.340 |
| H | 0.463 | 0.477 |
| h | 0.010 | 0.029 |
| L | 0.020 | 0.050 |
| | 0° | 8° |

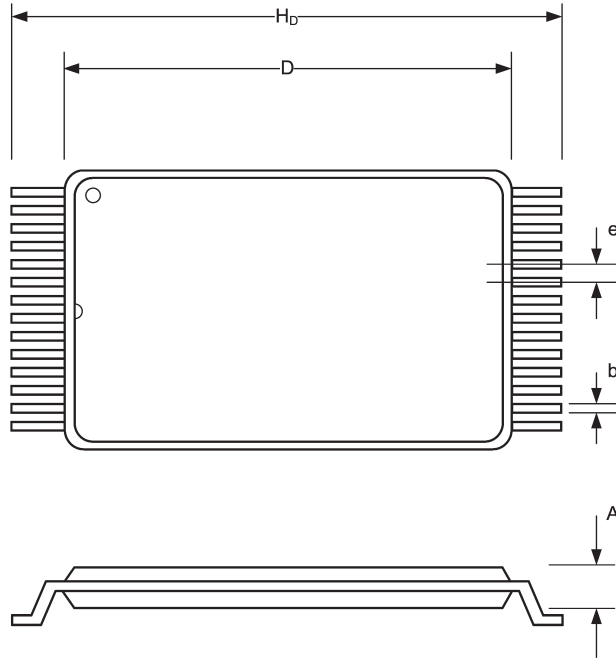
SOIC/SOP SMALL OUTLINE IC PACKAGE





| | | |
|----------------|------------|------------|
| Pkg # | T1 | |
| # Pins | 28 | |
| Symbol | Min | Max |
| A | 0.039 | 0.047 |
| A ₂ | 0.036 | 0.040 |
| b | 0.007 | 0.011 |
| D | 0.461 | 0.469 |
| E | 0.311 | 0.319 |
| e | 0.022 BSC | |
| H _b | 0.520 | 0.535 |

TSOP THIN SMALL OUTLINE PACKAGE



NOTE:
Orientation ID is either next to Pin 1 (midway along row of pins) or in corner on side of package containing Pin 1.

**REVISIONS**

| | |
|------------------------|--|
| DOCUMENT NUMBER | SRAM143 |
| DOCUMENT TITLE | P3C1256L LOW POWER 32K x 8 STATIC CMOS RAM |

| REV | ISSUE DATE | ORIGINATOR | DESCRIPTION OF CHANGE |
|------------|-------------------|-------------------|-------------------------------|
| OR | Jul-2011 | JDB | New Data Sheet |
| A | Oct-2011 | JDB | Added wide range power supply |