Product Description

The KXR94-2353 is a Tri-axis, silicon micromachined accelerometer with a full-scale output range of +/-2g (19.6 m/s/s). The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which further utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit. A separate ASIC device packaged with the sense element provides signal conditioning and self-test. The accelerometer is delivered in a 5 x 5 x 1.2 mm DFN plastic package operating from a 2.5 – 5.25V DC supply.
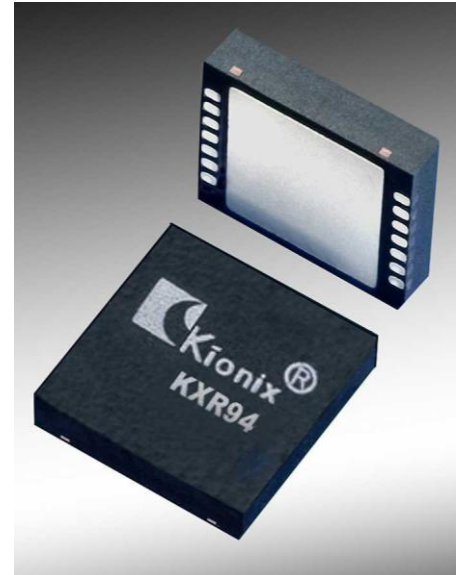
There are 4 factory programmable modes of operation for the KXR94:

Mode 00 – The three outputs (X, Y, Z) are read through the **digital** SPI interface, which is also used to command Selftest and Standby Mode. The digital I/O pads are powered from a separate power pin, and will interface to 1.8V logic.

Mode 01 – The three outputs (X, Y, Z) are provided on three **analog** output pins. The KXR94 also features an integrated **3-channel multiplexer** (X, Y, Z). The Enable pin must be **high** for normal operation and **low** for power shutdown.

Mode 10 – The three outputs (X, Y, Z) are provided on three **analog** output pins. The KXR94 also features an integrated **4-channel multiplexer** (X, Y, Z, Aux In). The Enable pin must be **high** for normal operation and **low** for power shutdown.

Mode 11 – The three outputs (X, Y, Z) are provided on three **analog** output pins. The KXR94 also features an integrated **4-channel multiplexer** (X, Y, Z, Aux In). The Enable pin must be **low** for normal operation and **high** for power shutdown.

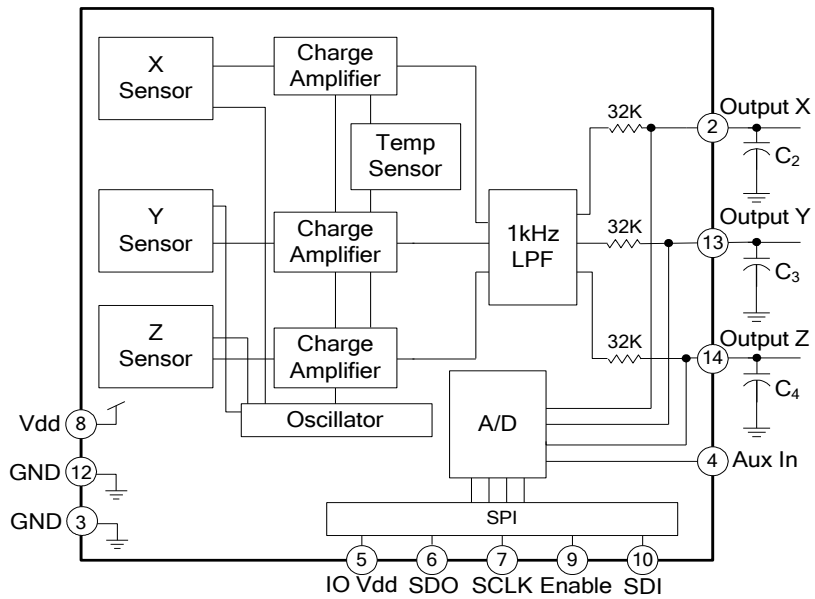The KXR94-2353 is factory programmed to be in MODE 00.

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Functional Diagram

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Product Specifications

Table 1. Mechanical

(specifications are for operation at 3.3V and T = 25C unless stated otherwise)

Parameters	Units		Min	Typical	Max
Operating Temperature Range		ºC	-40	-	85
Zero-g Offset	!	counts	1918	2048	2178
Zero-g Offset Variation from RT over Temp.		mg/ºC		0.2	
Sensitivity	!	counts/g	803	819	835
Sensitivity Variation from RT over Temp.		%/ºC		0.01 (xy) 0.02 (z)	
Offset Ratiometric Error (V_{dd} = 3.3V ± 5%)		mg		4	
Sensitivity Ratiometric Error (V_{dd} = 3.3V ± 5%)		%		1.25 (xy) 0.2 (z)	
Non-Linearity		% of FS		0.1	
Cross Axis Sensitivity[1]		%		2	
Self Test Output change on Activation		g		1.9 (xy) 0.5 (z)	
Bandwidth (-3dB)[2]		Hz		800	
Noise Density (on filter pins)		μg / √Hz		45	

! Denotes Special Characteristics: These characteristics have been identified as important to the customer.

Notes:
1. Cross axis sensitivity is dominated by the placement accuracy of the component during PCB assembly and in the application.
2. Bandwidth for internal low pass filter only. Lower frequencies are user definable with external capacitors. (See Application Design Equations)

Table 2. Electrical

(specifications are for operation at 3.3V and T = 25C unless stated otherwise)

Parameters			Units	Min	Typical	Max
Supply Voltage (V_{dd})	Operating		V	2.5	3.3	5.25
I/O Pads Supply Voltage (VIO)			V	1.7	-	Vdd
Current Consumption	Operating	*!*	μA	500	950	1400
	Standby		μA		-	5
Input Low Voltage			V	-	-	$0.2 * V_{IO}$
Input High Voltage			V	$0.8 * V_{IO}$	-	-
Input Pull-down Current			μA		60	
A/D Conversion time			μs		40	
SPI Communication Rate			MHz			5
Analog Output Resistance(R_{out})			kΩ	24	32	40

! Denotes Special Characteristics: These characteristics have been identified as important to the customer.

Table 3. Environmental

Parameters		Units	Min	Target	Max
Supply Voltage (V_{dd})	Absolute Limits	V	-0.3	-	7.0
Maximum Operating Temperature Range		ºC	-40	-	125
Storage Temperature Range		ºC	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms
ESD	HBM	V	-	-	3000

CAUTION:
ELECTROSTATIC
SENSITIVE COMPO-
NENT

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

RoHS
2002/95/EC

This product conforms to Directive 2002/95/EC of the European Parliament and of the Council of the European Union (RoHS). Specifically, this product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are "of uniform composition throughout."

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± 2g Tri-axis Digital
Accelerometer Specifications

PART NUMBER:

KXR94-2353
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HF — This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Soldering

Soldering recommendations available upon request or from www.kionix.com.

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Application Schematic
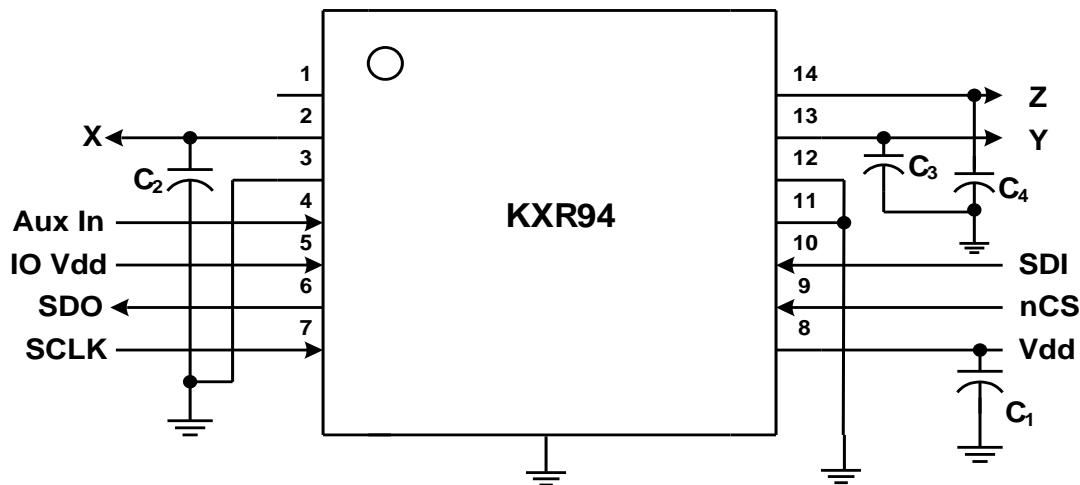
Table 4. KXR94 Pad Descriptions

Pad	Name	Description
1	NC	Not Connected Internally (can be connected to Vdd or Gnd)
2	X output	Analog output of the x-channel. Optionally, a capacitor (C_2) placed between this pin and ground will form a low pass filter.
3	GND	Ground
4	Aux In	Auxiliary input for analog-digital converter
5	IO Vdd	Power Supply for I/O pads
6	SDO	SPI Serial Data Output
7	SCLK	SPI Communication Clock
8	Vdd	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor (C_1).
9	nCS	SPI Chip Select
10	SDI	SPI Serial Data Input
11	NC	Not Connected Internally (can be connected to Vdd or Gnd)
12	GND	Ground
13	Y Output	Analog output of y-channel. Optionally, a capacitor (C_3) placed between this pin and ground will form a low pass filter.
14	Z Output	Analog output of z-channel. Optionally, a capacitor (C_4) placed between this pin and ground will form a low pass filter.
	Center pad	Ground

Application Design Equations

The bandwidth is determined by the internal 1kHz low pass filter. The user can lower the bandwidth by placing filter capacitors connected from pins 2, 13 and 14 to ground. The response is single pole. Given a desired bandwidth, f_{BW}, the filter capacitors are determined by:

$$C_2 = C_3 = C_4 = \frac{4.97 x 10^{-6}}{f_{BW}}$$

KXR94 Digital Interface

The Kionix KXR94 digital accelerometer has the ability to communicate on a SPI digital serial interface bus. This flexibility allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system micro-controllers.

The serial interface terms and descriptions as indicated in Table 6 below will be observed throughout this document.

Table 5. Serial Interface Terminologies

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals and terminates a transfer.
Slave	The device addressed by the Master.

SPI Interface

The KXR94 utilizes an integrated Serial Peripheral Interface (SPI) for digital communication. The SPI interface is primarily used for synchronous serial communication between one Master device and one or more Slave devices. The Master, typically a micro controller, provides the SPI clock signal (SCLK) and determines the state of Chip Select (nCS). The KXR94 always operates as a Slave device during standard Master-Slave SPI operation.

SPI is a 4-wire synchronous serial interface that uses two control and two data lines. With respect to the Master, the Serial Clock output (SCLK), the Data Output (MOSI) and the Data Input (MISO) are shared among the Slave devices. The Master generates an independent Chip Select (nCS) for each Slave device that goes low at the start of transmission and goes back high at the end. The Slave Data Output (SDO) line, remains in a high-impedance (hi-z) state when the device is not selected, so it does not interfere with any active devices. This allows multiple Slave devices to share a master SPI port as shown in Figure 1 below.

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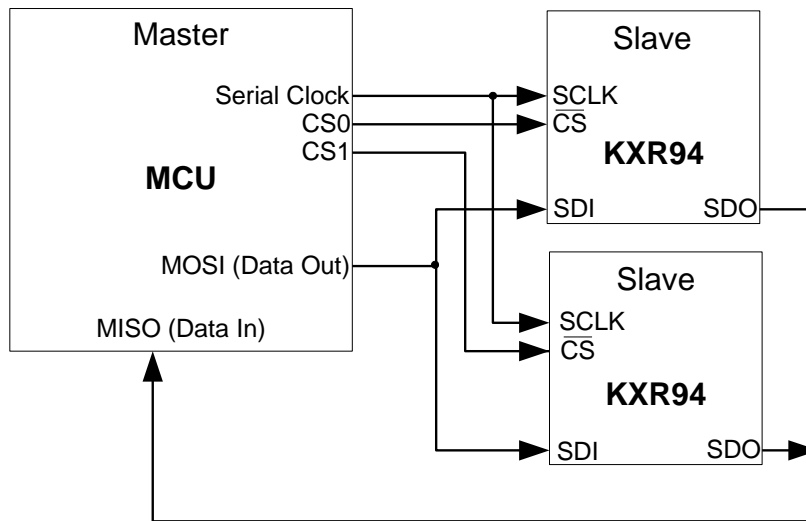352-1783-1011041430
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Figure 1 KXR94 SPI Connections

Control Register Write and Read

The control register embedded in the KXR94 has an 8-bit address. Upon power up, the Master must write to the accelerometer's control register to set its operational mode. On the falling edge of nCS, a 2-byte command is written to the control register. The first byte, 0x04, initiates the write to the appropriate register, and is followed by the user-defined, operational-mode byte. All commands are sent MSB (most significant bit) first, and the host must return nCS high for at least 200nS before the next data request. Figure 2 below shows the timing diagram for carrying out the 8-bit control register write operation.
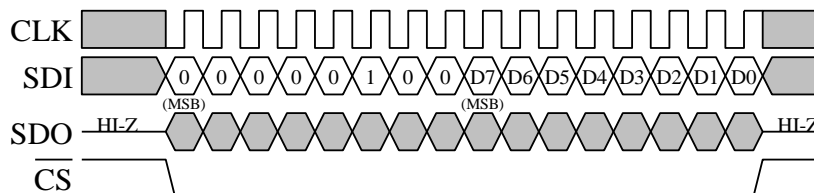

Figure 2 Timing Diagram for 8-Bit Control Register Write Operation

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In order to read the 8-bit control register, an 8-bit read command, 0x03, must be written to the accelerometer to initiate the read. Upon receiving the command, the accelerometer returns the 8-bit operational-mode data stored in the control register. This operation also occurs over 16 clock cycles. All returned data is sent MSB first, and the host must return nCS high for at least 200nS before the next data request. Figure 3 shows the timing diagram for an 8-bit control register read operation.
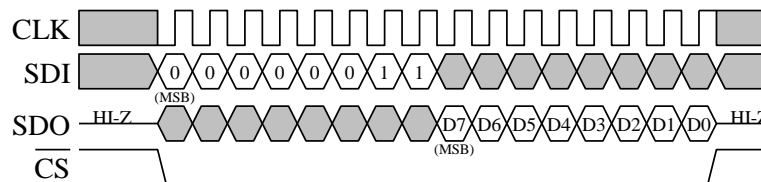

Figure 3 Timing Diagram for 8-Bit Control Register Read Operation

Accelerometer Read Back Operation

The KXR94 has an onboard 12-bit ADC that can sample, convert and read back sensor data at any time. Transmission of an 8-bit axis-conversion command (see Table 8) begins on the falling edge of nCS. After the eight clock cycles used to send the command, the host must wait for at least 40µs during the A/D conversion time. Note that all returned data is sent MSB first. Once the data is received, nCS must be returned high for 200nS before the next data request. Figure 4 and 5 this and on the following page show the timing and register diagrams for the accelerometer 12-bit ADC read operation.

The Read Back Operation is a 3-byte SPI command. The first byte of SDI contains the command to convert one of the axes. The second and third bytes of SDO contain the 12 bits of the A/D result plus four bits of padding in the LSB to make a total of 16 bits. See Figure 5 on next page.
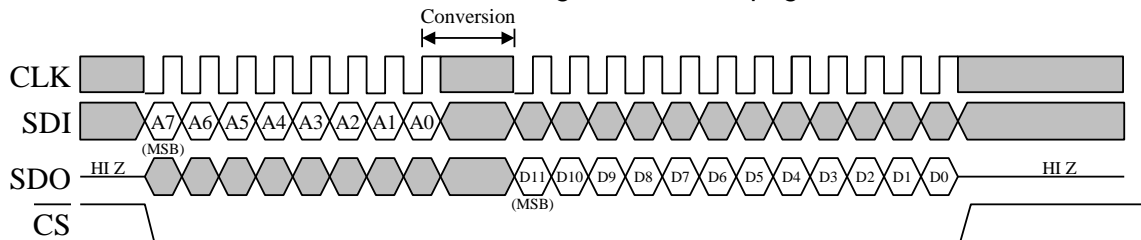

Figure 4 Timing Diagram for an A/D conversion and 12-Bit data read operation.

Axis Conversion Command
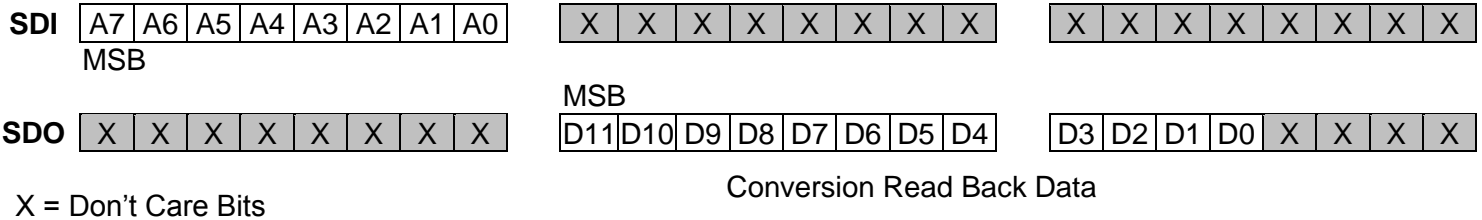

X = Don't Care Bits

Figure 5 Register Diagram for 12-Bit ADC Read Operation

SPI Commands

The accelerometer SPI interface uses an 8-bit command register to carry out all of its functions. The commands are given in Table 7.

Description	1st byte (SDI) (Command)
Convert X axis	0x00
Convert Y axis	0x01
Convert Z axis	0x02
Read Control Register	0x03
Write Control Register	0x04
Convert Aux In	0x07

Table 6 Command Register Bit Utilization

Convert X axis (0x00 or 0000 0000) samples the X-axis sensor data held on the filter cap, digitizes it and returns it as 12-bits through SDO.

Convert Y axis (0x01 or 0000 0001) samples the Y-axis sensor data held on the filter cap, digitizes it and returns it as 12-bits through SDO.

Convert Z axis (0x02 or 0000 0010) samples the Z-axis sensor data held on the filter cap, digitizes it and returns it as 12-bits through SDO.

Read Control Register (0x03 or 0000 0011) reads back the current contents of the control register and returns it as 8-bits through SDO.

Write Control Register (0x04 or 0000 0100) is used to initiate a write to the control register and set the operational mode of the accelerometer. The first byte initiates the write to the register, and the second byte specifies the operational mode.

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Convert Aux In (0x07 or 0000 0111) samples the auxiliary input data, digitizes it and returns it as 12-bits through SDO.

Accelerometer Operational Modes

The 8-bit read/write control register selects the various operational modes of the accelerometer. Table 8 shows the bit assignments for the available modes.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	Enable	Self test	Parity

Table 7 Read/Write Control Register

Parity reports on even (0) or odd (1) EEPROM parity. A properly functioning part will return even (0) EEPROM parity. This bit is read-only and operates independently of the other modes.

Enable powers up the accelerometer for operation.
Enable = 1 – normal operation
Enable = 0 – low-power standby

Self test activates the self-test function for the sensor elements on all three axes. A correctly functioning part will increase all channel outputs by approximately 1g when Self test = 1 and Enable = 1. This bit can be read or written.

Digital Accelerometer SPI Sequence

An example of a SPI sequence for reading sensor data is as follows:
1. Power up KXR94
2. nCS low to select
3. Write operational mode command to 8-bit control register – for example: 0x0404. The first 0x04 is the command to write to the control register, the second 0x04 sets the enable bit in the internal register.
4. nCS high for at least 200nS (SCLK = 5MHz)
5. nCS low to select
6. Send convert axis command – for example: 0x000000. The first 0x00 is the command to convert the X-channel. The second and third 0x00 are placeholders. There should be a minimum of 40µs between the first and second bytes in order to give the A/D conversion adequate time to complete.
7. The 12-bit A/D data is read in on the second and third SDO bytes.
8. nCS high for at least 200nS (SCLK = 5MHz)
9. Repeat data read cycle. Recommend reading X-axis, Y-axis, Z-axis, and the Control Register for each read cycle to verify the Control Register mode selection.

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Test Specifications

! *Special Characteristics:*

These characteristics have been identified as being critical to the customer. Every part is tested to verify its conformance to specification prior to shipment.

Table 8. Test Specifications

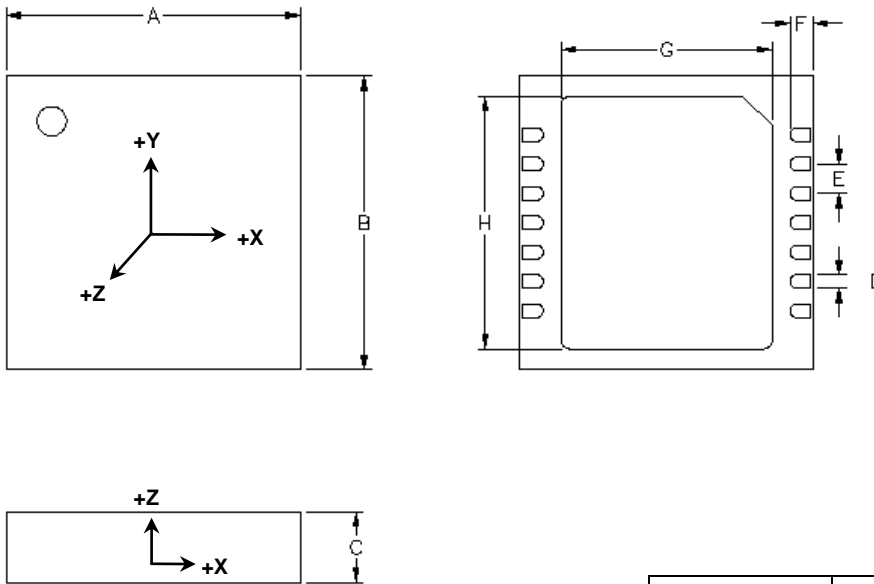| Parameter	Specification	Test Conditions
Zero-g Offset @ RT	2048 +/- 130 counts	25C, Vdd = 3.3 V
Sensitivity @ RT	819 +/- 16 counts/g	25C, Vdd = 3.3 V
Current Consumption -- Operating	500 <= Idd <= 1400 uA	25C, Vdd = 3.3 V

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Package Dimensions and Orientation

5 x 5 x 1.2 mm DFN

Dimension	mm			inch		
	Min	Nom	Max	Min	Nom	Max
A		5.00			0.197	
B		5.00			0.197	
C	1.10	1.20	1.30	0.043	0.047	0.051
D	0.18	0.23	0.28	0.007	0.009	0.011
E		0.50			0.020	
F	0.35	0.40	0.45	0.014	0.016	0.018
G	3.50	3.60	3.70	0.138	0.142	0.146
H	4.20	4.30	4.40	0.165	0.169	0.173

All dimensions and tolerances conform to ASME Y14.5M-1994

When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase.

± 2g Tri-axis Digital
Accelerometer Specifications

PART NUMBER:

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Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

Position	1	2	3	4	5	6
Diagram					Top / Bottom	Bottom / Top
X	2048 counts	2867 counts	2048 counts	1229 counts	2048 counts	2048 counts
Y	2867 counts	2048 counts	1229 counts	2048 counts	2048 counts	2048 counts
Z	2048 counts	2048 counts	2048 counts	2048 counts	2867 counts	1229 counts
X-Polarity	0	+	0	-	0	0
Y-Polarity	+	0	-	0	0	0
Z-Polarity	0	0	0	0	+	-

(1g)

Earth's Surface

Revision History

REVISION	DESCRIPTION	DATE
1	Initial Release	06-Aug-2007
2	Added Special Characteristics designation to property tables. Adjusted current specification to six sigma tolerances.	15-Nov-2009
3	Changed to new format, widened Zero-g Offset tolerance to 130 counts, updated SPI rate to 5MHz max, corrected Bandwidth footnote.	03-Nov-2010

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