SSM-2013

VOLTAGE-CONTROLLED AMPLIFIER

FEATURES
- 0.01% THD Typ
- 0.03% IMD Typ
- 800kHz Unity-Gain Bandwidth
- 12dB Headroom (at Rating)
- 40dB Gain Capability
- 106dB Dynamic Range (17.5 Bits)
- Full Class A Performance
- Mute and Exponential Controls

APPLICATIONS
- Compressor/Limiters
- Noise Gates
- Automatic Gain Control
- Noise Reduction Systems
- Telephone Line Interfaces

ORDERING INFORMATION

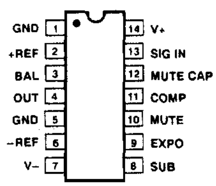
14-PIN PLASTIC DIP	OPERATING TEMPERATURE RANGE
SSM2013P	−10°C to +55°C

GENERAL DESCRIPTION

The SSM-2013 is a high-performance monolithic Class A Voltage Controlled Amplifier. Operating with current mode inputs and outputs, the SSM-2013 is ideal when logarithmic control of gain is needed. The output current gain or attenuation is controlled by applying a control voltage to the EXPO pin 9. The amplifier offers wide bandwidth, easy signal summing and minimum external component count.

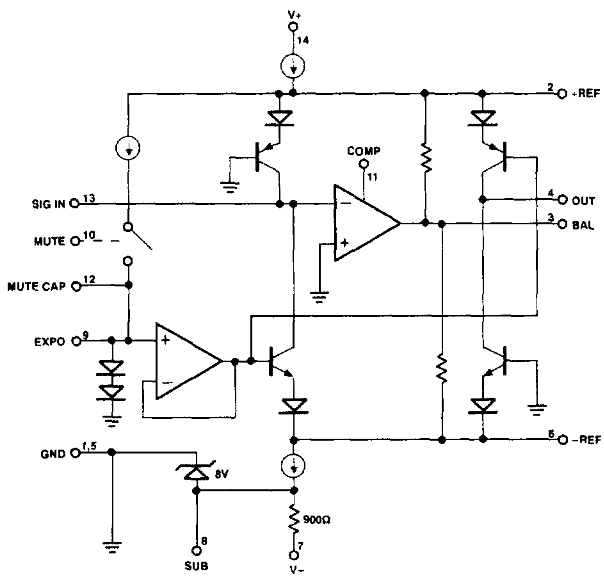
The SSM-2013 can operate with more than 12dB of headroom at the rated specifications or be configured for gains as high as 40dB. Inherently low control feedthrough and 2nd harmonic distortion make trimming unnecessary for most applications. An extremely wide control range of 110dB regulated by a flexible antilogarithmic control port make this VCA a versatile analog building block. With 800kHz bandwidth and 94dB S/N ratio at 0.01% THD, the SSM-2013 provides a useful solution for a variety of signal conditioning needs in applications ranging from professional audio to analog instrumentation, process controls and more.

PIN CONNECTIONS



14-PIN
EPOXY DIP
(P-Suffix)

SIMPLIFIED SCHEMATIC



7/89, Rev. A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... 36V or ±18V
Junction Temperature .... +150°C
Operating Temperature Range .... −10°C to +55°C
Storage Temperature Range .... −65°C to +150°C
Maximum Current into any Pin 10mA
Lead Temperature Range (Soldering 60 sec) .... 300°C

PACKAGE TYPE	θ_{JA} (NOTE 1)	θ_{JC}	UNITS
14-Pin Plastic DIP (P)	90	47	°C/W

NOTE:
1. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V and T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	SSM-2013 MIN	TYP	MAX	UNITS
Positive Supply Voltage		+12	+15	+18	V
Negative Supply Voltage (Note 1)		−7.6	−8.2	−8.7	V
Positive Supply Current		5.4	8.7	10.4	mA
Negative Supply Current		6.0	8.7	11.0	mA
Negative Supply Bias Resistor (Pin 7 to Pin 8)		675	900	1170	Ω
Expo Input Bias	V_e = GND (Note 2)	–	1.0	3.2	µA
Expo Control Sensitivity	at Pin 9	–	−10	–	mV/dB
Mute Off (Logic Low)		0.0	–	1.0	V
Mute On (Logic High)		3.0	5	15	V
Mute Attenuation	(@ 1kHz, $V_{PIN\ 10}$ = +5V)	–	−90	–	dB
Current Gain	V_e = GND	0.90	1.0	1.1	
Current Output Offset	V_e = GND	−7.5	0	+7.5	µA
Output Leakage	V_e = +600mV	−50	0	+50	nA
Max Available Output Current	V_e = GND, 15k (pin 3 to −V)	±1.2	–	–	mA
Current Bandwidth (3dB)	V_e = GND	–	800	–	kHz
Signal Feedthrough	V_e = +1.2V	–	−90	–	dB
Signal to Noise (20Hz - 20kHz) (Notes 3, 4)	V_e = GND, No Signal	–	−94	92.5	dB
THD (Untrimmed) (Note 4)	V_e = GND, I_{IN} = 600µA_{p-p}	–	0.01	0.06	%
THD (Trimmed)	V_e = GND, I_{IN} = 600µA_{p-p}	–	0.004	–	%
IMD (Untrimmed) SMPTE (Note 4)	V_e = GND, I_{IN} = 600µA_{p-p}	–	0.03	0.12	%
IMD (Trimmed) SMPTE	V_e = GND, I_{IN} = 600µA_{p-p}	–	0.012	–	%

NOTES:
1. Measured at pin 8, pin 7 = −15V.
2. V_e is voltage on pin 9 (V_{EXPO}).
3. Referred to a 400µA_{p-p} input level.
4. Parameter is sample tested to max limit (0.4% AQL).

Specifications subject to change; consult latest data sheet.

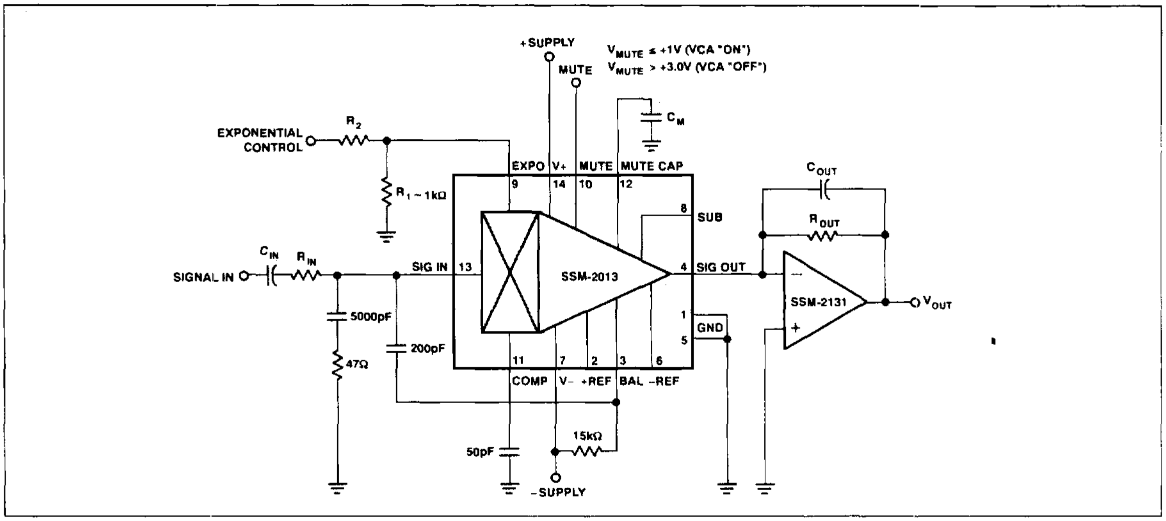


FIGURE 1: *Typical Connection*

THEORY OF OPERATION

The SSM-2013 is a current input/current output device. It is essentially a current mode amplifier where the output current/input current transfer function is controlled by a control voltage applied at the EXPO pin (9). Current mode operation allows easy adaptation to various voltage ranges at the input, output and control port. As configured, it offers large attenuation plus moderate gain capability.

CHOOSING R_{IN}

Most applications use the typical connection of Figure 1. In this configuration, The SSM-2013 will accomodate input currents up to 1.2mA without significant distortion or clipping. To set the maximum operating current to 1.2mA, select R_{IN} to equal Vpeak/1.2mA.

As an example: For a 7Vp-p nominal signal level (±3.5V), select R_{IN} = 12kΩ. Here, I_{IN} operating is: 3.5V/12k = 300μA, which yields 12dB headroom from 1.2mA. In some applications such as broadcast equipment, 16 - 24dB headroom may be required.

Selecting ±300μA nominal operating current yields 12dB headroom. Figure 2 shows the IMD/THD (Intermodulation and Total Harmonic Distortion) characteristics of the SSM-2013 at this 300μA or 600μA peak-to-peak operating level.

Operation at higher input currents will increase distortion effects whereas operation at lower currents will improve distortion but decrease the S/N ratio. For examle, operation with 20dB headroom versus 12dB will improve the relative effects of IMD/THD shown in Figure 2 by 2.5 times. For 20dB headroom, use ±120μA nominal operating input current. At this level, the signal-to-noise ratio will be 86dB.

The SSM-2013 is capable of 40dB gain and as much as −95dB attenuation. Gain or attenuation levels are set by the EXPO control pin as described in the next section. Figure 2 shows how IMD/THD performance degrades with current gain and attenuation. Note also that distortion in the SSM-2013 is nearly all 2nd harmonic. From a sonic standpoint, this is much less objectionable than other types of distortion.

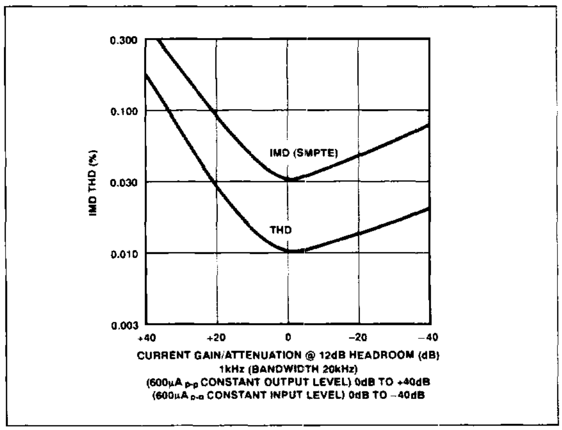


FIGURE 2

For best performance, choose C_{IN} and R_{IN} for a cutoff frequency below the audio band. C_{IN} will block DC offsets from previous stages.

OUTPUT SECTION

When establishing circuit gain or attenuation, it is important to consider the tradeoffs between gain/attenuation for the SSM-2013 versus the gain of the output amplifier/current to voltage converter. Operating the SSM-2013 with current gain above 20 or 30dB increases distortion as shown in Figure 2. Gain in the output amplifier amplifies the VCA noise. This will directly increase the equivalent VCA noise floor by the amplifier gain. A compromise within these constraints will determine the best tradeoff between SSM-2013 current gain and the amplifier gain. Figure 3 shows how output noise increases as current gain increases.

CONTROL PIN EXPO

The control port EXPO (pin 9) is a high impedance input with an exponential control sensitivity of −1dB/10mV or −10mV/dB. The overall control range is +40dB to −95dB. This pin is easily adaptable to any control voltage range by selecting the R_1 and R_2

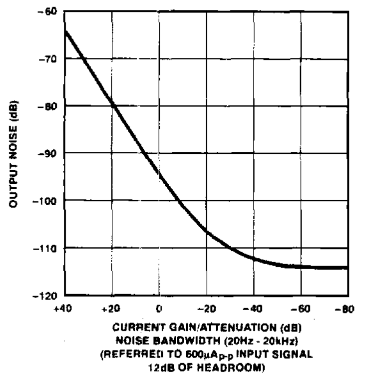


FIGURE 3

divider appropriately. Note the negative control relationship where positive voltages at pin 9 result in signal attenuation whereas negative voltages yield gain. The control pin is accurate to within ±1.5dB over a ±36dB range.

The transfer characteristics for the control pin is shown in Figure 4. Note the dotted line showing an optional improvement in gain accuracy. To achieve this improved transfer characteristic, refer to the circuit of Figure 5. As the recommended circuit for control summing applications, this technique offers a significant improvement in linearity over a wider control voltage range.

The control port sensitivity has a −3300ppm/°C temperature coefficient. To compensate for this drift, use a +3300ppm/°C tempsistor* in place of R_1 shown in Figure 1.

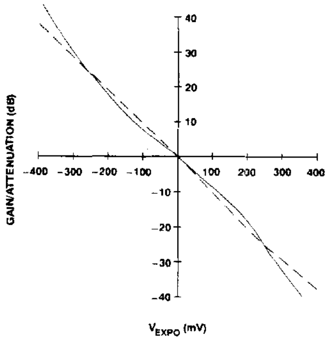


FIGURE 4: *Circuit Gain/Attenuation vs. V_{EXPO}*

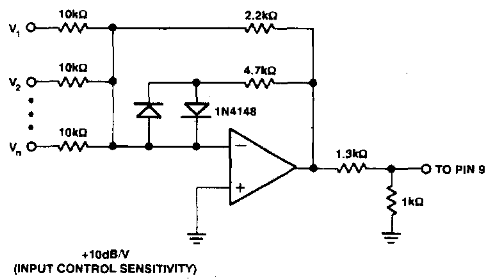


FIGURE 5: *Control Summer with Improved Linearity over Wider Control Range*

MUTING FUNCTION

The mute circuit turns the device on or off independent of the control pin EXPO. Muting is activated when the MUTE (pin 10) is raised above 3.0V and is compatible up to 15V. Muting is off when MUTE is below 1.0V.

A selectable MUTE CAP connected between pin 12 and ground determines the controlled turn on/turn off rate. The recommended 1μF mute cap and internal 10kΩ impedance gives a 10ms time constant. This transition timing is considered quick without being too abrupt or "poppy."

To disable the muting function, simply ground pin 10.

* RCD Components, Inc. Part Number LP1/4, 3301 Bedford Street, Manchester, NH U.S.A., (603) 669-0054, Telex 943512

APPLICATIONS INFORMATION

OUTPUT AMPLIFIER

Note the importance of including C_{OUT} in parallel with R_{OUT} to ensure stability under all signal and output loading conditions. A corner frequency of 300kHz for the R_{OUT}, C_{OUT} combination is sufficient, but a lower frequency may also be chosen to limit noise output the audio band. This, however will result in a slower transient response.

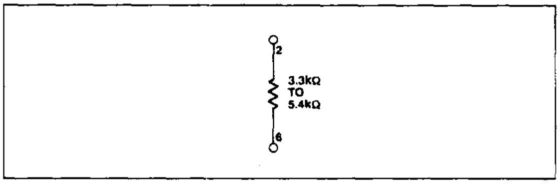


FIGURE 6

CONTROL FEEDTHROUGH TRIMMING

Control feedthrough is defined as the portion of the control signal fed to the output in the absence of an input signal. A single shunt resistor across pins 2 and 6 will reduce both control feedthrough and noise (see Figure 6). Values from 3.3kΩ to 5.4kΩ offer an improvement in control feedthrough from 20dB to 10dB, respectively.

This trim will tradeoff an increase in THD by roughly 3 to 5 times. THD increases slightly more using a lower resistor value. With 3.3kΩ, the worst case is about 0.4% over gain and attenuation. By comparison, THD ranges from 0.05% to 0.1% with no shunt resistor.

TRIMMING DISTORTION

The SSM-2013 has very good distortion, offset and control feedthrough at unity current gain. For applications requiring over 10dB to 20dB gain, trimming allows the best overall distortion versus gain.

Distortion Trim Procedure for High Gain Applications:

1. Apply voltage at pin 9 corresponding to maximum current gain.
2. Set input level so output is just below clipping.
3. Adjust trimming per Figure 7 until distortion is at a minimum.

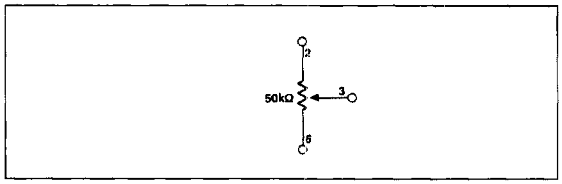


FIGURE 7

COMPENSATION

To compensate, connect a 50pF capacitor from pin 11 (COMP) to GND as shown in the typical connection.

ON-BOARD REFERENCE

An on-chip zener diode helps establish the –8V available at the SUB output (pin 8). This is a general purpose reference that can be used to introduce DC offsets.

BREADBOARDING THE SSM-2013

A typical connection identical to Figure 1 and redrawn for breadboarding purposes is shown in Figure 8.

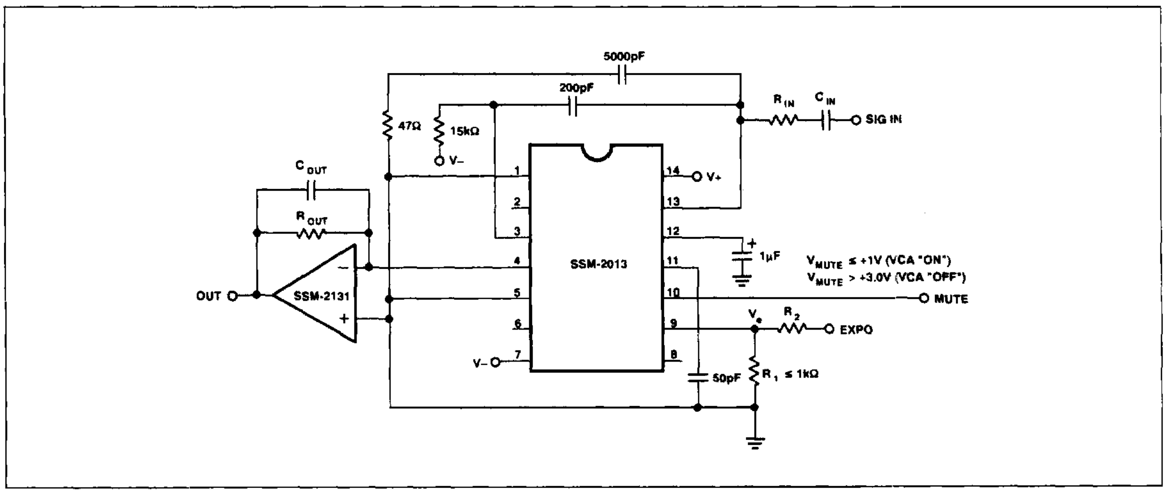


FIGURE 8: *Typical Connection for Breadboarding*

MEASURING NOISE

When measuring audio noise in the SSM-2013, bandwidth should be limited to 20kHz to 30kHz. This is due to the presence of broadband noise which is caused by a zero at 600kHz. The zero results from the 5000pF-47Ω network at the input. Beyond 30kHz, the noise floor increases at approximately 6dB per octave from 45kHz to 600kHz where it rolls off.

AGC AMPLIFIER DESIGN WITH ADJUSTABLE ATTACK AND RELEASE CONTROL

The automatic gain control (AGC) amplifier described below and shown in Figure 9, features selectable gain reduction compression ratios and time domain adjustable AGC attack and release. This design employs the SSM-2013 VCA, SSM-2110 precision level detector, two SSM-2134 low noise op amps, and an OP-215 FET input dual op amp.

The design features an inverting or noninverting input buffer amplifier, a voltage controlled amplifier with adjustable attack and recovery characteristics, driven by a true RMS level detector. Additionally, it provides selectable gain reduction compression, adjustable AGC output level, and maximum gain limit controls. Signal-to-noise ratio is better than 100dB and the RMS level detector allows the AGC amplifier to operate transparently throughout the audio spectrum.

The gain recovery is linear and time adjustable, and has maximum gain limiting (gating) to preclude input source noise floor rise.

The input circuit includes a line level (−10dBu to 0dBu) buffer amplifier, that accepts inverting or noninverting inputs with greater than 10kΩ loading impedance. The buffer also isolates the input source from the compressor gain reduction ratio selector, and limits step function slewing voltage.

The six-position gain reduction selector that follows the input amplifier provides adjustable compression that smoothes the AGC action. Six GAIN REDUCTION slope ratios of 2 to 22 can be selected, thus reducing the irritating *"hole producing and pumping"* character of most AGC circuits. The SSM-2013 VCA is chosen for its predictable behavior and its high performance. The dynamic range exceeds 94dB over the frequency range 20Hz to 20kHz. Over this frequency range, the amplifier achieves typically less than 0.01% THD + noise, and 0.03% IMD.

The SSM-2110's precision rectifier circuit produces the true RMS output that comprises a level detector. It results in a consistent and precise AGC action that retains good signal dynamics while leveling the input signal. It responds to the audio signal power density in a manner similar to human hearing.

Following the precision RMS rectifier is the VCA control voltage conditioning circuits. Constructed around U_6 (OP-215), the FET-input

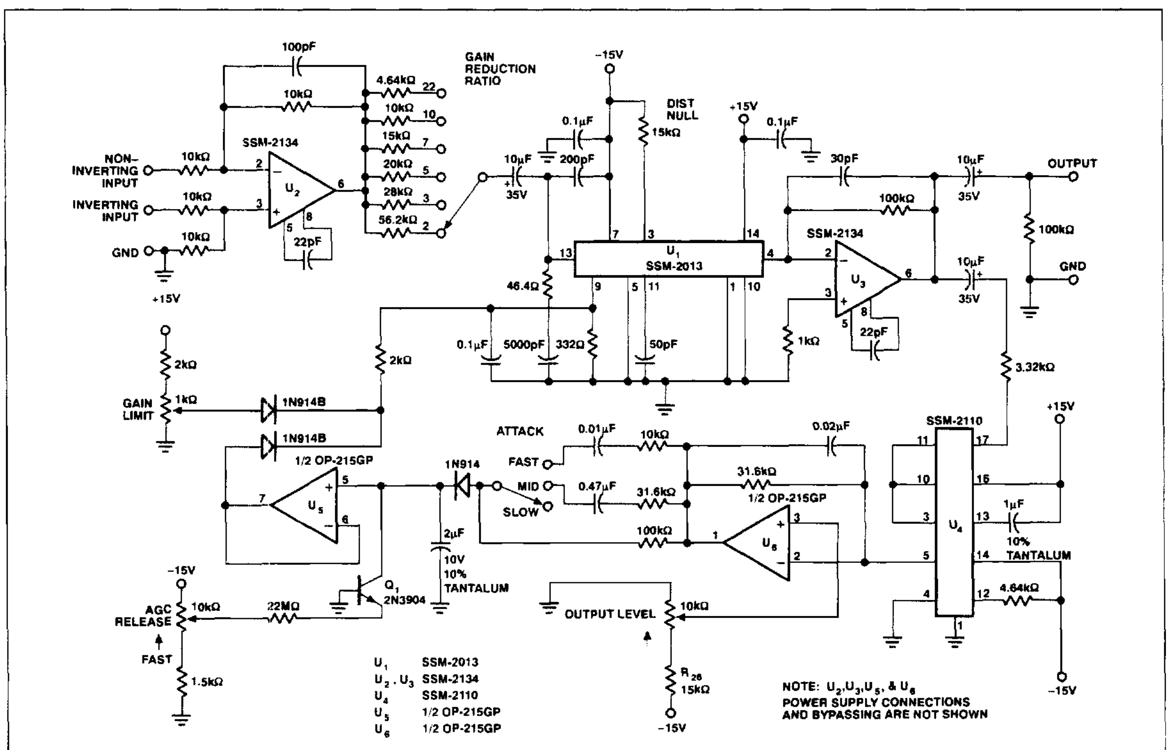


FIGURE 9

amplifier forms an integrator while the other amplifier provides the VCA control port buffer. The AGC output level is set by the rectified signal voltage compared to the reference voltage from the OUTPUT LEVEL control.

The AGC attack and compression response is altered by adjusting the integrator charging time constant or integrator wave shape current. The three-position ATTACK switch allows selection of fast, medium, and slow compression and AGC response. When the slow position is selected, an insignificant amount of compression will take place, while fast and medium combine compression with the AGC action. The AGC release rate is controlled by a constant current discharge of the integrator capacitor. The recovery time constant is linear and adjusted by changing the integrator discharge current supplied by Q_1 and regulated by the RELEASE rate control.

The SSM-2134 has been selected for its low noise and high performance characteristics. The AGC circuit described is of the feedback class, that is, the level detecting rectifier follows the voltage controlled amplifier stage. This class of AGC circuit combined with the complementary gain reduction compression, driven by RMS level detection, and adjustable attack and release AGC action, allows this circuit to be as unobtrusive or as conspicuous as desired.

The flexibility and high performance of this design, along with the simplicity and cost effectiveness, allows this design to be suitable for incorporating in mixing console designs, or in stand-alone products.

TABLE 1: Circuit Performance Specifications

Input Voltage Range (Nominal for 0dBu Out)	−26dBu to +10dBu (6mV to 2.45V_{RMS})
Rectifier Type	RMS
AGC Amplifier Class	Feedback
Attack Time	20 to 200ms
Recovery Time (6dB)	3 to 32 SEC
VCA Feedthrough (Trimmed)	−100dB
Gain Limit Range (Gain Reduction 22)	−26dBu to −12dBu
Frequency Response (20Hz to 20kHz)	±0.2dB
S/N Ratio (@ ±10dB Gain)	106dB
THD + Noise (@ +23dBu, 20Hz to 20kHz)	0.01%
IMD (@ + 23dBu, SMPTE 60Hz & 4kHz, 4:1)	0.02%
Output Voltage Slew Rate	6V/µs
Output Voltage (2kΩ Load)	+22dBu or 10V_{RMS}