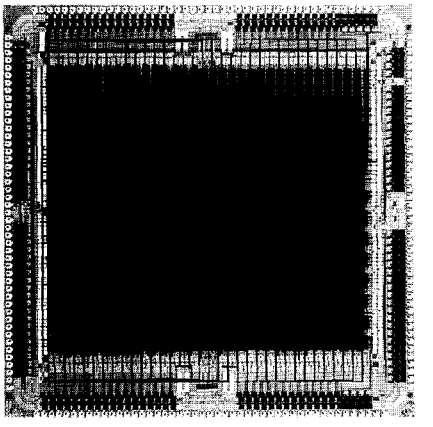
L64270
64 to 64
Crossbar Switch
(XBAR)

LSI LOGIC

Description

The L64270 is a 64 to 64 crossbar switch in which any of the 64 outputs can be connected to any of the 64 inputs without any blocking constraints. In addition, any output can be set to a constant value or put in a high impedance state. Each of the 64 switches can be operated in a flow through mode with a delay of 25 ns from input to output or in a pipelined mode with a delay of 15 ns from clock to output.

The device can be put into a bus and/or a bidirectional mode to simplify operation with multi-bit unidirectional or bidirectional buses. The L64270 is implemented in a 1.5-micron drawn gate length (0.9-micron effective channel length) low power HCMOS technology.



L64270 Chip

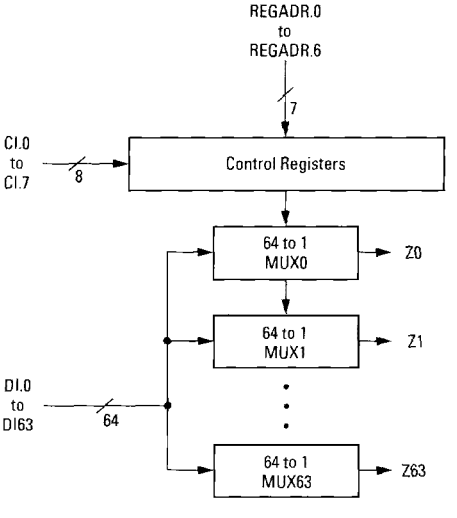
Features

- Non-blocking 64 to 64 crossbar switch
- Pipelined or flow through modes
- Multiple chips can be used to increase switch size
- Outputs can be set to constant values
- Can easily switch buses of different widths
- Can be be configured as 64 bidirectional ports
- Double buffered control signals
- Can perform arithmetic or logical shifting and bit rotation
- High data rates

	Pipelined Mode	Flow Through Mode
L64270-40	40 MHz	25 ns
L64270-30	30 MHz	35 ns

- 160-pin PQFP (Plastic Quad Flat Pack) or 180-pin PPGA (Plastic Pin Grid Array) package

Block Diagram



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Architecture

The L64270 consists of 64 identical circuits, each generating a single bit of the output (Z0-Z63). Each output can be connected to any of the 64 data inputs (DI0-DI63), a constant value or be made to float. Each output path can be individually configured as flow through or pipelined. In flow through mode new data presented on an input becomes valid at an output pin after a delay. In pipelined mode the data does not change until after a rising clock edge.

Each output has an 8-bit control word associated with it. This control word specifies the behavior of each output as outlined in the previous paragraph. The control information is double buffered. Control data can be loaded into the loading latch without disturbing the operation specified in the active latches. Setting BNKLDI HIGH transfers data from all 64 of the loading latches to the 64 active latches.

A mode latch is used to program the mode of the entire switch network.

Pin Listing and Description

DI0-DI63/I00-I063
64 data inputs in unidirectional system (BD LOW) or 64 data inputs for I/Os in bidirectional system (BD HIGH).

Z0-Z63/I00-I063
Sixty-four data outputs in unidirectional system (BD LOW) or 64 data outputs for I/Os in bidirectional system (BD HIGH, should be connected to I00-I063 above).

CI.0-CI.7
Control input bus. This bus is used to load the switch connection information and the bus mode control information. The data is loaded into the register specified by REGADR when $\overline{WE}$ is LOW.

REGADR.0-REGADR.6
Address of control register or mode latch which is to receive the data on the CI bus. If REGADR.6 is HIGH, the data on CI is loaded into the mode latch. If REGADR.6 is LOW, the control latch for the output determined by REGADR.0-REGADR.5 is loaded.

BDCYC1
When loading control words in the bidirectional mode, BDCY1 is HIGH during first $\overline{WE}$ cycle and LOW during second $\overline{WE}$ cycle. Ignored when the L64270 is used as a unidirectional switch (BD LOW). In this case BDCY1 may be tied HIGH or LOW.

$\overline{WE}$
Active LOW control data strobe. The data on the CI bus is latched into the master latch specified by REGADR when $\overline{WE}$ is LOW.

CLK
Pipeline register clock. All pipeline registers latch data at the positive edge of CLK. Not used if all pipeline registers are bypassed.

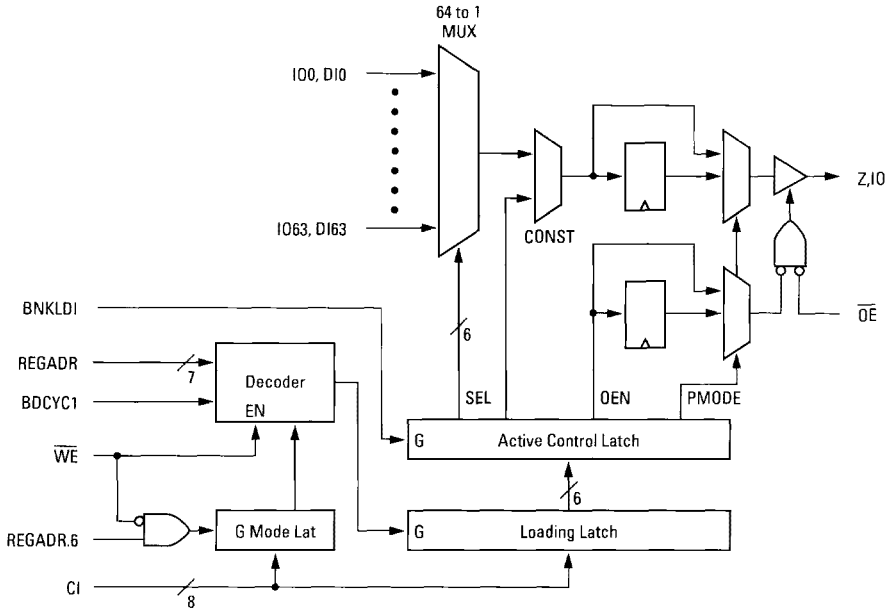
BNKDI
Transfers control data from the master slave latches when HIGH. Slave, or active latch is transparent HIGH.

$\overline{OE}$
Disables all outputs when HIGH. When LOW, the state of each output will be determined by the internally latched OEN signals.

Pin Description Summary

Pin	No. of Pins	I/O	Description
DI0–DI63 I00–I063	64 64	I I	64 inputs in unidirectional system 65 inputs for I/Os in bidirectional system
Z0–Z63 I00–I063	64 64	O O	64 outputs in unidirectional system 64 outputs for I/Os in bidirectional system (connected to I00–I063 above)
CI.0–CI.7	8	I	Control input bus
REGADR.0– REGADR.6	7	I	Address on control register or mode latch
BDCYC1	1	I	When loading bidirectional control words are HIGH during first $\overline{WE}$ cycle and LOW during second $\overline{WE}$ cycle
$\overline{WE}$	1	I	Active LOW control data strobe
CLK	1	I	Pipeline register clock active at rising edge
BNKLDI	1	I	Transfers control data from the master to slave latches when HIGH
$\overline{OE}$	1	I	Disables all outputs when HIGH

Detailed Architecture
(One for each output
Z0–Z63)



Loading the Control Words

A control word is loaded by putting the data on the CI pins, setting the proper register address on REGADR and pulling $\overline{WE}$ LOW. For bidirectional systems, two cycles are required, one with BDCYC1 LOW and one with BDCYC1 HIGH.

BNKLDI is used to transfer data from master to slave latches. New configuration information may be supplied while the switch is operating and transferred into the active latches in a single cycle, by asserting BNKLDI. If BNKLDI is tied HIGH, the registers operate in a flow through mode.

The memory map for the processor is given in the Memory Maps table for each bus width. For all cases, if REGADR $\geq$ 64 the mode latch is selected.

When REGADR < 64, the connection information for a particular output bus is loaded. The output pins that are affected for each control word are listed in the second column. If PMODE is HIGH, output for that particular bus is pipelined. To connect an output bus to an input bus, CI.6 is pulled LOW and the input bus number is specified on the CI.5 to CI.0 pins (SEL). Note that the input bus number has fewer bits for longer bus widths. If CI.6 is HIGH, the output bus driver will float if OEN is HIGH and will be set to the value of CONST if OEN is LOW.

If CI.6 is LOW, the output drivers are automatically enabled and a write operation with CI.6 HIGH should not be performed.

Bidirectional Bus Mode

The L64270 can be configured to operate with separate input and output buses or with one bidirectional bus. The bidirectional mode is selected by selecting the BD bit HIGH (see section on loading control words). In this mode the I/O pins, with the same name, must be externally connected to each other. Note that the numbering of these pins is not identical to the numbering of the DI and Z pins. Care should be taken to connect the pins correctly. Additionally, the loading of control words takes two cycles.

In the following sections on bus mode and loading control words, the references to inputs and outputs should be read as I/O pins when the device is in the bidirectional mode.

Bidirectional Bus Mode (Continued)

In bidirectional mode, the L64270 is wired (externally) to connect the 64 outputs in parallel with the 64 inputs. When the connection of the switch is changed, the device automatically and properly disables all outputs that are in parallel with active inputs. The user needs only to specify the desired connections. During the first cycle of loading a bidirectional control word (BDCNCI HIGH), the output in parallel with an active input is disabled. In the second cycle (BDCYC1 LOW), the active output is connected as specified.

For example, suppose we wish to connect IO0 ← IO1. This means that IO1 is an input and this data should appear on the output IO0. At the system level, the IO0 input DI0 is connected to the IO0 output, Z32. Similarly, the IO1 input DI1 is connected to the IO1 output, Z33. During the first loading cycle, Z33 is disabled. In the second cycle, Z32 is connected to DI1. To program the device for this connection, REGADR is set to 0 and CI is set to 1 and $\overline{WE}$ is strobed twice: once with BDCYC1 HIGH and once with BDCYC1 LOW.

Bus Mode

For systems in which all signals are grouped into buses with widths equal to 2^N, only one control word per bus needs to be set. This frees the user from having to explicitly declare the connections for every signal in every bus. The user sets the bus width via the internal control signals, MASK.0–MASK.5. The values of MASK.0–MASK.5 for various bus widths are given in the Bus Configuration table.

Bus Configuration

Bus Width (Bits)	MASK.5-MASK.0	Number of Buses
64	111111	1
32	011111	2
16	001111	4
8	000111	8
4	000011	16
2	000001	32
1	000000	64

For a bus width of W, the inputs and the outputs (or I/Os) are divided into 64/W buses. The first bus consists of the inputs and outputs numbered from 0 to W-1. The second bus consists of the inputs and outputs numbered from W to 2W-1. Finally, the last bus consists of inputs and outputs numbered from 64-W to 63.

The accompanying table shows the grouping of inputs and outputs when operating with 8-bit buses.

Pin Assignments for 8-Bit Buses

Bus Number	Input Pins (BD LOW)	Output Pins (BD LOW)	I/O Pins (BD HIGH)
0	DI0-DI7	Z0-Z7	I00-I07
1	DI8-DI15	Z8-Z15	I08-I015
2	DI16-DI23	Z16-Z23	I016-I023
3	DI24-DI31	Z24-Z31	I024-I031
4	DI32-DI39	Z32-Z39	I032-I039
5	DI40-DI47	Z40-Z47	I040-I047
6	DI48-DI55	Z48-Z55	I048-I055
7	DI56-DI63	Z56-Z63	I056-I063

Memory Maps

All Bus Widths

REGADR	CI.7	CI.6	CI.5	CI.4	CI.3	CI.2	CI.1	CI.0
64-127	–	BD	MASK.5	MASK.4	MASK.3	MASK.2	MASK.1	MASK.0

Bus Width = 1

REGADR	Z or IO Pins	CI.7	CI.6	CI.5	CI.4	CI.3	CI.2	CI.1	CI.0
63	63	PMODE63 PMODE63	0 1	SEL63.5 CONST63	SEL63.4 OEN63	SEL63.3	SEL63.2	SEL63.1	SEL63.0
62	62	PMODE62 PMODE62	0 1	SEL62.5 CONST62	SEL62.4 OEN62	SEL62.3	SEL62.2	SEL62.1	SEL62.0
61	61	PMODE61 PMODE61	0 1	SEL61.5 CONST61	SEL61.4 OEN61	SEL61.3	SEL61.2	SEL61.1	SEL61.0
≈									≈
0	0	PMODE0 PMODE0	0 1	SEL0.5 CONST0	SEL0.4 OEN0	SEL0.3	SEL0.2	SEL0.1	SEL0.0

Memory Maps
(Continued)

Bus Width = 2

REGADR	Z or 10 Pins	CI.7	CI.6	CI.5	CI.4	CI.3	CI.2	CI.1	CI.0
62	62–63	PMODE31 PMODE31	0 1	SEL31.4 CONST31	SEL31.3 OEN31	SEL31.2	SEL31.1	SEL31.0	NA
60	60–61	PMODE30 PMODE30	0 1	SEL30.4 CONST30	SEL30.3 OEN30	SEL30.2	SEL30.1	SEL30.0	NA
≈									≈
2	2–3	PMODE1 PMODE1	0 1	SEL1.4 CONST1	SEL1.3 OEN1	SEL1.2	SEL1.1	SEL1.0	NA
0	0–1	PMODE0 PMODE0	0 1	SEL0.4 CONST0	SEL0.3 OEN0	SEL0.2	SEL0.1	SEL0.0	NA

Bus Width = 4

REGADR	Z or 10 Pins	CI.7	CI.6	CI.5	CI.4	CI.3	CI.2	CI.1	CI.0
60	60–63	PMODE15 PMODE15	0 1	SEL15.3 CONST15	SEL15.2 OEN15	SEL15.1	SEL15.0	NA	NA
56	56–59	PMODE14 PMODE14	0 1	SEL14.3 CONST14	SEL14.2 OEN14	SEL14.1	SEL14.0	NA	NA
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4	4–7	PMODE1 PMODE1	0 1	SEL1.3 CONST1	SEL1.2 OEN1	SEL1.1	SEL1.0	NA	NA
0	0–3	PMODE0 PMODE0	0 1	SEL0.3 CONST0	SEL0.2 OEN0	SEL0.1	SEL0.0	NA	NA

Bus Width = 8

REGADR	Z or 10 Pins	CI.7	CI.6	CI.5	CI.4	CI.3	CI.2	CI.1	CI.0
56	56–63	PMODE7 PMODE7	0 1	SEL7.2 CONST7	SEL7.1 OEN7	SEL7.0	NA	NA	NA
48	48–55	PMODE6 PMODE6	0 1	SEL6.2 CONST6	SEL6.1 OEN6	SEL6.0	NA	NA	NA
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8	8–15	PMODE1 PMODE1	0 1	SEL1.2 CONST1	SEL1.1 OEN1	SEL1.0	NA	NA	NA
0	0–7	PMODE0 PMODE0	0 1	SEL0.2 CONST0	SEL0.1 OEN0	SEL0.0	NA	NA	NA

Bus Width = 16

REGADR	Z or 10 Pins	CI.7	CI.6	CI.5	CI.4	CI.3	CI.2	CI.1	CI.0
48	48-63	PMODE3 PMODE3	0 1	SEL3.1 CONST3	SEL3.0 OEN3	NA	NA	NA	NA
32	32-47	PMODE2 PMODE2	0 1	SEL2.1 CONST2	SEL2.0 OEN2	NA	NA	NA	NA
16	16-31	PMODE1 PMODE1	0 1	SEL1.1 CONST1	SEL1.0 OEN1	NA	NA	NA	NA
0	0-15	PMODE0 PMODE0	0 1	SEL0.1 CONST0	SEL0.0 OEN0	NA	NA	NA	NA

Bus Width = 32

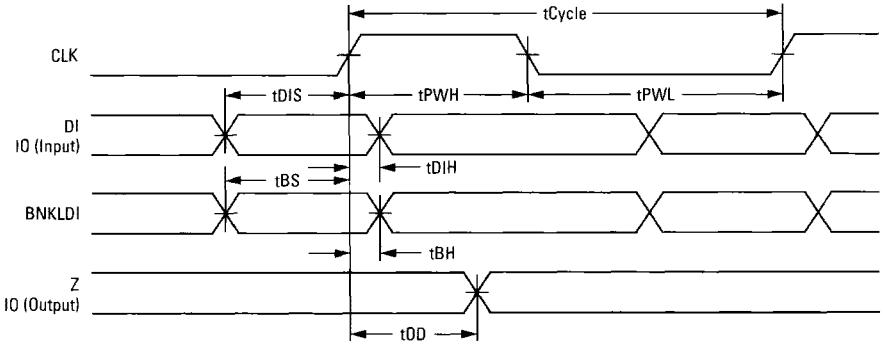
REGADR	Z or 10 Pins	CI.7	CI.6	CI.5	CI.4	CI.3	CI.2	CI.1	CI.0
32	32-63	PMODE1 PMODE1	0 1	SEL1.0 CONST1	NA OEN1	NA	NA	NA	NA
0	0-31	PMODE0 PMODE0	0 1	SEL0.0 CONST0	NA OEN0	NA	NA	NA	NA

Bus Width = 64

REGADR	Z or 10 Pins	CI.7	CI.6	CI.5	CI.4	CI.3	CI.2	CI.1	CI.0
0	0-63	PMODE0 PMODE0	0 1	NA CONST0	NA OEN0	NA	NA	NA	NA

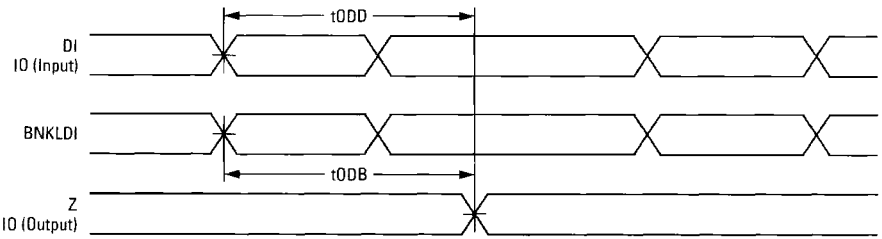
AC Timing Waveforms

I/O Timing, Pipelined Mode

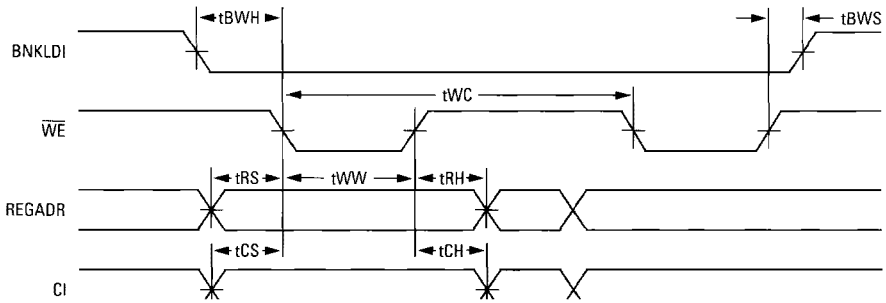


AC Timing Waveforms
(Continued)

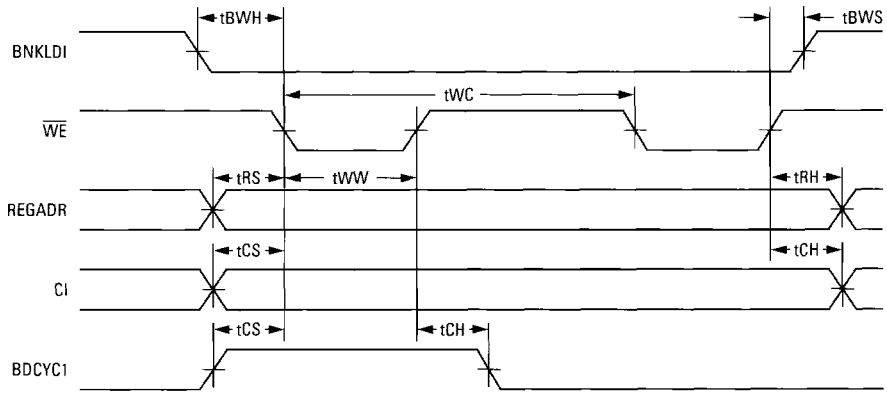
I/O Timing, Flow Through Mode



Parameter Loading Timing, Unidirectional Mode



Parameter Loading Timing, Bidirectional Mode



AC Switching Characteristics: Commercial: (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V)

Symbol	Parameter	L64270-40		L64270-30	
		Min	Max	Min	Max
tCYCLE	Minimum clock (CLK) cycle time[1]	25		33	
t PWH	Minimum clock (CLK) pulse width, HIGH[1]	8		11	
tPWL	Minimum clock (CLK) pulse width, LOW[1]	8		11	
tDIS	Input data (DI,IO) setup time[1]	12		14	
tDIH	Input data (DI,IO) hold time[1]	0		0	
tBS	BNKLDI setup time[1]	10		15	
tBH	BNKLDI hold time[1]	4		6	
tOD	Output delay (Z,IO) from CLK↑[1]		15		20
tODD	Output delay (Z,IO) from DI,IO[2]		25		35
tODB	Output delay (Z,IO) from BNKLDI[2]		30		40
tBWH	$\overline{WE}$ hold time with respect to BNKLDI ↓	10 + tPWH		15 + tPWH	
tBWS	$\overline{WE}$ setup time with respect to BNKLDI ↑	10		15	
tRS	REGADR setup time with respect to $\overline{WE}$ ↓	4		5	
tRH	REGADR hold time with respect to $\overline{WE}$↑	4		5	
tCS	CI setup time with respect to $\overline{WE}$ ↓	5		10	
tCH	CI hold time with respect to $\overline{WE}$ ↑	4		5	
tWW	Minimum $\overline{WE}$ pulse width, LOW	10		15	
tWC	Minimum $\overline{WE}$ cycle time	25		33	

Notes:
1. Output pipelined, COUT = 50 pF.
2. Output not pipelined, COUT = 50 pF.
3. All times are in ns.

Operating Characteristics

Absolute Maximum Ratings (Reference to GND)

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to +7	V
Input voltage	VIN	-0.3 to VDD + 0.3	V
DC input current	IIN	±10	mA
Storage temperature range	TSTG	-65 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	+3 to +6	V
Commercial range	TA	0 to +70	°C

DC Characteristics: Specified at VDD = 5 V over the specified temperature and voltage ranges[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIL	Low level input voltage				0.8	V
VIH	High level input voltage	0°C ≤ TA ≤ 70°C	2.0			V
IIN	Input current	VIN = VDD	-150		200	µA
VOH	High level output voltage	IOH = -4 mA	2.4	4.5		V
VOL	Low level output voltage	IOL = 4 mA		0.2	0.4	V
IOS	Output short circuit current[2]	VDD = Max, VO = VDD	15		130	mA
		VDD = Max, VO = 0V	-5		-100	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS			10	mA
IDD	Operating supply current[3]	tCYCLE = 25 ns		65		mA
CIN	Input capacitance	Any input		5		pF
COUT	Output capacitance	Any output		10		pF

Notes:
1. Commercial temperature range is 0°C to 70°C, ± 5% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.
3. For 40 MHz device.

AC Timing Waveforms
(Continued)

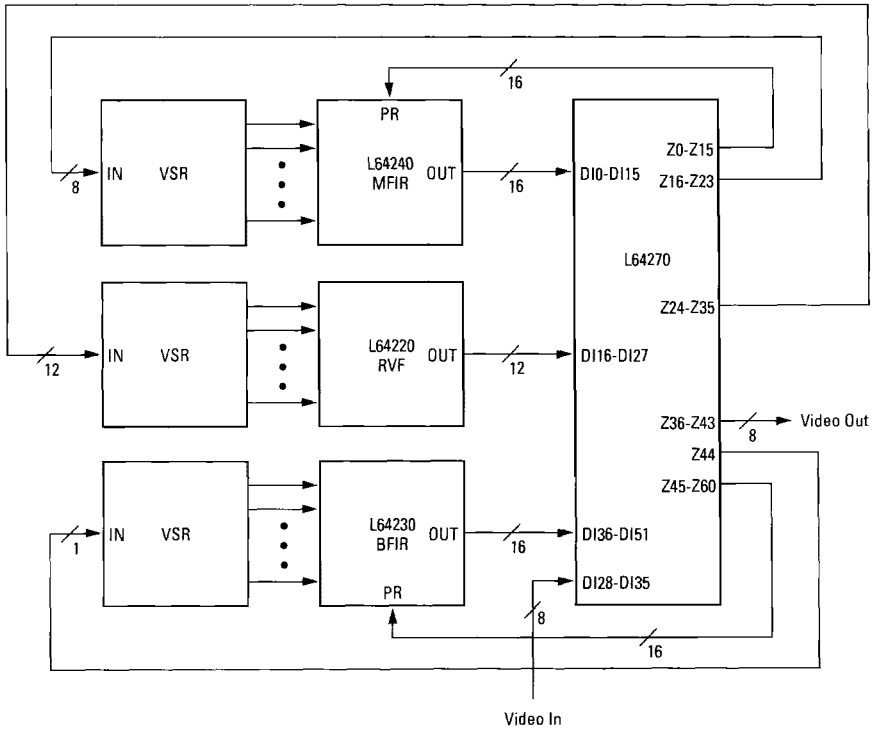
Connecting the L64200 Series Processors

The part is intended to be used in multiprocessor systems in which the configuration of processors must be changed electrically. The inputs and outputs of each processor and the system inputs and outputs would be connected to the switch. The user then has the ability to arbitrarily connect the output of every processor to the input of any other processor. Because each bit can be assigned independently, it is possible to connect the input of one processor to some bits of the output of one processor and some bits of the output of another.

With the ability to set any output bit to constant value, it is feasible to connect an 8-bit output to a 12-bit input while forcing the other four input bits low (or high if desired). The use of the single crossbar switch to control the interconnection of the L64220, L64230 and L64240 is shown. In this system, the processors can be connected in any order and the constant values can be used to fill in unused bits and to set the offset (threshold) values at the PR inputs.

In this example, because there is not a uniform bus width, each signal is switched independently.

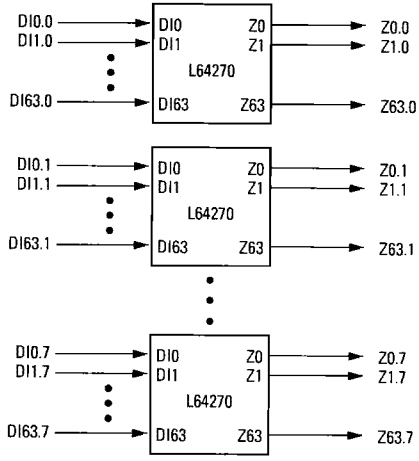
Use of Single L64270 to Interconnect L64200 Devices



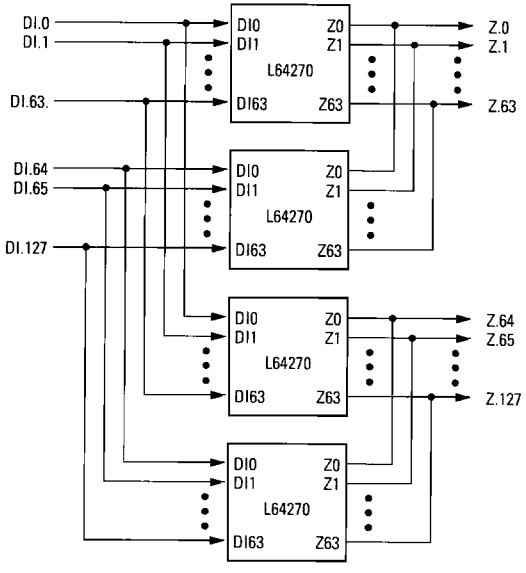
Creating Larger Switch Networks

Each output can be made to float to accommodate bidirectional pins in the system and also to allow for expansion of the switch size. There are two basic ways in which the switch size can be increased. In the first way, a full switch network is maintained, i.e., every output can be connected to any input as in the 128 to 128 unidirectional example. In the second way, some restrictions are placed on which input bits an output can be connected to. For example, if it is desired to switch 64 8-bit input buses to 64 8-bit output buses without bit crossings, the circuit shown can be used. In this case it is impossible to connect an output bit to an input bit with a different significance. However, this restriction results in a large savings in the number of switches required.

Using Eight Switches to Switch 64 (Unidirectional) 8-Bit Buses



Using Four Switches to form a 128 to 128 (Unidirectional) Crossbar Switch



L64270 Package Pin Information (160-Pin PQFP, by Pin Number)

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	ZO/IO32	28	DI20/IO20	55	Z46/IO14	82	DI58/IO58	109	DI32/IO32	136	Z21/IO53
2	REGADR.6	29	DI21/IO21	56	Z47/IO15	83	DI57/IO57	110	BDCYC1	137	Z20/IO52
3	$\overline{WE}$	30	DI22/IO22	57	Z48/IO16	84	DI56/IO56	111	REGADR.5	138	Z19/IO51
4	DI0/IO0	31	D123/IO23	58	Z49/IO17	85	DI55/IO55	112	REGADR.4	139	Z18/IO50
5	DI1/IO1	32	DI24/IO24	59	VSS	86	DI54/IO54	113	REGADR.3	140	VSS
6	DI2/IO2	33	DI25/IO25	60	VSS	87	DI53/IO53	114	REGADR.2	141	VSS
7	DI3/IO3	34	DI26/IO26	61	VDD	88	DI52/IO52	115	REGADR.1	142	VDD
8	DI4/IO4	35	DI27/IO27	62	Z50/IO18	89	DI51/IO51	116	REGADR.0	143	Z17/IO49
9	DI5/IO5	36	DI28/IO28	63	Z51/IO19	90	DI50/IO50	117	CI.7	144	Z16/IO48
10	DI6/IO6	37	DI29/IO29	64	Z52/IO20	91	DI49/IO49	118	CI.6	145	Z15/IO47
11	DI7/IO7	38	DI30/IO30	65	Z53/IO21	92	D148/IO48	119	CI.5	146	Z14/IO46
12	DI8/IO8	39	DI31/IO31	66	Z54/IO22	93	DI47/IO47	120	VDD	147	Z13/IO45
13	DI9/IO9	40	VDD	67	Z55/IO23	94	DI46/IO46	121	CI.4	148	Z12/IO44
14	DI10/IO10	41	Z32/IO0	68	Z56/IO24	95	D145/IO45	122	CI.3	149	Z11/IO43
15	DI11/IO11	42	Z33/IO1	69	Z57/IO25	96	DI44/IO44	123	CI.2	150	Z10/IO42
16	DI12/IO12	43	Z34/IO2	70	Z58/IO26	97	DI43/IO43	124	CI.1	151	Z9/IO41
17	DI13/IO13	44	Z35/IO3	71	Z59/IO27	98	DI42/IO42	125	CI.0	152	Z8/IO40
18	$\overline{OE}$	45	Z36/IO4	72	Z60/IO28	99	DI41/IO41	126	Z31/IO63	153	Z7/IO39
19	BNKLDI	46	Z37/IO5	73	Z61/IO29	100	DI40/IO40	127	Z30/IO62	154	Z6/IO38
20	VSS	47	Z38/IO6	74	Z62/IO30	101	VSS	128	Z29/IO61	155	Z5/IO37
21	CLK	48	Z39/IO7	75	Z63/IO31	102	DI39/IO39	129	Z28/IO60	156	Z4/IO36
22	DI14/IO14	49	Z40/IO8	76	DI63/IO63	103	DI38/IO38	130	Z27/IO59	157	Z3/IO35
23	DI15/IO15	50	Z41/IO9	77	DI62/IO62	104	DI37/IO37	131	Z26/IO58	158	Z2/IO34
24	DI16/IO16	51	Z42/IO10	78	DI61/IO61	105	DI36/IO36	132	Z25/IO57	159	Z2/IO33
25	DI17/IO17	52	Z43/IO11	79	DI60/IO60	106	DI35/IO35	133	Z24/IO56	160	VDD
26	DI18/IO18	53	Z44/IO12	80	VDD	107	DI34/IO34	134	Z23/IO55		
27	DI19/IO19	54	Z45/IO13	81	DI59/IO59	108	DI33/IO33	135	Z22/IO54		

Package Pin Information (160-Pin PQFP, by Pin Name)

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
110	BDCYC1	24	DI16/IO16	97	DI43/IO43	111	REGADR.5	148	Z12/IO44	48	Z39/IO7
19	BNKLDI	25	DI17/IO17	96	DI44/IO44	2	REGADR.6	147	Z13/IO45	49	Z40/IO8
125	CI.0	26	DI18/IO18	95	DI45/IO45	40	VDD	146	Z14/IO46	50	Z41/IO9
124	CI.1	27	DI19/IO19	94	DI46/IO46	61	VDD	145	Z15/IO47	51	Z42/IO10
123	CI.2	28	DI20/IO20	93	DI47/IO47	80	VDD	144	Z16/IO48	52	Z43/IO11
122	CI.3	29	DI21/IO21	92	DI48/IO48	120	VDD	143	Z17/IO49	53	Z44/IO12
121	CI.4	30	DI22/IO22	91	DI49/IO49	142	VDD	139	Z18/IO50	54	Z45/IO13
119	CI.5	31	DI23/IO23	90	DI50/IO50	160	VDD	138	Z19/IO51	55	Z46/IO14
118	CI.6	32	DI24/IO24	89	DI51/IO51	20	VSS	137	Z20/IO52	56	Z47/IO15
117	CI.7	33	DI25/IO25	88	DI52/IO52	59	VSS	136	Z21/IO53	57	Z48/IO16
21	CLK	34	DI26/IO26	87	DI53/IO53	60	VSS	135	Z22/IO54	58	Z49/IO17
4	DI0/IO0	35	DI27/IO27	86	DI54/IO54	101	VSS	134	Z23/IO55	62	Z50/IO18
5	DI1/IO1	36	DI28/IO28	85	DI55/IO55	140	VSS	133	Z24/IO56	63	Z51/IO19
6	DI2/IO2	37	DI29/IO29	84	DI56/IO56	141	VSS	132	Z25/IO57	64	Z52/IO20
7	DI3/IO3	38	DI30/IO30	83	DI57/IO57	3	$\overline{WE}$	131	Z26/IO58	65	Z53/IO21
8	DI4/IO4	39	DI31/IO31	82	DI58/IO58	1	ZO/IO32	130	Z27/IO59	66	Z54/IO22
9	DI5/IO5	109	DI32/IO32	81	DI59/IO59	159	Z1/IO33	129	Z28/IO60	67	Z55/IO23
10	DI6/IO6	108	DI33/IO33	79	DI60/IO60	158	Z2/IO34	128	Z29/IO61	68	Z56/IO24
11	DI7/IO7	107	DI34/IO34	78	DI61/IO61	157	Z3/IO35	127	Z30/IO62	69	Z57/IO25
12	DI8/IO8	106	DI35/IO35	77	DI62/IO62	156	Z4/IO36	126	Z31/IO63	70	Z58/IO26
13	DI9/IO9	105	DI36/IO36	76	DI63/IO63	155	Z5/IO37	41	Z32/IO0	71	Z59/IO27
14	DI10/IO10	104	DI37/IO37	18	$\overline{OE}$	154	Z6/IO38	42	Z33/IO1	72	Z60/IO28
15	DI11/IO11	103	DI38/IO38	116	REGADR.0	153	Z7/IO39	43	Z34/IO2	73	Z61/IO29
16	DI12/IO12	102	DI39/IO39	115	REGADR.1	152	Z8/IO40	44	Z35/IO3	74	Z62/IO30
17	DI13/IO13	100	DI40/IO40	114	REGADR.2	151	Z9/IO41	45	Z36/IO4	75	Z63/IO31
22	DI14/IO14	99	DI41/IO41	113	REGADR.3	150	Z10/IO42	46	Z37/IO5		
23	DI15/IO15	98	DI42/IO42	112	REGADR.4	149	Z11/IO43	47	Z38/IO6		

Package Pin Information (180-Pin PPGA, by Pin Name)

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	VDD	C1	Z0/IO32	E1	$\overline{WE}$	H11	VSS	M1	NC	P1	DI31/IO31
A2	NC	C2	DI3/IO3	E2	DI5/IO5	H12	NC	M2	DI23/IO23	P2	DI25/IO25
A3	NC	C3	Z13/IO45	E3	DI10/IO10	H13	DI43/IO43	M3	DI18/IO18	P3	Z39/IO7
A4	Z1/IO33	C4	Z14/IO46	E4	NC	H14	DI48/IO48	M4	DI14/IO14	P4	Z40/IO8
A5	Z2/IO34	C5	Z15/IO47	E8	VSS	H15	DI54/IO54	M5	VDD	P5	Z41/IO9
A6	Z3/IO35	C6	Z16/IO48	E12	DI38/IO38	J1	DI26/IO26	M6	NC	P6	Z42/IO10
A7	Z4/IO36	C7	Z17/IO49	E13	DI34/IO34	J2	DI20/IO20	M7	Z32/IO0	P7	Z43/IO11
A8	Z5/IO37	C8	VDD	E14	REGADR.4	J3	DI15/IO15	M8	Z48/IO16	P8	Z56/IO24
A9	Z30/IO62	C9	Z21/IO53	E15	CI.6	J4	NC	M9	Z49/IO17	P9	Z57/IO25
A10	Z31/IO63	C10	Z22/IO54	F1	DI0/IO0	J12	DI40/IO40	M10	VSS	P10	Z58/IO26
A11	CI.0	C11	Z23/IO55	F2	DI6/IO6	J13	DI44/IO44	M11	NC	P11	Z59/IO27
A12	CI.1	C12	Z24/IO56	F3	DI11/IO11	J14	DI49/IO49	M12	VDD	P12	Z60/IO28
A13	CI.2	C13	DI32/IO32	F4	$\overline{OE}$	J15	DI55/IO55	M13	DI47/IO47	P13	Z61/IO29
A14	CI.3	C14	REGADR.2	F12	DI39/IO39	K1	DI27/IO27	M14	DI52/IO52	P14	Z62/IO30
A15	NC	C15	NC	F13	DI35/IO35	K2	DI21/IO21	M15	DI58/IO58	P15	NC
B1	NC	D1	REGADR.6	F14	REGADR.5	K3	DI16/IO16	N1	DI29/IO29	R1	DI30/IO30
B2	Z6/IO38	D2	DI4/IO4	F15	CI.7	K4	CLK	N2	DI24/IO24	R2	Z33/IO1
B3	Z7/IO39	D3	DI9/IO9	G1	DI1/IO1	K12	DI41/IO41	N3	DI19/IO19	R3	Z34/IO2
B4	Z8/IO40	D4	VSS	G2	DI7/IO7	K13	DI45/IO45	N4	Z44/IO12	R4	Z35/IO3
B5	Z9/IO41	D5	VSS	G3	DI12/IO12	K14	DI50/IO50	N5	Z45/IO13	R5	Z36/IO4
B6	Z10/IO42	D6	Z18/IO50	G4	BNKLDI	K15	DI56/IO56	N6	Z46/1O14	R6	Z37/IO5
B7	Z11/IO43	D7	Z19/IO51	G12	NC	L1	DI28/IO28	N7	Z47/IO15	R7	Z38/IO6
B8	Z12/IO44	D8	Z20/IO52	G13	DI36/IO36	L2	DI22/IO22	N8	Z50/IO18	R8	Z63/IO31
B9	Z25/IO57	D9	CI.4	G14	BDCYC1	L3	DI17/IO17	N9	Z51/IO19	R9	DI63/IO63
B10	Z26/IO58	D10	NC	G15	REGADR.0	L4	NC	N10	Z52/IO20	R10	DI62/IO62
B11	Z27/IO59	D11	NC	H1	DI2/IO2	L8	VSS	N11	Z53/1021	R11	DI61/IO61
B12	Z28/IO60	D12	DI37/IO37	H2	DI8/IO8	L12	DI42/IO42	N12	Z54/IO22	R12	DI60/IO60
B13	Z29/IO61	D13	DI33/IO33	H3	DI13/IO13	L13	DI46/IO46	N13	Z55/IO23	R13	NC
B14	REGADR.1	D14	REGADR.3	H4	NC	L14	DI51/IO51	N14	DI53/IO53	R14	NC
B15	VDD	D15	CI.5	H5	VSS	L15	DI57/IO57	N15	DI59/IO59	R15	VDD

L64270 Package Pin Information (180-Pin PPGA, by Signal Name)

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
G14	BDCYC1	N3	DI19/IO19	J14	DI49/IO49	D5	VSS	C11	Z23/IO55	N11	Z53/IO21
G4	BNKLDI	J2	DI20/IO20	K14	DI50/IO50	E8	VSS	C12	Z24/IO56	N12	Z54/IO22
A11	CI.0	K2	DI21/IO21	L14	DI51/IO51	H11	VSS	B9	Z25/IO57	N13	Z55/IO23
A12	CI.1	L2	DI22/IO22	M14	DI52/IO52	H5	VSS	B10	Z26/IO58	P8	Z56/IO24
A13	CI.2	M2	DI23/IO23	N14	DI53/IO53	L8	VSS	B11	Z27/IO59	P9	Z57/IO25
A14	CI.3	N2	DI24/IO24	H15	DI54/IO54	M10	VSS	B12	Z28/IO60	P10	Z58/IO26
D9	CI.4	P2	DI25/IO25	J15	DI55/IO55	E1	$\overline{WE}$	B13	Z29/IO61	P11	Z59/IO27
D15	CI.5	J1	DI26/IO26	K15	DI56/IO56	C1	Z0/IO32	A9	Z30/IO62	P12	Z60/IO28
E15	CI.6	K1	DI27/IO27	L15	DI57/IO57	A4	Z1/IO33	A10	Z31/IO63	P13	Z61/IO29
F15	CI.7	L1	DI28/IO28	M15	DI58/IO58	A5	Z2/IO34	M7	Z32/IO0	P14	Z62/IO30
K4	CLK	N1	DI29/IO29	N15	DI59/IO59	A6	Z3/IO35	R2	Z33/IO1	R8	Z63/IO31
F1	DI0/IO0	R1	DI30/IO30	R12	DI60/IO60	A7	Z4/IO36	R3	Z34/IO2	A15	NC
G1	DI1/IO1	P1	DI31/IO31	R11	DI61/IO61	A8	Z5/IO37	R4	Z35/IO3	A2	NC
H1	DI2/IO2	C13	DI32/IO32	R10	DI62/IO62	B2	Z6/IO38	R5	Z36/IO4	A3	NC
C2	DI3/IO3	D13	DI33/IO33	R9	DI63/IO63	B3	Z7/IO39	R6	Z37/IO5	B1	NC
D2	DI4/IO4	E13	DI34/IO34	F4	$\overline{OE}$	B4	Z8/IO40	R7	Z38/IO6	C15	NC
E2	DI5/IO5	F13	DI35/IO35	G15	REGADR.0	B5	Z9/IO41	P3	Z39/IO7	D10	NC
F2	DI6/IO6	G13	DI36/IO36	B14	REGADR.1	B6	Z10/IO42	P4	Z40/IO8	D11	NC
G2	DI7/IO7	D12	DI37/IO37	C14	REGADR.2	B7	Z11/IO43	P5	Z41/IO9	E4	NC
H2	DI8/IO8	E12	DI38/IO38	D14	REGADR.3	B8	Z12/IO44	P6	Z42/IO10	G12	NC
D3	DI9/IO9	F12	DI39/IO39	E14	REGADR.4	C3	Z13/IO45	P7	Z43/IO11	H12	NC
E3	DI10/IO10	J12	DI40/IO40	F14	REGADR.5	C4	Z14/IO46	N4	Z44/IO12	H4	NC
F3	DI11/IO11	K12	DI41/IO41	D1	REGADR.6	C5	Z15/IO47	N5	Z45/IO13	L4	NC
G3	DI12/IO12	L12	DI42/IO42	A1	VDD	C6	Z16/IO48	N6	Z46/IO14	J4	NC
H3	DI13/IO13	H13	DI43/IO43	B15	VDD	C7	Z17/IO49	N7	Z47/IO15	M1	NC
M4	DI14/IO14	J13	DI44/IO44	C8	VDD	D6	Z18/IO50	M8	Z48/IO16	M11	NC
J3	DI15/IO15	K13	DI45/IO45	M12	VDD	D7	Z19/IO51	M9	Z49/IO17	M6	NC
K3	DI16/IO16	L13	DI46/IO46	M5	VDD	D8	Z20/IO52	N8	Z50/IO18	P15	NC
L3	DI17/IO17	M13	DI47/IO47	R15	VDD	C9	Z21/IO53	N9	Z51/IO19	R13	NC
M3	DI18/IO18	H14	DI48/IO48	D4	VSS	C10	Z22/IO54	N10	Z52/IO20	R14	NC

Packaging

160-Pin Plastic Quad Flat Pack: See PF Package in Package Selector Guide
180-Pin Plastic Pin Grid Array: See NF Package in Package Selector Guide

Ordering Information