



BSN20

DATA SHEET

N-channel enhancement mode
vertical D-MOS transistor

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FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Thin and thick film circuits
- General purpose fast switching applications.

DESCRIPTION

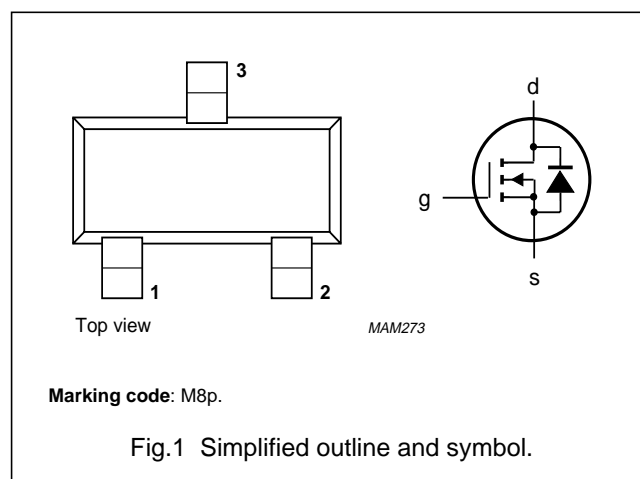
N-channel enhancement mode vertical D-MOS transistor in a SOT23 SMD package.

CAUTION

The device is supplied in an antistatic package.
The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		50	V
I_D	drain current (DC)		100	mA
R_{DSon}	drain-source on-state resistance	$I_D = 100 \text{ mA}; V_{GS} = 10 \text{ V}$	15	Ω
V_{GSth}	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{GS} = V_{DS}$	1.8	V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	50	V
V_{GSO}	gate-source voltage (DC)	open drain	–	± 20	V
I_D	drain current (DC)		–	100	mA
I_{DM}	peak drain current		–	300	mA
P_{tot}	total power dissipation	up to $T_{amb} = 25\text{ °C}$; note 1	–	300	mW
		up to $T_{amb} = 25\text{ °C}$; note 2	–	250	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	430	K/W
		note 2	500	K/W

Notes to the Limiting values and Thermal characteristics

1. Device mounted on a ceramic substrate, $10 \times 8 \times 0.7$ mm.
2. Device mounted on a printed-circuit board.

CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 10\ \mu\text{A}$	50	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1\ \text{mA}$	0.4	–	1.8	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 40\ \text{V}$	–	–	1	μA
I_{GSS}	gate-source leakage current	$V_{DS} = 0$; $V_{GS} = \pm 20\ \text{V}$	–	–	± 100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$; $I_D = 100\ \text{mA}$	–	8	15	Ω
		$V_{GS} = 5\ \text{V}$; $I_D = 100\ \text{mA}$	–	14	20	Ω
		$V_{GS} = 2.5\ \text{V}$; $I_D = 10\ \text{mA}$	–	18	30	Ω
$ y_{fs} $	forward transfer admittance	$V_{DS} = 10\ \text{V}$; $I_D = 100\ \text{mA}$	40	80	–	mS
C_{iss}	input capacitance	$V_{GS} = 0$; $V_{DS} = 10\ \text{V}$; $f = 1\ \text{MHz}$	–	8	15	pF
C_{oss}	output capacitance	$V_{GS} = 0$; $V_{DS} = 10\ \text{V}$; $f = 1\ \text{MHz}$	–	7	15	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0$; $V_{DS} = 10\ \text{V}$; $f = 1\ \text{MHz}$	–	2	5	pF

Switching times

t_{on}	turn-on time	$V_{GS} = 0$ to $10\ \text{V}$; $V_{DD} = 20\ \text{V}$; $I_D = 100\ \text{mA}$	–	2	5	ns
t_{off}	turn-off time	$V_{GS} = 10$ to $0\ \text{V}$; $V_{DD} = 20\ \text{V}$; $I_D = 100\ \text{mA}$	–	5	10	ns